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RESEARCH ARTICLE

Improved Synchronous Space Vector Pulse Width Modulation Strategy for Three-Level With Common-Mode Voltage Suppression

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ABSTRACT In addressing the issue of high common-mode voltage amplitude and output waveform distortion caused by low switching frequency in medium and high-voltage high-power variable frequency speed control systems, the neutral-point clamped three-level inverter is taken as the research object, from the perspective of switching sequence design, a detailed analysis of the switching sequence design method to mitigate the common-mode voltage amplitude, minimize the switching times and enhance output waveform quality. An improved synchronous space vector pulse width modulation strategy is proposed. Secondly, the improved strategy is applied to the closed-loop control of permanent magnet synchronous motor. Aiming at the defects of single modulation mode, the multi-mode modulation strategy based on the improved strategy is proposed, and the smooth switching of modulation mode is realized by limiting the switching phase. The compensation schemes for angular deviation under synchronous modulation and angular delay under digital control are studied to improve the system's stability. Finally, a simulation and experimental platform is built to verify the correctness and effectiveness of the improved and multi-mode modulation strategies.

INDEX TERMS Common-mode voltage, closed-loop control, multi-mode modulation, permanent magnet synchronous motor, space vector pulse width modulation, three-level inverter.

I. INTRODUCTION

Compared with other three-level inverters, the NPC (neutral-point-clamped) three-level inverter has the advantages of simple topology and control algorithm, high output voltage and current quality, low dv/dt, high efficiency [1], [2], [3], [4] have been widely used in AC (alternating current) speed control systems and other voltage source inverter fields. In the high-power AC speed regulation system, to ensure the safe operation of the inverter, the switching frequency of the inverter is generally less than 1kHz [5], which leads to a large number of low-order harmonics in the output waveform of the inverter, causing stator current distortion and torque fluctuation [6]. To solve the problems of high harmonic content and significant switching loss of the inverter output waveform, synchronous modulation strategy is usually adopted. The existing synchronous modulation strategies mainly include SHEPWM (selected harmonic elimination pulse width modulation) [7], CHMPWM (current harmonic minimum pulse width modulation) [8], and synchronous SVPWM (space vector pulse width modulation) [9]. Among them, the synchronous SVPWM strategy has the advantages of simple implementation and good harmonic performance [10] and has been extensively studied.

In [11], four SDPWM$_{\mathrm{I\sim IV}}$ (synchronized discontinuous pulse width modulation) strategies are proposed to eliminate three multiple harmonics in the output line voltage waveform and improve the output waveform quality. Reference [12] analyzed the switching sequence's design principles to improve the output waveform's synchronization and symmetry and improved the output waveform quality by selecting the switch sequence with the lowest WTHD (weighted total harmonic distortion). In [13], an optimized synchronous

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SVPWM strategy, which reduces the current harmonics in the over-modulation region, was proposed.

The above modulation strategy effectively reduces the harmonic content in the output waveform and improves the quality of the output waveform, but less consideration is given to suppressing the CMV (common-mode voltage) amplitude. When the inverter usually works, the output side of the inverter will inevitably make CMV, which will generate a large shaft current on the motor shaft, destroy the insulation performance of the motor, and reduce the service life of the motor [14], [15], [16]. Therefore, it is necessary to suppress the CMV amplitude. The CMV suppression strategies mainly include RCMVPWM (reduced common-mode voltage pulse width modulation) [17], [18], ZCMVPWM (zero common-mode voltage pulse width modulation) [19], and VSVPWM (virtual space vector pulse width modulation) [20], [21], [22], etc. These strategies can suppress or eliminate CMV in asynchronous modulation, but they cannot be well applied to synchronous modulation strategies at low switching. Reference [11] proposed a synchronous SDPWM$_0$by redesigning the switching sequence modulation strategy, which reduces the CMV amplitude to $V_{dc}/6$. In [23], the CMV amplitude in the low modulation region was reduced to $V_{dc}/6$ by re-dividing small sectors. The above studies have achieved CMV suppression in the low modulation region. However, the output CMV amplitude is still $V_{dc}/3$ in other modulation regions, and the CMV suppression in the entire linear modulation region has not been achieved.

For the frequency conversion speed regulation system of medium and high voltage and high-power PMSM (permanent magnet synchronous motor), a multi-mode modulation strategy is usually adopted to solve the defects of a single modulation strategy [24]. However, the smooth switching between different modulation strategies is critical for multi-mode modulation strategies. At the same time, for the multi-mode modulation strategies under closed-loop control, the problems of reference vector angular deviation [25] and digital control delay should also be solved to ensure the synchronization of the output waveform and system stability.

In this paper, to improve the output waveform quality and reduce the amplitude of common-mode voltage at low switching frequency, an improved synchronous SVPWM modulation strategy with three-level inverter common-mode voltage suppression is proposed, and the strategy is applied to the vector control of permanent magnet synchronous motor. Firstly, the basic principle of synchronous SVPWM strategy is described, and the distribution mode of the reference vector and the design principle of the switching sequence is introduced. Then, the design method of switching sequence is analyzed to reduce the amplitude of common-mode voltage, reduce the number of switches, and improve the symmetry of output waveform. By establishing an alternative switching sequence and merging the modulation system segment, the switching sequence in each modulation system segment is designed, the amplitude of CMV in the whole linear modulation region is reduced to $V_{dc}/6$, and the quality of the output waveform is improved. On this basis, the improved strategy is applied to the vector control of permanent magnet synchronous motor, and a multi-mode modulation strategy is proposed, which realizes the smooth switching of modulation mode by switching phase limit. Based on the traditional current controller with delay compensation, the problem of angular deviation under synchronous modulation is solved by correcting the switching period T_s. Finally, the correctness and effectiveness of the strategy are verified by simulation and experiment.

TABLE 1. Switching state and output voltage of three-level inverter.

Switch Status	Output Voltage	S_{X1}	S_{X2}	S_{X3}	S_{X4}
P (+1)	$+V_{dc}/2$	ON	ON	OFF	OFF
O (0)	0	OFF	ON	ON	OFF
N (-1)	$-V_{dc}/2$	OFF	OFF	ON	ON

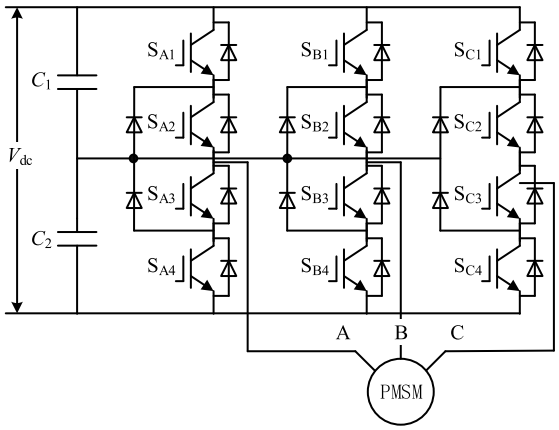

FIGURE 1. Topology diagram of NPC three-level inverter.

II. SYNCHRONOUS SVPWM STRATEGY

The topology of NPC three-level inverter is shown in Fig. 1. Each phase bridge arm of the inverter can be in three different switching states. The definition of the switch state and its corresponding output voltage are shown in Table 1. S_{X1}- S_{X4} represent the on-off states of the 4 IGBTs (insulate-gate bipolar transistor) of phase X, respectively, where X is A, B, or C.

There is a total of 3^3 =27 switching states of NPC three-level inverter; each switching state can get a basic voltage space vector, and each space vector is:

$$V = \frac{2V_{dc}}{3}\left(S_A + S_B e^{j\frac{2}{3}\pi} + S_C e^{-j\frac{2}{3}\pi}\right) \quad (1)$$

where, S_A, S_B andS_C are the switching states of phases A, B, and C, respectively.

Substituting the optional switching states of ABC three-phase into (1), getting the 27 different space vectors, merging the space vectors with the same amplitude and phase, and mapping the combined 19 basic space vectors to the complex plane, the space vector diagram is obtained, as shown in Fig.2.

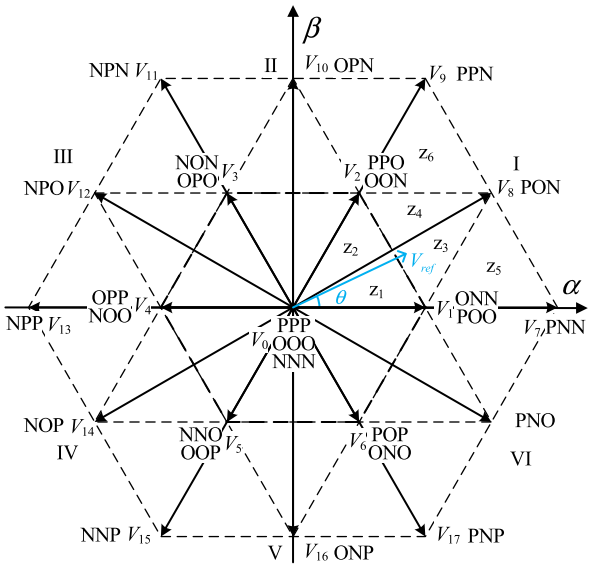

FIGURE 2. Diagram of space vector.

It can be seen from Fig. 2 that 19 basic space vectors divide the entire complex plane into six large sectors I-VI, and each large sector can be divided into six small sectors z_1- z_6.

The theoretical basis of the synchronous SVPWM strategy is the volt-second balance principle. In a switching period T_s, three basic voltage vectors are selected according to the principle of the nearest three vectors to synthesize the reference vector V_{ref}. Taking the small sector z_3 in sector I as an example, the action time of space vectors V_1, V_2 and V_8 can be solved according to (2):

$$\begin{cases} V_{ref}T_s = V_1T_1 + V_2T_2 + V_8T_8 \\ T_s = T_1 + T_2 + T_8 \end{cases} \tag{2}$$

where, T_1, T_2 and T_8 are respectively the action time of space vector V_1, V_2 and V_8.

A. REFERENCE VECTOR DISTRIBUTION

In the synchronous SVPWM strategy, to ensure the synchronization and symmetry of the output waveform, it is necessary that the reference vectors are evenly distributed in large sectors I-VI, and the interval between two adjacent reference vectors is $\pi/3N$. Where N is the number of reference vectors in each large sector. The angle θ_i between the ith reference vector and axis α in large sector I is:

$$\theta_i = \frac{\pi}{6N} + \frac{\pi}{3N}(i-1), \quad \forall i \in \{1, 2, \ldots, N\} \tag{3}$$

It can be seen from (3) that the distribution mode of reference vectors is related to the number of reference vectors N. When N is an odd number, there must be a reference vector with the same phase as the basic space vector V_8, in which case, i= $(N+1)/2$, θ_i=$\pi/6$.

When the modulation index is used to represent the amplitude of the reference vector, the modulation index m is

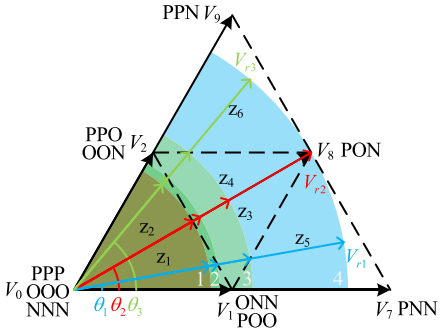

FIGURE 3. Distribution of reference vectors.

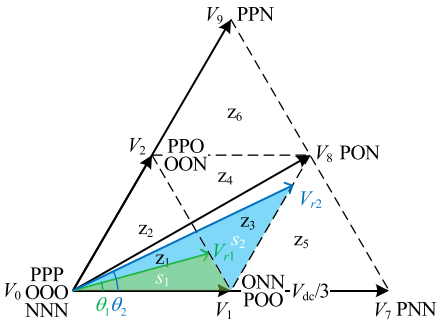

FIGURE 4. Segmented calculation of modulation.

defined as:

$$m = \frac{\sqrt{3}V_{ref}}{V_{\mathrm{dc}}} \tag{4}$$

The distribution sector of reference vectors is related to the number of reference vectors and the modulation index. Taking the reference number N= 3 as an example, when the modulation index m increases from 0 to 1, the distribution of reference vectors is shown in Fig. 3.

It can be seen from Fig. 3 that when the number of reference vectors is N= 3, there are four different distribution modes of the reference vectors. When designing the switching sequence, it is necessary to select the basic space vector according to the distribution sector of the reference vector and then synthesize the reference vector according to the principle of the nearest three vectors.

As shown in Fig. 4, in the triangle s_1, according to the sine theorem:

$$\frac{V_1}{\sin\left(\frac{\pi}{3} + \theta_1\right)} = \frac{V_{r1}}{\sin\left(\frac{\pi}{3}\right)} \tag{5}$$

Substitute $V_1 = V_{\mathrm{dc}}/3$, $m_1 = \sqrt{3}V_{r1}/V_{\mathrm{dc}}$ into (5) get:

$$m_1 = \frac{1}{2\sin\left(\frac{\pi}{3} + \theta_1\right)} \tag{6}$$

In the triangle s_2:

$$m_2 = \frac{1}{2\sin\left(\frac{\pi}{3} - \theta_2\right)} \tag{7}$$

TABLE 2. Synchronization, TPS, and HWS constraints.

	Synchronization	HWS	TPS
θ	$\theta \pm 2\pi$	$\theta \pm 2/3\pi$	$\theta \pm \pi$
$S_A S_B S_C$	$S_A S_B S_C$	$S_C S_A S_B$	$S'_A S'_B S'_C$

Substituting (3) into (6) and (7), it can be obtained that when N is odd, the modulation index of the upper boundary of each segment is:

$$m_i = \frac{1}{2\cos\left(\frac{\pi}{3N}(i-1)\right)}, \quad \forall i \in \{1, 2, \ldots, N+1\} \tag{8}$$

When N is even, the upper boundary modulation index for each segment is:

$$m_i = \frac{1}{2\cos\left(\frac{\pi}{3N}\left(i-\frac{1}{2}\right)\right)}, \forall i \in \left\{1, 2, \ldots, N, N+\frac{1}{2}\right\} \tag{9}$$

B. SWITCH SEQUENCE DESIGN

To ensure the synchronization and symmetry of the output waveform, the synchronization, TPS (three-phase symmetry), and HWS (half-wave symmetry) constraints that the switching states S_A, S_B, and S_C of the inverter need to meet are shown in Table 2.

The switch states S'_A, S'_B, *and* S'_C *are* complementary states of the switch states S_A, S_B, and S_C, respectively. The complement state of the 'P' state is the 'N' state, and the complement state of the 'O' state is the 'O' state.

Under the constraints of synchronization, HWS, and TPS conditions, the switch state of the next sector can be calculated by using the switch state of the current sector:

$$\begin{cases} S_A\left(\theta + \pi/3\right) = S'_B\left(\theta\right) \\ S_B\left(\theta + \pi/3\right) = S'_C\left(\theta\right) \\ S_C\left(\theta + \pi/3\right) = S'_A\left(\theta\right) \end{cases} \tag{10}$$

When designing the switching sequence, the switching times should be reduced as much as possible to reduce the switching loss. Therefore, the following three constraints need to be followed:

Constraint 1: When the switching state occurs, only the state 'P' and the state 'O' are allowed to switch between each other, the state 'O' and the state 'N' are allowed to switch between each other, and the state 'P' and the state 'N' are not allowed to switch between;

Constraint 2: When the switch state is switched, only the switch state of one phase should be switched, and only the switch state of two phases is allowed to switch at most, and the switch state of three phases is not allowed to switch at the same time;

Constraint 3: The start vector of the following sampling period should be the same as the end vector of the previous period; avoid switch state switching during sector switching.

When the number of reference vectors N= 4, under the constraints of the above conditions, the SDPWM$_{\text{I}\sim\text{IV}}$ strategies can be obtained in the modulation index segments $m\in$[0, 0.5043) and $m\in$[0.8213, 1.0], as shown in Table 3.

TABLE 3. Switch sequence of SDPWM$_{\text{I}\sim\text{IV}}$ when N = 4.

m	i	Switch Sequence	
		SDPWM$_{\text{I}}$	SDPWM$_{\text{II}}$
[0, 0.5043)	1	POO-PPO-PPP	POO-PPO-PPP
	2	PPP-PPO-POO	PPP-PPO-POO
	3	OON-ONN-NNN	POO-PPO-PPP
	4	NNN-ONN-OON	PPP-PPO-POO
		SDPWM$_{\text{III}}$	SDPWM$_{\text{IV}}$
	1	OON-ONN-NNN	OON-ONN-NNN
	2	NNN-ONN-OON	NNN-ONN-OON
	3	OON-ONN-NNN	POO-PPO-PPP
	4	NNN-ONN-OON	PPP-PPO-POO
		SDPWM$_{\text{I}}$	SDPWM$_{\text{II}}$
[0.8213, 1.0]	1	POO-PON-PNN	PNN-PON-POO
	2	PNN-PON-POO	POO-PON-PNN
	3	OON-PON-PPN	PON-PPN-PPO
	4	PPN-PON-OON	PPO-PPN-PON
		SDPWM$_{\text{III}}$	SDPWM$_{\text{IV}}$
	1	PON-PNN-ONN	PON-PNN-ONN
	2	ONN-PNN-PON	ONN-PNN-PON
	3	OON-PON-PPN	PON-PPN-PPO
	4	PPN-PON-OON	PPO-PPN-PON

III. IMPROVED SYNCHRONOUS SVPWM STRATEGY

A. CMV SUPPRESSION PRINCIPLE

CMV usually refers to the voltage between the load neutral point N and the reference potential point O. According to Kirchhoff's voltage law, the three-phase voltage output by the inverter can be obtained as:

$$\begin{cases} U_{AO} = L_s \dfrac{\mathrm{d}i_A}{\mathrm{d}t} + R_s i_A + U_{COM} \\ U_{BO} = L_s \dfrac{\mathrm{d}i_B}{\mathrm{d}t} + R_s i_B + U_{COM} \\ U_{CO} = L_s \dfrac{\mathrm{d}i_C}{\mathrm{d}t} + R_s i_C + U_{COM} \end{cases} \tag{11}$$

where, i_A, i_B, i_C are the three-phase output current respectively, L_s are the load inductance, R_s are the load resistance, and U_{COM} is the CMV.

For three-phase symmetrical loads, it is satisfied $i_A + i_B + i_C = 0$. Substituting into (11), the CMV can be obtained U_{COM} as:

$$U_{COM} = \frac{V_{dc}\left(S_A + S_B + S_C\right)}{6} \tag{12}$$

(12) shows that the switching state of ABC three-phase determines the amplitude of the inverter output CMV. When the switching states of the three phases remain unchanged, the output CMV amplitude remains unchanged. Substituting the switch states corresponding to the 27 basic space vectors output by the NPC three-level inverter into (12), the

TABLE 4. CMV amplitudes of 27 space vector outputs.

U_{COM}	Space Vector
0	Zero vector: OOO
$\pm V_{dc}/6$	Medium vectors: PON, OPN, NPO, NOP, ONP, PNO
	Large vectors: PNN, PPN, NPN, NPP, NNP, PNP
	Small vectors: POO, OON, OPO, NOO, OOP, ONO
$\pm V_{dc}/3$	Small vectors: ONN, PPO, NON, OPP, NNO, POP
$\pm V_{dc}/2$	Zero vectors: PPP, NNN

CMV amplitudes of the 27 space vector outputs are obtained, as shown in Table 4.

It can be seen from Table 4 that there are redundant zero vectors and small vectors among the 27 basic space vectors output by the NPC three-level inverter, and the CMVs of these zero vectors and small vectors are not the same. Therefore, to reduce the CMV amplitude of the inverter output, when selecting the small vector synthesis switching sequence, the small vectors POO, OON, OPO, NOO, OOP, and ONO should be preferred; When choosing a zero vector, the zero vector OOO should be selected, and the zero vector PPP and NNN should be avoided.

B. ANALYSIS OF SWITCH SEQUENCE DESIGN

To reduce the CMV amplitude in the linear modulation region, new constraints are added based on constraints 1-3:

Constraint 4: When selecting a small vector for switching sequence design, the small vector whose output common-mode voltage amplitude is $\pm V_{dc}/6$ is preferred; when selecting the zero vector, only the zero vector OOO is selected, not the zero vector PPP and NNN.

1) SWITCHING TIMES

The number of trigger pulses in a fundamental period P defined as:

$$P = \frac{6N\delta + 6\varepsilon}{12} = \frac{N\delta + \varepsilon}{2} \tag{13}$$

where, δ is the number of switching times within a sampling period T_s; ε indicates the number of switching times when sectors are switched.

To obtain minor trigger pulses P with a fixed number of reference vectors N, reducing the switching times δ within each sampling period and avoiding switching actions during sector switching is necessary. Therefore, make changes to constraints 2 and 3:

Constraints 2: When the switch state is switched, only the switch state of one phase is allowed to switch;

Constraints 3: The start vector of the following sampling period must be the same as the end vector of the previous period, and switching action is prohibited during sector switching.

TABLE 5. Symmetry relation of space vector in the sector I.

Number	Relation	Number	Relation
1	OOO ↔ OOO	2	POO ↔ OON
3	PON ↔ PON	4	PNN ↔ PPN

2) QUARTER-WAVE SYMMETRY CONDITION

The symmetry condition of the quarter wave is:

$$\begin{cases} U_{AO}(\theta_A + \theta) = U_{AO}(\theta_A - \theta) \\ U_{BO}(\theta_B + \theta) = U_{BO}(\theta_B - \theta) \\ U_{CO}(\theta_C + \theta) = U_{CO}(\theta_C - \theta) \end{cases} \tag{14}$$

where, θ_A, θ_B and θ_C are the peak voltage positions of the ABC three-phase bridge arm, respectively.

The QWS (quarter-wave symmetry) condition shows that if two reference vectors in a large sector are symmetrical about the middle of the sector, then the switching sequence for synthesizing the two reference vectors is also symmetrical about the middle of the sector. Taking N= 3 as an example, when the first reference vector switch sequence in large sector I is POO-PON-PNN, the fifth reference vector switch sequence can be PPN-PON-OON according to the symmetry relation of space vectors shown in Table 5.

3) SWITCH SEQUENCE DESIGN

According to (8) and (9), the number of modulation segments equals N+ 1. When the number of reference vectors Nincreases, the number of modulation segments also increases, which makes the design of switching sequences more complicated, and the storage of switching sequences consumes more space.

To solve the above problems, an optimal alternative switching sequence with low common-mode voltage amplitude and low switching times can be designed for z_1, z_3, and z_5 in large sector I according to conditions 1-4 constraints. The alternative switching sequences design is shown in Table 6. Then, follow the steps below to design the switching sequence:

Step.1: Segment the modulation index according to the distribution sector of the reference vector;

Step.2: Determine the starting space vector of the switching sequence in each segment;

Step.3: Find the switching sequence of the current reference vector in Table 6 according to the small sector where the current reference vector is located and the starting space vector;

Step.4: Take the end space vector of the switching sequence as the start space vector of the following reference vector;

Step.5: Repeat steps 3 and 4 until the switching sequence of the last reference vector in the first half of large sector I is designed;

Step.6: According to the QWS constraint, calculate the switching sequence in the second half of large sector I.

TABLE 6. Alternative switch sequences in the sector I.

Small Sector	Starting space vector	Switching sequence
z_1	POO	POO-OOO-OON
	OON	OON-OOO-POO
z_3	POO	POO-PON-OON
	OON	OON-PON-POO
z_5	PNN	PNN-PON-POO
	POO	POO-PON-PNN

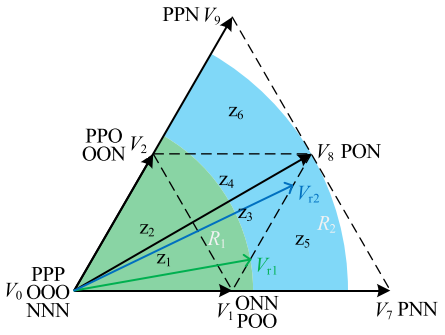

FIGURE 5. The merged modulation index segments.

Step.7: According to synchronicity, TPS, and HWS constraints, calculate the switching sequence in large sectors II-VI.

Before designing the switching sequence, it is necessary to determine the starting space vector in each modulation index segment. As shown in Fig. 5, before the reference vector V_{r1} enters the small sector z_5, only POO can be selected as the starting vector. When the reference vector V_{r1} enters the small sector z_5, POO or PNN can be chosen as the starting vector. Therefore, all modulation index segments are combined into two segments, R_1 and R_2, based on the above differences.

When $N$is even, the upper bound of the modulation index segment R_1 is:

$$m_{\frac{N+2}{2}} = \frac{1}{2\cos\left(\frac{\pi}{3N}\left(\frac{N+2}{2}-\frac{1}{2}\right)\right)} = \frac{1}{2\cos\left(\frac{\pi}{6}+\frac{\pi}{6N}\right)} \quad (15)$$

When $N$is odd, the upper bound of the modulation index segment R_1 is:

$$m_{\frac{N+3}{2}} = \frac{1}{2\cos\left(\frac{\pi}{3N}\left(\frac{N+3}{2}-1\right)\right)} = \frac{1}{2\cos\left(\frac{\pi}{6}+\frac{\pi}{6N}\right)} \quad (16)$$

When the reference vectors are all located in the modulation index segment R_1, POO is selected as the starting vector;

When the reference vectors are all located in the modulation index segment, R_2, POO, and PNN can be selected as the starting vectors. However, for the first reference vector V_{r2} in z_3, because there is only one starting vector POO on the boundary between z_3 and z_5, the start vector of the switching sequence can only be POO, and the end vector of the switching sequence of the last reference vector in z_5 is also POO. The beginning vector in z_5 can be calculated from the end vector in z_5. Take N= 3 as an example, the end vector of z_5 is POO, and the switching sequence of the last reference vector is determined to be PNN-PON-POO, so the starting vector in z_5 is PNN.

According to the above switching sequence design steps and starting vector selection method, when N= 3, the switching sequences in each modulation index segment in large sector I are shown in Table 7.

TABLE 7. Switching sequence of improved modulation strategy when $N = 3$.

m	i	Switch sequence
[0, 0.5)	1	POO-OOO-OON
	2	OON-OOO-POO
	3	POO-OOO-OON
[0.5, 0.5321)	1	POO-OOO-OON
	2	OON-PON-POO
	3	POO-OOO-OON
[0.5321, 0.6527)	1	POO-PON-OON
	2	OON-PON-POO
	3	POO-PON-OON
[0.6527, 1.0)	1	PNN-PON-POO
	2	POO-PON-OON
	3	OON-PON-PPN

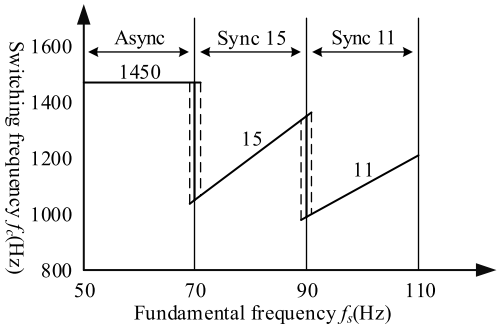

FIGURE 6. Multi-mode modulation strategy.

IV. MULTI-MODE MODULATION STRATEGIES

Asynchronous modulation has the advantages of easy implementation and a high carrier ratio in the low-frequency band. However, in the middle and high-frequency band, the carrier ratio decreases, and the harmonic content in the output waveform increases, resulting in the poor quality of the waveform. Synchronous modulation can ensure the synchronization and symmetry of waveform and effectively suppress harmonics. However, at low fundamental frequencies, the switching frequency is less utilized. Considering the advantages and disadvantages of the above two modulation strategies, the proposed multi-mode modulation strategy is shown in Fig. 6.

Where, f_c is the switching frequency, for synchronous modulation:

$$f_c = Pf_s \quad (17)$$

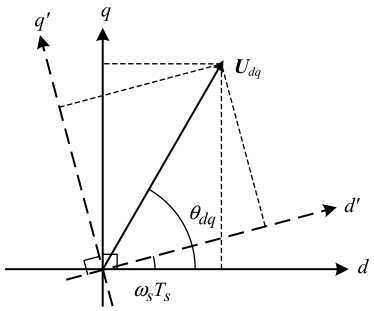

FIGURE 7. Schematic diagram of angular delay.

A multi-mode modulation strategy must achieve smooth switching of different modulation strategies to reduce the current and torque impact during switching. When switching from asynchronous modulation to synchronous 15, because there are more sampling points, it can be directly switched, and the angular deviation between the reference vector and the voltage vector can be corrected by angular deviation compensation.

When switching between synchronization 15 and 11, select the midpoint of each large sector to switch. The sampling points are set at the midpoint of each large sector in synchronization 15 and 11, which can ensure the continuity of the stator flux trajectory and reduce the current and torque impact during switching.

At the same time, to avoid frequent modulation strategy switching, a frequency hysteresis is set near the mode switching point.

When the multi-mode modulation strategy is applied to the closed-loop control of PMSM, the angle delay caused by the digital control may cause the current loop to lose stability and the system to oscillate. The angular deviation between the voltage vector and the reference vector may generate the reference vector index i to fail to change continuously in the designed order, resulting in reduced output waveform quality and additional switching action. To solve the above problems, it is necessary to compensate for the angle delay and angle deviation.

A. ANGULAR DELAY COMPENSATION

For digital controllers such as DSP (digital signal processing), the duty cycle calculated in the current switching period will not be updated until the next switching period, resulting in an angle delay between the electrical angle used in the inverse Park conversion and the actual electrical angle. The angle of delay is related to the switching period T_s. At low switching frequency, T_s is longer, making the angular delay and system stability worse. In the traditional controller design, angle delay compensation is usually introduced to solve this problem.

As shown in Fig. 7, after controller delay, the d axis has been rotated to d', at which time the voltage vector $\boldsymbol{U}_{dq}$ is:

$$\begin{cases} U_d = \left|\boldsymbol{U}_{dq}\right| \cos\theta_{dq} \\ U_q = \left|\boldsymbol{U}_{dq}\right| \sin\theta_{dq} \end{cases} \tag{18}$$

The voltage component of $\boldsymbol{U}_{dq}$ in the $d'q'$ axis is:

$$\begin{cases} U_{d'} = \left|\boldsymbol{U}_{dq}\right| \cos\left(\theta_{dq} - \omega_s T_s\right) \\ U_{q'} = \left|\boldsymbol{U}_{dq}\right| \sin\left(\theta_{dq} - \omega_s T_s\right) \end{cases} \tag{19}$$

Convert (18) and (19) to space vector form:

$$\boldsymbol{U}_{d'q'} = \boldsymbol{U}_{dq} e^{-\mathrm{j}\omega_s T_s} \tag{20}$$

where, $\boldsymbol{U}_{d'q'}$ is the voltage vector under the $d'q'$axis.

Angular delay is required to compensate to obtain the same voltage vector in the d'q' axis. Multiply the $\boldsymbol{U}_{d'q'}$ by the delay compensation term to get:

$$\boldsymbol{U}_{d'q'} e^{\mathrm{j}\omega_s T_s} = \boldsymbol{U}_{dq} e^{(-\mathrm{j}\omega_s T_s + \mathrm{j}\omega_s T_s)} = \boldsymbol{U}_{dq} \tag{21}$$

The trigonometric function operation is introduced in (21). To reduce the amount of calculation, the angular delay can be compensated by the inverse Park transformation. The compensated transformation matrix is:

$$\begin{bmatrix} \cos\left(\theta_e + \omega_s T_s\right) & -\sin\left(\theta_e + \omega_s T_s\right) \\ \sin\left(\theta_e + \omega_s T_s\right) & \cos\left(\theta_e + \omega_s T_s\right) \end{bmatrix} \tag{22}$$

B. ANGULAR DEVIATION COMPENSATION

The synchronous modulation strategy distributes the reference vector evenly throughout the complex plane according to the angle calculated by (3). However, ensuring that the voltage vector's angle matches the reference vector's angle under closed-loop control isn't easy.

Define the angular deviation θ_{err} between two vectors as:

$$\theta_{err} = \theta_{ref} - \theta_u \tag{23}$$

where, θ_{ref} is the angle between the reference vector and α axis, θ_u is the angle between the voltage vector and α axis. θ_{ref} is calculated according to (3), then:

$$i = \mathrm{round}\left(\frac{\pi\theta_u}{3N} - \frac{1}{2}\right) \tag{24}$$

When θ_{err} is large, it may cause the reference vector index i to jump. For example, i might go directly from 1 to 3, instead of from 1 to 3. When i jumps, the synchronization of the system deteriorates, and the output waveform quality decreases.

To solve the angle deviation problem, the action time of the reference vector can be adjusted, and the angle deviation between the voltage vector and the reference vector can be compensated by correcting T_s.

Define the switching period T_{err} to be compensated as:

$$T_{err} = \frac{\theta_{err}}{\omega_s} = \frac{\theta_{err}}{2\pi f_s} \tag{25}$$

where, ω_s is the fundamental angular frequency, f_s is the fundamental frequency.

Correct T_{err} into T_s, the corrected T_s is:

$$T_s = \frac{1}{6Nf_s} + T_{err} \tag{26}$$

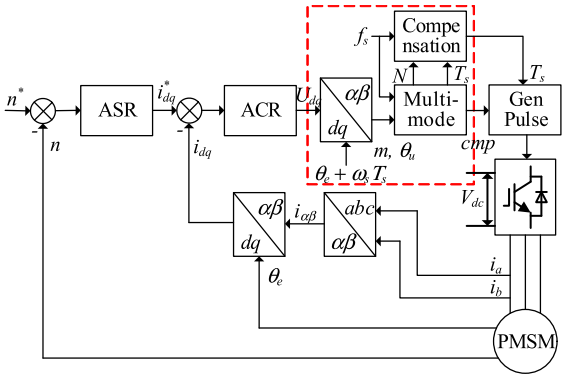

FIGURE 8. Vector control block diagram of multi-mode modulation strategy.

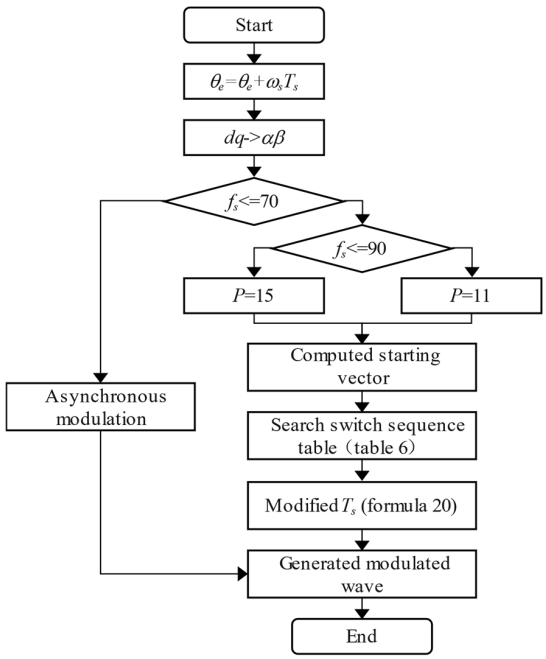

FIGURE 9. Multi-mode modulation strategy flow.

C. MULTI-MODE MODULATION STRATEGY FOR ANGLE DEVIATION COMPENSATION AND ANGLE DELAY COMPENSATION

Fig. 8 is the vector control block diagram of permanent magnet synchronous motor $i_d* = 0$. The software execution flow of the multi-mode modulation strategy with angular delay compensation and angular deviation compensation is shown in Fig. 9. After the delay compensation is performed on θ_e, the U_{dq} is transformed by inverse Park to obtain m and θ_u. The multi-mode modulation module switches modulation modes according to f_s and uses m and θ_u to synthesize modulation waves of corresponding modes. If the current mode is synchronous modulation, correct T_s by (26) to compensate for angular deviation.

V. SIMULATION ANALYSIS

A. IMPROVED MODULATION STRATEGY ANALYSIS

Simulink is used to simulate and analyze the improved modulation strategy to verify the effectiveness of the improved synchronous modulation strategy. Simulation parameters are as follows: direct current bus voltage $V_{dc} = 90$V, fundamental

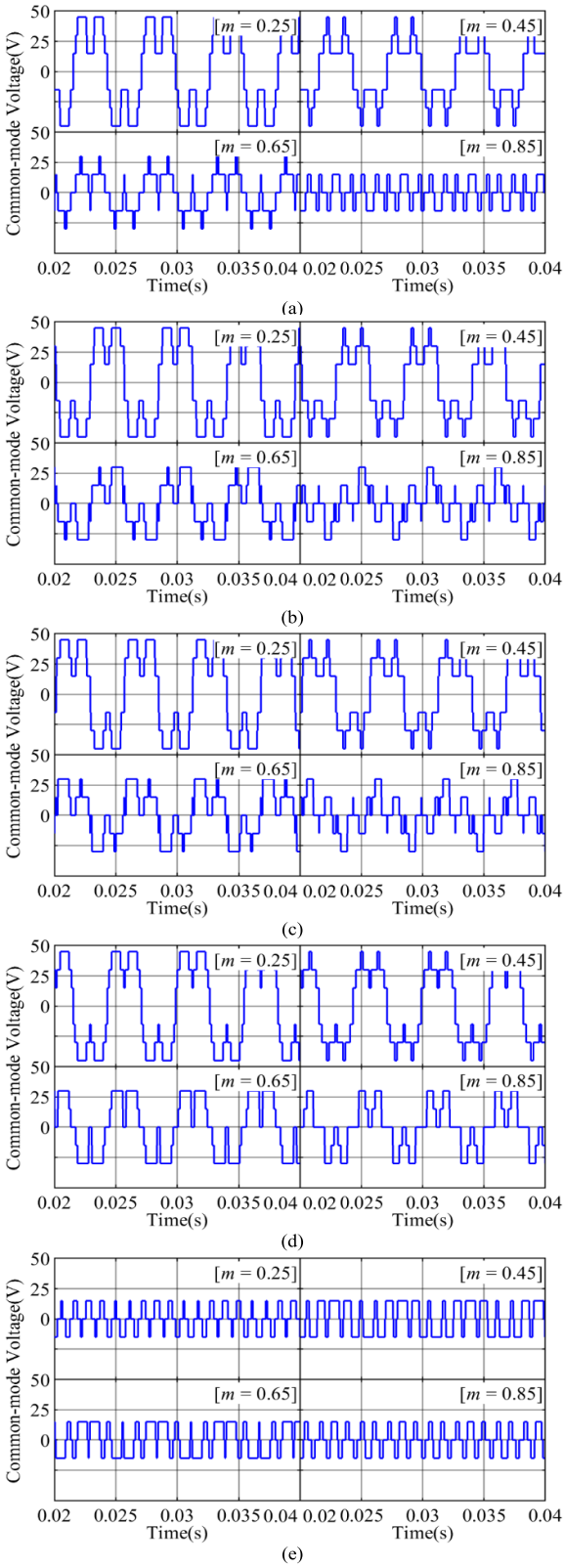

FIGURE 10. Simulation waveform of common-mode voltage of $SDPWM_{I\sim IV}$ and improved strategy under different modulation regimes. (a) $SDPWM_{I}$ (b) $SDPWM_{II}$ (c) $SDPWM_{III}$ (d) $SDPWM_{IV}$ (e) Improvement strategy.

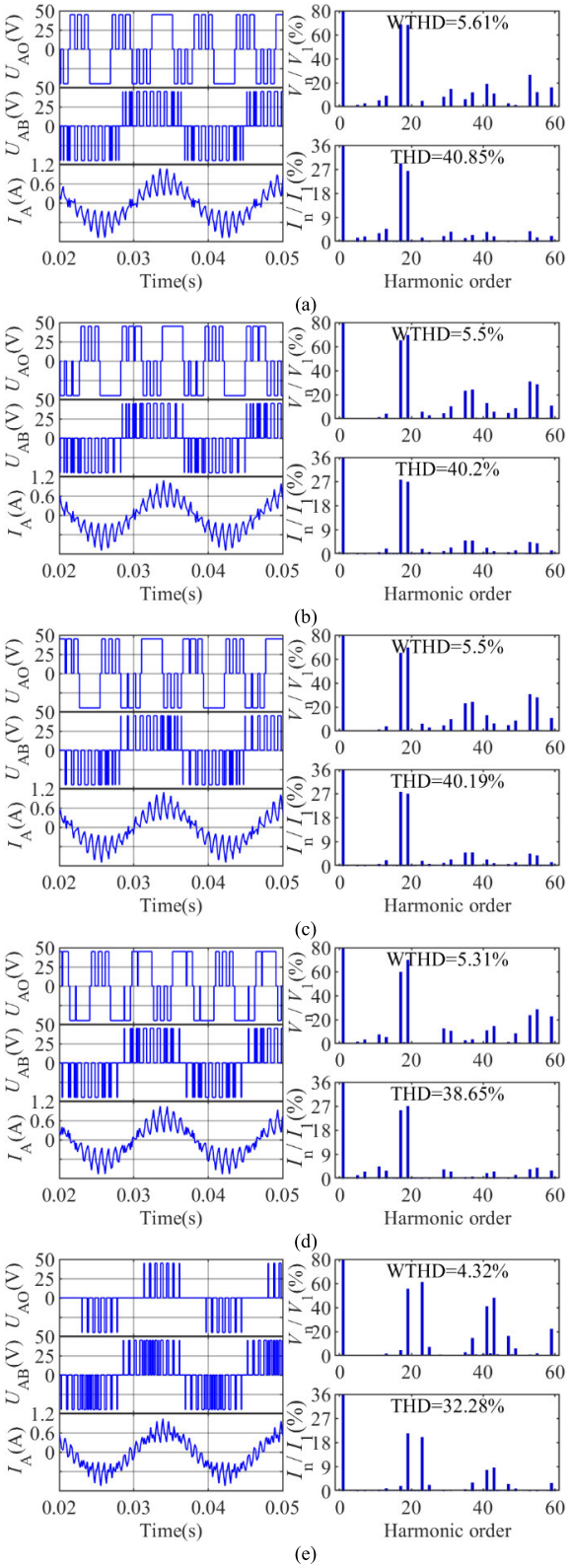

FIGURE 11. When P=7, m=0.25, the voltage and current simulation waveform under different modulation strategies. (a) $SDPWM_{I}$ (b) $SDPWM_{II}$ (c) $SDPWM_{III}$ (d) $SDPWM_{IV}$ (e) Improvement strategy

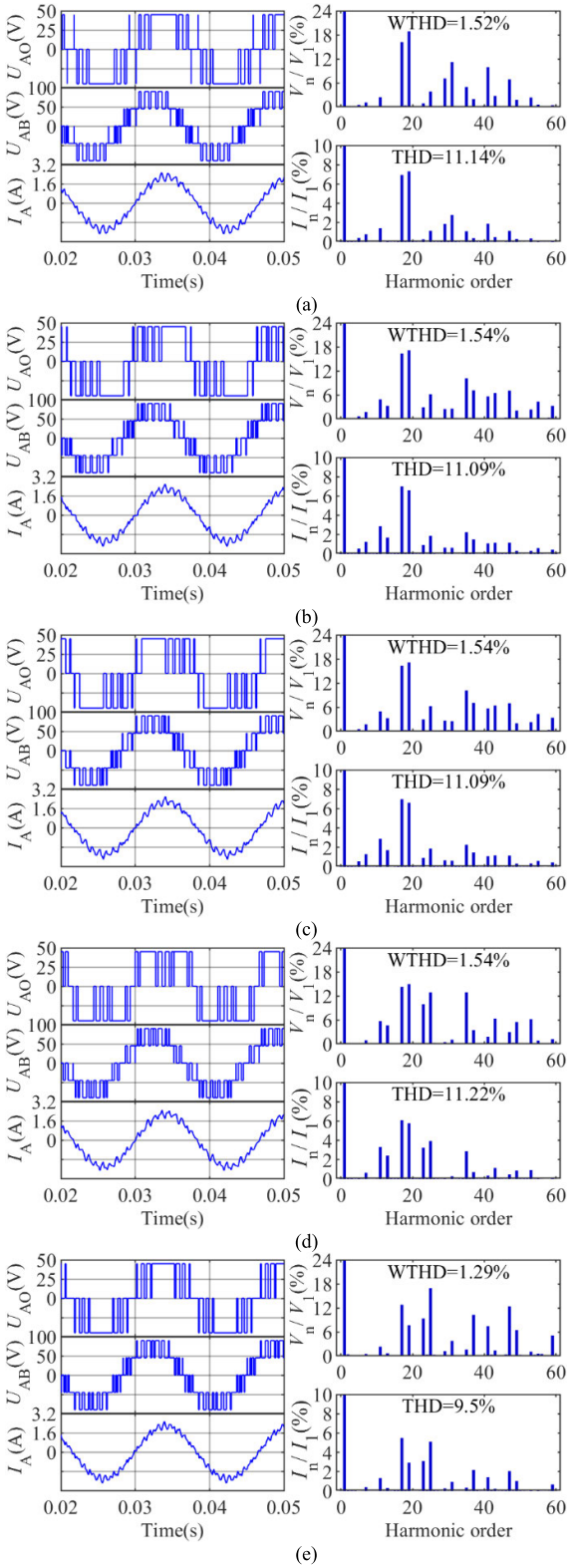

FIGURE 12. When P=7, m=0.85, the voltage and current simulation waveform under different modulation strategies. (a) $SDPWM_{I}$ (b) $SDPWM_{II}$ (c) $SDPWM_{III}$ (d) $SDPWM_{IV}$ (e) Improvement strategy.

frequency $f_s = 60$Hz, load resistance R = 20Ω, load inductance L = 6.7 mH.

1) SWITCHING TIMES

As shown in Table 3, when N= 4, m ∈[0, 0.5043), $SDPWM_{I\sim III}$ modulation strategy generates one additional

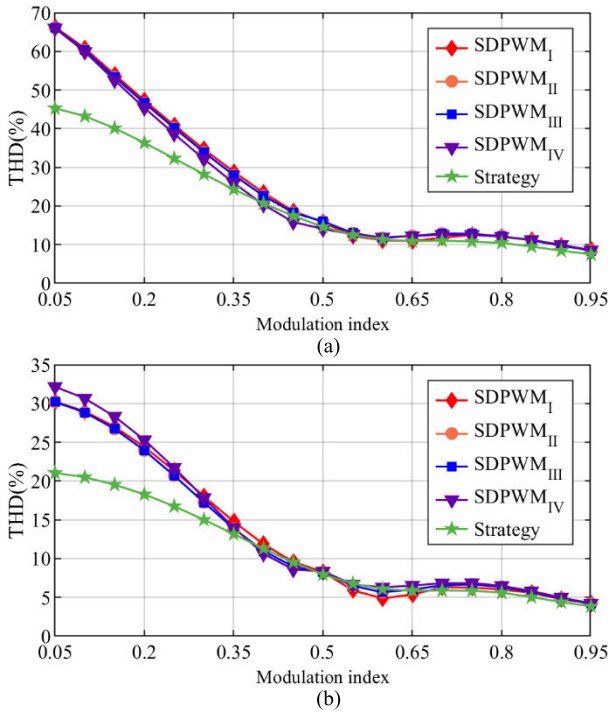

FIGURE 13. Comparison of phase current THD simulation results under different modulation strategies (a) P = 7 (b) P =13.

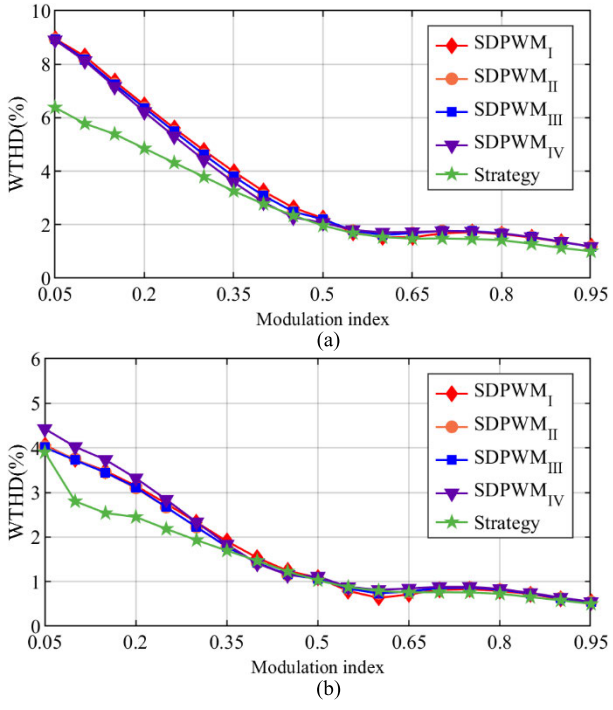

FIGURE 14. Comparison of WTHD simulation results of line voltage under different modulation strategies (a) P = 7 (b) P =13.

switching action during sector switching, and SDPWM$_{IV}$ modulation strategy generates two additional switching actions during sector switching. In this case, the P of the four modulation strategies is 5, 5, 5, and 6, respectively. In the whole linear modulation region, when N is even, $P = N + 1$ or

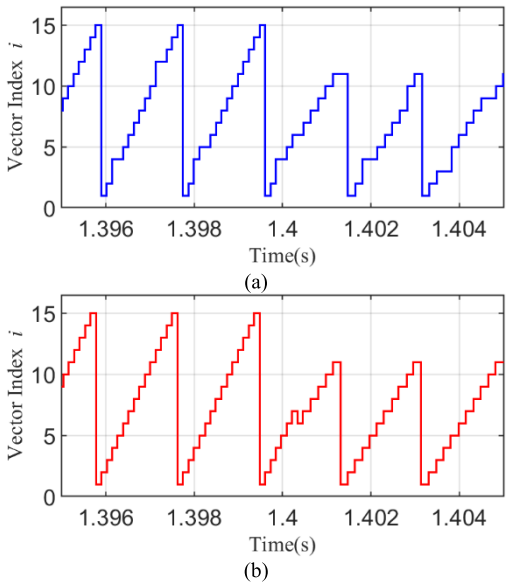

FIGURE 15. Simulation results of reference vector number change under different compensation strategies (a) no angular deviation compensation (b) angular deviation compensation.

TABLE 8. Motor parameters.

Parameter	Value	Parameter	Value
Rated power	0.4 kW	Number of pole-pairs	5
Rated torque	1.27 N·m	Stator inductance	6.71 mH
Rotor flux linkage	0.048 Wb	Stator resistance	1.62 Ω

$P = N + 2$ for four modulation strategies; when N is odd, $P = N + 2$ or $P = N + 3$ for four modulation strategies.

As seen from Table 6, when $N = 4$, $m \in [0, 0.5)$, the switching action of the improved strategy has two switching actions in each switching period, while no switching action occurs during sector switching. In this case, the P of the improved policy is 3. In the linear modulation region, for the improved strategy, when N is even, $P = N + 1$; when N is odd, $P = N$.

The comparison shows that when N is even, the P of the improved strategy is less than or equal to that of the four SDPWM modulation strategies. When N is odd, the improved strategy has the minor P.

2) COMMON-MODE VOLTAGE

Fig. 10 shows the common-mode voltage waveforms of the four SDPWM strategies and the improved modulation strategies when the modulation index $m = 0.25$ to 0.85.

When $m = 0.25$ and $m = 0.45$, PPP and NNN are used in the switching sequence of the four SDPWM strategies, so the output common-mode voltage amplitude is $V_{dc}/2$. When $m = 0.65$, PPO or ONN is used in the switching sequence of the four SDPWM strategies, so the output common-mode voltage amplitude is $V_{dc}/3$. When $m = 0.85$, the output common-mode voltage amplitude of the SDPWMI strategy is $V_{dc}/6$, and the other three SDPWM strategies use PPO,

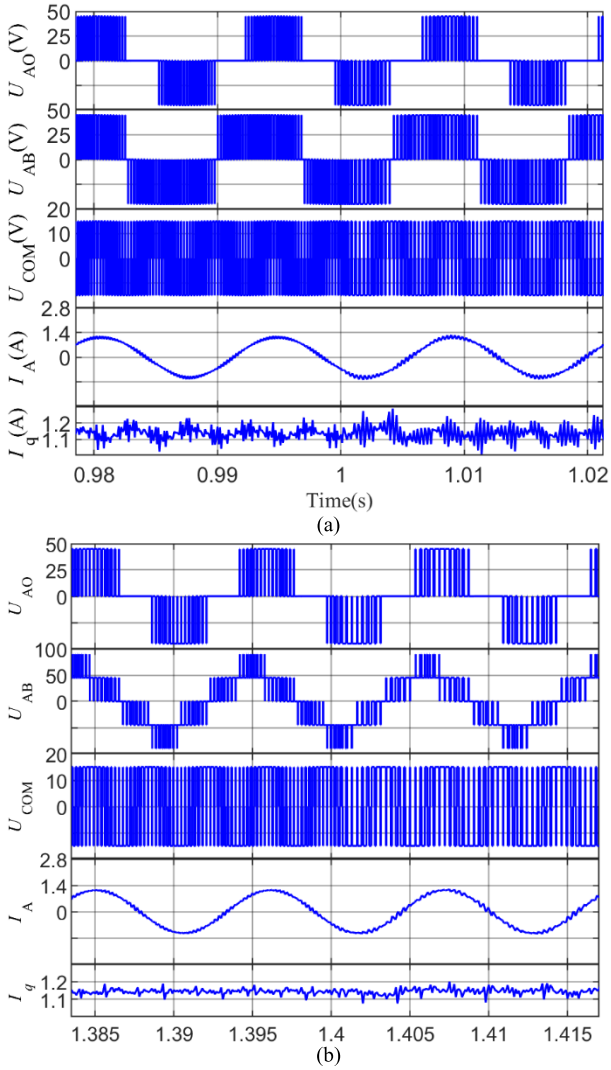

FIGURE 16. Simulation results of modulation strategy switchingwhen $T_L = 0.4$N m (a) asynchronous modulation switches to Sync 15 (b) Sync 15 switches to Sync 11.

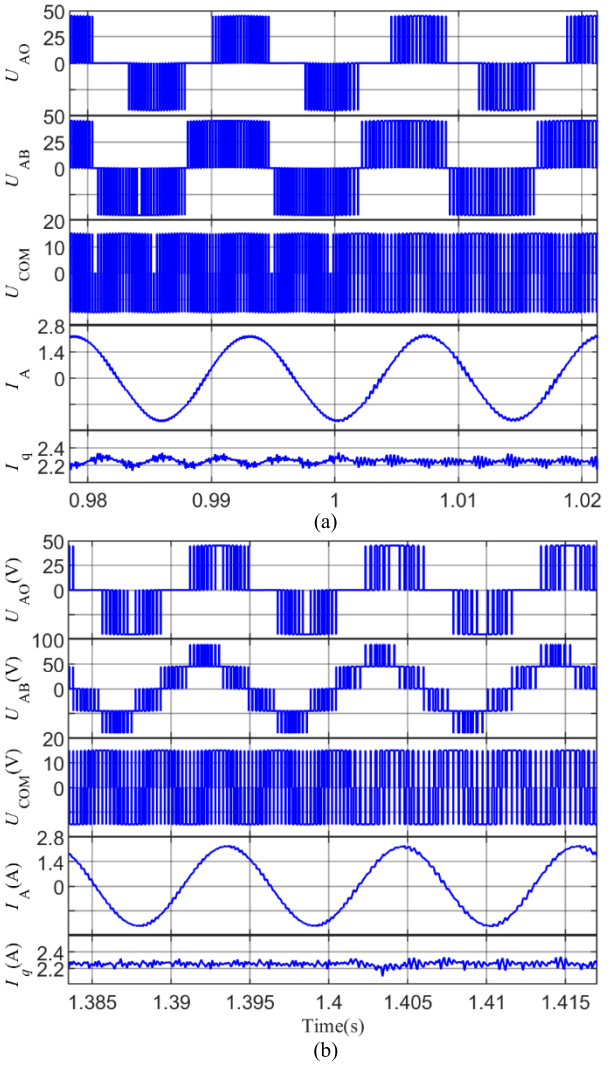

FIGURE 17. Simulation results of modulation strategy switching when $T_L = 0.8$N m (a) asynchronous modulation switches to Sync 15 (b) Sync 15 switches to Sync 11.

ONN, and PPO, respectively, so the output common-mode voltage amplitude is $V_{dc}/3$. The proposed improved strategy strictly abides by constraint 4 when designing the switching sequence. Therefore, the output CMV amplitude of the improved strategy is $V_{dc}/6$ in the whole linear modulation region.

3) OUTPUT WAVEFORM QUALITY ANALYSIS

Figs. 11 and 12 show the waveforms of phase voltage U_{AO}, line voltage U_{AB}, and phase current I_A output by the inverter, as well as the harmonic analysis results of U_{AB} and I_A under the action of the four SDPWM modulation strategies and improved modulation strategies, respectively, when $P = 7$ and $m = 0.25$ and $P = 7$ and $m = 0.85$. As shown in Fig 11 and Fig 12, the output voltage waveform of the inverter under the improved modulation strategy meets the requirements of synchronization, HWS, and QWS. When $m = 0.25$, the improved strategy has the lowest harmonic distortion rate and

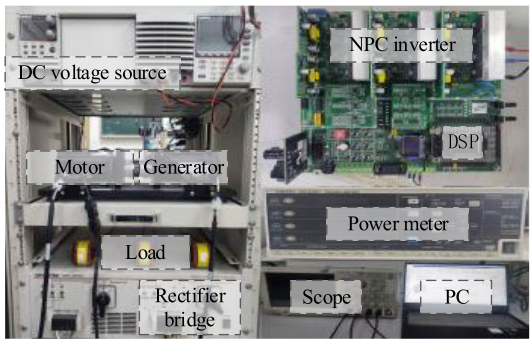

FIGURE 18. The experimental platform of NPC three-level inverter.

can effectively reduce the 3rd and 5th harmonics. When $m = 0.85$, the harmonic distortion rate of the improved strategy is basically the same as that of the four SDPWM strategies.

Figs. 13 and 14 show the simulation results of A-phase current THD (total harmonic distortion) and AB line voltage WTHD of four SDPWM strategies and improved strategies

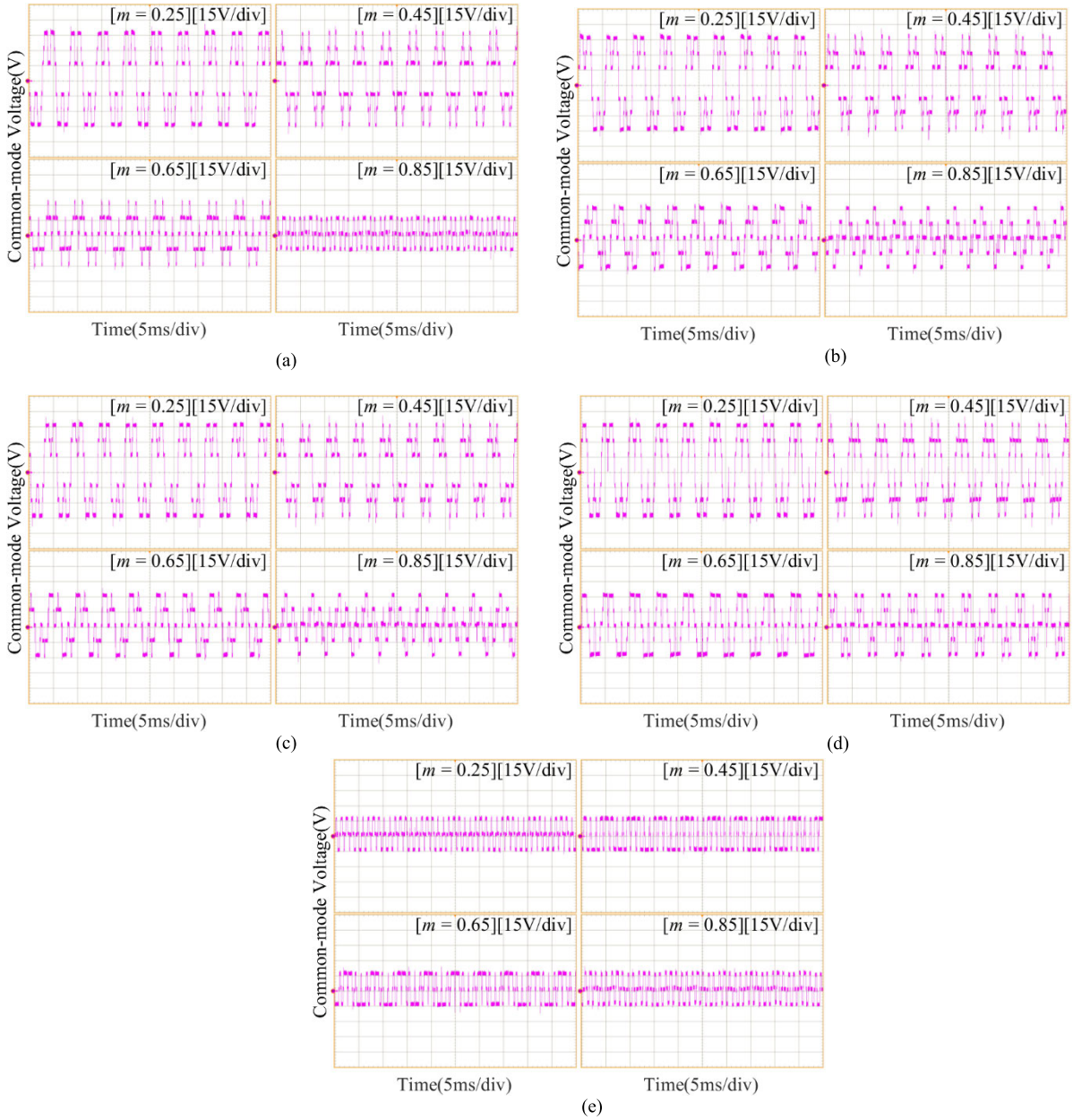

FIGURE 19. The experimental waveform of common-mode voltage of SDPWM$_{I\sim IV}$ and improved strategy under different modulation regimes. (a) SDPWM$_{I}$ (b) SDPWM$_{II}$ (c) SDPWM$_{III}$ (d) SDPWM$_{IV}$ (e) Improvement strategy.

when the modulation regime m increases from 0.05 to 0.95, respectively.

The simulation results show that when the modulation system $m\in[0.05, 0.35)$, the improved strategy has the smallest current THD and voltage WTHD and the highest output waveform quality. When $m\in(0.35, 0.95)$, the current THD and voltage WTHD of the improved strategy are basically equal to four SPDWM strategies, and the output waveform quality is the same.

B. ANALYSIS OF MULTI-MODE MODULATION STRATEGY

To verify the effectiveness of the multi-mode modulation strategy, the simulation model of the vector control of the permanent magnet synchronous motor $i_d^*=0$ is built by using Simulink software for simulation analysis. direct current bus voltage $V_{dc} = 90$V, and the motor parameters are shown in Table 8.

Fig. 15 shows the simulation results of reference vector index changes under different compensation strategies during the switching from synchronization 15 to synchronization 11. As shown in Fig. 15(a), at 1.398s, because only delay compensation was carried out without correcting the angular deviation between the voltage vector and the reference vector, i jumped from 2 to 4, reducing the synchronization of the output waveform. At the same time, the switch status changes from POO to OON, adding two additional switching actions.

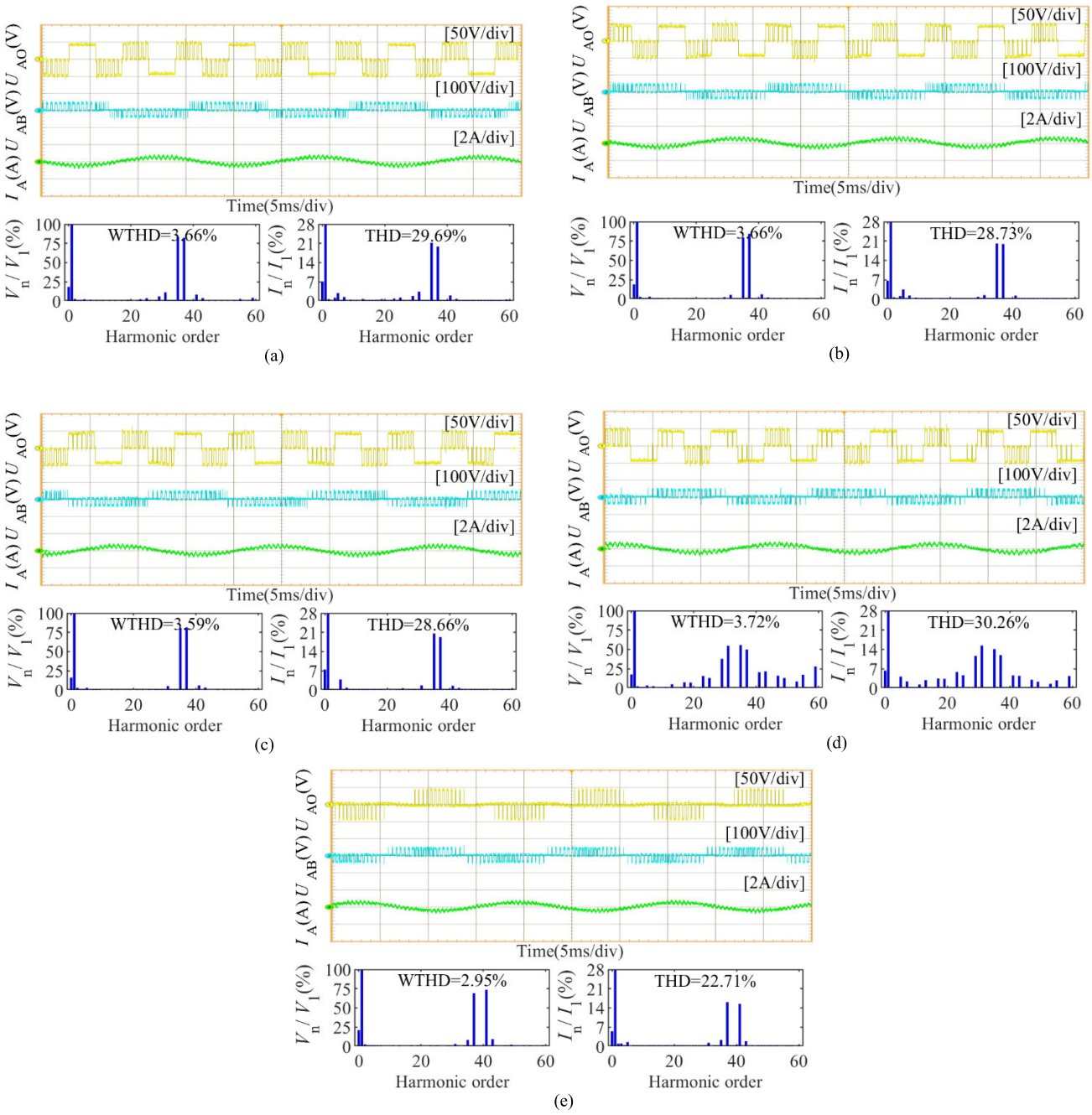

FIGURE 20. When P=13, m=0.25, the voltage and current experimental waveforms under different modulation strategies. (a) SDPWM$_{\mathrm{I}}$ (b) SDPWM$_{\mathrm{II}}$ (c) SDPWM$_{\mathrm{III}}$ (d) SDPWM$_{\mathrm{IV}}$ (e) Improvement strategy.

As shown in Fig. 15(b), after angular deviation compensation, i changes continuously, improving the synchronization of the output waveform and avoiding additional switching actions.

Figs. 16 and 17 show the simulation waveforms of phase voltage U_{AO}, line voltage U_{AB}, common-mode voltage U_{COM}, current i_{A}, and motor Q-axis current i_q output by the inverter before and after multi-mode modulation strategy switching when loading torque T_L =0.4N·m and 0.8N·m, respectively.

According to the simulation results, using different load torques and modulation modes, the multi-mode modulation strategy can effectively reduce the output common-mode voltage amplitude of the inverter to $V_{\mathrm{dc}}/6$. There is no current impact when switching from asynchronous modulation to synchronous 15 and from synchronous 15 to synchronous 11, realizing the smooth transition of modulation modes.

VI. EXPERIMENTAL VERIFICATION

To further verify the effectiveness of the proposed improved and multi-mode modulation strategies, an NPC three-level inverter experiment platform was built, as shown in Fig. 18, and TMS320F28335 was used to implement the

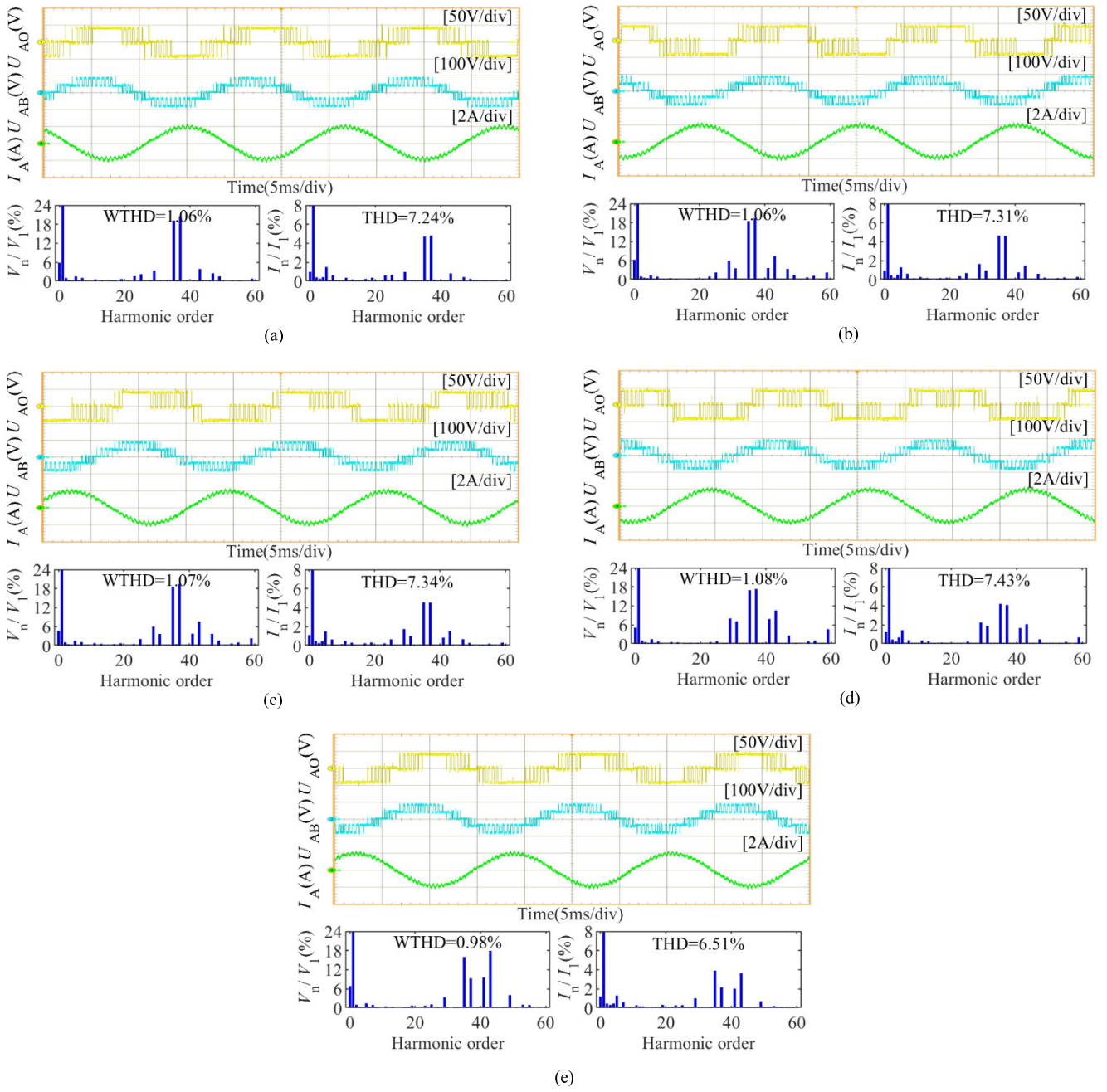

FIGURE 21. When P=13, m=0.85, the voltage and current experimental waveforms under different modulation strategies. (a) SDPWM$_{\mathrm{I}}$ (b) SDPWM$_{\mathrm{II}}$ (c) SDPWM$_{\mathrm{III}}$ (d) SDPWM$_{\mathrm{IV}}$ (e) Improvement strategy.

control strategy. The RL load and motor parameters used in the experiment were the same as those used in the simulation.

A. 5.1 IMPROVED MODULATION STRATEGY

1) COMMON-MODE VOLTAGE

Fig. 19 shows the common-mode voltage experimental waveforms of four SDPWM modulation strategies and the improved modulation strategies when the modulation index $m = 0.25$ to $m = 0.85$.

The experimental results show that compared with the four SDPWM strategies, the improved strategy can reduce the common-mode voltage amplitude to $V_{\mathrm{dc}}/6$ in different modulation regions.

2) OUTPUT WAVEFORM QUALITY

Figs. 20 and 21 show the waveforms of phase voltage U_{AO}, line voltage U_{AB}, and phase current I_{A} output by the inverter, as well as the harmonic analysis results of U_{AB} and I_{A} under different modulation strategies, respectively, when $P = 13$ and

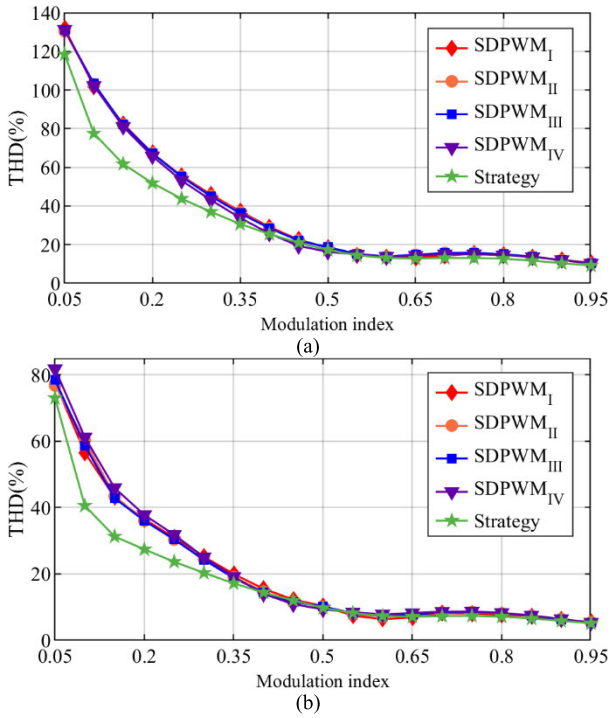

FIGURE 22. Comparison of phase current THD experimental results under different modulation strategies (a) P = 7 (b) P =13.

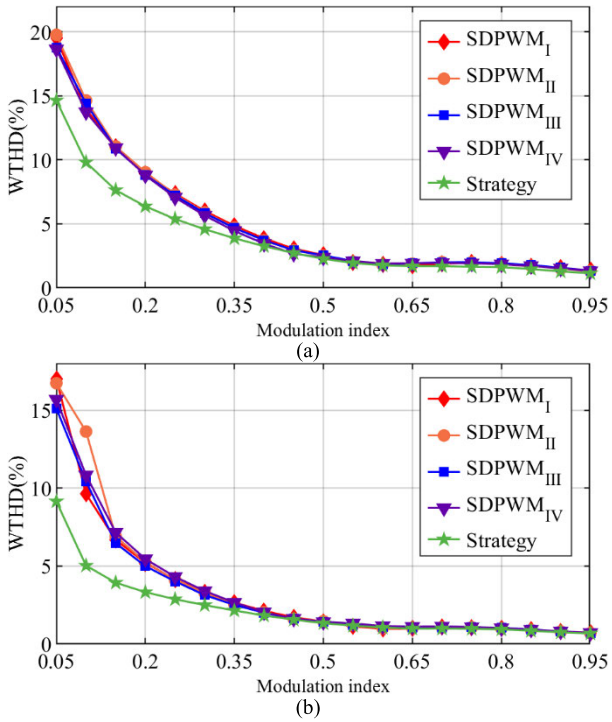

FIGURE 23. Comparison of WTHD experimental results of line voltage under different modulation strategies (a) P = 7 (b) P =13.

m= 0.25 and P= 13 and m= 0.85. As shown in Fig 20 and Fig 21, the output waveform of the inverter under the improved strategy meets the synchronization and symmetry

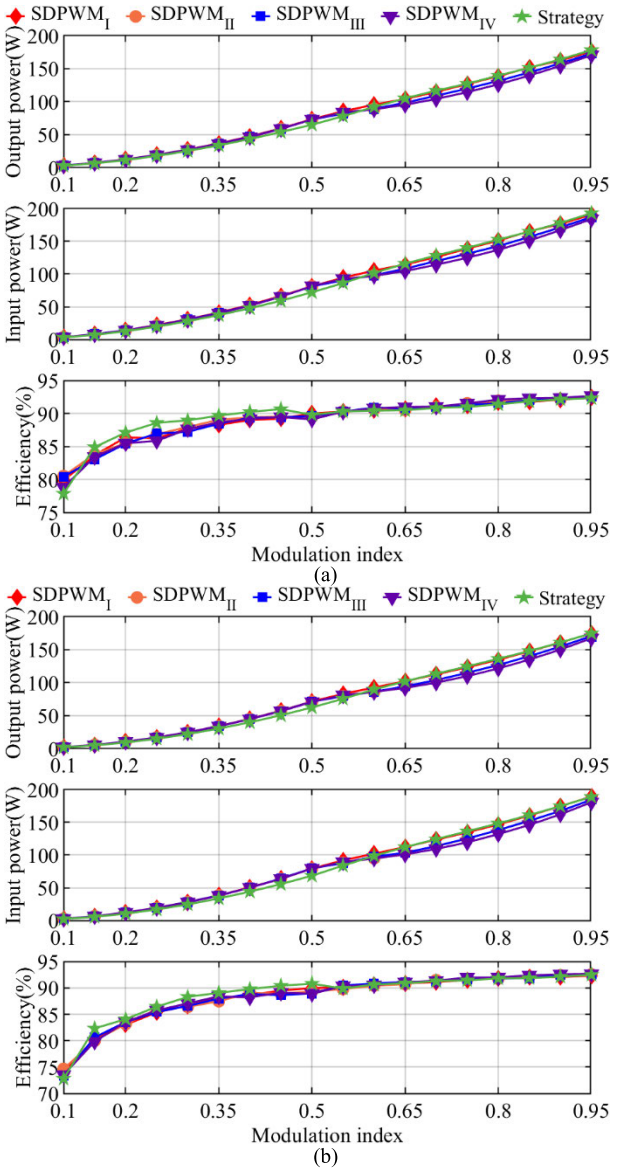

FIGURE 24. Comparison of experimental results of efficiency under different modulation strategies (a) P = 7 (b) P =13.

constraints, and can effectively reduce the amplitude of low-order harmonics when m= 0.25, the harmonic distortion rate of the improved strategy is the lowest. when m= 0.85, the harmonic distortion rate of the improved strategy is basically the same as that of the four SDPWM strategies.

Figs. 22 and 23 compare the experimental results of A-phase current THD and AB line voltage WTHD of four SDPWM strategies and the improved strategy when the modulation index m increases from 0.05 to 0.95. When the m ∈ [0.05, 0.35), the current THD and voltage WTHD of the improved strategy are smaller than those of the four SDPWM modulation strategies, and the output waveform quality is the highest. When m ∈ (0.35, 0.95), the current THD and voltage WTHD of the improved strategy are basically equal to those of the four SPDWM strategies, and the output waveform quality is the same.

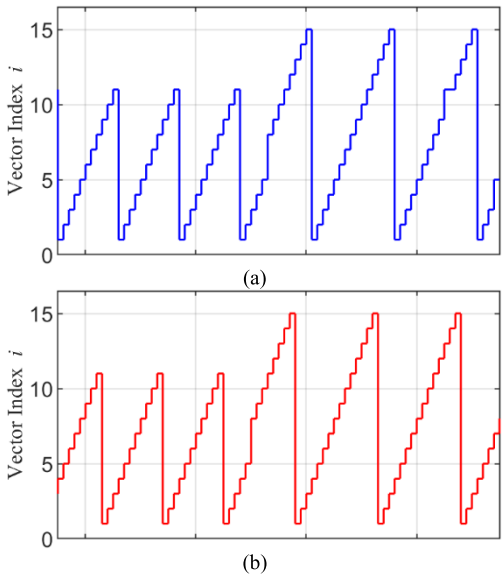

FIGURE 25. Experimental results of reference vector number change under different compensation strategies (a) no angular deviation compensation (b) angular deviation compensation.

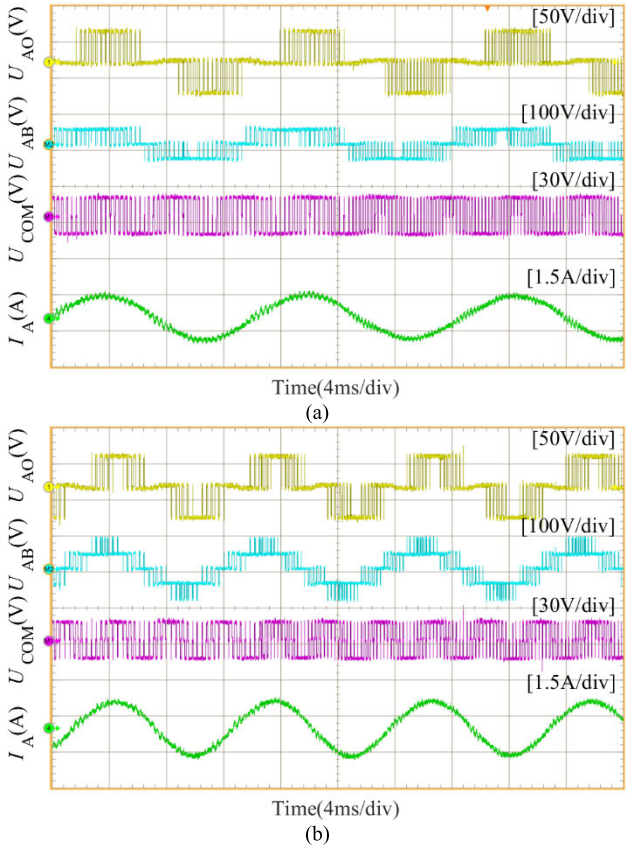

FIGURE 26. Experimental results of modulation strategy switching when $R_L = 42\Omega$ (a) Sync 15 switches to asynchronous modulation (b) Sync 11 switches to Sync 15.

3) EFFICIENCY

The efficiency of the inverter is measured using the PW3337 power meter. Fig. 24 shows the experimental results of the efficiency of four SDPWM strategies and improved strategies

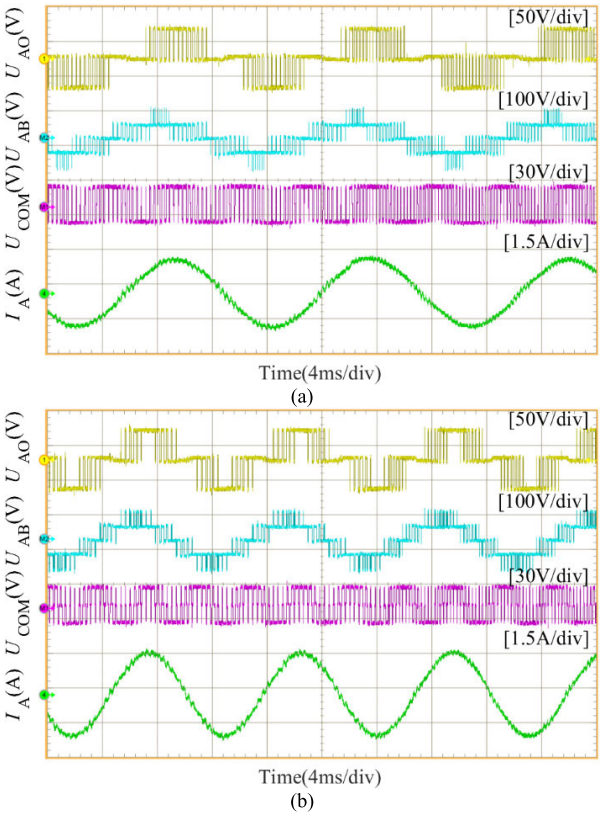

FIGURE 27. Experimental results of modulation strategy switching when $R_L = 21\Omega$ (a) Sync 15 switches to asynchronous modulation (b) Sync 11 switches to Sync 15.

when the modulation index m increases from 0.1 to 0.95. As seen in Figure 24, the inverter's efficiency is related to m, and with the increase of m, the efficiency also gradually increases. When $m < 0.5$, the efficiency of the improved strategy is higher than that of the four SDPWM strategies. When $m > 0.5$, the efficiency of the improvement strategy begins to be lower than that of the four SDPWM strategies, but the difference is not much. By comparing Fig. 24(a) and 24(b), as can be seen that when m is small, the switching times and switching losses increase due to the increase in the number of trigger pulses P, resulting in a lower efficiency when $P = 13$ than when $P = 7$ when the modulation index m is the same.

B. MULTI-MODE MODULATION STRATEGY

Fig. 25 shows the experimental results of reference vector index changes under different compensation strategies during the switching from synchronization 11 to synchronization 15.

As shown in Fig. 25(a), without angular deviation compensation, there is a situation where i mutates from 9 to 11. At this point, the switch status changes from OON to POO, adding two additional switching actions. After angular deviation compensation, i changes continuously, and no additional switching action exists.

The three-phase voltage output by the generator is rectified and then connected to the load resistance RL. Figs. 26 and 27 show the voltage and current waveforms before and after

switching the multi-mode modulation strategy when the load resistance $R_L = 42\ \Omega$ and $21\ \Omega$, respectively.

According to the experimental results, no current impact is generated when switching from synchronization 11 to synchronization 15 or synchronization 15 to asynchronous modulation at different load resistors, and the smooth transition of modulation mode is realized. Under the action of varying modulation strategies, or before and after modulation mode switching, the multi-mode strategy can reduce the common-mode voltage amplitude to $V_{dc}/6$.

VII. CONCLUSION

Aiming at the output waveform distortion caused by high common-mode voltage amplitude and low switching frequency of NPC three-level inverters, this paper analyzes the switching sequence design method to reduce switching times, reduce common-mode voltage amplitude, and improve output waveform symmetry from the perspective of switching sequence design and then proposes an improved modulation strategy. On this basis, the improved strategy is applied to the vector control of PMSM, and a multi-mode modulation strategy for angular deviation and angular delay compensation is proposed. Through the simulation analysis and experimental verification, the following conclusions:

1) Compared with the four SDPWM strategies, the proposed improved strategy reduces the common-mode voltage amplitude in the linear modulation region to $V_{dc}/6$.When N is odd, the improved strategy has fewer switches. The improved strategy's output waveform quality and efficiency are basically the same as the four SDPWM strategies. When the modulation index $m \in [0.05,0.35)$, the improved strategy has lower voltage WTHD and current THD, and higher output waveform quality. When $m < 0.5$, the improved strategy demonstrates higher efficiency.

2) In the closed-loop control, the proposed angular deviation and angular delay compensation scheme can ensure the continuous change of reference vector number and synchronization of the output waveform and avoid additional switching action.

3) The proposed multi-mode modulation strategy ensures the continuity of stator flux trajectory before and after mode switching by limiting the switching phase, reducing the current impact during mode switching, and realizing the smooth transition of modulation modes.

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