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RESEARCH ARTICLE

Effective DC Link Utilization of Multilevel Dual Inverter With Single Source in the Maximal Distention Mode

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ABSTRACT This paper presents an effective voltage control scheme for an open-end winding (OEW) inverter topology with a single DC supply. The proposed configuration consists of a 3-level flying capacitor inverter at one end, and a floating capacitor fed 2-level inverter at the other end. This dual inverter configuration is operated in the maximal distention mode. i.e. the voltage ratio of the inverters is maintained at 4:1 to get the largest number of effective pole voltage levels. Maximal distention mode has the advantage of good power quality and low voltage stress. A major drawback of open-end winding inverter topology with a single source in maximal distention mode is the inability to charge balance the floating capacitor in the full space vector region, which limits the battery utilization as well as the magnitude of output voltage. In this work, a modified modulation technique is proposed to maintain the floating capacitor at the desired level, attaining a 13.1% increase in the output voltage magnitude, resulting in an improvement in the battery utilization in the same proportion, yielding a smaller and less expensive system. Simulation and experimental results corroborate the proposed modulation technique and voltage control scheme on a 3HP, 3-phase, 415V, 1440 rpm open-end winding induction motor.

INDEX TERMS Dual inverter (DI), flying capacitor multilevel inverter (FCMLI), maximal distention, open-end winding induction motor (OEWIM), space vector pulse width modulation (SVPWM).

I. INTRODUCTION

Multilevel inverters (MLIs) are quite popular as it has many advantages like low Total Harmonic Distortion (THD) in current and voltage and reduced switch voltage stress compared to conventional 2-level inverters. Neutral Point Clamped (NPC), Flying Capacitor, Cascade H-bridge, etc. are some of the widely used MLI topologies. As the number of voltage levels in an MLI increases, the NPC MLI and Flying Capacitor MLI (FCMLI) topologies require additional components like clamping diodes and flying capacitors respectively, whereas the cascade H-bridge MLIs require a greater number of isolated sources [1], [2], [3]. Besides these topologies, there are multilevel inverter schemes such as dual inverter open-end winding (OEW) schemes, and modular MLI as derived from the conventional topologies [4]. The main advantage of the dual inverter fed open-end winding configuration is that it has reduced DC link requirement and low voltage rating for the switching devices. Based on the number of sources used, open-end winding MLIs can be classified into two: single source topology and multi-source topology. Single source topology is of two types: (i) single source feeding both the inverters after eliminating common mode voltage [5], [6] (ii) single source feeding one inverter and the other inverter powered by floating capacitor [7], [8], [9], [10]. The main disadvantage of the second scheme is its ineffective utilization of the linear modulation range due to floating capacitor charge balance issues. In [11], OEWIM supplied by two flying capacitor multilevel inverters are discussed. However, the configuration requires two voltage sources. Several OEW topologies are realized with a reduced number of switches in [12]. However, all these configurations

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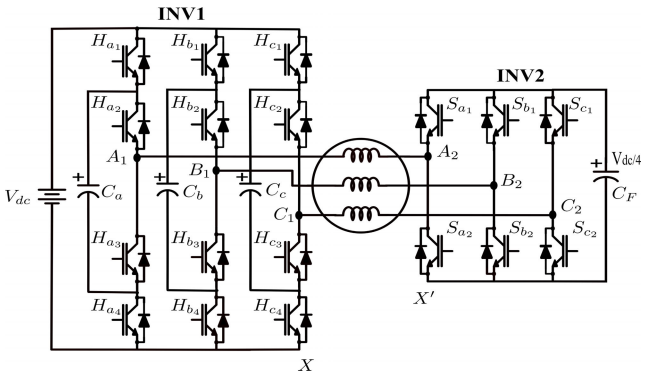


FIGURE 1. Multilevel inverter configuration for the proposed control scheme.

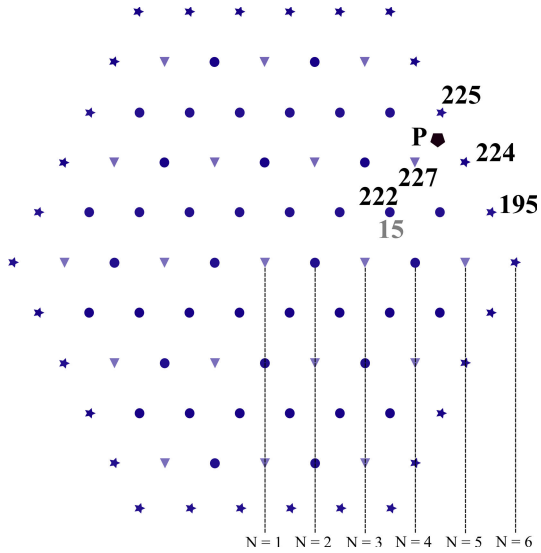


FIGURE 2. Voltage space vector locations in the maximal distention mode. (Yielding 6-Level Space Vector Diagram.)

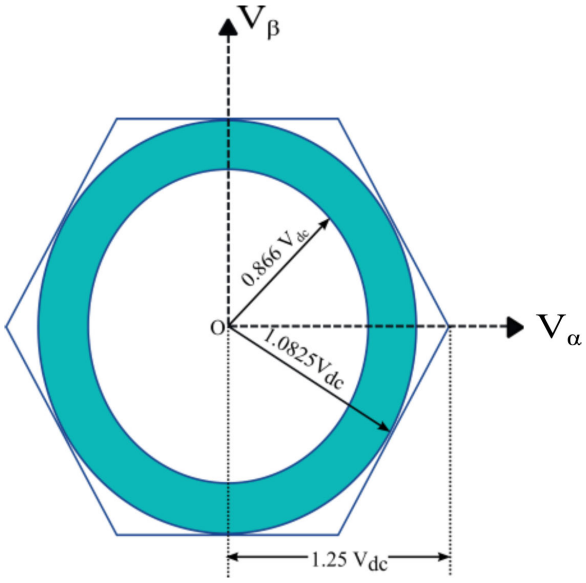


FIGURE 3. Extension of linear modulation range.

use two voltage sources. In [13], an open-end dual source multilevel inverter topology eliminates all the $6n \pm 1$ (n is an odd positive integer) harmonics from the phase voltages in the entire modulation range. Again, this configuration requires two voltage sources. In [14], a 3-level and 2-level inverter are used to feed an OEWIM. With this scheme, a higher waveform quality and an enhancement in linear modulation range are achieved. However, this scheme requires three isolated voltage sources.

A 5-level inverter scheme using a single DC link with a reduced number of floating capacitors and switches for OEWIM drives is proposed in [9]. At a source voltage ratio of 4:1 (see Fig. 1), this topology can generate the maximum number of effective pole voltage levels giving a 6-level space vector diagram (maximal distention mode) [15], [16]. However, due to floating capacitor charge balance issues, the outermost layer of space vectors (Fig. 2) could not be utilized (i.e., space vector locations up to a space vector level of N = 5 could only be used). This restricted the linear modulation range to $0.866V_{dc}$, whereas it could go theoretically up to $1.0825V_{dc}$ as shown in Fig. 3. This reduces the utilization of DC link voltage. In [17], an MLI scheme with cascade H-Bridges is presented. This scheme achieves an extension of the linear modulation range of $0.955V_{dc}$ but uses 30 switches and 6 capacitors. In [18], a 5-level cascade H-Bridge topology with a single source has been proposed. This uses only 21 switches as compared to that in [17], but extension achieved is only upto $0.945V_{dc}$. In [19], an OEWIM scheme capable of extending the linear modulation range to $0.955V_{dc}$ is presented. However, this configuration requires a large number of switches (24 nos.) to get the extended linear modulation range. In [20], two numbers of 3-level NPC inverters are used. The linear modulation range is extended to $0.955V_{dc}$. But the configuration is not operated in maximal distention mode and the configuration requires 24 switches and 4 capacitors.

From the above discussion, it is clear that the existing OEW topologies with a single source in the maximal distention mode do not properly utilize the entire linear modulation range due to less number of redundant states for charge balancing of capacitor. In this paper, a voltage control scheme for a 6-level dual inverter topology for OEW configuration with a single source and reduced number of switches (18nos.) is proposed. This voltage control scheme helps to increase the magnitude of output voltage in the linear modulation range, resulting in increased DC link utilization. By incorporating suitable changes in the modulation technique, the space vectors in the outermost layer are effectively utilized yielding a linear modulation range up to $0.98V_{dc}$.

This paper is organized as follows: Section II discusses the cascade 3-Level-2-Level dual inverter (DI) topology. The operating principle, capacitor voltage control, and modulation technique are explained in section III. Sections IV and V discuss the simulation and hardware results respectively.

Finally, section VI summarizes the key findings and benefits of this work.

II. CASCADE 3-LEVEL-2-LEVEL DI TOPOLOGY

The circuit diagram of the 3-level-2-level cascade DI topology is shown in Fig. 1. The induction motor is fed by a 3-level FCMLI on one end and the other end of the motor is connected to a conventional 2-level inverter with a floating capacitor. A single DC source, V_{dc} is utilized which is connected to the 3-level FCMLI, and this in turn charge balances the floating capacitor of the 2-level inverter at $V_{dc}/4$. Here $H_{a_1}, H_{a_2}, H_{a_3}, H_{a_4}$ are the switches of the phase-A of the flying capacitor inverter (INV1), and S_{a_1}, S_{a_2} are the switches of the phase-A of the 2-level inverter (INV2). H_{a_3} and H_{a_4} are complements of H_{a_2} and H_{a_1} respectively. Also, S_{a_1} is the complement of S_{a_2}. For the FCMLI, level 2 indicates that the top two switches (H_{a_1}, H_{a_2}) are ON, level 1 means alternate switches (H_{a_1} and H_{a_3} or H_{a_2} and H_{a_4}) are ON and level 0 means bottom two switches (H_{a_3}, H_{a_4}) are ON.

- Pole voltage of the 3-level inverter is given by

$$[V_{A_{1X}} \quad V_{B_{1X}} \quad V_{C_{1X}}] = 0.5V_{dc}[H_a \quad H_b \quad H_c] \tag{1}$$

  where, $V_{A_{1X}}$, $V_{B_{1X}}$ and $V_{C_{1X}}$ are the pole voltages of inverter 1 (INV1) and H_a, H_b, and H_c are switching functions that can take values 0, 1 or 2.
- Pole voltage of the 2-level inverter is given by

$$[V_{A_{2X'}} \quad V_{B_{2X'}} \quad V_{C_{2X'}}] = 0.25\ V_{dc}[S_a \quad S_b \quad S_c] \tag{2}$$

  where, $V_{A_{2X'}}$, $V_{B_{2X'}}$, and $V_{C_{2X'}}$ are the pole voltages of inverter 2 (INV2) and S_a, S_b, and S_c are switching functions that can take values 0 or 1.

The resultant voltage space vector or equivalently, the reference voltage V_{ref} for the resultant space vector [13] is given by

$$V_{ref} = V_{A_1A_2} + V_{B_1B_2}e^{j120^\circ} + V_{C_1C_2}e^{j240^\circ} \tag{3}$$

The topology is capable of generating a 6-level space vector diagram, based on this equation, as shown in Fig. 2 for a voltage ratio of 4:1. More details are given in the next section. The outer layer is also considered in this work unlike that in [9] where charge balance issues in the floating capacitor limit the magnitude of V_{ref} to $0.866V_{dc}$ only as already mentioned in the introduction.

III. PRINCIPLE OF OPERATION

A. SPACE VECTOR STRUCTURE

The 6-level space vector structure (SVS) in Fig. 2 represents all the possible pole voltage combinations obtained by superimposing 3-level inverter space vectors and 2-level inverter space vectors [9]. In the 6-level space vector structure, there are a total of 216 states occupying 91 space vector locations. Space vector locations indicated by star notations are states without redundancies. There are adequate numbers of redundant states in the inner layers as denoted by circle or triangle notations. Space vector locations indicated by circles have both charging as well as discharging states. Space vector locations denoted by triangles indicate neutral state locations i.e., the voltage level of the floating capacitor is unaffected [21].

TABLE 1. Mapping of switching function with switching states.

Switching states	1	2	3	4	5	6	7	8	9
Switching function	100	110	010	011	001	101	111	000	002
Switching states	10	11	12	13	14	15	16	17	18
Switching function	012	020	021	022	102	112	120	121	122
Switching states	19	20	21	22	23	24	25	26	27
Switching function	200	201	202	210	211	212	220	221	222

TABLE 2. Status of capacitor C_F, based on switching function of inverter 2 and phase current direction.

Current Direction	Switching function of INV 2							
	000	100	110	010	011	001	101	111
$i_a \geq 0, i_b < 0, i_c < 0$	N	C	C	D	D	D	C	N
$i_a < 0, i_b \geq 0, i_c \geq 0$	N	D	D	C	C	C	D	N
$i_b \geq 0, i_a < 0, i_c < 0$	N	D	C	C	C	D	D	N
$i_b < 0, i_a \geq 0, i_c \geq 0$	N	C	D	D	D	C	C	N
$i_c \geq 0, i_a < 0, i_b < 0$	N	D	D	D	C	C	C	N
$i_c < 0, i_a \geq 0, i_b \geq 0$	N	C	C	C	D	D	D	N

B. CAPACITOR VOLTAGE BALANCING

The voltage of the flying capacitors C_a, C_b, and C_c are maintained at $V_{dc}/2$ and their charging and discharging depend on the respective phase current directions. Voltage balancing of the flying capacitors can be done only during level 1 of the INV1 i.e., when the alternate switches H_{a1} and H_{a3} or H_{a2} and H_{a4} of the INV1 are ON. Charge balancing of the floating capacitor C_F depends on the direction of all the three- phase currents i_a, i_b, and i_c. Table 2 gives the charging and discharging states according to the direction of current for the floating capacitor C_F. Here 'C' stands for charging, 'D' for discharging, and 'N' for neutral status. The currents i_a, i_b, and i_c are taken as positive when they flow from INV1 to INV2 through the respective phase windings.

Consider a point 'P' (indicated by a pentagon notation) in Fig. 2. The nearest 3 vectors concerning point 'P' are 227, 224, and 225. However, it may be noted that by switching these vectors, the balancing of the floating capacitor C_F is not possible due to the absence of a sufficient number of redundant switching states. To balance

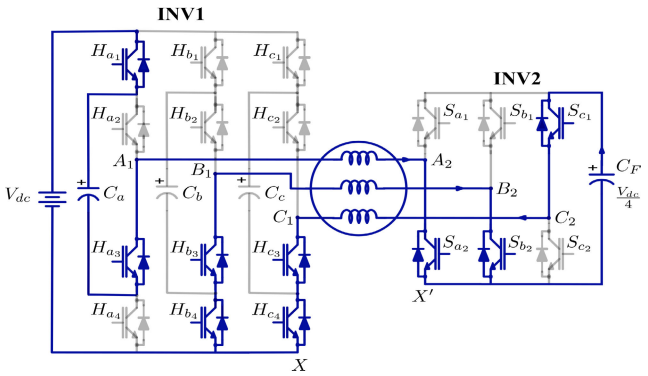


FIGURE 4. Charging of capacitor C_a and discharging of C_F (State 15).

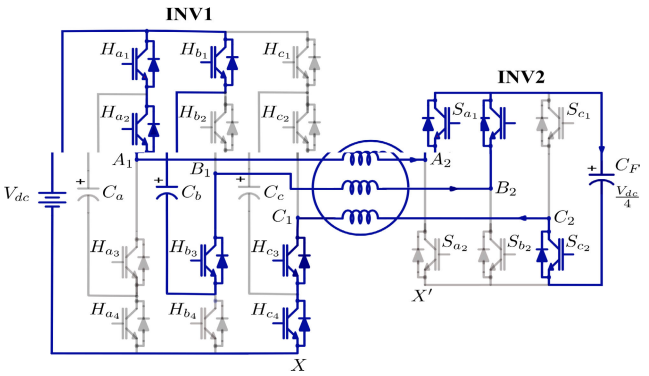


FIGURE 5. Charging of both Capacitor C_b and C_F (state 222).

the capacitor, vectors 222 & 15, 195, and 225 are switched instead of the nearest three vectors. Table 1 indicates all the possible switching states of the inverters (Inverter-I and Inverter-II) and the corresponding switching functions. It may be noted that inverter-II is a 2- level inverter and has only 8 switching states, shown as switching states from 1 to 8 (switching states 1 corresponds to the switching function 100, switching state 2 corresponds to the switching function 110 etc.). Inverter-I is a 3-level inverter and it can have all the 27 states. ie. switching states from 1 to 27 (ie. switching functions from 100 to 222) as indicated in table 1. It may be noted that the last digit of the vector denotes the switching state of INV2. The remaining digits denote the switching state of INV1. The switching state representation of the switching functions makes the notations very compact. For example, in state 15 (see Fig.2), the first number '1' indicates the switching state of INV1 and the second number '5' indicates the switching state of INV2. From Table 1, '1' stands for 100, and '5' stands for 001. Similarly for state 222, '22' (first two digits of '222') stands for 210 (INV1), and 2 (last digit of '222') stands for 110 (INV2). Floating capacitor C_F discharges during state 15 and charges during state 222. Fig. 4 and Fig. 5 show the current paths for states 15 and 222

To understand the charging and discharging of flying capacitor 'C_a', consider INV1 in Fig.4, here the alternate switches of phase-A are ON, say $H_{a_1} = 1$ and $H_{a_2} = 0$. For $i_a \geq 0$, $H_{a1} = 1$; $H_{a_2} = 0$, charges C_a and $H_{a1} = 0$; $H_{a2} = 1$, discharges C_a. But if $i_a < 0$, $H_{a_1} = 0$; $H_{a_2} = 1$, charges C_a and $H_{a_1} = 1$; $H_{a_2} = 0$, discharges C_a. Similar is the case with other phases.

C. MODULATION TECHNIQUE

In this paper, the modulation index is defined as

$$M = \frac{V_{ref}}{1.25 V_{dc} \cos 30^\circ} \tag{4}$$

where V_{ref} is the length of the reference vector.

For the modulation, space vector pulse width modulation (SVPWM) is implemented using the hexagonal decomposition method, i.e., each hexagon is mapped to a 2-level hexagon [22]. For higher level multi-level inverters where the density of space vectors in the space vector diagram is very large, nearest vector switching methods [23], [24] may also be attempted which obviates duty cycle computation burden at the expense of slightly higher harmonic distortion. However, since the number of levels is not large (6-levels in this paper), the hexagonal-decomposition based duty cycle computation is adopted and it is a very simple and straightforward scheme.

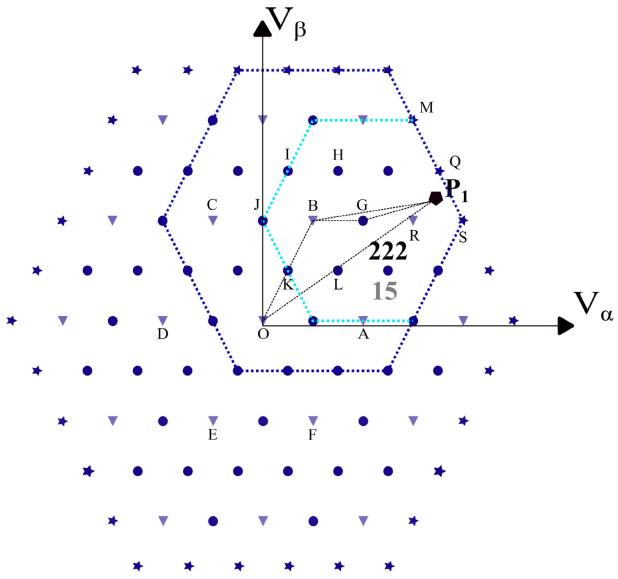


FIGURE 6. Mapping for $V_{ref} > 0.866 V_{dc}$, outer layer.

In the outer layer i.e., $V_{ref} > 0.866 V_{dc}$, the 6-level hexagon (outermost hexagon) is divided into six 4-level hexagons, then each 4-level hexagon is further divided into six 3-level hexagons. These 3-level hexagons are mapped to the vectors of the basic 2-level hexagon as shown in Fig. 6. The centre of the 6-level hexagon is indicated as 'O'. Points A, B, C, D, E, and F are the centres of the 4-level hexagons. Points G, H, I, J, K, and L are the centres of the 3-level hexagons.

Consider any arbitrary point 'P_1' in the outer layer (see Fig. 6). Point 'P_1' lies in the 3-level hexagon with centre 'G',

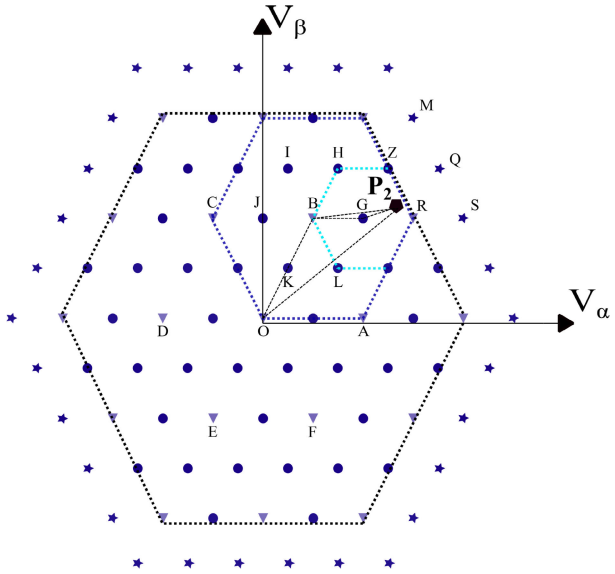


FIGURE 7. Mapping for $V_{ref} \leq 0.866V_{dc}$, inner layer.

which is a part of the 4-level hexagon with centre 'B'. The criteria for selecting the switching vectors are as follows:

1) Shift the centre 'O' to centre 'B'.
   $BP_1 = OP_1 - OB$
2) Shift the centre 'B' to centre 'G'.
   $GP_1 = BP_1 - BG$
3) Nearest vectors are Q, R, and S but to balance the floating capacitor voltage, vectors M, G, and S are switched.

The switching time T_1, T_2, and T_0 are given by:

$$T_1 = K\left(V_{\alpha 0}\sin\left(\frac{n\pi}{3}\right) - V_{\beta 0}\cos\left(\frac{n\pi}{3}\right)\right) \tag{5}$$

$$T_2 = K\left(V_{\beta 0}\cos\left(\frac{(n-1)\pi}{3}\right) - V_{\alpha 0}\sin\left(\frac{(n-1)\pi}{3}\right)\right) \tag{6}$$

$$K = \left(\frac{T_s}{\sin(\frac{\pi}{3})\frac{V_{dc}}{2}}\right) \tag{7}$$

$$T_0 = T_s - (T_1 + T_2) \tag{8}$$

Here $V_{\alpha 0}$ and $V_{\beta 0}$ are the components of vector GP_1 in $\alpha - \beta$ frame. The switching time of the active vectors is denoted by T_1 and T_2 and that of the null vector is T_0. T_s is the switching period and n is the sector number which can vary from 1 to 6.

Selection of switching vectors for the inner layer i.e., $V_{ref} \leq 0.866V_{dc}$ is depicted in Fig. 7. Here the 5-level hexagon with centre 'O' is considered and divided into six 3-level hexagons with centres at A, B, C, D, E, and F. Next each 3-level hexagon is further divided into six 2-level hexagons with centres G, H, I, J, K, and L. For an arbitrary point P_2 in the inner layer, the nearest vectors G, R, and Z are switched and the corresponding switching times are calculated using (5)-(8) by replacing $\frac{V_{dc}}{2}$ with $\frac{V_{dc}}{4}$.

IV. SIMULATION RESULTS

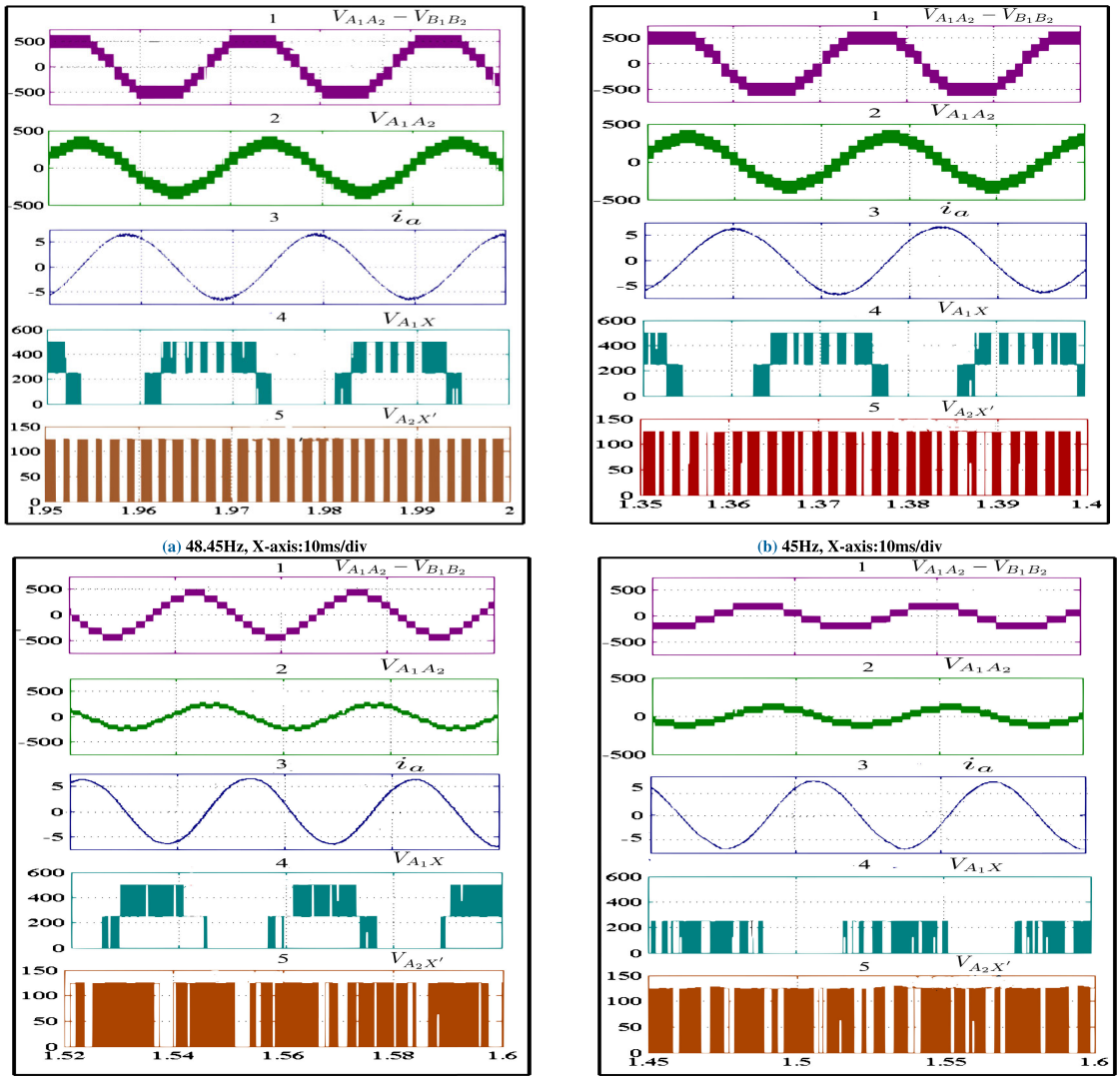
The simulation was done using MATLAB and PLECS software. All the results are shown at no load operation as it gives the worst case THD performance. Fig. 8 shows the simulation results for 15Hz, 30Hz, 45Hz, and 48.45Hz operation. It can be noted that as frequency decreases, the number of levels gets reduced. At 48.45Hz, 45Hz, and 30Hz, the pole voltage of INV1 has 3 levels, while at 15 Hz, it has only 2 levels. As shown in Fig. 8 pole voltage of INV2 has a 2-level operation at all frequencies.

The performance of capacitors during charging is shown in Fig. 9. No pre-charging is used and therefore initially the capacitor voltages are zero and rise to the desired values from the initial uncharged voltage. The flying capacitor C_a and floating capacitor C_F are maintained at $V_{dc}/2$ and $V_{dc}/4$ respectively, irrespective of the magnitude of output voltage. However, for the outer space vector region, charge balancing of floating capacitor C_F is quite difficult as the redundant state switching time is less. Therefore, it takes a longer time (about 3s) to reach the steady state value (refer to Fig. 9d). It may also be noted that the time to attain a steady state value for flying capacitor voltage V_{C_a} is quite small and is not affected by the change in magnitude of V_{ref}.

Fig. 10 shows the simulated plot of the harmonic spectrum of the phase current (magnitude in % of fundamental) and the THD_i Vs frequency graph is shown in Fig. 10b. It can be seen that the modulation strategy gives low THD. Theoretically, the magnitude of V_{ref} could be varied up to $1.0825V_{dc}$ (refer Table 3) i.e., an increase of 25% in the linear range. Due to charge balance issues, the magnitude of V_{ref} could be varied only up to $1.05V_{dc}$ (21.25% increase in the linear region) in the simulation study with the switching frequency of 5kHz. A lower value is obtained for V_{ref} in the hardware experiment compared to the simulation due to various non-idealities and power losses. Table 3 gives a comparison of attainable modulation index, maximum V_{ref}, and DC link utilization attained with the proposed scheme with that in [9] of the 3-level-2-level DI in the maximal distention mode. It can be noted that the proposed method gives much better performance.

V. EXPERIMENTAL RESULTS

Open loop v/f control is performed on a 3-phase 2.2kW, 415V, 50Hz 1440 rpm OEW induction motor to verify the operation of the proposed modulation technique. The experimental setup is shown in Fig. 11. The proposed scheme is implemented using DSP TMS320F28335 and FPGA spartan 6. The block diagram of the implementation scheme is shown in Fig. 12. The FPGA was used to provide deadtime for all the switches and also for realizing the space vector PWM and capacitor charge balance through suitable operation of power switches from the PWM data as available on the PWM ports of the DSP and the capacitor charge status (Please see Fig. 12). The DSP processor alone cannot do the operations as the DSP operates sequentially whereas the PWM operation and charge balance of the FC multilevel inverter demands



(a) 48.45Hz, X-axis:10ms/div

(b) 45Hz, X-axis:10ms/div

(c) 30Hz, X-axis:20ms/div

(d) 15Hz, X-axis:50ms/div

FIGURE 8. Relevant waveforms at (a) 48.4 Hz operation (b) 45 Hz operation, (c) 30Hz operation, (d) 15 Hz operation, Traces : (1) Line-Line Voltage of the system ($V_{A_1A_2} - V_{B_1B_2}$), Y-axis : 500V/div (2) Phase Voltage $V_{A_1A_2}$, Y-axis : 500V/div (3) Phase Current I_A, Y-axis: 5A/div (4) INV1 Pole Voltage V_{A_1X}, 200V/div (5) INV2 Pole Voltage $V_{A_2X'}$, Y-axis : 50V/div.

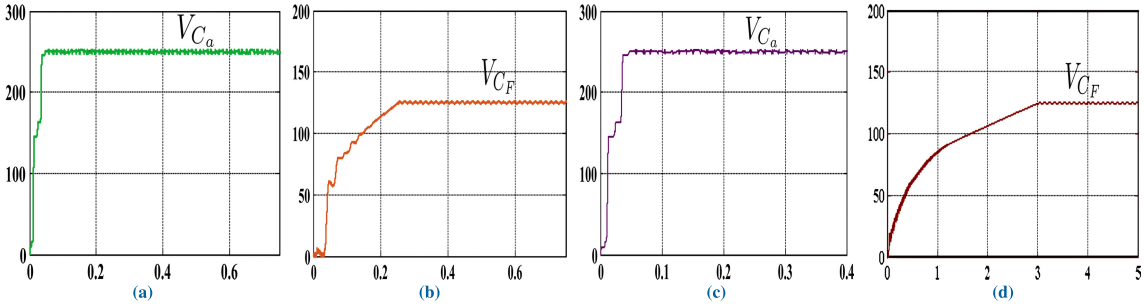
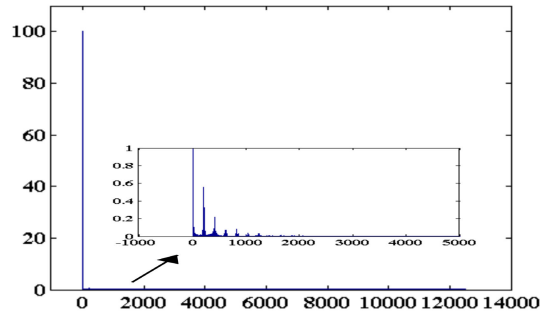
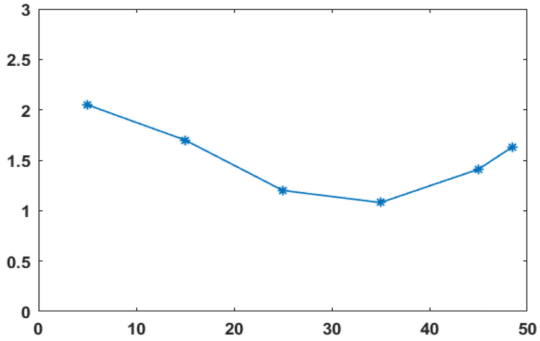


FIGURE 9. Performance of the capacitors during charging: (a) Capacitor Voltage V_{C_a} at 45Hz Y-axis:100V/div, X-axis: 0.2s/div; (b) Capacitor Voltage V_{C_F} at 45Hz Y-axis:50V/div, X-axis: 0.2s/div; (c) Capacitor Voltage V_{C_a} at 48.45Hz Y-axis:100V/div, X-axis: 0.1s/div; (d)Capacitor Voltage V_{C_F} at 48.45Hz Y-axis:50V/div, X-axis: 1s/div.

simultaneous operation of different switches. Two current sensors and five voltage sensors are used to convey the status of the stator currents and DC link and capacitor voltages to the ADC of the DSP. The PWM signals and status of voltages and currents are communicated to FPGA and the switches are triggered after decoding the information. The switching



(a) Simulated plot of the harmonic spectrum of the phase current (magnitude in % of fundamental) at 48.45Hz:Y-axis: 20%/div, X-axis:2000 Hz/div THD_i=1.62%



(b) THD_i Vs frequency plot;Y-axis: 0.5%/div, X-axis:10Hz/div

FIGURE 10. Current THD : Simulation results.

TABLE 3. Control strategy comparison.

Modulation Technique		Maximum Modulation Index	DC Link Utilization	Maximum Output Voltage
Theoretical Value		1	100%	$1.0825V_{dc}$
Scheme used in paper [9]		0.8	80%	$0.866V_{dc}$
Modified Modulation Technique	Simulation Results	0.97	97%	$1.05V_{dc}$
	Hardware Results	0.905	90.5%	$0.98V_{dc}$

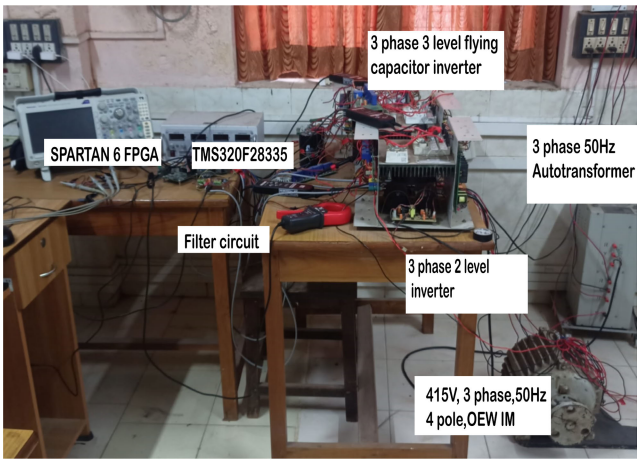


FIGURE 11. Experimental setup.

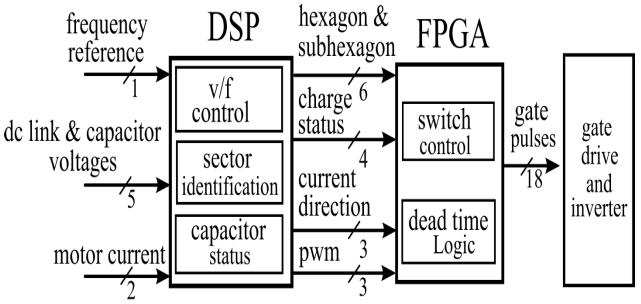


FIGURE 12. Functional block diagram of the control scheme.

frequency is 5kHz and a dead time of 2 μs is also provided. The design of capacitors is done according to the equation $C = (I_p T_s/\Delta V)$. Here, I_p is the peak phase current, T_s is the sampling period and ΔV is the peak ripple voltage of the capacitor. The capacitance value is proportional to the magnitude of the current. So as power rating increases current increases and hence required capacitance value also increases. The pole voltages are measured using high voltage differential voltage probes (Tektronics P5200A). The phase currents are measured using current probes (Tektronics A621). The inverter and motor specifications are shown in Table 4. The steady-state results are shown in Fig. 13. The phase voltage, phase current, and pole voltage of inverter 1 and inverter 2 for 45Hz, 30Hz, and 15 Hz are depicted in Fig. 13 (a), (b), and (c) respectively. It can be seen that the current waveform is sinusoidal with low distortion. Fig. 13 (d) shows the inverter 1 floating capacitor voltage, inverter 2 flying capacitor voltage, and input DC link voltage respectively. The results are shown at no load for a DC link voltage of 470V. At 45 Hz and 30 Hz operation, the pole voltages of inverter 1 have 3-level output, and inverter 2 has 2-level output.

But at 15Hz operation pole voltages of both the inverters have 2-level output. Fig.15 shows the DC link voltage and flying capacitor voltages of respective phases. It can be observed that the all the flying capacitor voltages are well balanced at $V_{dc}/2$. Fig. 17 illustrates the effectiveness of the proposed charge controlling scheme in reinstantiating the capacitor voltage. Fig. 17 shows the phase current i_a, the flying capacitor voltage V_{C_a}, and the floating capacitor voltage V_{C_F}. At points 'A' and 'C' the charge control of V_{C_a} and V_{C_F} is disabled and is re-established at 'B' and 'D' respectively. The time taken for C_F to regain the voltage is a bit longer when compared to that of C_a. This is because as 'V_{ref}' increases the time taken in stabilizing

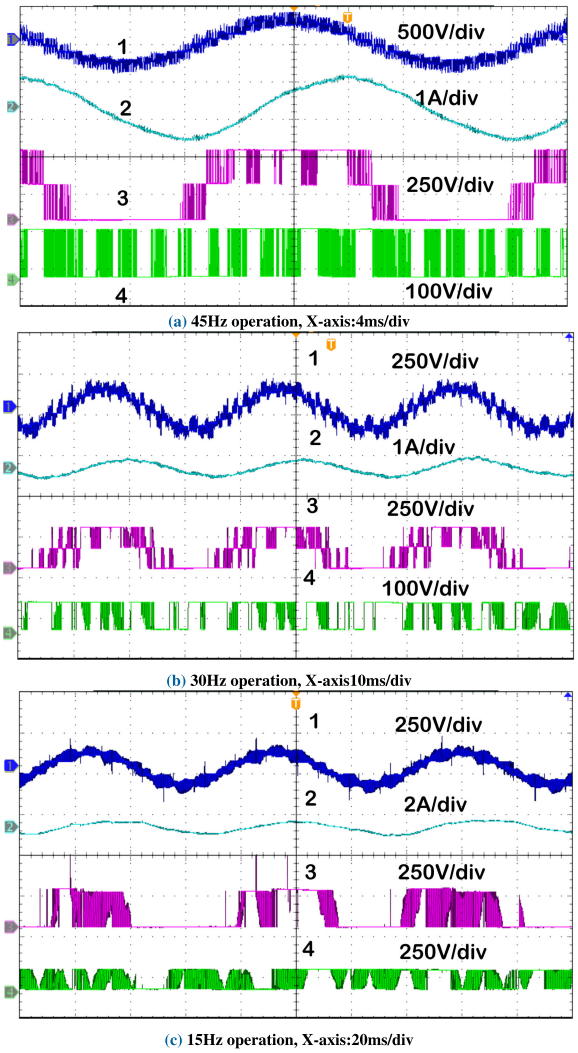


FIGURE 13. Relevant waveforms at (a) 45Hz operation, (b) 30Hz operation, (c) 15Hz operation, Traces: (1) Phase Voltage $V_{A_1A_2}$, (2) Phase Current I_A, (3) INV1 Pole Voltage V_{A_1X}, (4) INV2 Pole Voltage $V_{A_2X'}$.

TABLE 4. Inverter and motor specifications.

Components	Specifications
Motor specifications:	3 HP, 3-Phase induction motor Voltage: 415V Current: 4.2A Speed: 1440 rpm Poles: 4
Inverter specifications:	IGBT:SKM100GB12T4 DC rail voltage: 470V DC rail Capacitor: 1100μF Flying Capacitor : 2200μF Floating Capacitor 4400μF
DSP Processor	TMS320F28335 CPU Frequency:150MHz ADC resolution: 12 bit
FPGA	SPARTAN 6 CPU Frequency: 50MHz

the voltage of floating capacitor V_{C_F} is more, due to the lack of sufficient redundant states in the outer layer. Fig.16a shows the measured harmonic spectrum of phase current

TABLE 5. Comparison of other 5-Level inverters with extension of linear modulation range.

TOPOLOGY	Switches	Capacitors	Diodes	DC Supply	Linear Modulation Range
Paper [17]	30	6	0	1	$0.955V_{dc}$
Paper [18]	21	5	12	1	$0.945V_{dc}$
Paper [19]	24	4	0	1	$0.955V_{dc}$
Paper [20]	24	4	12	1	$0.955V_{dc}$
Proposed Scheme	18	4	0	1	$0.98V_{dc}$

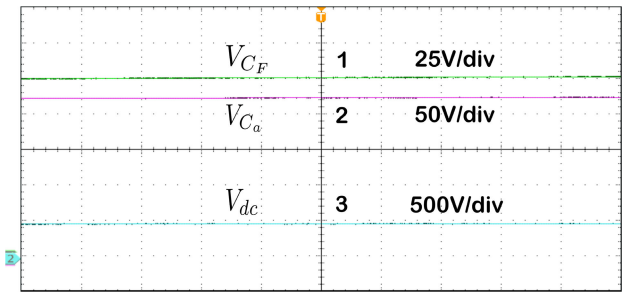


FIGURE 14. Capacitor Voltages Traces: (1) INV2 Floating capacitor Voltage V_{C_F}, (2) INV1 Phase A Flying capacitor Voltage V_{C_a}, (3) Input DC link Voltage V_{dc}.

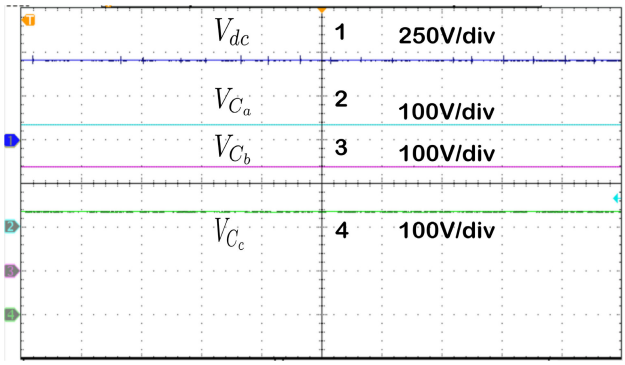
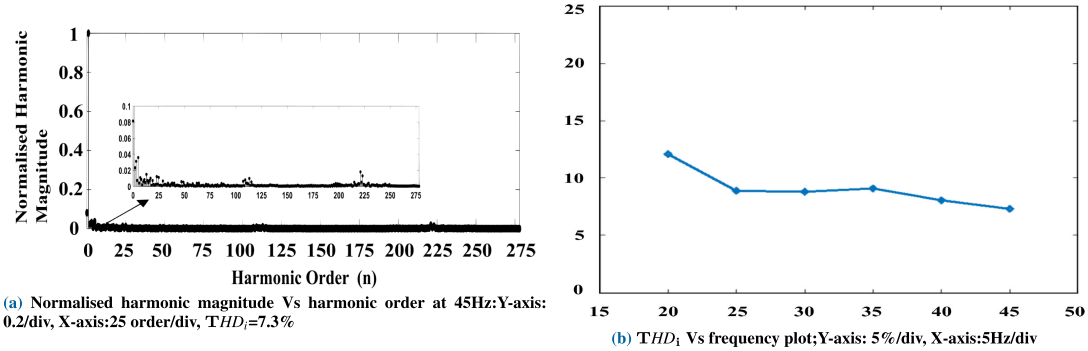


FIGURE 15. DC link and Flying capacitor voltages, Traces : (1) DC link voltage V_{dc} (2) Phase-A flying capacitor voltage V_{C_a} (3) Phase-B flying capacitor voltage V_{C_b} (4) Phase-C flying capacitor voltage V_{C_c}, at 45 Hz operation.

at 45 Hz. In hardware the measured THD is 7.3 %. Fig.16b depicts the THD Vs frequency plot. It can be noted that at higher frequencies THD is lower compared to that at lower frequencies. The THD figures are higher in the hardware results due to various non-idealities such as deadtime, switching delays, core saturation etc.

The waveforms during the starting of the motor are shown in Fig. 18. It can be seen that the floating capacitor and flying capacitor voltages rise to the desired value without any pre-charging requirement. The acceleration characteristics are illustrated in Fig. 19. It can be noted that smooth acceleration is obtained with the proposed scheme. In both steady and transient states, the capacitor voltages are well balanced. As given in Table 3, the modified modulation technique achieves 90.5% DC link utilization. The modulation index



(a) Normalised harmonic magnitude Vs harmonic order at 45Hz:Y-axis: 0.2/div, X-axis:25 order/div, THD_i=7.3%

(b) THD_i Vs frequency plot;Y-axis: 5%/div, X-axis:5Hz/div

FIGURE 16. Current THD : Hardware results.

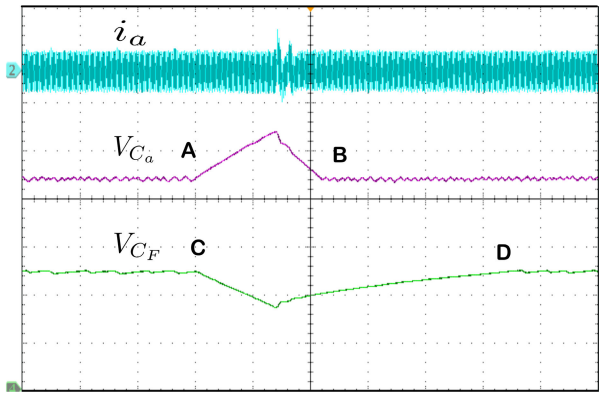


FIGURE 17. Disabling the charge control scheme of flying capacitor V_{C_a} of inverter 1 at time 'A' and re-establishing the charge control at 'B'; and that of floating capacitor V_{C_F} at time 'C' and reestablishing the charge control at 'D', at 45 Hz operation and x-axis:1s/div.

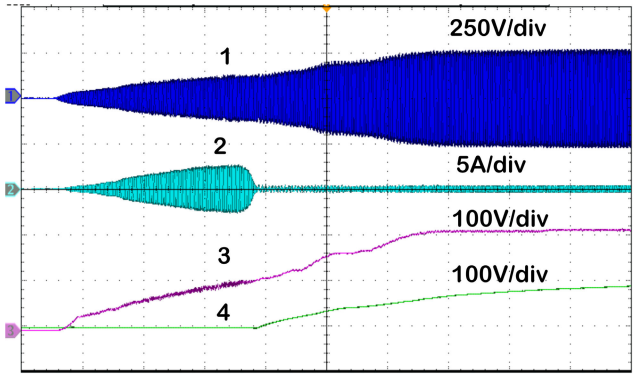


FIGURE 18. Voltage and current waveforms of Phase-A during starting up of the motor, x-axis 2s/div, Traces (1) Phase 'A' voltage; (2) Phase 'A' current; (3) Flying capacitor voltage V_{C_a}; (4) Floating capacitor voltage V_{C_F}.

could be varied up to 0.905, whereas in [9], it was limited to 0.8. Also, the maximum possible V_{ref} is extended to $0.98V_{dc}$, which was earlier limited to $0.866V_{dc}$. Thus, the magnitude of output voltage could be increased by 13.1% in the linear region. This improvement could be achieved without any topological change demanding more switches as that in [19], demonstrating the usefulness of the proposed scheme. Table 5 essentially gives a comparison with other 5-level inverters which attempts linear modulation range extension.

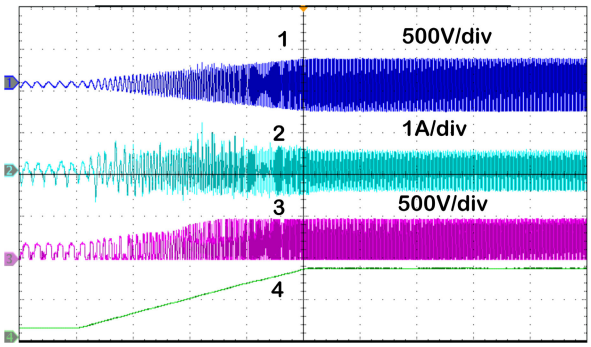


FIGURE 19. Voltage and current waveforms of Phase-A during acceleration of the motor, x-axis 1s/div: Traces (1) Phase voltage $V_{A_1A_2}$; (2) Phase current i_a; (3) inverter 1 pole voltage; (4) frequency reference.

The proposed scheme achieves the largest extension of linear modulation with lowest number of devices.

VI. CONCLUSION

The space vector modulation and charge balancing of capacitors of a dual inverter with a minimum number of switches, fed from a single DC source have been analyzed and the results are presented. With the proposed modulation technique, the partitioning of the space vector diagram has been modified to achieve charge balance for the floating capacitors thus utilizing the entire space vector region for the modulation unlike that has been reported hitherto in literature.

The proposed modulation strategy accounts for a 25% increase in the magnitude of output voltage in the linear modulation range theoretically. However, this demands very large capacitance values and a high switching frequency. With a realistic switching frequency of 5kHz for medium voltage drives and capacitance values of 2200μF and 4400μF respectively for flying and floating capacitors, the output voltage magnitude and battery utilization could be increased by 13.1%, which is a significant achievement as it helps to achieve a more compact and cost-effective system. The proposed scheme can be effectively used in applications where the load can be open-ended such as high-power motor drives in ship propulsion & e-mobility, grid interactive inverters, and STATCOMS with open end winding transformers.

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