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RESEARCH ARTICLE

An Active Track and Hold Circuit With Linearity Enhancement Technique and Its Analysis Using Volterra Series

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ABSTRACT This paper presents a comprehensive analysis of active track and hold (T/H) circuits that utilize switched source followers and time-divided post-distortion cancellation. In the track phase, the circuit acts as an active buffer and transfers an input signal, including track-mode distortion caused by the buffer's nonlinear transconductance. In the hold phase, the transferred signal is held but hold-mode distortion is added, including hold-mode feed-through and hold pedestal error, causing deterioration of the circuit's linearity. The time-divided post-distortion cancellation technique improves the circuit's linearity by cancelling the track-mode distortion with the hold-mode distortion. Volterra series analysis offers a comprehensive understanding of the operation. 17 sample chips were measured to verify stable cancellation operation. It shows a mean SFDR value of 77.1 dB and a standard deviation of 1.8 dB with 9mW power consumption.

INDEX TERMS CMOS, track and hold, RF sampling, source follower, Volterra analysis, distortion cancellation.

I. INTRODUCTION

Interest in high-speed time interleaved (TI) ADCs has risen as they have the potential to reduce the complexity, power consumption, and cost of the traditional receiver due to its wide band characteristic [1], [2], [3], [4], [5], [6], [7], [8], [9], [10]. Similarly, the use of front-end track and hold (T/H) circuits to drive TI ADC has gained attention [5], [6], [7], [8], [9], [10], [11], [12], [13]. With the rise in ADC speed and performance, demanding performance requirements are placed on T/H circuits [14], [15], resulting in various efforts to enhance their performance [6], [7], [8], [9], [10], [11], [16], [17], [18], [19], [20]. An active T/H circuit has benefits on speed, but it requires a design consideration for linearity issue [11], [21], [22]. As the active T/H circuit, studies on switched-buffer T/H circuits using an InP/SiGe HBT bipolar or CMOS process to perform charge-domain sampling exist [11], [21], [22], [23], [24], [25], [26], [27]. One of the popular T/H circuits is composed of a common-source amplifier as a pre-amplifier, a switched source follower (SF) as a buffer and a hold capacitor (C_H) shown in Fig. 1 (a). It performs charge-domain sampling, which offers improved speed [11], [21]. However, it has a drawback for the linearity. During the track phase, the switched SF transfers a signal to the hold capacitor as an SF. The output contains distortion from the nonlinear transconductance of the SF, which is called track-mode distortion. After entering the hold phase, the SF maintains the hold voltage at v_{out} by decreasing the voltage at the gate node (V_b) as much as $I_2 \times R_{load}$ and turning off the M_S. This is achieved by switching the current path with the switch (S_1), as shown in Fig. 1 (b). In the hold mode, hold-mode distortion occurs due to the track-to-hold transition and other hold-mode errors. To overcome the problem of hold-mode distortion, previous studies have been conducted on the linearization of switched-buffer or Switched SF T/H circuits. One technique is the cross-coupled capacitor approach to address the

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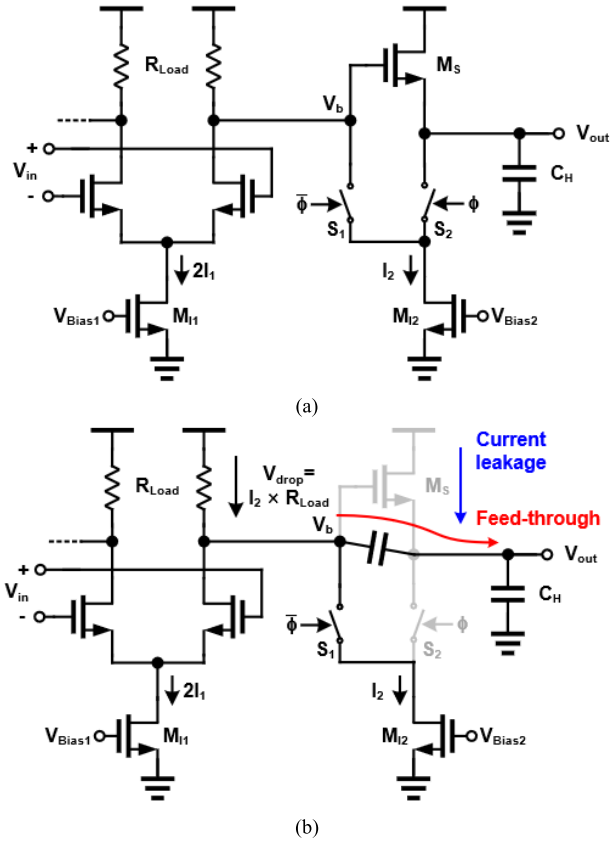

FIGURE 1. (a) Diagram for the conventional active T/H circuit using switched SF and (b) its hold-mode diagram.

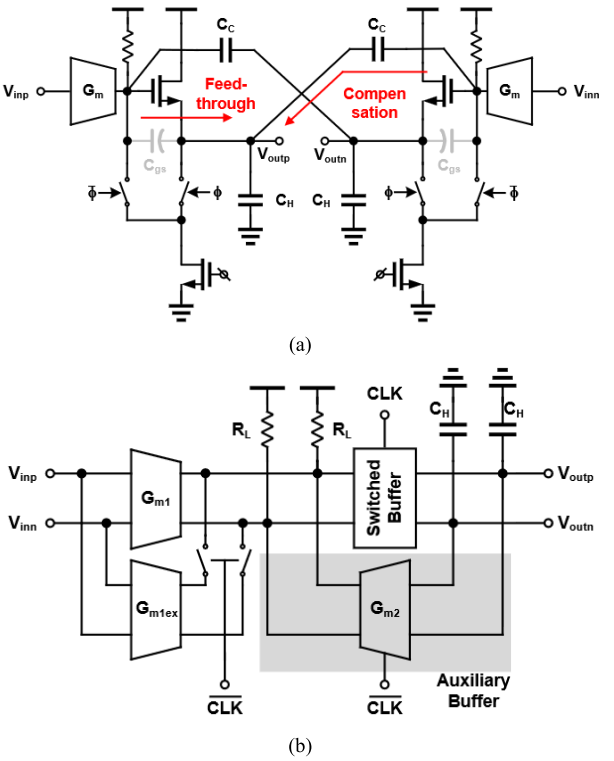

FIGURE 2. Schematic diagrams of the T/H circuit with the (a) cross-coupled capacitor technique [9], [24], [25] and (b) mode-switching architecture [25], [26].

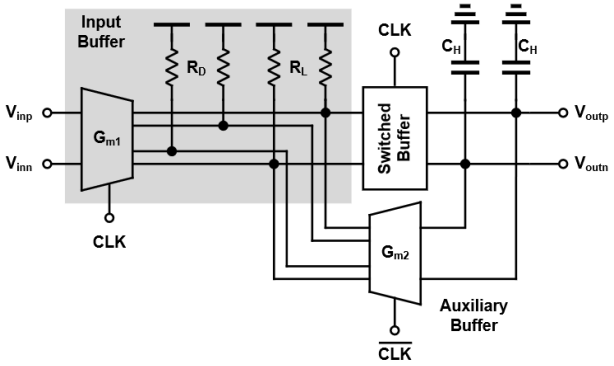

FIGURE 3. Schematic diagram of the T/H circuit with double-switching architecture [18].

feed-through problem. This aims to reduce clock leakage to the hold capacitor [11], [26], [28]. Fig. 2 (a) shows an example circuit for this technique. Dummy capacitors (C_C) are used to compensate the feed-through from the gate-source capacitor (C_{gs}) through a cross-coupled connection. Another technique is the mode-switching architecture. To avoid reliance on the matching of capacitors, mode-switching architectures have been proposed [28], [29]. Fig. 2 (b) shows the circuit diagram of this architecture. It uses an additional transconductance stage (G_{m1ex}) connected to the load resistors (R_L) during the hold phase. During this phase, the G_{m1ex} stage produces an opposing phase signal, canceling and reducing the signal transferred by the G_{m1} stage. As a result, the transconductance stage operates in common mode and reduces the feed-through problem, but a matching issue still exists between G_{m1ex} and G_{m1}.

To reduce dependence on matching, the double-switching architecture was proposed based on the mode-switching architecture [18]. Fig. 3 shows the diagram of this architecture. It involves switching the buffer connection by directing the output between the actual load R_L and the dummy load R_D using switches. Since it does not require cancellation with an opposing signal, the G_{m1ex} stage is not necessary in this structure.

The time-divided post-distortion cancellation (TDPD) was proposed which can enhance the linearity of a switched source follower T/H circuit [19]. The TDPD technique enhance linearity by canceling the track mode nonlinearity with the hold mode nonlinearity. The TDPD circuit acts as an active buffer and transfers an input signal, including track-mode distortion caused by the buffer's nonlinear transconductance in the track phase. In the hold phase, the transferred signal is held but hold-mode distortion is added, including hold-mode feed-through and hold pedestal error which deteriorate linearity in a conventional switched source follower T/H circuit. The TDPD improves linearity by cancelling the track-mode distortion from transconductance with the hold-mode distortion from the hold pedestal error while minimizing the hold-mode feedthrough.

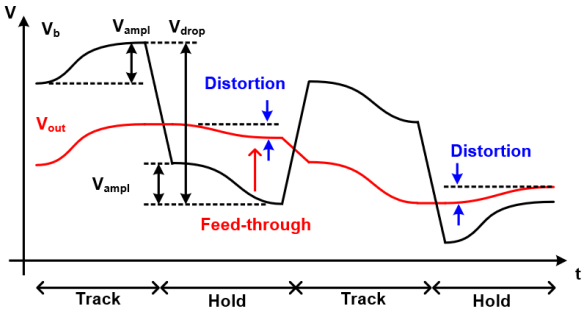

FIGURE 4. Timing diagram for V_b and v_{out} node of Fig. 1.

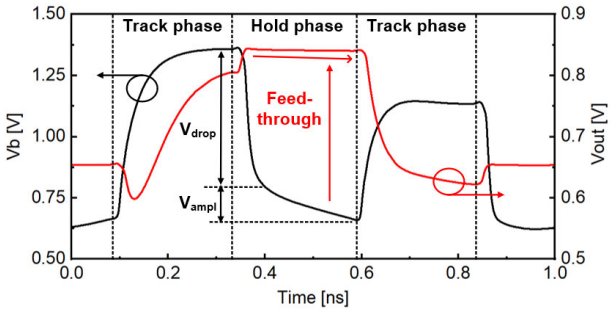

FIGURE 5. Simulation result for the hold-mode feed-through.

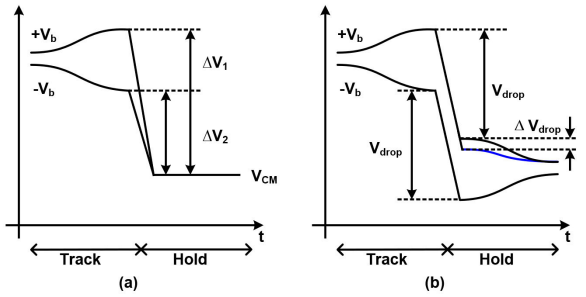

FIGURE 6. Timing diagram of differential V_b node (a) for transitioning to V_{CM} and (b) for decreasing as much as V_{drop}.

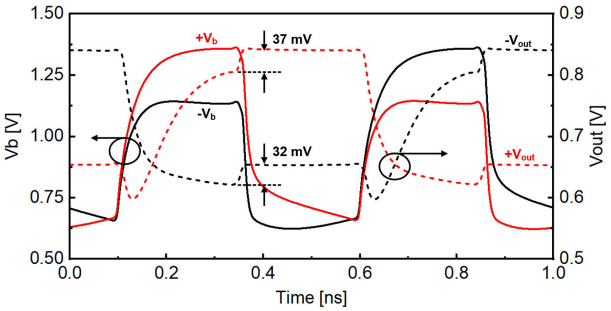

FIGURE 7. Simulation result for the hold pedestal error.

This paper aims to provide a comprehensive explanation of the TDPD T/H circuit with a mathematical analysis using Volterra series starting from the understanding of the track and hold mode behaviors of the switched source follower T/H circuit. Measurement results from multiple sample chips are provided to verify stable cancellation operation of the TDPD.

The remainder of this paper is organized as follows. Section II. discusses the behaviors and distortion of the switched source follower T/H circuit. Section III discusses the design of the TDPD T/H circuit. In Section IV, Volterra series analysis is performed for the equations for both the track-mode and hold-mode distortions. Further, the role of an additional MOS capacitor in the distortion cancellation is described. Section V presents the measurement results. Finally, Section VI presents the conclusions.

II. DISTORTION OF SWITCHED SOURCE FOLLOWER

A. HOLD-MODE DISTORTION (1): FEED-THROUGH

Hold-mode distortions were identified as a cause of poor linearity performance in the switched SF shown in Fig. 1. The first source of hold-mode distortion is hold-mode feed-through. As shown in Fig. 4, it occurs due to changes in the input signal during the hold phase and becomes more pronounced as the signal frequency approaches the Nyquist rate. During the hold phase, a signal swing is induced at the V_b node and approaches the peak amplitude (V_{ampl}). Subsequently, the signal is transferred to the C_H through the gate-source capacitance (C_{gs}) of the M_S. This results in the creation of a distortion that depends on the frequency and magnitude of the input signal. Fig. 5 illustrates the simulation results of the V_b and v_{out} nodes. When the input signal is close to the Nyquist rate during the hold phase, it alters the V_b node, causing distortions in the v_{out} node. Studies have been conducted to address this hold-mode distortion problem, but they have drawbacks such as increased power consumption, complicated design, or limitations in performance due to matching properties [11], [21], [22], [26], [28], and [29]. Moreover, if the magnitude of V_{drop} is insufficient to turn off M_S completely, current leakage occurs in addition to feed-through, leading to further distortion. Therefore, a high voltage drop (V_{drop}), which is the product of Is and R, is necessary to ensure complete turn-off of the M_S, but this leads to high current consumption.

B. HOLD-MODE DISTORTION (2): HOLD PEDESTAL ERROR

The next distortion is the hold pedestal error, which is caused by the voltage drop that occurs at the track-to-hold transition [20], [22]. $+V_b$ and $-V_b$ in Fig. 6 indicate the differential signal at the V_b node in Fig. 1 (a). As shown in Fig. 6 (a), when the voltages of the two nodes decrease to the specific voltage (V_{CM}) to turn off the SF, there are different voltage drops, ΔV_1 and ΔV_2, depending on the input signal. These voltage drops affect the differential output differently through the parasitic capacitance between the V_b and v_{out} nodes. Previous studies have tried to make a constant voltage drop (V_{drop}) independent of the input signal, as shown in Fig. 6 (b), utilizing the pre-amplifier's load resistor and current source. However, there are still the differences in V_{drop} (ΔV_{drop}) and the pedestal error due to the channel length modulation.

In addition, during the hold phase, the signal is not transferred to the output, but the pre-amplifier and current sources

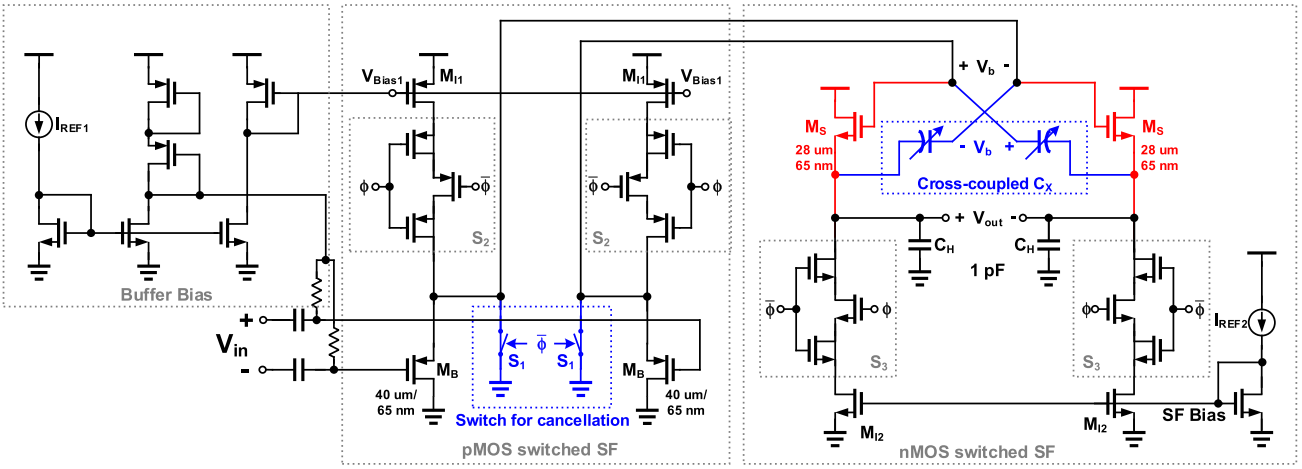

FIGURE 8. Schematic of the TDPD T/H circuit.

still consume static current. This transfers the signal to the V_b node and causes a feed-through problem. Fig. 7 shows the simulation results for this limitation. The difference in V_{drop} between the $+V_b$ and $-V_b$ nodes results in different effects on v_{out} at 37 and 32 mV. To generate a more constant V_{drop}, there were studies [20], [22], at the cost of the current consumption during the hold phase.

Consequently, the first pre-amplifier stage exhibits design difficulties because it not only has a better linearity than the following SF stage, but also makes the specific voltage decrease and is affected by the signal leakage at the hold phase.

III. TWO-STAGE SWITCHED SF T/H CIRCUIT

This section explained the design of the TDPD T/H circuit and how it addresses the transition from track-to-hold mode and the distortion in hold-mode.

A. SCHEMATIC OF T/H CIRCUIT

The TDPD T/H circuit based on a two-stage switched SF, as shown in Fig. 8, approached the problems in the hold phase from a different perspective. First, the pMOS SF was employed as the pre-amplifier instead of a common source amplifier to secure bandwidth and drive the subsequent nMOS SF. To start the hold phase, switches (S_1-$_3$) are activated to deactivate both M_S by pulling down differential V_b nodes and preventing the current from the source. This approach offers several benefits. Firstly, the circuit can be turned off simply with the switch architecture. The voltage drop is achieved using switches only, without the need for resistors or current sources, allowing for flexible design of the current and components in each stage. Secondly, there is no current consumption as the current sources are blocked. Lastly, this method reduces hold-mode feed-through, which will be discussed in the next section.

B. HOLD-MODE FEED THROUGH

As shown in Fig. 9, M_S has a negative gate-source voltage (V_{gs}) generated by the hold capacitor C_H and the pull-down

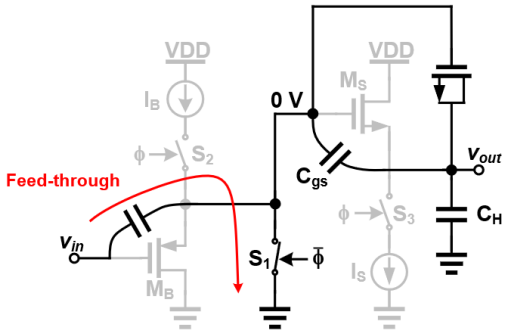

FIGURE 9. Reduction of hold mode feed-though in the TDPD T/H circuit.

switch S_1. The voltage of the current source I_S results in negative V_{gs} exceeding 300 mV even considering the input signal. Further, it suppresses the current leakage of the M_S during the hold phase. Because the pMOS SF stage is turned off together, it helps alleviate the hold-mode feed-through problem with the parasitic capacitance of the M_B and S_1. The C_{gd} capacitance serves as one of the load impedances for the pMOS source follower in track mode. However, C_{gd} capacitance is relatively small (~20fF) compared to other load impedances like C_H (1pF), resulting in a negligible effect on the pMOS source follower's operation at the operating frequency. Also, the C_{gd} capacitance is grounded through the S_1 switch, ensuring it doesn't influence the operation.

Fig. 10 shows simulation results where V_b node is grounded, reducing the hold-mode feed-through by blocking signal transmission during hold phase. However, the method using S_1 does not completely solve the problems mentioned. It causes an input signal-dependent voltage drop on the V_b node at the track-to-hold transition, leading to an increase in hold pedestal error and resulting in hold-mode distortion. However, the TDPD utilized this distortion as the cancellation purpose for track-mode distortion of SF and improved the linearity of the T/H circuit.

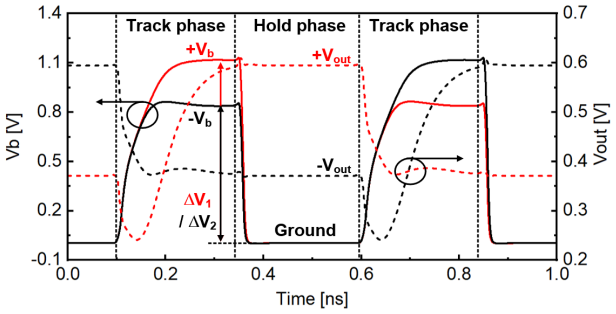

FIGURE 10. Simulation result for hold-mode feed-though of the TDPD T/H circuit.

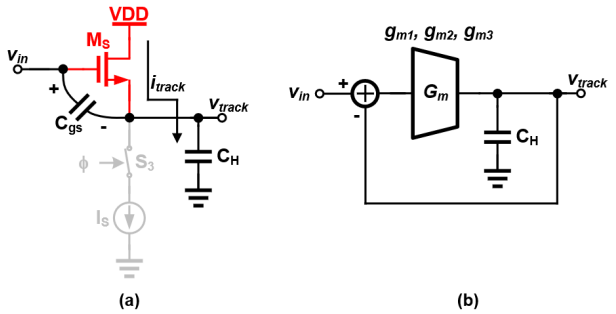

FIGURE 11. (a) Diagram of nMOS SF for the track mode and (b) its feedback system representation.

IV. DISTORTION ANALYSIS USING VOLTERRA SERIES

A. TRACK-MODE DISTORTION

This section analyzes track-mode operation using Volterra series analysis. The Volterra series can be applied to a small signal weakly nonlinear time-invariant system with a memory effect. In track mode, the circuit functions as a source follower, which can be considered a small signal weakly nonlinear time-invariant system with a memory effect.

During track phase, T/H operates as SF, transferring input signal to large capacitor (C_H). This process causes distortion due to the nonlinear transconductance of the transistor, which is transferred along with the signal. When entering the hold phase, the SF is turned off by the switches, and the transferred signal is stored. This is referred to as the track-mode distortion. In the analysis, only the nMOS SF driving C_H was considered, as shown in Fig. 11 (a). The first pMOS SF stage was excluded because it has a small effect on the overall distortion due to the small load capacitance originating from the parasitic capacitance of the 2nd stage. Even though the transfer function of SF was introduced in previous literatures [26], [30], and [31], this study treats SF as a feedback system and analyzes the distortion based on a loop gain (T) to provide design insights.

The SF and hold capacitances in the track-mode comprise a feedback loop as shown in Fig. 11 (b). The transfer function between the input (v_{in}) and output (v_{Track}) is defined as follows:

$$v_{Track} \triangleq H_1(j\omega_a)^{\circ} v_{in} + H_2(j\omega_a, j\omega_b)^{\circ} v_{in}^2 + H_3(j\omega_a, j\omega_b, j\omega_c)^{\circ} v_{in}^3 \quad (1)$$

where ω_a, ω_b, and ω_c are the input frequencies of SF. Volterra kernels $H_1(j\omega_a)$, $H_2(j\omega_a, j\omega_b)$, and $H_3(j\omega_a, j\omega_b, j\omega_c)$ are the linear gain, 2nd-order harmonic distortion, and 3rd-order harmonic distortion coefficients of the buffer, respectively. These are solved using the current formulas (2) and (3).

$$i_{track} = \frac{\partial C_H v_{track}}{\partial t} \quad (2)$$

$$\begin{aligned} i_{track} &= G_m (v_{in} - v_{track}) \\ &= g_{m1} (v_{in} - v_{track}) + g_{m2} (v_{in} - v_{track})^2 \\ &\quad + g_{m3} (v_{in} - v_{track})^3 \end{aligned} \quad (3)$$

where g_{mn} is the nth-order nonlinear coefficient of M_S. Based on the loop gain of SF expressed in (4), the Volterra kernels are presented as follows: The 1st term is (5) and the 2nd, 3rd terms are obtained as in (6) and (7), respectively. Each term contains loop gains $T(\omega_a + \omega_b)$ and $T(\omega_a + \omega_b + \omega_c)$ for the harmonic frequency. g_{m1} and C_H determine the bandwidth, as shown in $T(\omega_a)$ and $H_1(j\omega_a)$. Therefore, g_{m1} must be set by the input frequency and operation speed of the T/H. Since the T/H circuit was measured with a signal frequency input, $H_3(j\omega_a, j\omega_b, j\omega_c)$, which relates to 3rd-order distortion, can be expressed as (8) under the condition $\omega_a = \omega_b = \omega_c = \omega_1$.

$$i_{track} = \frac{g_{m1}}{j\omega_a C_H} \quad (4)$$

$$H_1(j\omega_a) = \frac{T(j\omega_a)}{[1 + T(j\omega_a)]} \quad (5)$$

$$H_2(j\omega_a, j\omega_b) = \frac{[g_{m2}/j(\omega_a + \omega_b) C_H]}{\{[1+T(\omega_a)][1+T(\omega_b)][1+T(\omega_a + \omega_b)]\}} \quad (6)$$

$$H_3(j\omega_a, j\omega_b, j\omega_c) = \frac{\left\{g_{m3}\overline{[1-H_1(j\omega_a)]^3} - 2g_{m2}\overline{[1-H_1(j\omega_a)]\, H_2(j\omega_b, j\omega_c)}\right\}}{\{[1+T(\omega_a+\omega_b+\omega_c)]\times j(\omega_a+\omega_b+\omega_c) C_H\}} \quad (7)$$

$$H_3(j\omega_1) = \frac{\{g_{m3} - 2g_{m2}^2/[g_{m1} + j2\omega_1 C_H]\}}{j3\omega_1 C_H [1+T(\omega_1)]^3 [1+T(3\omega_1)]} \quad (8)$$

Subsequently, using (5) to (8), the ratio of the 3rd-order distortion to the fundamental tone (HD3) can be expressed as in (9).

$$HD3 = \left[\frac{|H_3(j\omega_1)|}{|4H_1(j\omega_1)|}\right] v_{in}^2 \quad (9)$$

Generally, a differential circuit can neglect the 2nd-order harmonic distortion and the 3rd-order harmonic distortion is considered as a major nonlinearity term. Therefore, reducing H_3 related to HD3 is important for achieving a high spurious-free dynamic range (SFDR) performance. The 3rd-order linearity performance primarily depends on the loop gain ($T(\omega_1)$), which increases as the frequency decreases. As seen in (8), a low input frequency (ω_1) or small

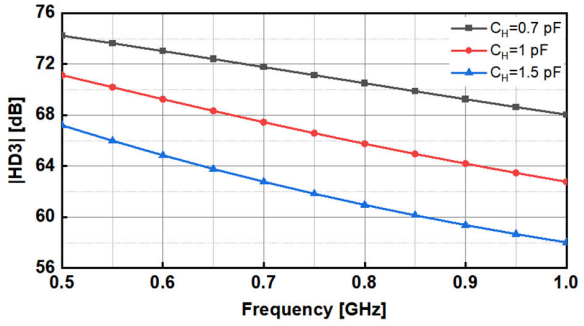

FIGURE 12. Calculated HD3 of SF according to input frequency and load capacitance.

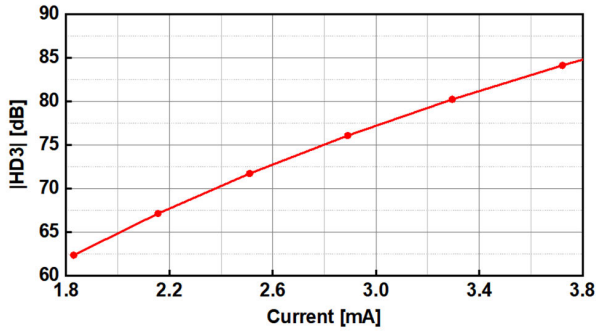

FIGURE 13. Calculated HD3 of SF according to current consumption at 1 GHz input frequency.

C_H results in a high $T(\omega_1)$, improving the HD3 performance. This trend can be confirmed in the calculation results shown in Fig. 12.

However, when striving for a high-speed and high-performance T/H circuit, it is necessary to operate at a high input frequency and implementing a small load capacitance can be challenging due to the large input impedance of the subsequent stage, such as a large C-DAC or interleaving paths in a TI ADC. Therefore, $H_3(j\omega_1)$ can be reduced by reducing g_{m3} or increasing g_{m1}, which increases the loop gain of the feedback. These approaches are greatly influenced by the current, so the linearity is closely related to power consumption. Fig. 13 shows the calculation results of the magnitude of HD3 at an input frequency of 1 GHz. As shown in Fig. 13, HD3 improves by burning more current. Thus, it is important to employ a linearity enhancement technique to improve linearity which can relax the relationship between linearity performance and current consumption.

Fig. 14 presents the simulation and calculation result of the SFDR of a track-mode T/H circuit, where the SFDR performance decreases as the frequency increases as the loop gain decrease over the frequency.

B. HOLD-MODE DISTORTION

1) GATE-SOURCE CAPACITOR

The T/H circuit enters the hold mode by lowering the V_b node to ground, which results in hold-mode distortion due to the hold pedestal error.

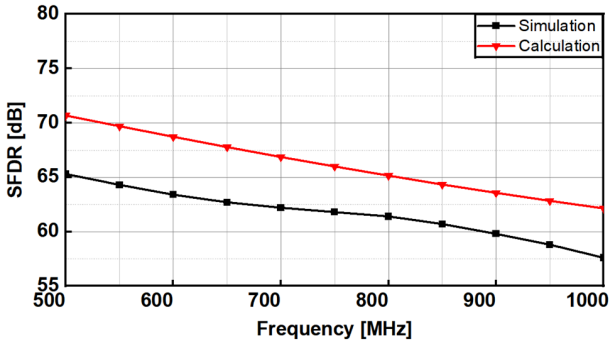

FIGURE 14. Calculation and simulation results for SFDRs.

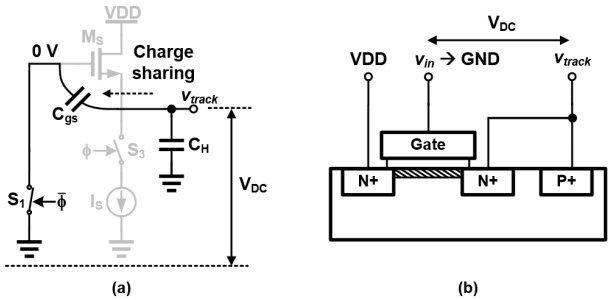

FIGURE 15. (a) Diagram of nMOS SF for the hold phase, (b) the diagram of nonlinear parasitic capacitor.

The TDPD technique attempts to cancel the track-mode distortion that occurred during the previous track phase by using the hold-mode distortion. This section explains the cancellation method through an analysis of the charge sharing process related to the nonlinear capacitor, which is the cause of hold-mode distortion.

Nonlinear capacitors can be explained using the nMOS SF transistor and the hold-mode generation method. As shown in Fig. 15 (a), when the hold phase is entered, the gate node of the M_S drops to ground, and V_{gs} becomes less than 0 V, thus creating a new capacitance. The vertical diagram of this capacitance is shown in Fig. 15 (b), and it varies according to V_{gs}. This can be expressed as (10) with a polynomial for V_{gs} ($= v_{track}$), like transconductance (3).

$$\begin{aligned} C_{gs} = \mathrm{f}\left(v_{gs}\right) &\approx C_{gs0} + C_{gs1} v_{gs} + C_{gs2} v_{gs}^2 \\ &\approx C_{gs0} - C_{gs1} v_{track} + C_{gs2} v_{track}^2 \end{aligned} \tag{10}$$

where C_{gs0} is the static capacitance, C_{gs1} and C_{gs2} are 1st and 2nd-order derivatives of the gate-source capacitance, respectively. Fig. 16 shows the simulation plot of the C_{gs} and C_{gs2} according to V_{gs}. The coefficients of (10) are determined by the size of the transistor and the static voltage (V_{DC}) for the source node of the M_S in the hold phase, and the static gate voltage applied to the SF during the track phase.

Because C_{gs} is newly generated in the hold phase, the charge stored in the v_{track} node (Q_H) is maintained, as shown in (11), leading to charge sharing between C_H and C_{gs}. Herein, a new distortion arises due to the nonlinearity of C_{gs},

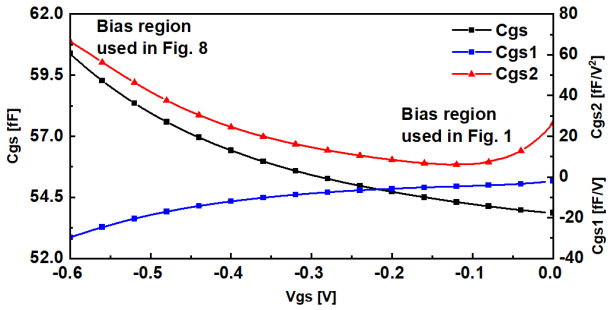

FIGURE 16. Simulation result for the gate-source capacitance according to gate-source voltage calculation and simulation results for SFDRs.

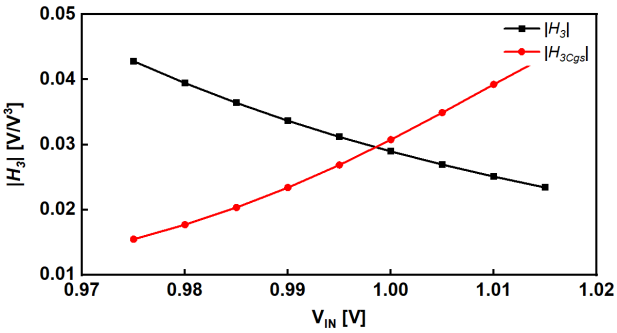

FIGURE 17. Calculation results for the distortion parameter to the input voltage.

which can be verified using (12). It represents the hold phase output voltage (v_{Hold}).

$$Q_H = C_H v_{track} = \left(C_H + C_{gs}\right) v_{Hold} \tag{11}$$

$$\begin{aligned} v_{Hold} &\cong \left[1 - \frac{C_{gs}}{C_H}\right] v_{track} \\ &\cong \left(1 - \frac{C_{gs0}}{C_H}\right) v_{track} + \left(\frac{C_{gs1}}{C_H}\right) v_{track}^2 \\ &\quad - \left(\frac{C_{gs2}}{C_H}\right) v_{track}^3 \end{aligned} \tag{12}$$

According to the equation, 3rd-order distortion is generated by the 2nd-order coefficient of C_{gs}, resulting in hold-mode distortion. The hold-mode distortion can be represented by the coefficient H_{3Cgs} in (13). By combining this with the transfer function of the previous track phase, the final transfer function of the T/H circuit can be obtained as shown in (14).

$$H_{3C_{gs}} \triangleq \left[C_{gs2}/C_H\right] \left[H_1\left(j\omega_1\right)\right]^3 \tag{13}$$

$$v_{Hold} cong H_1\left(j\omega_1\right)^\circ v_{in} + H_3\left(j\omega_1\right)^\circ v_{in}^3 - H_{3C_{gs}}\left(j\omega_1\right)^\circ v_{in}^3 \tag{14}$$

For simplicity, the impact of charge sharing on the 1st-order was ignored, and the 2nd-order term was omitted due to the differential structure. As shown in (14), the track-mode 3rd-order distortion ($H_3(j\omega_1)$) can be cancelled with the hold-mode 3rd-order distortion ($H_{3Cgs}(j\omega_1)$), despite occurring at different time modes. Fig. 17 displays the calculation and simulation results of H_3 and H_{3cgs} with respect to the static input voltage of the SF. Both parameters are complex values, so their absolute values are displayed in the graph for ease of interpretation. Consequently, with proper bias point and size of the transistor, the track mode 3rd-order distortion ($H_3(j\omega_1)$) could be cancelled with the hold-mode 3rd-order distortion ($H_{3Cgs}(j\omega_1)$). When it comes to selecting transistor sizes, the suggested cancellation method boosts nonlinearity by counterbalancing the nonlinearity originating from the gate-source capacitance with the transconductance's nonlinearity The third-order distortion from the transconductance is inversely proportional to the square of the transistor size, whereas the third-order distortion from the gate-source capacitance (C_{gs}) nonlinearity is directly proportional to the transistor size. Therefore, we meticulously select the optimal transistor size to minimize the overall distortion. Fig. 18 presents a graph comparing the simulation and calculation results of SFDR under cancellation.

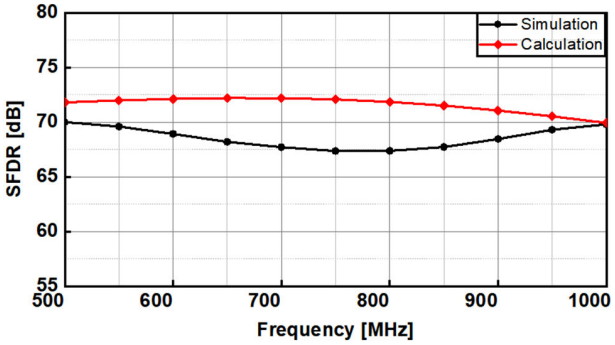

FIGURE 18. The calculation and simulation results for SFDRs.

2) CROSS-COUPLED CAPACITOR

Because the hold-mode distortion caused by C_{gs} and the track-mode distortion caused by g_m are complex values, if their phases are not properly aligned, the cancellation is not perfect, which limits the linearization. The phases of each term are as follows: as shown in Fig. 19, the track-mode distortion (D_T) has a specific phase (P_T), which is influenced by the hold capacitor and input frequency. To achieve complete cancellation, a distortion of opposite phase ($-P_T$) and magnitude is required from the hold-mode. However, the hold-mode distortion (D_H) has a phase (P_H) of $H_1(j\omega_1)$ in (13), which has some error compared to $-P_T$, even if the magnitude is set properly. Therefore, some cancellation is possible, but some residual distortion (D_E) remains, limiting the enhancement of linearity.

To improve the cancellation further, an additional MOS capacitor C_X was added between the input (v_{in}) and output (v_{out}) of the nMOS SF, as shown in Fig. 20 which shows an equivalent half circuit diagram. In the equivalent half circuit diagram, v_{in} is applied through an inverting buffer, which can be implemented using a cross-coupled connection based on a differential structure.

$$C_X = f\left(v_{gs}\right) \approx C_{X0} + C_{X1} v_{gs} + C_{X2} v_{gs}^2 \tag{15}$$

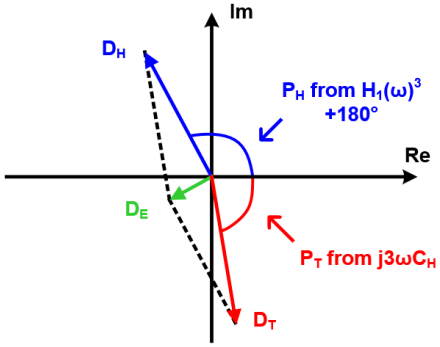

FIGURE 19. Phase diagram of track-mode and hold-mode distortion.

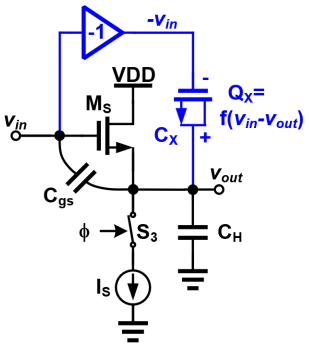

FIGURE 20. Equivalent Half circuit diagram of nMOS SF with additional capacitor.

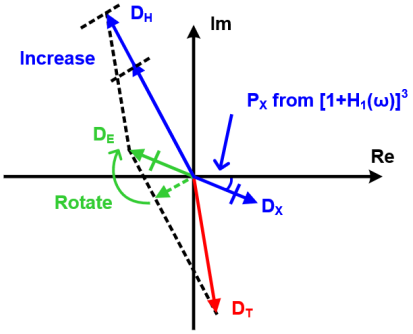

FIGURE 21. The modified phase diagram of track-mode and hold-mode distortion.

$$
\begin{aligned}
Q_X &= C_X(v_{track} + v_{in}) \\
&= C_{X0}\left(H_1\left(j\omega_1\right)+1\right)v_{in} - C_{X1}\left(H_1\left(j\omega_1\right)+1\right)^2 v_{in}^2 \\
&\quad + C_{X2}\left(H_1\left(j\omega_1\right)+1\right)^3 v_{in}^3 \qquad (16)
\end{aligned}
$$

$$
H_{3C_X} \triangleq \left[C_X / C_H\right]\left[1 + H_1\left(j\omega_1\right)\right]^3 \qquad (17)
$$

$$
\begin{aligned}
v_{Hold} &\cong H_1\left(j\omega_1\right)^\circ v_{in} + H_3\left(j\omega_1\right)^\circ v_{in}^3 - H_{3C_{gs}}\left(j\omega_1\right)^\circ v_{in}^3 \\
&\quad + H_{3C_X}\left(j\omega_1\right)^\circ v_{in}^3 \qquad (18)
\end{aligned}
$$

The voltage difference between v_{in} and v_{out} is experienced by C_X, causing the signal-dependent charge Q_X to be stored in its nonlinear capacitance during the track phase. Similar

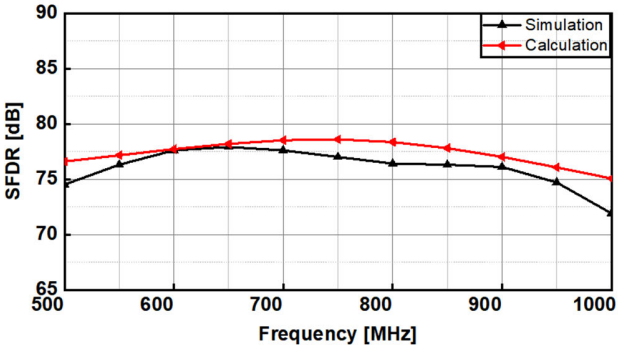

FIGURE 22. Calculation and simulation results for SFDRs.

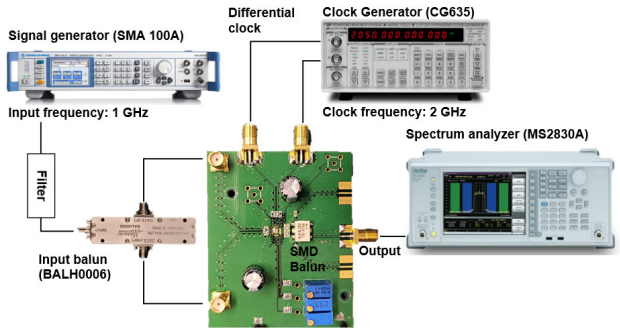

FIGURE 23. Measurement setup.

to C_{gs}, the capacitance of C_X can also be expressed in terms of v_{gs}, as shown in (15). As a result, Q_X can be expressed in relation to v_{in}, as shown in (16). This charge is transmitted and influences the stored hold voltage based on the change in bias voltage of C_X in the hold phase. If the effect of C_X is defined as a coefficient, as shown in (17), the effect of C_H can be summarized in (18).

Here, it is stated that the addition of a capacitor, C_X, between the input and output of an nMOS SF circuit can improve the SFDR (Spurious Free Dynamic Range) performance further. The new capacitor, C_X, experiences a voltage difference between the input and output, which creates a nonlinear charge, Q_X, that affects the stored hold voltage. This effect is represented as a 3rd-order distortion (H_{3CX}) and its phase is determined by $(1+ H_1(j\omega_1))$. The phase diagram including the new distortion (D_X) is shown in Fig. 21, which provides additional cancellation of distortions. The phase of the hold-mode distortion (D_H) must be partially adjusted so that the vector sum (D_E) of the track-mode distortion (D_T) and D_H is close to the opposite phase and magnitude of D_X. This can further improve the overall SFDR performance, as shown in Fig. 22 which shows the simulation and calculation result of SFDR including C_X.

V. MEASUREMENT RESULTS

Seventeen sample chips which were fabricated with a 65 nm CMOS were used for measurement. The mean value of the power consumption of the chips is 9mW at a 1.5 V supply. Fig. 23 shows measurement setup of the T/H chip.

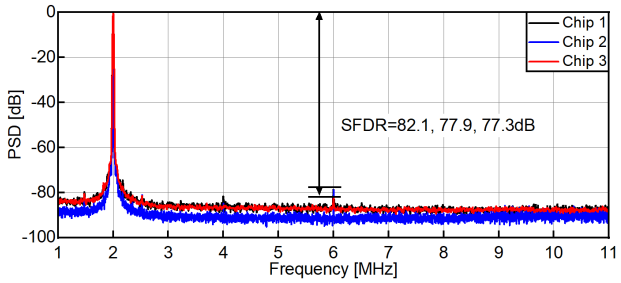

FIGURE 24. The measured output spectrum at 2 GS/s for a 700-mV_{PP} 998 MHz sinusoidal input with 3 chips.

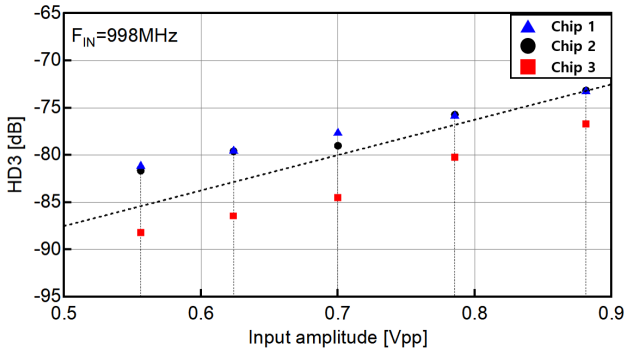

FIGURE 25. The measured HD3 versus the input amplitudes with 3 chips.

Fig. 24 shows the measurement results of the output spectrum at 2 GS/s (F_S) for a 998 MHz sinusoidal input (F_{IN}) with 700 mV_{PP} with three sample chips The results showed SFDRs of 82.1 dB, 77.9 dB, and 77.3 dB respectively. Among the results, the best performance showed an improvement of 20.5 dB in distortion cancellation. As a result, an SFDR-based figure of merit (FoM) of 192.5 was obtained. The FoM was calculated using (19) which took into accounting both power consumption and energy-efficiency. Fig. 25 shows the measured HD3 versus the input amplitude for these chips. Fig. 26 shows the measurement results of the SFDR variation with respect to the bias current. The highest SFDR was achieved at 6 mA, and a lower or higher bias current resulted in a lower SFDR performance. Even though a higher bias current increases the linearity of the SF, it decreases the overall performance due to deviation from the cancellation condition between track-mode distortion and hold-mode distortion. Seventeen samples were used to measure the variation in SFDR, and Fig. 27 shows the measurement results according to the bias condition when a 2 GS/s 700 mV_{PP} 998 MHz sinusoidal input was applied for all the samples. The statistic variations of the SFDR shows mean value of 73.7, 75.3 and 76.1 dB with sigma of 2.8, 2.3 and 2.0 dB respectively at 2 G/s for a 700 mV_{PP} 998 MHz sinusoidal input according to the bias conditions for (a) 5.7 mA, (b) 6mA, and (c) 6.6 mA. A conventional T/H circuit without cancellation was also measured which shows an SFDR of 61.6 dB at 14mW power consumption. When each sample was set to the optimal bias, an SFDR of 77.1 dB was obtained which is 15.5 dB improvement over the conventional T/H circuit even with 5mW less

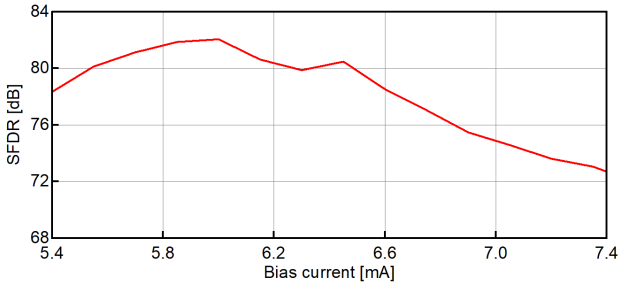

FIGURE 26. The measured SFDR according to the bias current.

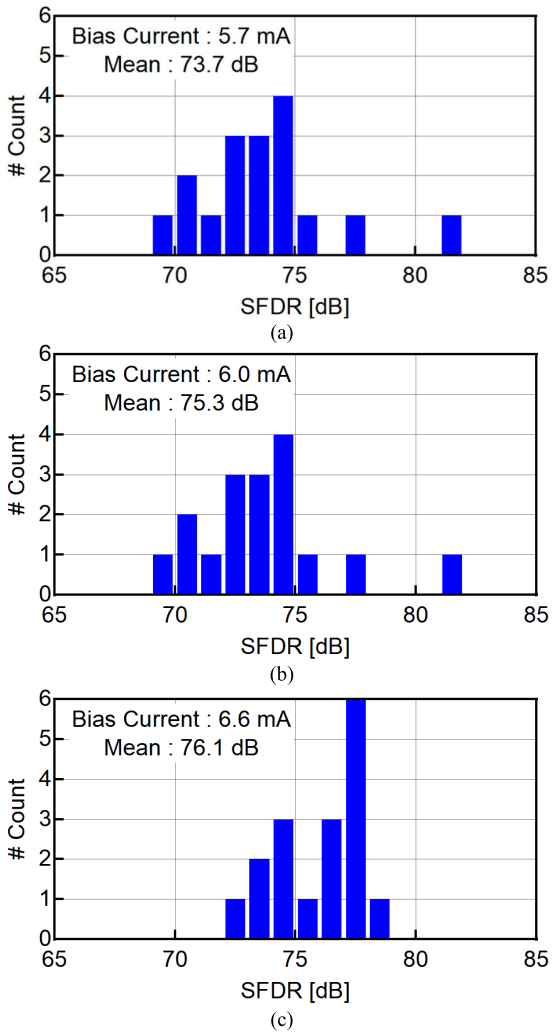

FIGURE 27. The statistic variations of the SFDR at 2 GS/s for a 700 mV_{PP} 998 MHz sinusoidal input for 17 samples according to the bias conditions for (a) 5.7 mA, (b) 6mA, and (c) 6.6 mA.

power consumption. Table 1 summarizes the measurement results of the conventional T/H circuit, the multiple TDPD T/H chips and compares them with other state-of-the-art T/H chips.

$$\mathrm{FoM_{SFDR}} = \mathrm{SFDR} + 10\log_{10}\frac{F_S}{2 \times \mathrm{Power}} \qquad (19)$$

TABLE 1. Performance summary and comparison.

Feature		Tech. [nm]	F_{IN} [GHz] / F_S [GS/s]	Supply Voltage [V]	Power [mW]	SFDR at F_{IN} [dB]	FoM_{SFDR} [dB]*
This Work	**w/o Cancellation**	**65**	**1/2**	**1.5**	**14**	**61.6**	**170.1**
	Chip1				**8.6**	**77.3**	**188.0**
	Chip2				**9.5**	**77.9**	**187.8**
	Chip3				**9**	**82.1**	**192.5**
	Avg. (17 Chips)				**9**	**77.1**	**187.5**
JSSC20 Ali [8]		16	4/10	1.8	220	65	168.6
JSSC14 Ali [16]		65	0.14/1	3.3	99	86	183
JSSC17 S. D. [7]		28	4/10	3	400	66	167
ISSCC17 Vaz [9]		16	2/4	-	282	67	165.5
RFIC21 E. W. [17]		22	3/3	2.8	167	67.5	167.5

* FoM_{SFDR} is expressed at equation (19)

VI. CONCLUSION

This study provides design insight and mathematical analysis of the active T/H circuits based on a switched SF and TDPD technique and shows measurement result of multiple sample chips. The track-mode distortion was explained by expressing the SF through the Volterra series from a feedback viewpoint. During the hold phase, the hold-mode feedthrough can be minimized by the structure. In contrast, the increased hold pedestal error caused by nonlinear parasitic capacitance was analyzed through charge sharing, and it was introduced as hold-mode distortion. The cancellation between track-mode and hold-mode distortion was explained in light of these distortions. Additionally, the explanation and analysis of additional cancellation with an extra capacitance (C_X) was provided. Seventeen samples were measured and showed stable cancellation operation. When each sample was set to the optimal bias, an average of SFDR of 77.1 dB was obtained which is 15.5 dB (max. 20.5dB) improvement even with 5mW less power consumption over the conventional T/H circuit without cancellation.

The operational frequency of this system is, in fact, constrained by the speed of the clock distribution network for the sampling clock (2Gs/s). Without accounting for this limitation in clock distribution speed, the sampler itself could potentially operate at over 10Gs/s [11]. Additionally, the cancellation technique remains unaffected by the operating frequency, allowing us to enhance the operating frequency by adopting more advanced CMOS technology.

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