IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 18 December 2023, accepted 26 January 2024, date of publication 31 January 2024, date of current version 6 February 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3360884

RESEARCH ARTICLE

Fabrication Error Modeling and Analysis of an *E*-Band MHMIC Balanced Power Detector

MEHRDAD HARIFI-MOOD[1], NIMA SOUZANDEH[1], PEYMAN POURMOHAMMADI[1], (Student Member, IEEE), DJILALI HAMMOU[1], BRYAN HOSEIN[2], SONIA AÏSSA[1], (Fellow, IEEE), AND SERIOJA OVIDIU TATU[1], (Senior Member, IEEE)

[1]Institut National de la Recherche Scientifique (INRS-EMT), Université du Québec, Montreal, QC H5A 1K6, Canada
[2]Focus Microwaves Group, Montreal, QC H4S 1A8, Canada

Corresponding author: Mehrdad Harifi-Mood (mehrdad.harifi-mood@inrs.ca)

This work was supported by the Natural Sciences and Engineering Research Council of Canada (NSERC).

ABSTRACT This study models and analyses the fabrication errors of an ultra-wideband (UWB) Schottky diode power detector using miniature hybrid-microwave integrated-circuit (MHMIC) technology. The fabricated balanced power detector is composed of two zero-bias GaAs Schottky diodes, a 90°-hybrid coupler, and two pairs of broadband butterfly open stub reflectors. The circuit is designed on a thin film ceramic substrate having a thickness of 127 μm with a 1 μm gold conductive layer, and a 20 nm Titanium Oxide (TiO_2) resistive layer. The simulations use a computer model of the broadband coupler from on-wafer measurements to obtain an authentic fabrication error analysis. Moreover, the trade-off between the maximum efficiency and the fabrication error tolerance of the balanced power detectors is discussed. It is shown that the performance of the balanced power detector is dependent on different fabrication errors. Based on the measurement results, one of the fabricated detectors with minimum fabrication errors demonstrates a return loss of better than 10 dB over the entire frequency band of 60 to 90 GHz.

INDEX TERMS Balanced power detector, error analysis, high data-rate, integrated circuit (IC), mm-Wave communication systems, zero bias Schottky diode.

I. INTRODUCTION

By the soaring demand of high data-rate wireless communications, recent years witnessed substantial growth in the design of ultra-wideband systems [1]. So far, millimeter wave (mm-wave) frequencies have shown promising potential for several applications. Multi-Gb/s wireless communications [2], meteorology radars, imaging systems [3], and short-range remote sensing [4] are some examples that can be enabled by mm-wave technologies. E-band frequencies in mm-wave can carry higher data traffic mainly due to the wider channels, making this frequency band a proper solution for future communications needs [5]. However, designing such systems requires a precise design and fabrication procedure simultaneously [6]. Hence, having a solid grasp of different possibilities of fabrication errors and their impacts on the circuit results is essential to estimate and then enhance the yield of the system.

In general, the microwave power detector converts a microwave signal into DC or low frequency signals and is widely used in the power measurement [7], network analyzers, communication and radar receivers [8], six-port modules [9], [10], etc. The power detectors can be implemented by various topologies, and technologies such as Silicon-on-Insulator (SOI) [11], BiCMOS [12], GaAs [13], etc. Balanced topology is a popular structure in designing mm-wave circuits. In this topology, the signal divides at the input, and combines at the output for different purposes, such as bandwidth widening, linearity and matching improvement, etc. From the other side, employing this topology leads to higher power consumption, system complexity, and relatively larger occupied area.

In this article, a balanced power detector is designed using several commercial software such as Advanced Design System (ADS), of Keysight Technologies, Computer Simulation

The associate editor coordinating the review of this manuscript and approving it for publication was Derek Abbott.

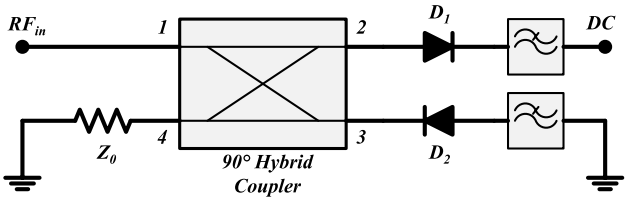

FIGURE 1. Schematic of the balanced power detector.

Technologies (CST) Microwave Studio, and ANSYS High-Frequency Structure Simulator (HFSS). The proposed circuit is fabricated in MHMIC technology. Balanced power detector topology is utilized mainly to minimize the return loss of the circuit over an extended mm-wave band [14]. However, due to the use of two individual non-linear components, the performance of the balanced power detectors is highly dependent on the symmetry of the topology. Therefore, any fabrication or design error that disarranges the symmetry of the circuit can lead to lower performances.

Fig. 1 shows a simplified schematic of the circuit. The circuit consists of one 90°-hybrid coupler, two zero-bias diodes and two low pass filters acting as reflectors for mm-waves. By considering a perfect design procedure the purpose of this article is mainly to investigate the impact of the fabrication errors on the performance of the balanced power detectors. Moreover, the tolerance of this topology to different fabrication errors is discussed in detail by assuming different values for reflection coefficients of the diodes. To the best of the author's knowledge, this is the first study that investigates the fabrication errors of the balanced power detectors (balanced topology in general) in MHMIC technology.

The rest of the paper is organized as follows: First, the design principles of the balanced power detector are briefly discussed in section II. Also, section III is specified for the fabrication error modeling approach that is utilized in this paper. Then in section IV, the fabrication details of the proposed circuit are given. Section V describes the different fabrication errors and their impact on the circuit results analytically. The combination of different fabrication error possibilities is also simulated to represent a practical outcome. The measurement results of the proposed balanced power detector are shown in section VI. Finally, the conclusion of the paper is presented in section VII.

II. DESIGN PRINCIPLES

To analyze the functionality of the circuit the port numbers are considered as shown in Fig. 1. Therefore, considering non-identical diodes, a perfect termination at port 4, and a conventional scattering matrix for the 90°-hybrid coupler, the reflected waves (b_n) can be calculated as follows:

$$\begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 0 & j & 1 & 0 \\ j & 0 & 0 & 1 \\ 1 & 0 & 0 & j \\ 0 & 1 & j & 0 \end{bmatrix} \begin{bmatrix} a_1 \\ \Gamma_{D1} \\ \Gamma_{D2} \\ 0 \end{bmatrix} \tag{1}$$

where Γ_{D1} and Γ_{D2} represent the reflection coefficients of the diodes, which are defined as (a_2/b_2) and (a_3/b_3) respectively. As known, the incident normalized wave at port n is denoted by a_n, while the reflected wave is represented by b_n. Therefore, the reflected wave at port 1 can be obtained as below:

$$b_1 = \frac{a_1}{2}(\Gamma_{D2} - \Gamma_{D1}) \tag{2}$$

As can be inferred from (2), by increasing the difference of the diodes' reflection coefficients the reflected wave of the circuit (port 1) increases (i.e., the reflection coefficient of the circuit Γ_{in} increases). In addition, the delivered mm-wave power to the input of D_1 (port 2) is given by:

$$P_2 = \frac{1}{2}|b_2|^2 - \frac{1}{2}|a_2|^2 \tag{3}$$

So:

$$P_2 = \frac{|a_1|^2}{4}(1 - |\Gamma_{D1}|^2) \tag{4}$$

Similarly, the delivered mm-wave power to port 4 can be calculated as:

$$P_4 = \frac{1}{4}|\Gamma_{D1} + j\Gamma_{D2}|^2 \tag{5}$$

Since port 4 is terminated with Z_0, the delivered power to this port is considered dissipation. Mathematically, the dissipated power at port 4 can be mitigated by alleviating the reflection coefficients of the diodes employing a matching network. On the other side, it can be proven that bandwidth of the circuit can be limited in proportion of the magnitude of the reflection coefficient of the diodes [14]. Using any shunt, or series resistor in the DC path of the detector degrades the efficiency of the circuit, as well.

By defining the input reflection coefficient of the circuit from (2) as (Γ_{D2} -Γ_{D1})/2, the maximum efficiency of the balanced power detector can be described as follows:

$$\eta_{max} = \frac{P_{2(AVL)}}{P_{in}(1 - \left|\frac{\Gamma_{D2} - \Gamma_{D1}}{2}\right|^2)} \tag{6}$$

where P_{in}, and $P_{2(AVL)}$ represent the input power of the circuit, and the available power at port 2, respectively. Obviously, the efficiency of the detector can reach the maximum (i.e. 50%) by using two identical diodes with two perfect matching networks. Although designing a matching network without any resistor and showing a linear response over a wide bandwidth is arduous. Besides, different fabrication errors affect the reflection coefficients of each diode individually. The effect of different fabrication errors on the performance of the balanced power detectors are discussed in section V.

III. 90°-HYBRID COUPLER

S-parameter measurements of MHMIC multi-port components in mm-wave frequencies are challenging and costly because for each two-port measurement a different circuit must be used (required integrated loads at all other ports).

However, keeping symmetry in the design of such circuits can significantly reduce the number of two-port measurements [15]. Therefore, due to the symmetry of the designed coupler the following assumptions are valid:

$$S_{12} = S_{34} \tag{7a}$$
$$S_{14} = S_{23} \tag{7b}$$
$$S_{11} = S_{33} \tag{7c}$$
$$S_{22} = S_{44} \tag{7d}$$

To have a reliable fabrication error analysis, the gap between the simulation and measurement results should be minimized. Hence, the 90°-hybrid coupler of the proposed power detector is fabricated and measured separately. Fig. 2 (a) shows one of the fabricated couplers for measurement with one of the terminated ports by an integrated load (Fig. 2 (b)).

To achieve a practical design ratio between the quarter wavelength and width of the lines, the circuit is designed on a high dielectric thin film ceramic substrate. The substrate exhibits a dielectric constant of 9.9 with a thickness of 127 μm. On top of the substrate, a Titanium Oxide (TiO_2) layer with a thickness of 20 nm is used for integrating the resistors. This layer shows a sheet resistance of 100 Ω/sq. For metallization, a 1 μm gold layer is employed, which is on top of the resistive layer.

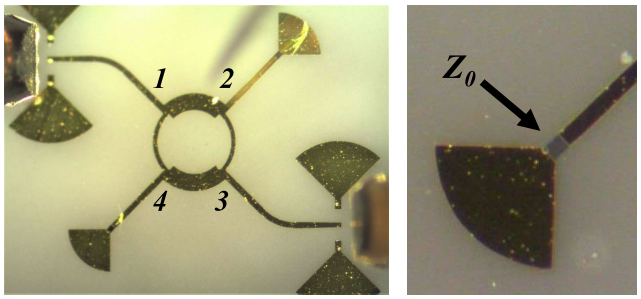

FIGURE 2. Microphotograph of (a) one of the fabricated ring-shaped 90°-hybrid couplers, and (b) a terminated port with an integrated load.

As it is obvious, the designed coupler has a symmetry shape. The on-wafer measurements of the fabricated couplers utilized the E8362 PNA Network Analyzer with the Agilent N5260A mm-wave head controller technology. In addition, for WR-12 waveguide operation using this set-up, two mm-wave extenders (from OML Inc.) are used. Two bent WR-12 waveguides are connected to Cascade Microtech Ground-Signal-Ground (GSG) waveguide probes with a pitch of 150 μm. The measurement results of the fabricated coupler are shown in Fig. 3, and 4.

Based on the measurement results, the ring-shaped 90°-hybrid coupler exhibits a good performance over a wide frequency band of 60 to 90 GHz. It can be clearly seen in Fig. 3 (a), the return loss of the coupler is better than 10 dB for each port. Also, Fig. 3 (b) shows that the input power is split between the two outputs (e.g., ideally should

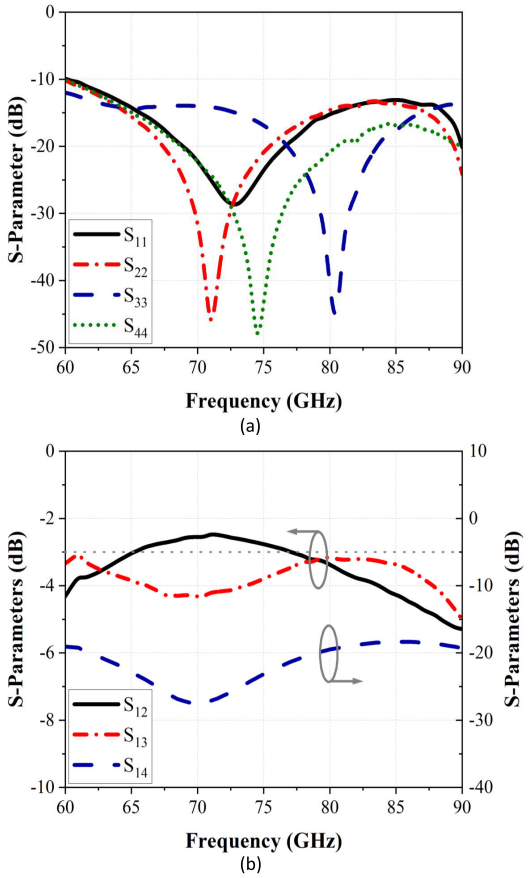

FIGURE 3. Measured S-parameters of the wide-band 90°-hybrid coupler: (a) return loss, (b) S_{12}, S_{13}, and S_{14}.

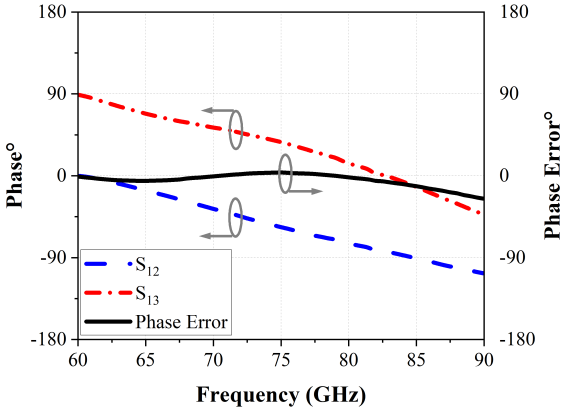

FIGURE 4. Phase measurement results of S_{12}, S_{13}, and the phase error over the frequency band.

be equal to −3 dB). In addition, the S_{14} of the circuit is plotted in Fig. 3 (b). Fig. 4 shows the phase measurement results of the coupler between ports 1, and 2, as well as ports 1 and 3. Ideally, the phase difference between these two measurements should exhibit a consistent value of 90° across the frequency band, which is depicted as Δ in Fig.4. Now, using non-ideal measurement results of the designed coupler

as a computer model will lead to an authentic fabrication error analysis of the proposed circuit.

IV. BALANCED POWER DETECTOR FABRICATION

The proposed power detector is composed of two zero bias GaAs Schottky diodes (HSCH 9161), a ring-shaped 90°-hybrid coupler as described before, and two broadband reflectors. In order to achieve the maximum efficiency throughout the entire frequency band of 30 GHz, the design of a matching network is omitted. Yet, utilizing the wideband coupler an acceptable matching for the circuit is expected. The HSCH 9161 diode is designed for zero-bias detecting applications up to the frequency of 110 GHz [16]. The input of the detector is connected to a microstrip to WR-12 transition, which is introduced in [8]. Fig. 5 shows the photo of the fabricated balanced power detector.

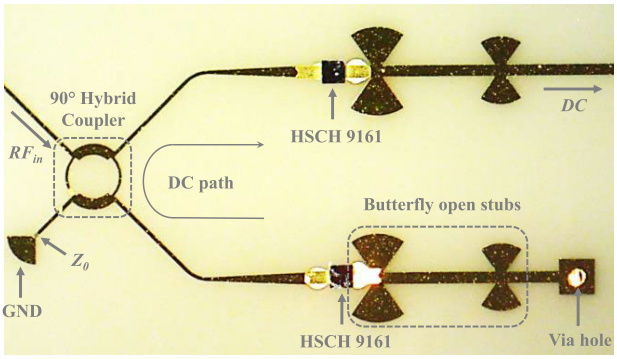

FIGURE 5. Microphotograph of the fabricated balanced power detector on a ceramic substrate with a thickness of 127 μm.

V. ANALYSIS AND MODELING OF FABRICATION ERRORS

In the process of micro-fabrication for mm-wave circuits, performance of the circuit can be drastically impacted by errors that may arise from human manipulation and/or equipment tolerances. Hence, it is essential to firstly, predict the different possibilities of fabrication errors and secondly, estimate their impact on the performance of the circuit. However, in practice, the combination of different fabrication errors made the estimation of the results difficult. Generally, two types of errors can occur in the fabrication of the planar diode-based detectors. The errors that contribute to the metallization process and to the diode mounting.

In this design, the errors that contribute to the metallization process can be evaluated in Fig. 3 (a). Since these results are gathered from 2-port measurements of 2 couplers on one die. The measured return losses of the coupler at all of the ports are in an acceptable range throughout the frequency band. Hence, it can be concluded that the metallization errors in this design have a negligible impact on the performance of the circuit. Although the high inherent reflection coefficient of the diodes makes the analysis of the diode mounting process crucial.

A. DIODES ADJUSTMENT

One of the common errors that might occur in mounting or soldering diodes of a balanced power detector is the positioning of the diodes compared to each other. Generally, if non-linear components in a balanced topology do not excite with a same wave (e.g., with distinct phases), even by assuming a perfect matching for those components, reflection is expected. Thereby, as can be revealed from (6), the maximum efficiency of the circuit will be diminished. This error can be seen in the microphotograph of one of the fabricated circuits in Fig. 6.

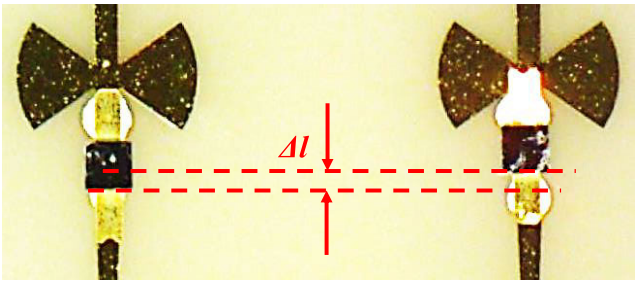

FIGURE 6. Microphotograph of the relative position of the diodes of the balanced power detector.

To assess the impact of the error on the reflection coefficient of the circuit reflection coefficient of each arm can be determined as below:

$$\Gamma_1 = \Gamma_{D1}.e^{-j2\beta l} \tag{8a}$$

$$\Gamma_2 = \Gamma_{D2}.e^{-j2\beta(l+\Delta l)} \tag{8b}$$

While Γ_1, and Γ_2 are assumed as the reflection coefficients of the arms of diode 1 and 2, respectively. In this equation, β represents the propagation coefficient of the substrate, l is the length of the transmission line, and Δl is the error of the relative position between the diodes. Fig. 7 depicts the schematic of the proposed circuit.

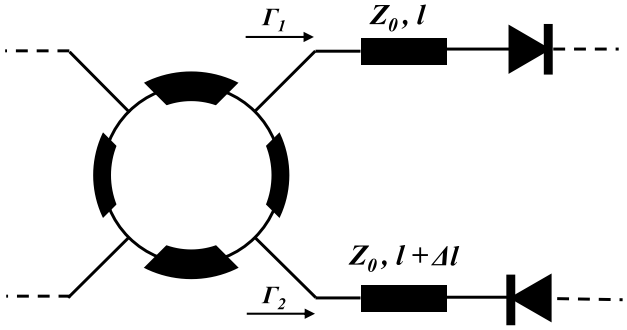

FIGURE 7. Schematic of the proposed balanced power detector.

Now, by assuming two identical diodes (e.g., $\Gamma_{D1} = \Gamma_{D2}$), and substituting the obtained Γ_1, and Γ_2 in (2), the reflection coefficient of the circuit can be given as follows:

$$\Gamma_{in} = \frac{1}{2}\left\{\left(\Gamma_D \times e^{-j2\beta(l+\Delta l)}\right) - \left(\Gamma_D \times e^{-j2\beta l}\right)\right\} \tag{9}$$

By considering a length of λ for the diodes' arms equation (9) can be rewritten as below:

$$\Gamma_{in} = \frac{\Gamma_D}{2}\{cos(2\beta\Delta l) + jsin(2\beta\Delta l) - 1\} \qquad (10)$$

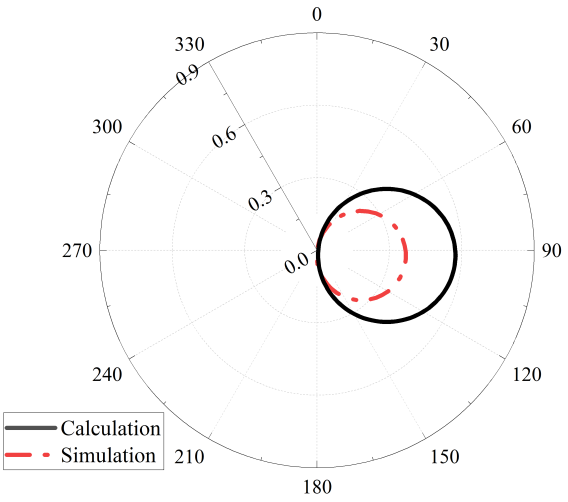

FIGURE 8. Calculated and simulated results of the input reflection coefficient of the balanced power detector (Γ_{in}) for $0° < \phi < 180°$ ($\Gamma_D = 0.75$) (at frequency of 75 GHz).

This error (Δl) causes an electric phase difference of ϕ. To visualize the calculations, Fig. 8 plotted the calculated reflection coefficient of the circuit versus different values of the ϕ in a polar plane. As it can be revealed from Fig.8, and equation (10) the center of the plotted circle is located at coordinates $-\Gamma_D/2$, which is obtained by the SPICE model of the diode. To evaluate the validity of the calculations the circuit is simulated in ADS using the measurement of the fabricated coupler from section III. Fig. 8 also shows the simulation results of the circuit at the frequency of 75 GHz for different values of the ϕ (0° to 180°, corresponding to up to half of the guided wavelength) for a usual magnitude of Γ_D.

As can be seen in Fig. 8, the simulation results of the circuit are similar to the calculations; minimum ϕ corresponds to the best reflection coefficient. It is noteworthy that some discrepancies between the calculations and simulation results are mainly due to the inaccuracy of the SPICE model of the diode, and simulation approach, which is based on the real measurement results having a certain insertion loss.

B. CONDUCTIVE ADHESIVE

As operating frequency increases, the size of the discrete components decreases (i.e., the wavelength decrease). Hence, assembling and/or soldering tiny components could become very challenging. The proposed balanced power detector needs 2 beam-lead diodes to be mounted on the ceramic substrate. To this aim, EPO-TEK H20E is utilized as the conductive adhesive, which is a two-component, 100% solids silver-filled epoxy system for chip bonding in microelectronics and optoelectronics applications [17]. The volume of this conductive adhesive, after a thermal step of 100°C/1 hour, can play a critical role in the results.

On one hand, the extra amount of adhesive increases the width of the transmission lines, which can lead to more reflection, then may result in mismatching in the circuit. On the other hand, using less than the desired amount of adhesive can made cavities between the diodes' beams and the transmission lines. Therefore, some parasitic capacitors may be produced intrinsically that can degrade the maximum efficiency of the circuit as well.

For modeling the impact of the adhesive, a cylindrical shape is considered for the conductive adhesive between the diodes' beams and the substrate. The height of the cylinder depends on the pressure that exerts on top of the diodes. The value of the exerted force on the diode is mainly due to the weight of the diode itself. So, as the weights of the diodes are almost equal, the heights of the cylinder can be assumed equal as well.

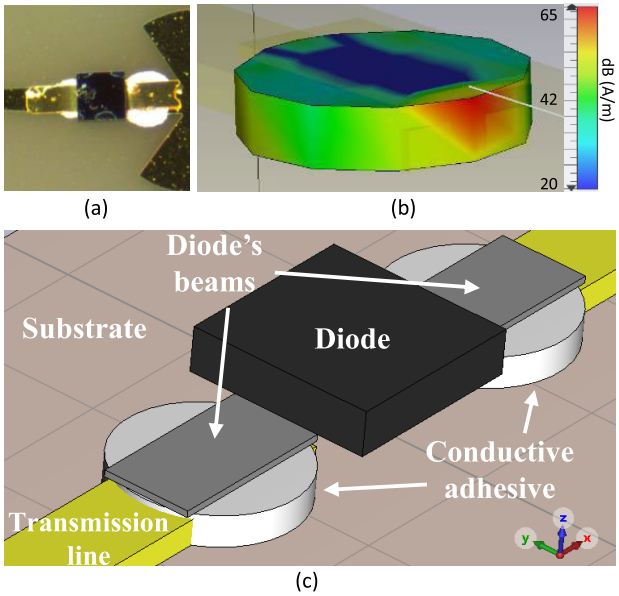

FIGURE 9. (a) Microphotograph of the diode, (b) current distribution of the adhesive cylinder, and (c) 3D model of the diode in CST.

Based on the microscopic observations of fabricated circuits, the height of the adhesive cylinders is estimated to be 10 % higher than the thickness of the transmission lines. The different possibilities of errors in this procedure are analyzed and simulated by ADS and CST. Fig. 9 (a) shows the microphotograph of a mounted diode, (b) the current distribution in the adhesive cylinder, and (c) the 3D model of the diode in CST. Fig. 10 shows the simulated S_{11} of each arm versus the different diameters of the adhesive cylinders.

Based on the simulation results, each arm exhibits the minimum reflection with the adhesive cylinders having 100 μm diameter approximately.

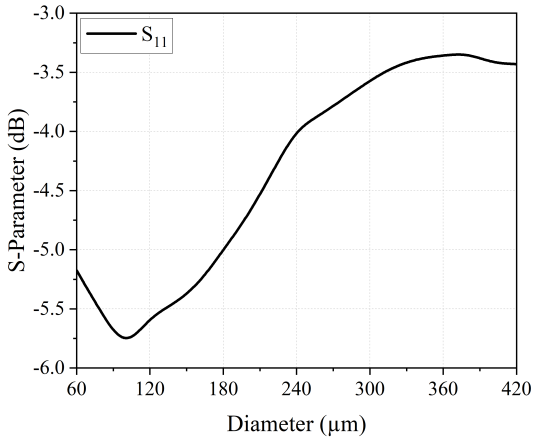

FIGURE 10. Simulated S_{11} of a diode's arm versus different diameters of the conductive adhesive.

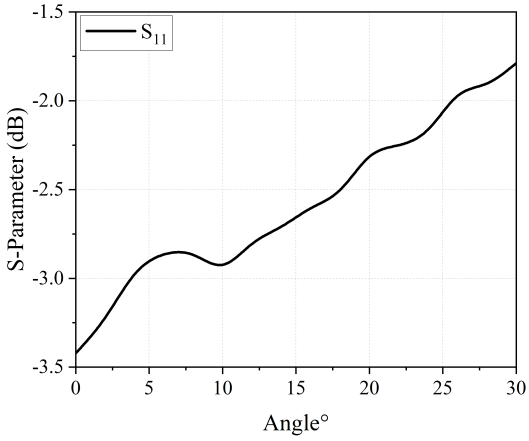

FIGURE 12. Simulated S_{11} of a diode's arm versus different angles of the diode and the transmission line.

C. DIODES ANGULAR ALIGNMENT

If one or both diodes are not perfectly aligned with the transmission lines, the reflection coefficients of the diodes are not equal anymore. Which, based on (2) and (5), leads to a higher reflection coefficient of the circuit and lower maximum efficiency. Basically, this error can change the width of the transmission lines to a higher value of the calculated width considering the desired Z_0. Fig. 11 shows the microphotograph of a mounted diode which has an angle of $\theta°$ with the transmission line axis.

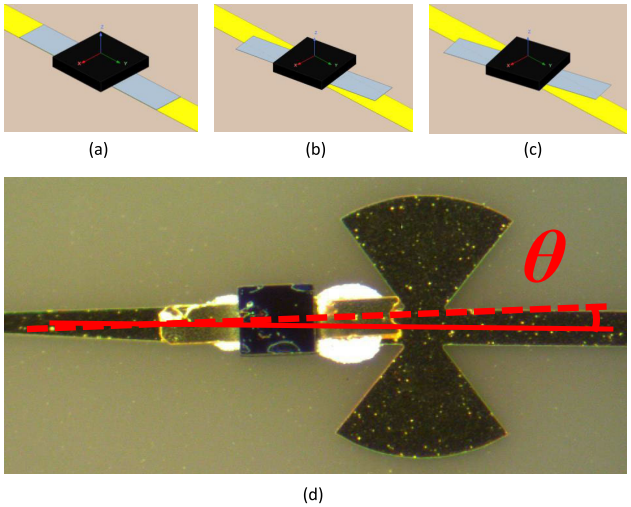

FIGURE 11. (a) 3D model of the aligned diode on the transmission line (b), a misaligned diode with an angle of 15°, (c) 30°, and a microphotograph of a misaligned diode with an angle of $\theta°$.

The alignment error is simulated in HFSS by using the measurement results of the fabricated couplers, as well. Fig. 12 depicts the return loss of each arm versus the angle between the diodes' beams and the transmission line. In this simulation, each of the arms is composed of an HSCH-9161 diode and butterfly reflectors.

As can be seen, the reflection of each arm increases by increasing the angle between the diodes' beams and the axis of the transmission line.

D. COMBINATION OF ERRORS

As mentioned earlier, in practice, a combination of different errors affects the performance of the proposed balanced power detector. However, all the fabrication errors mainly can increase the difference of the reflection coefficients of diodes' arms. On the other hand, the excitation phase difference between the diodes, due to the relative position of the diodes, can deteriorate the performance of the circuit. Therefore, by considering all the errors in the fabrication process of the balanced power detector, the reflection coefficient of the circuit can be given as follows:

$$\Gamma_{in} = \frac{1}{2}\{\Gamma_1 cos(2\beta\Delta l) - \Gamma_2 + j\Gamma_1 sin(2\beta\Delta l)\} \qquad (11)$$

Fig. 13 depicts the reflection coefficient of the proposed circuit versus the differences between the excitation phase of the diodes (ϕ), and the magnitude of the reflection coefficient of one arm (Γ_1) that is swept between -1 and $+1$ on the real axis.

Based on the simulation results of the diodes and the reflectors, the magnitude of the reflection coefficient of the other arm (Γ_2) is considered $+0.75$.

As shown, when the relative position of the diodes (ϕ) is minimum and under the condition of $\Gamma_1 = \Gamma_2$ the circuit exhibits the best reflection coefficient. In other words, the best performance of the circuit is expected when the fabrication errors are minimized.

The reflection coefficient of each arm can be alleviated by designing a good input matching circuit for the diode over the entire band. However depending on the inherent reflection coefficient of the diode itself, designing a matching network with a flat response over a wide frequency band of 30 GHz without using any resistor is not possible. Although practically, the overall efficiency of the power

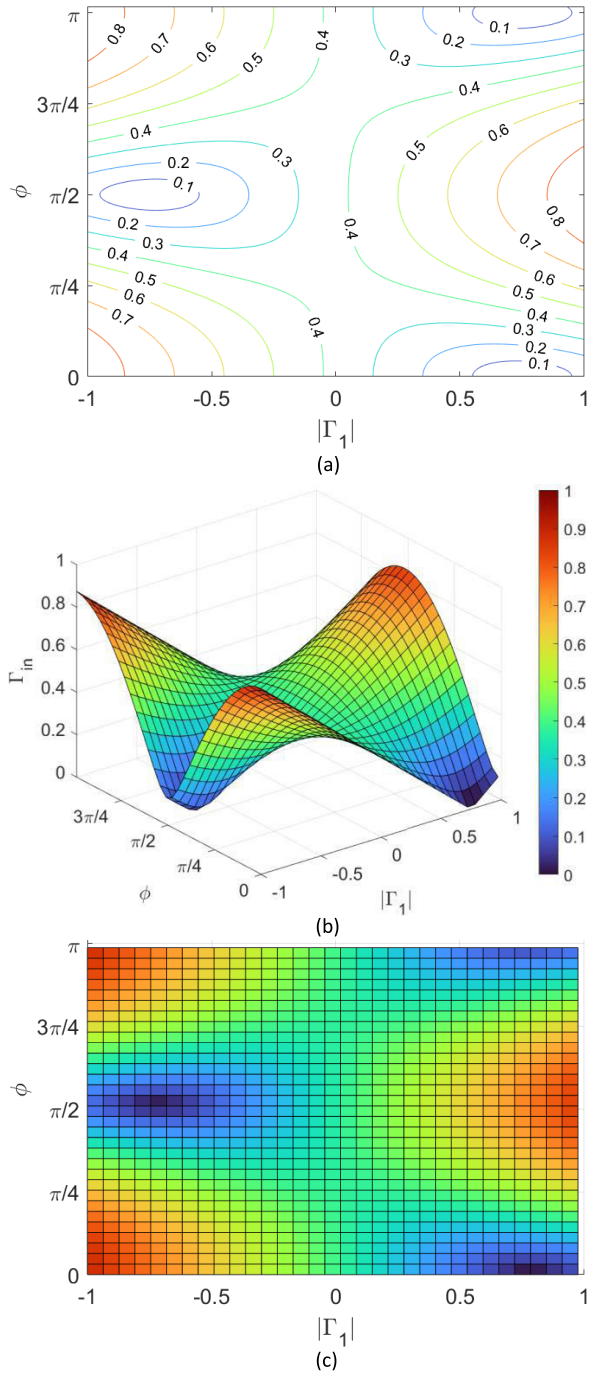

FIGURE 13. The simulated reflection coefficient of the circuit (Γ_{in}). (a) Contour, (b) 3D diagram, and (c) top view of the 3D diagram.

detector diminishes by using any shunt or series resistor in the DC path of the circuit. So, there is a trade-off between having a good matching for each arm and the efficiency of the circuit throughout a wide frequency band using the balanced topology.

Fig. 14 plots the reflection coefficient of the circuit by simulating different values for the magnitude of the reflection coefficients of the diodes. To check the impact of the input

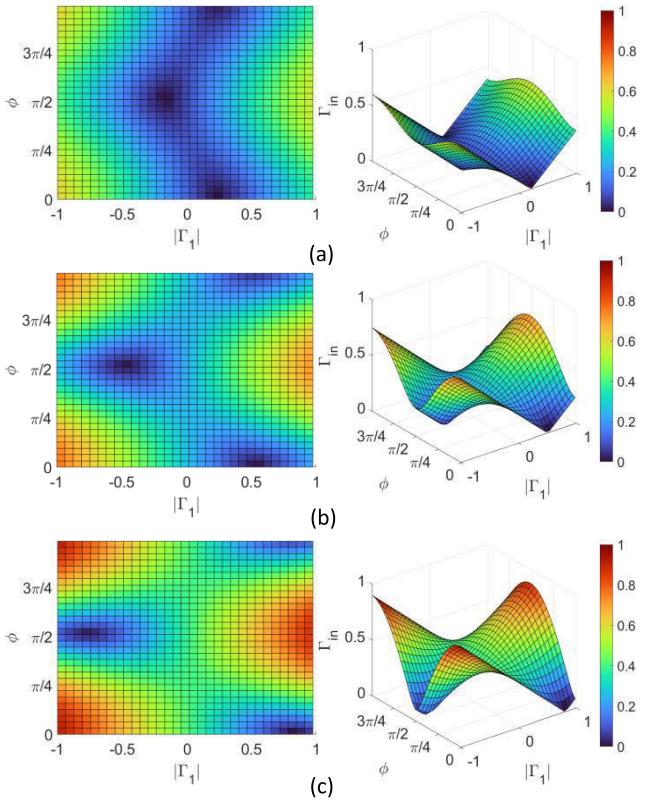

FIGURE 14. The simulated reflection coefficient of the circuit (Γ_{in}) by assuming values of (a) 0.2, (b) 0.5, and (c) 0.8 for magnitude of Γ_2 versus magnitude of Γ_1, and ϕ.

matching network of the diodes, in each of the simulations, the reflection coefficient of one arm (Γ_2) is considered constant with a real value of 0.2, 0.5, and 0.8 respectively. While the reflection coefficient of the other arm (Γ_1) is swept between -1 to $+1$ and the value of the ϕ is between 0 to π radian.

It is obvious from Fig. 14 that the fabrication errors significantly demonstrate a fewer impact on the reflection coefficient of the circuit in case of having a better matching for the diodes. Besides, the matching network of the diodes should exhibit a maximally flat response throughout the entire frequency band to obtain a steady response of the circuit. Also, these networks should be designed without any shunt or series resistors in the DC path of the detector in order to gain a better efficiency.

VI. MEASUREMENT RESULTS

The fabricated power detector, which is situated in a metallic base, utilizes an optimized microstrip to WR-12 transition [8] for the input signal of 60 - 90 GHz. Also the DC path shown in Fig. 5, is connected to a SMA connector. In this measurement, the E8362 PNA Network Analyzer with the Agilent N5260A mm-wave head controller technology is used. The power of the input RF signal is approximately 0 dBm over the frequency band, which is provided by a mm-wave source module type of S12MS (by OML Inc.).

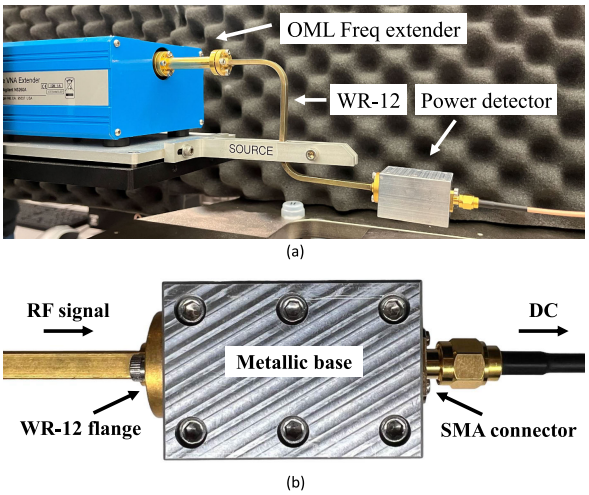

FIGURE 15. (a) The measurement setup and, (b) the proposed power detector situated in a metallic base.

In addition, the DC output voltage of the proposed circuit is measured with the Agilent 34401A digital multimeter. Fig. 15 shows the measurement setup, and the fabricated circuit in the metallic base. The measurement results are illustrated in Fig. 16, as well.

Due to the high inherent reflection coefficient of the utilized diodes (i.e., $|0.71|\, e^{j96.5}$ at 75 GHz) designing a matching network for each arm over the frequency band of 30 GHz is not possible [14]. Also, to alleviate the detector efficiency over the wide operating frequency band, the circuit is designed without any resistive matching network, despite their potential to improve the matching. In this circumstance, the performance of the circuit is highly sensitive to any fabrication error. Based on the measurement results of one the tested circuits with minimum fabrication error, the balanced detector exhibits S_{11} of lower than -10 dB through the wide frequency band of 60 to 90 GHz. The matching results of the circuit is mainly attributed to the utilization of a wide-band matched 90°-hybrid coupler. Considering an acceptable return loss of 10 dB, the maximum tolerable difference between the reflection coefficients of the diodes' arms should be approximately equal to 0.2, in this design. Practically, based on equation (10), the maximum misalignment between the position of the diodes can be calculated as 40 μm. Plus, the diameter of the conductive adhesive can't exceed the approximate value of 350 μm (Fig. 10). In addition, as can be revealed from Fig. 12, the maximum angular misalignment between the diodes and the transmission line is 30°.

The high inherent reflection coefficient of the diode causes power dissipation at port 4 of the coupler. Hence, even though the efficiency of the balanced power detector is at the maximum (i.e., without fabrication error), the output DC voltage is depended on the reflection coefficient of each diode's arm. Fig 16 (b) shows the DC output voltage over the 30 GHz band. Maximum efficiency is obtained at the lower end, over the V-band, where the utilized Schottky diode

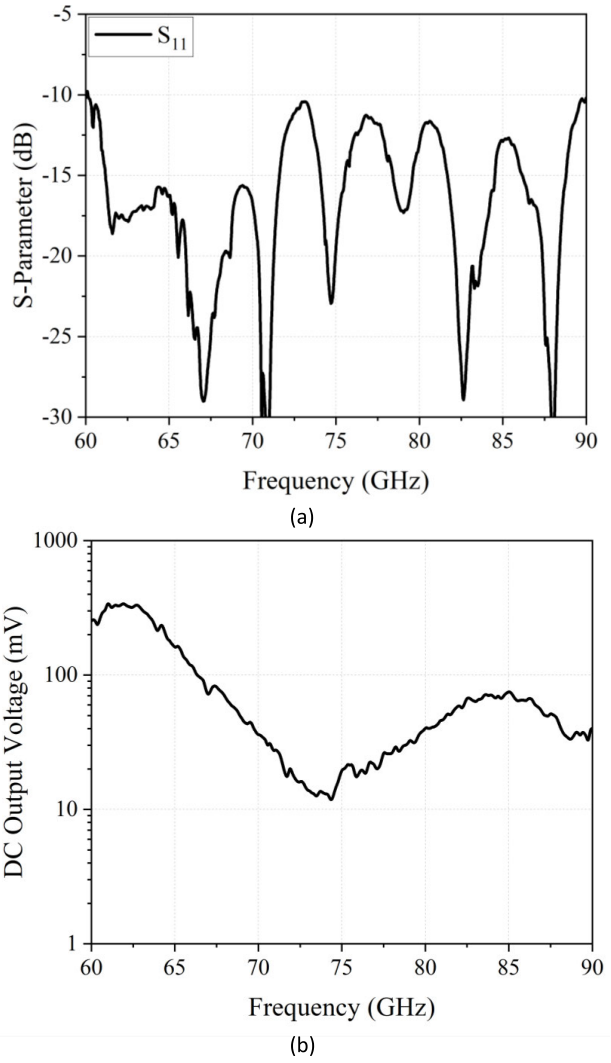

FIGURE 16. Measurement results of the proposed balanced power detector. (a) measured S_{11}, and (b) DC output voltage versus frequency.

operates better. The DC output voltage can be improved by using a matching network (without any resistive components at the DC path) considering a narrower operating frequency band.

VII. CONCLUSION

In this article, a balanced power detector is designed, and fabricated over the frequency band of 60 to 90 GHz. The proposed power detector is designed on the ceramic substrate with a thickness of 127 μm in MHMIC technology. To gain a better understanding of the differences between the simulation and measurement results, different error possibilities that can occur during the fabrication process are analyzed and simulated in ADS, HFSS and CST. To increase the validity of the results of this study, the article used on-wafer measurement results of the fabricated coupler. Also, this article has investigated the dependency of the maximum efficiency and the fabrication errors tolerance of the balanced

power detectors. It is shown that considering an acceptable return loss of 10 dB (i.e., $|\Gamma_{in}| = 0.31$) for the circuit, and using the HSCH 9161 zero bias diode on a 127-μm ceramic substrate, the maximum tolerable misalignment between the diodes in the fabrication process is 40 μm. The diodes' reflection coefficients should be kept equal by using the same amount of conductive adhesive for mounting them alongside the transmission lines. Also, the tolerable angular misalignment between the diodes and the transmission lines is 30°, approximately. The results of this paper can be used to design mm-wave balanced power detector or any other mm-wave circuit that uses similar topology with non-linear components (e.g., transistor, varactor, etc). In addition, these results can give better sight to the designers to predict the impact of the fabrication errors on the performance of the balanced power detectors or any other circuit with balanced topology in planar structures.

REFERENCES

[1] G. Shen, W. Che, W. Feng, Y. Shi, and Y. Shen, "Low insertion-loss MMIC bandpass filter using lumped-distributed parameters for 5G millimeter-wave application," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 11, no. 1, pp. 98–108, Jan. 2021.

[2] W. Deng, Z. Song, R. Ma, J. Lin, Y. Li, J. Ye, S. Kong, S. Hu, H. Jia, and B. Chi, "An energy-efficient 10-Gb/s CMOS millimeter-wave transceiver with direct-modulation digital transmitter and I/Q phase-coupled frequency synthesizer," *IEEE J. Solid-State Circuits*, vol. 55, no. 8, pp. 2027–2042, Aug. 2020.

[3] A. Mostajeran, A. Cathelin, and E. Afshari, "A 170-GHz fully integrated single-chip FMCW imaging radar with 3-D imaging capability," *IEEE J. Solid-State Circuits*, vol. 52, no. 10, pp. 2721–2734, Oct. 2017.

[4] Z. Ni and B. Huang, "Gait-based person identification and intruder detection using mm-Wave sensing in multi-person scenario," *IEEE Sensors J.*, vol. 22, no. 10, pp. 9713–9723, May 2022.

[5] H. Ghannam, D. Nopchinda, M. Gavell, H. Zirath, and I. Darwazeh, "Experimental demonstration of spectrally efficient frequency division multiplexing transmissions at E-band," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 5, pp. 1911–1923, May 2019.

[6] W. Chen, N. Cai, Z. Wu, H. Wang, and J. Ma, "IC solder joints inspection via an optimized statistical modeling method," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 12, no. 2, pp. 341–348, Feb. 2022.

[7] C. Hannachi, B. Zouggari, R. I. Cojocaru, T. Djerafi, and S. O. Tatu, "A V-band high dynamic range planar integrated power detector: Design and characterization process," *Microw. Opt. Technol. Lett.*, vol. 59, no. 11, pp. 2742–2748, Nov. 2017.

[8] S. O. Tatu and E. Moldovan, "Millimeter wave multi-port interferometric radar sensors: Evolution of fabrication and characterization technologies," *Sensors*, vol. 20, no. 19, p. 5477, Sep. 2020.

[9] C. Hannachi, M. E. Romaric, S. O. Tatu, and K. Wu, "Simplified implementation of millimetre-wave zero-bias detector for an accurate detection in six-port-based receivers," *Electron. Lett.*, vol. 56, no. 1, pp. 13–15, Jan. 2020.

[10] B. Zouggari, D. Hammou, C. Hannachi, and S. O. Tatu, "High dynamic range low power drive quadrature millimeter-wave demodulator," in *Proc. 48th Eur. Microw. Conf. (EuMC)*, Sep. 2018, pp. 255–258.

[11] D. Munzer, N. S. Mannem, E. F. Garay, and H. Wang, "Single-ended quadrature coupler-based VSWR resilient joint mm-wave true power detector and impedance sensor," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 5, pp. 2802–2814, May 2022.

[12] A. Serhan, E. Lauga-Larroze, and J.-M. Fournier, "A 700 MHz output bandwidth, 30dB dynamic range, common-base mm-wave power detector," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2015, pp. 1–3.

[13] V. T. Vo and Z. Hu, "Optimization and realization of planar isolated GaAs zero-biased planar doped barrier diodes for microwave/millimeter-wave power detectors/sensors," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 11, pp. 3836–3842, Nov. 2006.

[14] G. Gonzalez, *Microwave Transistor Amplifiers: Analysis and Design*, 2nd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 1997, pp. 327–333.

[15] D. Hammou, T. Djerafi, M. Nedil, and S. O. Tatu, "Considerations for on-wafer millimeter-wave measurements on thin ceramic substrate," *IEEE Trans. Instrum. Meas.*, vol. 65, no. 2, pp. 441–447, Feb. 2016.

[16] *HSCH-9161 Keysight Technologies HSCH-9161 HSCH-9162 GaAs Detector Diode, Data Sheet*. Accessed: Jan. 31, 2024. [Online]. Available: https://www.keysight.com/ca/en/assets/7018-01511/data-sheets/5989-6228.pdf

[17] *EPO-TEK H20E Technical Data Sheet for Reference Only Electrically Conductive, Silver Epoxy*. Accessed: Jan. 31, 2024. [Online]. Available: https://www.epotek.com/docs/en/Datasheet/H20E.pdf

MEHRDAD HARIFI-MOOD received the B.Sc. degree in electrical and electronics engineering and the M.Sc. degree in electronics-IC design from the University of Birjand, Iran, in 2017 and 2020, respectively. He is currently pursuing the Ph.D. degree in telecommunication with Institut National de la Recherche Scientifique (INRS), University of Quebec, Montreal, Canada.

His research interests include passive and active RF/microwave/millimeter-wave components and circuit design. Currently, he is working on designing linear and reliable mm-wave components for lab measurement equipment.

NIMA SOUZANDEH received the B.Sc. degree in electrical and electronics engineering from the University of Tabriz, Iran, in 2014, and the M.Sc. degree in electronics and communications engineering from the Sahand University of Technology, Iran, in 2016. He is currently pursuing the Ph.D. degree in telecommunication with Institut National de la Recherche Scientifique (INRS), University of Quebec, Montreal, Canada.

His research interests include mm-Wave transceiver design, MMIC, remote sensing, and mm-Wave radar for automotive applications.

PEYMAN POURMOHAMMADI (Student Member, IEEE) received the B.Sc. degree in electrical engineering (control systems) from Sadjad University, Iran, in 2009, and the M.Sc. degree in electrical and electronics engineering from Islamic Azad University, Iran, in 2012. He is currently pursuing the Ph.D. degree with Institut National de la Recherche Scientifique (INRS), Université du Quebec, Montreal, Canada. From 2017 to 2021, he was a Research Assistant with the ESAT-WaveCore Division, KU Leuven, Belgium. His research interests include reconfigurable antennas using AFSS structures, SIW-based antennas, metamaterial antennas, wireless body area networks, and wearable and implantable antennas.

DJILALI HAMMOU received the B.Sc. and M.Sc. degrees in electrical engineering from the University of Technology, Oran, Algeria, in 1983 and 2002, respectively, and the Ph.D. degree in telecommunications from Institut National de la Recherche Scientifique-Énergie Matériaux et Télécommunications, Montreal, in 2011. He is currently an Associate Researcher with Institut National de la Recherche Scientifique (INRS-EMT), Montreal, Canada. His research interests include passive microwave millimeter-wave circuit design, hardware and software radio receivers, radio propagation, and telecommunication systems.

BRYAN HOSEIN received the degree from Concordia University, in 2003. He is currently the Vice President of Engineering with Focus Microwaves, Montreal, Canada. His professional experience spans 20 years of research and development work in impedance tuners, software algorithms, and measurement methodologies in various RF device characterization disciplines. Such work includes the development of the Focus MPT series of harmonic tuners, hybrid-active load pull, and wideband noise parameter characterization systems.

SONIA AÏSSA (Fellow, IEEE) received the Ph.D. degree in electrical and computer engineering from McGill University, Montreal, QC, Canada, in 1998.

Since then, she has been with Institut National de la Recherche Scientifique (INRS), Montreal, where she is currently a Full Professor. During her career in telecommunications, she has held various research posts in Canada, Japan, Malaysia, and the U.K. Her research interests include the modeling, design, and performance analysis of wireless communication systems and networks, and wireless power technologies.

Prof. Aïssa is a fellow of the Canadian Academy of Engineering. Her awards include the NSERC University Faculty Award, in 1999; the Quebec Government FRQNT Strategic Faculty Fellowship, from 2001 to 2006; the INRS Performance Award multiple times, for outstanding achievements in research, teaching, and outreach; the 2007 FRQNT-SYTACom Technical Community Service Award; the 2021 IEEE WICE Outstanding Achievement Award; and the 2022 IEEE VTS Women's Distinguished Career Award. She was a recipient of multiple IEEE Best Paper Awards and the 2012 IEICE Best Paper Award. She was a recipient of the NSERC Discovery Accelerator Supplement Award. She was a Distinguished Lecturer of the IEEE Communications Society (ComSoc), from 2013 to 2016. She has an outstanding record of service to the IEEE and serves regularly on many of its committees. She was a Member-at-Large of ComSoc's Board of Governors, from 2014 to 2016. Her editorial activities include, such as an Area Editor of IEEE TRANSACTIONS ON WIRELESS COMMUNICATIONS, from 2014 to 2019; an Editor of IEEE TRANSACTIONS ON WIRELESS COMMUNICATIONS, from 2004to 2012; an Associate Editor and a Technical Editor of *IEEE Communications Magazine*, from 2004 to 2015; a Technical Editor of *IEEE Wireless Communications Magazine*, from 2006 to 2010; and an Editor-at-Large of IEEE TRANSACTIONS ON COMMUNICATIONS, from 2020 to 2023. She currently serves as an Editorial Board Member for IEEE ACCESS. She has been involved in organizing many flagship conferences of the IEEE, including the 2021 IEEE International Conference on Communications for which she served as the TPC Chair. She is active in promoting women in engineering and is the Founder of the IEEE Women in Engineering Affinity Group, Montreal. She is a Member-at-Large of the ComSoc's Board of Governors, from 2023 to 2025.

SERIOJA OVIDIU TATU (Senior Member, IEEE) received the B.Sc. degree in radio engineering from Polytechnic University, Bucharest, Romania, in 1989, and the M.Sc.A. and Ph.D. degrees in electrical engineering from École Polytechnique of Montréal, Canada, in 2001 and 2004, respectively.

He was with the National Company of Telecommunications, Rom-Telecom, Bistrita-Nasaud, Romania; the RF Engineer and the Head of the Telecommunications Laboratory, from 1989 to 1993, and the Technical Manager, from 1993 to 1997. Since 2005, he has been with Institut National de Recherche Scientifique-Énergie Matériaux et Télécommunications, Montreal, QC, Canada. His current research interests include six-port technology, microwave/millimeter-wave circuit design, radio transceivers, and radar sensors.