IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 4 January 2024, accepted 23 January 2024, date of publication 26 January 2024, date of current version 2 February 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3358888

RESEARCH ARTICLE

Switched-LC Hybrid Converters for Versatile Power Supply With DC and Multiple AC Outputs

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ABSTRACT This paper presents, switched-LC hybrid converters for versatile power supply with single DC and multiple AC outputs. The proposed converters are two types i.e., 1) parallel and 2) series switched-LC hybrid multi-output converters (SLCHMOC$_S$). The parallel-series SLCHMOC$_S$ offer multiple 3-phase AC and single-boost DC outputs simultaneously in a single stage. Parallel SLCHMOC$_S$ provide n AC outputs with variable voltage and diverse load currents, alongside single boost DC. However, series SLCHMOC$_S$ is capable of giving n number of AC outputs with the same load current and different voltages. To operate the proposed converters, a hybrid sinusoidal pulse width modulation with constant frequency shoot-through is used. In this work, the proposed converters are implemented for two units operating in a closed loop, supplying one DC and two AC outputs simultaneously at different voltage/current levels. As the proposed converters are capable of delivering multiple AC and single boost DC outputs, they can be applied to the hybrid microgrids. The converters' steady-state, dynamic and efficiency analyses explain their behaviour. Experimental results validate their performance.

INDEX TERMS Constant frequency shoot-through (CFST), digital control, hybrid multi-outputs converter (HMOC$_s$), sinusoidal pulse width modulation (SPWM), three-phase inverter.

I. INTRODUCTION

In recent years, there has been a significant surge in the development of AC/DC hybrid microgrids, representing a systematic approach to integrating various converter outputs, renewable energy sources, energy storage systems (ESS), and local loads within specific regions. These hybrid microgrids offer numerous advantages, including the provision of cost-effective and clean energy, enhanced local resilience, and improved operation and stability of regional electric grids [1], [2]. As a result, it is becoming increasingly clear that hybrid microgrids will be a mandatory requirement for households equipped with both AC and DC loads in the future. Conventional single-output converters, however, fall short in meeting the simultaneous voltage output demands of modern electrical applications, such as hybrid microgrids, hybrid electric vehicles, and standby power supplies [3], [4], [5]. Therefore, the growing demand for hybrid microgrid applications and residential loads necessitates power converters capable of delivering concurrent AC and DC outputs. To address this need, parallel-series switched-LC hybrid multi-output converters (SLCHMOC$_S$) are gaining popularity for their ability to provide simultaneous AC and DC output capabilities. These converters offer a plethora of benefits, including increased power density, compactness, cost-effectiveness, and enhanced reliability [6].

Given the demand and benefits of these proposed SLCHMOC$_S$, extensive research is currently underway in this field, resulting in the evolution of various multi-port output converters and hybrid converter topologies. Some of the multi-output converters discussed in [7], [8], [9], [10], [11], and [12] predominantly focus on DC/DC converters capable of delivering multiple DC outputs; however, they do not have the capability to produce AC output. In [13], a

The associate editor coordinating the review of this manuscript and approving it for publication was Santu Giri.

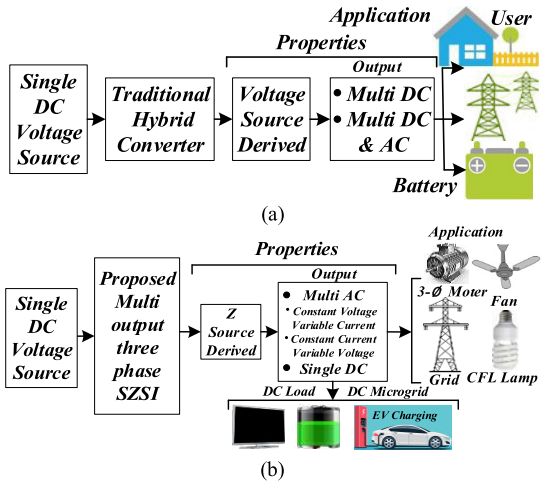

FIGURE 1. Shows Block diagram of (a) conventional and (b) proposed SLCHMOC$_S$.

Z-source inverter with two DC inputs and two AC outputs is presented, although it lacks a DC output. [14] discusses a multilevel inverter with one AC and one DC output. Hybrid converters discussed in [15], [16], [17], and [18] provide two simultaneous outputs (one DC and one AC), but they are not designed to provide simultaneous multi-AC outputs. Split source-based hybrid converters, which produce one single-phase AC and one DC output, are introduced in [19] and [20]. In [21], the presented hybrid converter provides multi-single-phase AC and single DC outputs. However, as it is based on the conventional source-based inverter, it inherits the shoot-through problem. Reference [22] discusses a family of hybrid converter topologies based on Z-source, which can supply both single DC and AC loads simultaneously. In [23], a hybrid quasi-Z-source inverter (qZSI) is presented with dual DC and single AC output, while [24] explores multi-AC output three-phase qZSIs, although they cannot provide both AC and DC outputs simultaneously. References [25], [26], and [27] utilize the series, parallel, and cascaded operation of Z-source converters. In [25], a step-up DC/DC converter with a cascaded (two-stage) qZS-network is introduced by adding one diode, one inductor, and two capacitors to the traditional qZSI. This topology reduces the shoot-through duty cycle by over 30% while maintaining the same voltage boost factor. Reference [26] employs an output-series input-parallel connection of qZSI DC/DC converters with a single-phase isolation transformer and a voltage doubler rectifier to enhance semiconductor device stress and increase DC voltage gain over a wide range of input voltages, all while maintaining the duty cycle of the switches within a reasonable range. In [27], a multiphase quasi-Z-source (qZS) DC-DC converter is presented to increase the DC voltage gain for distributed energy generation applications. It comprises single-switch quasi-Z-source isolated DC-DC cells connected in parallel at the input side and in series at the output side with a voltage doubler rectifier. However, these topologies in [25], [26], and [27] provide only DC output/outputs and lack the capability to generate AC output. Moreover, the presence of transformers in these configurations reduces power density.

In summary, it has been observed that conventional voltage and impedance source multi-output converters generally do not have the capability to deliver multiple AC and DC outputs simultaneously.

To address this limitation and achieve the provision of multiple AC outputs in addition to DC outputs, parallel-series switched-LC hybrid multi-output converters (SLCHMOC$_S$) are proposed in this work. The proposed converters have the capability to simultaneously provide multiple regulated three-phase AC outputs along with one boost DC output. The block diagram shown in Fig. 1(a) represents the conventional SLCHMOC$_S$ for microgrid and residential loads. As conventional SLCHMOC$_S$ is derived from voltage source inverters, they are limited to voltage buck capabilities. Additionally, they suffer from an inherent shoot-through problem due to the misgating of the switches. A representative block diagram of the proposed SLCHMOC$_S$ is shown in Fig. 1(b). It is evident from Fig. 1(b) that the proposed SLCHMOC$_S$ can supply multiple three-phase AC outputs and one boost DC output. These converters have evolved from the quasi-impedance network and inherit all the properties of the qZSI. The proposed SLCHMOC$_S$ have the capability to deliver both buck and boost AC outputs and come equipped with built-in shoot-through protection capability. Moreover, all the outputs of the proposed SLCHMOC$_S$ can be independently regulated to achieve the desired load voltages. These versatile converters can be effectively employed for both DC-DC and DC-AC conversions in a wide range of applications, including hybrid microgrids, renewable energy systems, uninterrupted power supplies, and industrial AC/DC loads. Therefore, the proposed converter has the following merits:

1. The proposed converters can produce regulated multiple three-phase AC outputs and single DC output simultaneously with different voltage/current.
2. The proposed converters inherit all the features of the quasi-Z-source inverter.
3. The proposed converters have inherent shoot-through (ST) protection with buck and boost AC as well as DC voltage capability.
4. Due to single-stage conversion, the proposed converters have fewer losses and are compact, which results in higher power density and efficiency compared to the traditional multi-output converter.
5. The proposed converters are less susceptible to electromagnetic interference (EMI).

The structure of this paper is organized as follows: Section II provides a detailed description of the proposed SLCHMOC$_S$ and their operational principles. Section III delves into the hybrid pulse width modulation technique and control schemes. In Section IV, experimental verification of the proposed SLCHMOC$_S$ is presented, and finally, Section V draws conclusions based on the research findings.

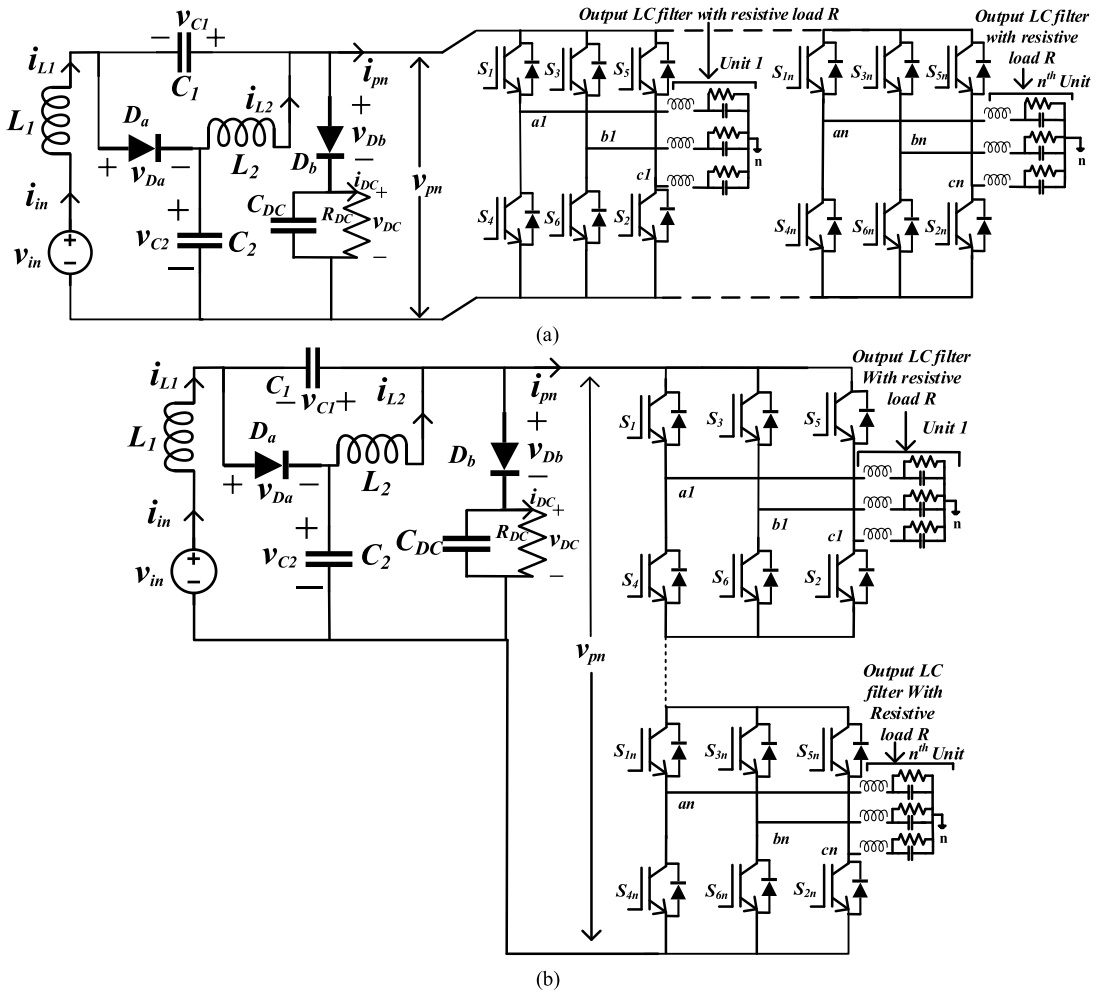

FIGURE 2. Proposed (a) Parallel and (b) Series SLCHMOC$_S$.

II. PROPOSED CONVERTER

Figs. 2(a) and 2(b) illustrate the circuit diagrams for the parallel and series switched-LC Hybrid Multi-Output Converters (SLCHMOC$_S$) proposed in this study. These configurations are achieved by replacing the inverter switch in a switched impedance inverter with multiple three-phase inverters connected either in parallel or in series. The parallel SLCHMOC$_S$ facilitates the simultaneous generation of n sets of three-phase AC outputs along with one DC output. Conversely, the series SLCHMOC$_S$ enables the supply of n sets of three-phase AC outputs with constant current alongside one DC output.

To get the DC output, the switched impedance network undergoes modification by introducing a parallel branch comprising a capacitor (C_{DC}) and a diode (D_b) connected in series across the input of each unit of the three-phase inverter. The D_b serves as a protective component for the capacitor C_{DC} in the event of a shoot-through condition in the circuit. To extract the DC power, a resistive load (R_{DC}) is connected across the capacitor C_{DC} in the switched impedance. Although the combination of R_{DC}, C_{DC}, and D_b resembles a snubber circuit, it actually represents a structural modification in the circuit to enable the supply of DC output.

It is worth mentioning that the proposed SLCHMOC$_S$ have been validated specifically for the case where n equals 2, resulting in two AC outputs and one DC output in this particular study.

A. OPERATING PRINCIPLE, ANALYSIS OF CIRCUIT AND DERIVATION OF BOOST FACTOR

The proposed SLCHMOCs operate in two different modes i.e., shoot-through (ST) and Non-shoot-through (NST) states.

1) SHOOT-THROUGH (ST) STATE

The operation of the proposed SLCHMOCs during the shoot-through (ST) state, along with their equivalent circuits, are illustrated in Fig. 3(a), 3(b) and 3(c). To analyze the circuit behavior, the inverters are replaced with short-circuited switches, resulting in the simplified equivalent circuit shown in Fig. 3(c). During the ST state, both the lower and upper switching devices of all three legs are simultaneously turned ON, which leads to a voltage boost. Additionally, the diodes

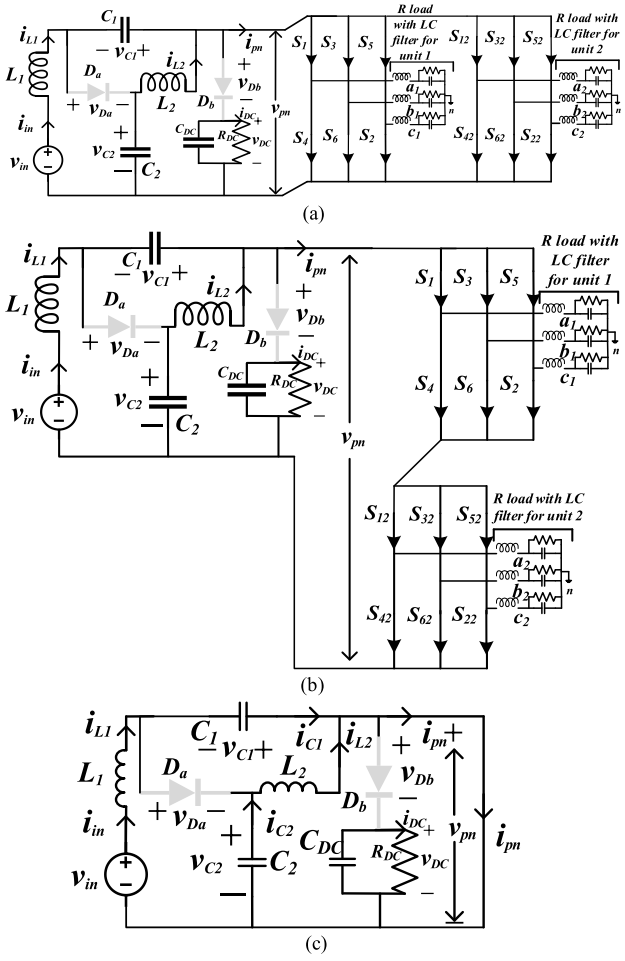

FIGURE 3. Shows proposed (a) parallel, (b) series SLCHMOC$_S$ and (c) Equivalent circuit during ST state.

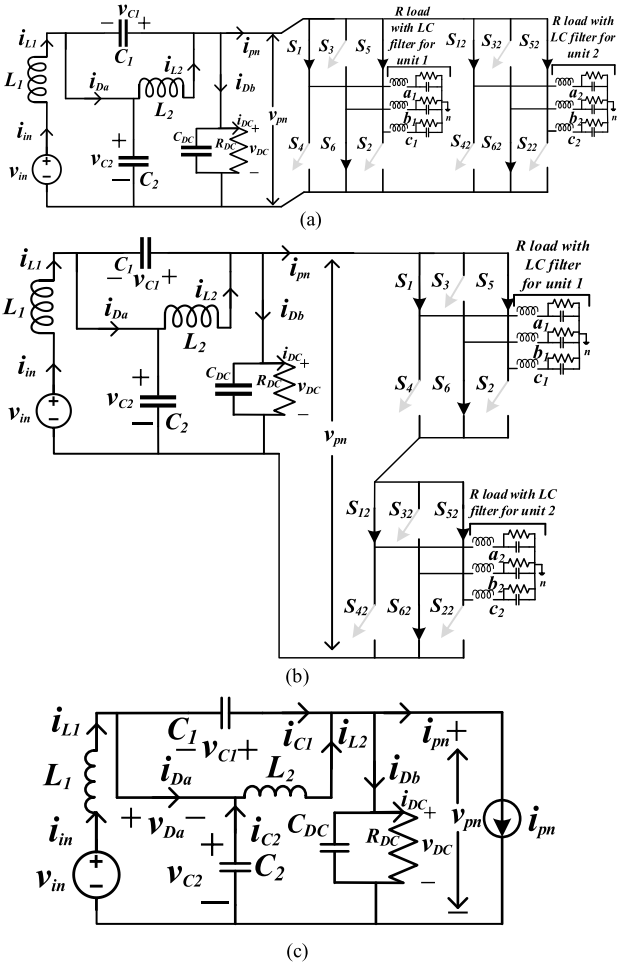

FIGURE 4. Shows proposed (a) parallel (b) series SLCHMOCS and (c) Equivalent circuit during NST state.

D_a and D_b are reverse-biased during this state. It is worth noting that the reverse-biased diode D_b prevents a short circuit across the capacitor C_{DC}, thereby ensuring protection for the proposed SLCHMOCs. The inductors L_1 and L_2 in the impedance source network are charged through the capacitors C_1 and C_2. Moreover, the switch-node voltage v_{pn} is zero in this mode. To determine the inductor voltages and capacitor currents under steady-state conditions, Kirchhoff's voltage law is applied to the impedance source network. which is as follows:

$$\left.\begin{aligned} &L_1\frac{di_{L1}}{dt} = v_{in} + v_{c1}, L_2\frac{di_{L2}}{dt} = v_{c2} \\ &C_1\frac{dv_{c1}}{dt} = -i_{L1}, C_2\frac{dv_{c2}}{dt} = -i_{L2} \\ &v_{pn} = 0, C_{\mathrm{DC}}\frac{dv_{\mathrm{CDC}}}{dt} = -i_{DC} = -\frac{v_{DC}}{R_{DC}}. \end{aligned}\right\} \quad (1)$$

2) NON-SHOOT-THROUGH (NST) STATE

The operation of the proposed parallel and series SLCHMOCs during the non-shoot-through (NST) state, along with their equivalent circuits, is depicted in Fig. 4(a), 4(b), and 4(c). To explain the circuit behavior, the three-phase inverter units are simplified by representing them with an inverted current source (i_{pn}) and the potential difference v_{pn}, as shown in Figure 4(c). During the NST state, it can be observed that neither the lower nor the upper power devices of any one-phase, any two-phase, or all three-phase legs are turned ON simultaneously. Additionally, the diodes D_a and D_b are forward-biased in this state. The inductors L_1 and L_2 in the impedance source network discharge, while the capacitors C_1 and C_2 store energy. Importantly, the voltage v_{pn} is not equal to zero in this state. To determine the inductor voltages and capacitor currents under steady-state conditions, their respective equations are derived based on the circuit configuration and operation during the NST state.

$$\left.\begin{aligned} &L_1\frac{di_{L1}}{dt} = v_{in} - v_{c2}, L_2\frac{di_{L2}}{dt} = -v_{C1} \\ &C_1\frac{dv_{c1}}{dt} = i_{L1} - i_{Da}, C_2\frac{dv_{c2}}{dt} = i_{L2} - i_{Da} \\ &v_{pn} = v_{c1} + v_{c2}, C_{\mathrm{DC}}\frac{dv_{\mathrm{CDC}}}{dt} = i_{Db} - i_{DC}. \end{aligned}\right\} \quad (2)$$

Applying the flux balance principle to the inductors L_1 and L_2 from (1) and (2) over one switching period T, the following

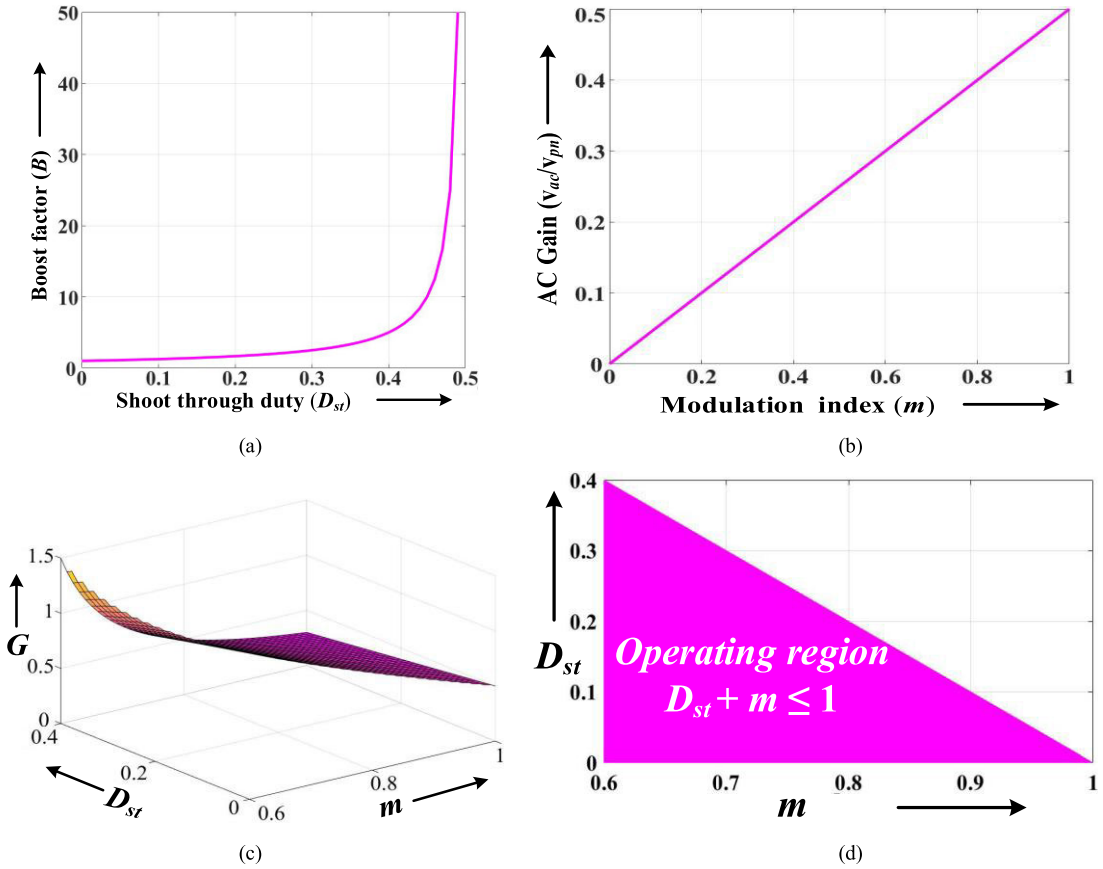

FIGURE 5. (a) Variation of boost factor (B) with ST duty ratio (D_{st}). (b) Variation of V_{AC}/V_{pn} with modulation index (m). (c) Variation of gain (G) with m and D_{st}. (d) Operating region of the proposed converters.

relationship can be derived.

$$\left.\begin{aligned} v_{L1} &= \overline{v_{L1}} = \tfrac{T_s(v_{in}+v_{c1})+T_P(v_{in}-v_{c2})}{T} = 0 \\ v_{L2} &= \overline{v_{L2}} = \tfrac{T_s v_{C2}-T_P v_{C1}}{T} = 0. \end{aligned}\right\} \tag{3}$$

where T_s and, T_p is the time period during ST and NST states, and T is the switching period.

From (3), the following is obtained

$$\left.\begin{aligned} v_{C1} &= \tfrac{D_{st}}{1-2D_{st}} v_{in},\ v_{C2} = \tfrac{1-D_{st}}{1-2D_{st}} v_{in} \\ v_{pn} &= v_{DC} = \tfrac{1}{1-2D_{st}} v_{in}. \end{aligned}\right\} \tag{4}$$

Similarly, applying the charge balance principle to the capacitors C_1 and C_2 from (1) and (2), the following can be obtained.

$$\left.\begin{aligned} i_{C1} &= \overline{i_{C1}} = \tfrac{T_s(-i_{L1})+T_P(i_{L1}-i_{Da})}{T} = 0 \\ i_{C2} &= \overline{i_{C2}} = \tfrac{T_s(-i_{L2})+T_P(i_{L2}-i_{Da})}{T} = 0. \end{aligned}\right\} \tag{5}$$

From (5), the expression for i_{L1} and i_{L2} are obtained as

$$i_{L1} = \frac{(1-D_{st})}{(1-2D_{st})} i_{Da}, \quad i_{L2} = \frac{(1-D_{st})}{(1-2D_{st})} i_{Da}. \tag{6}$$

From (4), the DC boost factor (B) is expressed as

$$B = \frac{\hat{v}_{pn}}{v_{in}} = \frac{1}{1-2D_{st}}. \tag{7}$$

The peak AC voltage of the fundamental component of the output is

$$(\hat{v}_{AC})_{fundamental} = \hat{v}_{AC} = \frac{m}{2} v'_{pn} = \frac{m}{2}\left(\frac{1}{1-2D_{st}}\right) v_{in}. \tag{8}$$

where m is the modulation index of the inverter. v'_{pn} is the input voltage for each unit and is equal to v_{pn} and $v_{pn}/2$ for the parallel and series SLCHMOCs respectively.

The ratio of the fundamental peak to the input voltage (v_{in}) is known as the gain of the inverter and is given by

$$G = \frac{(\hat{v}_{AC})_{fundamental}}{v_{in}} = \frac{m}{2}\left(\frac{1}{1-2D_{st}}\right). \tag{9}$$

The gain of the proposed SLCMOCs is the same as the gain of conventional qZSI. By varying the ST duty ratio (D_{st}) and m, the gain (G) of the converter can be varied.

The constraint (10) for sinusoidal pulse width modulation (SPWM) with ST duty ratio in the proposed SLCHMOCs states that the sum of m and D_{st} should be less than or equal to 1. This constraint ensures that the modulation index and the duty cycle do not exceed the maximum allowable values.

$$m + D_{st} \leq 1. \tag{10}$$

Fig. 5 provides graphical representations of various voltage gains with respect to D_{st} and m. Fig. 5(a) shows the variation

of parameter B with D_{st}. Fig. 5(b) illustrates the relationship between the ratio of the output AC voltage (v_{AC}) and the peak switch node voltage (peak v_{AC}/v_{pn}) with m. Fig. 5(c) presents a 3D graphical representation depicting the variation of the gain G (ratio of v_{AC} and input DC voltage v_{in}) with both D_{st} and m. Finally, Fig. 5(d) displays the operating region of the proposed converters.

B. AC AND DC POWER EXPRESSION OF THE PROPOSED SLCHMOCS

The AC and DC expression for the proposed SLCHMOCS are expressed in the following subsection.

1) PROPOSED PARALLEL SLCHMOCS

Moving on to the AC and DC power expressions, let's consider the proposed parallel SLCHMOCs with two inverter units. In this mode, both inverter units receive the same input voltage (v_{pn}), and the peak AC voltages ($\hat{v}_{AC1}$ and $\hat{v}_{AC2}$) are equal. These peak AC voltages are determined by (8) and are dependent on the reference voltages (v_{ref}) and balance AC loads. Since both inverter units receive the same input voltage (v_{pn}), the $\hat{v}_{AC1}$ and $\hat{v}_{AC2}$ will differ based on the assigned v_{ref} values. The gain G, given by equation (9), remains the same for both converters.

From (9), the rms AC output voltage ($v_{ac,rms} = \frac{\hat{v}_{AC}}{\sqrt{2}}$) is

$$v_{AC,rms} = \frac{\hat{v}_{AC}}{\sqrt{2}} = \frac{Gv_{in}}{\sqrt{2}} = \frac{m}{2\sqrt{2}}\left(\frac{1}{1-2D_{st}}\right)v_{in}. \quad (11)$$

The three-phase AC power output ($P_{3-\emptyset}$) of both units at the same v_{ref} is

$$P_{3-\emptyset} = 6\frac{v_{AC,rms}^2}{R_{AC}} = 6\frac{m^2B^2v_{in}^2}{8R_{AC}}. \quad (12)$$

Similarly, the three-phase AC power output $P_{3-\emptyset}$ of both the units at different v_{ref} is given as

$$P_{3-\emptyset} = 3\frac{(m_1^2+m_2^2)B^2v_{in}^2}{8R_{AC}}. \quad (13)$$

where R_{AC} is the load resistance, and m_1 and m_2 are the modulation indices of converter units 1 and 2, respectively.

The DC output power P_{DC} of the proposed converter in parallel SLCHMOCs is

$$P_{DC} = \frac{v_{DC}^2}{R_{DC}} = \frac{v_{in}^2}{R_{DC}(1-2D_{st})^2}. \quad (14)$$

where R_{DC} is the DC load resistance of the proposed converter. It is clear from (13) and (14) that $P_{3-\emptyset}$ depends on both m and D_{st}, whereas P_{DC} depends on D_{st} only.

2) PROPOSED SERIES SLCHMOCS

In series SLCHMOCs with two units, the switch node voltage (v_{pn}) is equally distributed across the inverter units to achieve a balanced AC load. In this configuration, the peak AC voltages ($\hat{v}_{AC1}$ and $\hat{v}_{AC2}$) are equal when the same reference voltage (v_{ref}) is applied. These peak AC voltages can be calculated using (8), which is as follows:

$$\hat{v}_{AC1} = \hat{v}_{AC2} = \frac{m}{2}\frac{v_{pn}}{2} = \frac{m}{4}\left(\frac{1}{1-2D_{st}}\right)v_{in} \quad (15)$$

The rms AC voltage ($v_{AC,rms}$) for both the units is given as

$$v_{AC,rms} = \frac{\hat{v}_{AC}}{\sqrt{2}} = \frac{m}{4\sqrt{2}}\left(\frac{1}{1-2D_{st}}\right)v_{in}. \quad (16)$$

The three-phase AC power output $P_{3-\emptyset}$ of a single unit is

$$P_{3-\emptyset} = 3\frac{v_{AC,rms}^2}{R_{AC}} = 3\frac{m^2B^2v_{in}^2}{32R_{AC}}. \quad (17)$$

TABLE 1. Voltage and current stresses of the proposed topology.

Parameter	Voltage stress	Parameter	Current stress
C_1	$\frac{(D_{st})\,v_{in}}{(1-2D_{st})}$	L_1	i_{in}
C_2	$\frac{(1-D_{st})\,v_{in}}{(1-2D_{st})}$	L_2	$\frac{(1-D_{st})\,i_{pn}}{(1-2D_{st})}$
C_{DC}	$\frac{v_{in}}{(1-2D_{st})}$	D_a	$\frac{i_{pn}}{(1-2D_{st})}$
D_a, D_b	$\frac{v_{in}}{(1-2D_{st})}$	D_b	$\frac{i_{dc}}{(1-D_{st})}$

TABLE 2. Cost of two single-unit individual converters.

Component Name	Item No/ Rating	Price per component	No of components required	Total price (USD)
Inductors	3.5 mH, 15 A	7.15	4	28.6
Capacitors	470 uF, 250 V	4.66	6	27.96
Diodes	40EPF06	4.56	4	18.24
Inverter switches	FGH40T65UPD	4.63	12	55.56
Total number of components			26	---
			Total Cost	130.36

TABLE 3. Cost of proposed converters with two units.

Component Name	Item No/Rating	Price per component	No of components required	Total price (USD)
Inductors	5.3 mH, 20 A	12.66	2	25.32
Capacitors	470 uF, 400 V	8.28	3	24.84
Diodes	DWD10G120C5XKSA1	5.51	2	11.02
Inverter switches	FGH40T65UPD	4.63	12	55.56
Total number of components			19	---
			Total Cost	116.74

TABLE 4. Comparison among previously reported switched capacitor-based and proposed SLCHMOCs.

Reference	No. of Outputs	Advantages	Disadvantages
[31]	1	✓ High gain converter ✓ Less number of passive components ✓ NO need of output AC filter	× Unable to produce multiple AC × The number of switches is high- for single AC outputs, nine switches, two diodes and two capacitors are required × Unable to produce DC output × Not suitable for high power application
[32]	1	✓ High gain converter ✓ Less number of passive components ✓ NO need of output AC filter ✓ High efficiency	× No multiple AC output × No three-phase AC output × The number of switches is high- for single AC outputs, ten switches, one diode and two capacitors are required × Unable to produce DC output × Not suitable for high power application
[33]	1	✓ Multi input single output converter ✓ Less number of passive components ✓ NO need of output AC filter	× Input filter required due to discontinuous input current × Low voltage gain × No multiple AC output × No three-phase AC output × The number of switches is high- for single AC output, seven switch, two diodes, one capacitor and two DC source are required
[34]	1 (extendable)	✓ Seven level inverters with switched capacitor technique ✓ Reduced components ✓ Less over all voltage stress ✓ Natural balance	× Low voltage gain × No multiple AC output × No three-phase AC output × The number of switches is high-for single AC output, nine switch and three capacitors are required
Proposed Converters	3 (Extendable)	✓ Multiple three-phase AC with one boost DC outputs simultaneously ✓ Less no of passive components (two inductors and two capacitors) irrespective of the no. of AC outputs ✓ Higher power density ✓ Suitable for high-power applications ✓ NO input filter is required ✓ Inherent ST protection ✓ All the outputs are independently regulated	× Low voltage gain Remark: The limitations given above in the previous topologies have been taken care of in the proposed converters.

The three-phase AC power output ($P_{3-\emptyset}$) of both units is

$$P_{3-\emptyset} = 6\frac{v_{AC,rms}^2}{R_{AC}} = 6\frac{m^2B^2v_{in}^2}{32R_{AC}}. \tag{18}$$

The DC output power (P_{DC}) of the parallel and series SLCHMOCs is equal, as expressed in (14).

In voltage control mode, the peak AC voltage ($\hat{v}_{\mathrm{AC}}$) is directly proportional to the m of the inverter. Additionally, in the series mode converter, $\hat{v}_{\mathrm{AC}}$ is equal to the peak value of the reference voltage (v_{ref}). Therefore, as the v_{ref} is increased, the m also increases. This relationship causes the output power to increase correspondingly. Conversely, when v_{ref} is decreased, the m decreases, resulting in a decrease in output power.

C. COMPONENTS VOLTAGE/CURRENT STRESSE AND COST ANALYSIS

Table 1 provides information on the voltage and current stresses of each component in the proposed SLCHMOCs, which is crucial for selecting the appropriate component ratings based on the mode (parallel or series) and the number of units in the converter.

In the parallel SLCHMOCs, increasing the number of units results in more current stresses on L_1, L_2, and D_a because the input and switch node currents (i_{in} and i_{pn}) increase. However, the voltage stresses on capacitors and diodes depend on the ST duty ratio D_{st}. Therefore, when operating with constant switch node voltages stresses on capacitors and diodes depend on the ST duty ratio D_{st}. Therefore,

when operating with constant switch node voltages (v_{pn}), D_{st} remains constant, and consequently, the voltage stresses are also constant. In the series SLCHMOCs, as the number of units increases, i_{pn} and i_{in} remain the same for all units. Hence, the current stresses remain constant. However, as v_{pn} increases with the number of units, D_{st} also increases. As a result, the voltage stresses on capacitors and diodes increase.

Increasing stress on front-end components (inductors and capacitors) raises their ratings and costs. However, the proposed converters with multiple units remain more cost-effective than using the same number of independent converters, even for three-phase loads. This justifies their practical application.

Tables 2 and 3 provide a cost analysis of two single-unit converters and the proposed converters with two units in parallel, both delivering 2.18 kW. The fixed number of front-end components in the proposed converters contributes to their cost advantage. Thus, implementing these converters with multiple units offers a cost-efficient solution without compromising performance for various real applications.

In the scenario of two single-unit individual converters, the total component count, including passive elements and switches, is 26, amounting to a cost of 130.36 USD.

Conversely, the proposed converter with two units requires only 19 components, costing 116.74 USD. The reduced component count in the proposed converters is primarily due to the fixed front-end passive components. Despite the higher price per component in the proposed converters, resulting from increased stress/rating, the overall cost is lower compared to using two single-unit individual converters. This cost advantage can be attributed to the decreased number of components and the utilization of fixed front-end passive elements in the proposed converter configuration.

In summary, the proposed converters exhibit different stress characteristics depending on the mode and number of units. Despite the increased stress/rating on individual components, the overall cost of the converters with multiple units are lower than using the same number of independent converters. This cost advantage arises from the fixed front-end component count and the reduced number of components in the proposed converters. Therefore, employing the proposed converters with multiple units is a practical and cost-effective choice for various applications.

D. COMPARATIVE ANALYSIS AMONG EXISTING AND PROPOSED PSHOMOCS

Table 4 illustrates the advantageous features of the proposed SLCHMOCs when compared to existing switched capacitor-based converters, showcasing their meaningful benefits.

III. CONTROL SCHEME FOR THE PROPOSED SLCHMOC$_S$

The following subsections described control schemes for regulating DC/AC power flow in the proposed converters.

A. HYBRID PWM TECHNIQUE FOR THE SLCHMOC$_S$

A hybrid sinusoidal pulse width modulation (SPWM) scheme with constant frequency shoot-through (CFST) has been implemented on the DSP board TI-TMS320F28335 to operate the proposed converters. The switching signals for generating NST (non-shoot-through) and ST (shoot-through)

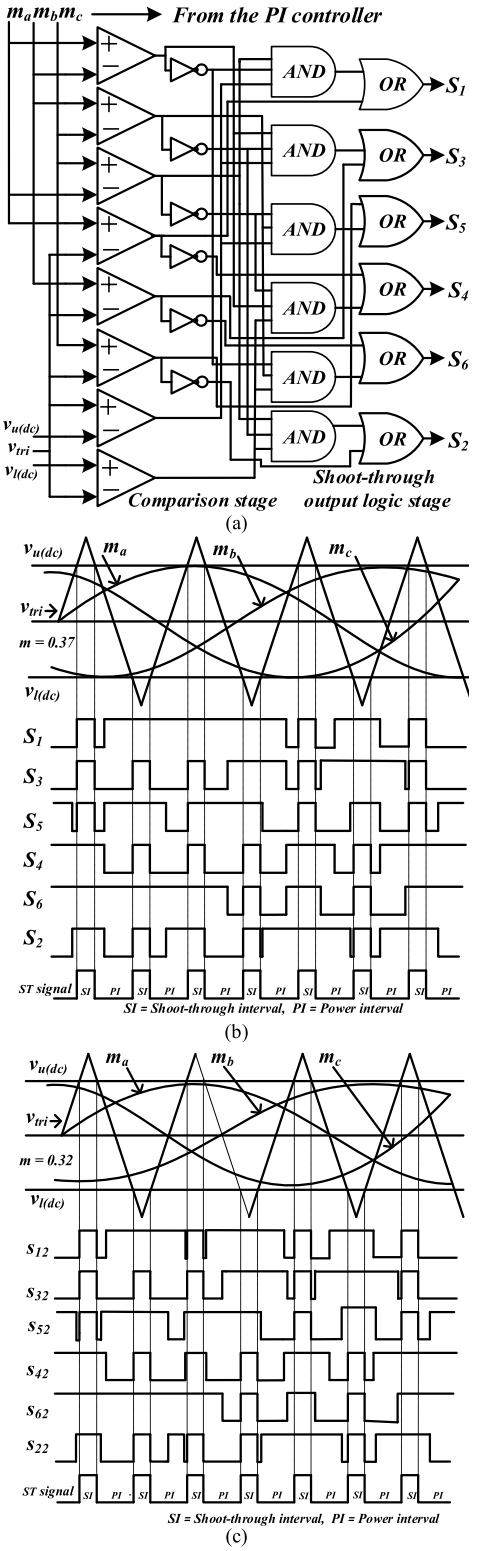

FIGURE 6. (a) PWM control logic. (b) PWM signals of converter unit 1 with $V_{ref} = 70$ V ($m = 0.37$) and (c) unit 2 with $V_{ref} = 60$ V ($m = 0.32$) for the proposed converters.

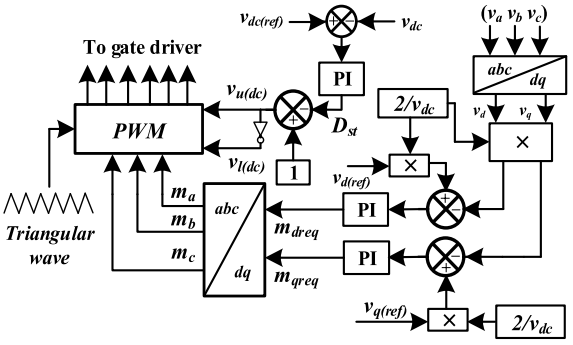

FIGURE 7. The control scheme for the proposed converters.

states in the Z-source inverters are obtained using this hybrid modulation scheme [28]. The overall modulation scheme of the proposed converters, along with the switching signals, is depicted in Fig. 6. Fig. 6(a) illustrates the logic diagram for the modulation scheme, while Fig. 6(b) and 6(c) display the corresponding switching signals for two parallel units. In this particular case, the value of D_{st} is set to 0.3289, which remains the same for both units to maintain a constant switch node voltage of 380 V. However, the modulation indices differ based on the desired AC output voltage requirements. For unit 1 (with a 70 V output), the modulation index is 0.3684, while for unit 2 (with a 60 V output, as shown in Fig. 11(d)), the modulation index is 0.3157. The ST states, characterized by the duty ratio D_{st}, are determined by comparing the reference triangular waves with two constant DC signals: an upper $v_{u(dc)}$ and a lower $v_{l(dc)}$. The magnitudes of these DC signals are determined by the desired DC output voltage. When the carrier wave is higher than the upper constant DC signal $v_{u(dc)}$ or lower than the lower DC signal $v_{l(dc)}$, the ST signals are generated. In the ST state, all three leg switches (S_1 to S_6) are turned ON simultaneously. In the NST state, the switching signals for the first leg switches (S_1 and S_4) of the inverter are generated by comparing m_a and its complementary signal with the triangular carrier wave. Similarly, the switching signals for the second leg (S_3, S_6) and third leg (S_5, S_2) are generated by comparing the carrier wave with m_b and m_c, respectively.

B. CONTROLLER DESIGN FOR THE PROPOSED SLCHMOCs

The block diagram of the overall control scheme for the proposed converters are presented in Fig. 7. To control the three-phase output voltages (v_a, v_b, and v_c) of the inverter units, *d-q* control mode operation is employed along with a PI controller. The sensed AC output voltages are transformed into their *d-q* components using Park's and Clark's transformations. These transformed values are then compared with the reference voltage of the *d-q* components. Subsequently, sinusoidal modulating signals (m_a, m_b, and m_c) are generated by the controller. To regulate the DC voltage, a comparison is made between the required DC voltage and the reference DC voltage, and the resulting error is passed through a PI

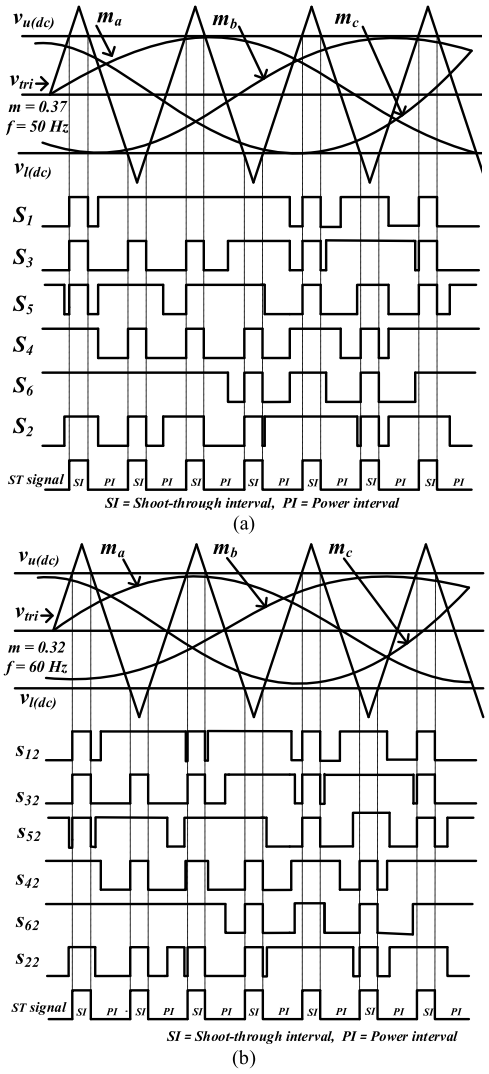

FIGURE 8. Switching signals for (a) unit 1 with output voltages 70 V (peak), 50 Hz (b) unit 2 with output voltage 60 V (peak), 60 Hz.

controller. This process yields DC-modulating signals for the shoot-through (ST) periods. The switching signals for PWM operation are generated by utilizing these modulating signals in conjunction with triangular signals.

C. PWM SIGNALS AND OPERATION OF THE PROPOSED CONVERTERS WITH MULTIPLE UNITS FOR DIFFERENT VOLTAGES AND FREQUENCIES

The proposed SLCHMOCs offer complete flexibility in operating multiple converter units without the need for additional front-end components. These converter units can operate individually at different voltages and frequencies, as required, within the proposed scheme. To illustrate this flexibility, let's consider an example of two converter units connected in parallel.

Fig. 8(a) and (b) depict the switching signal generations for these parallel units. Unit 1 is required to deliver an output voltage magnitude of 70 V (peak) at a frequency of 50 Hz, while unit 2 needs to provide an output voltage magnitude

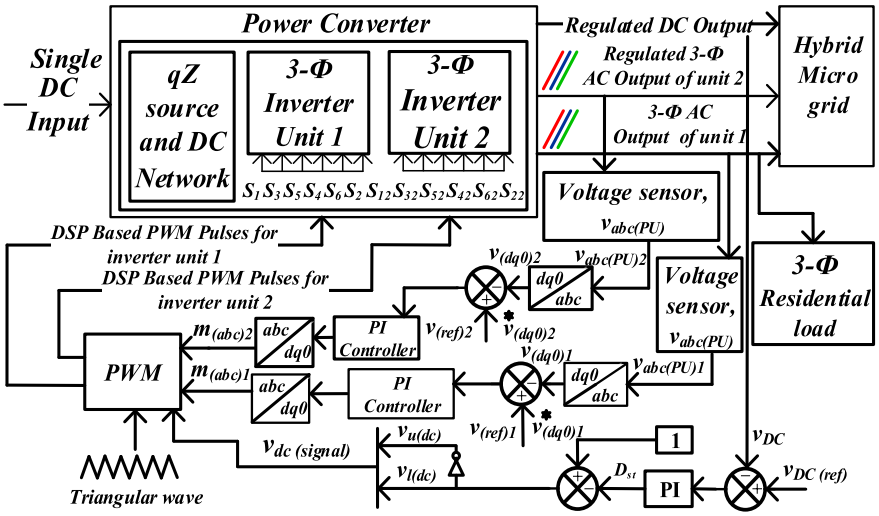

FIGURE 9. Overall implementation of the proposed SLCHMOC**S**.

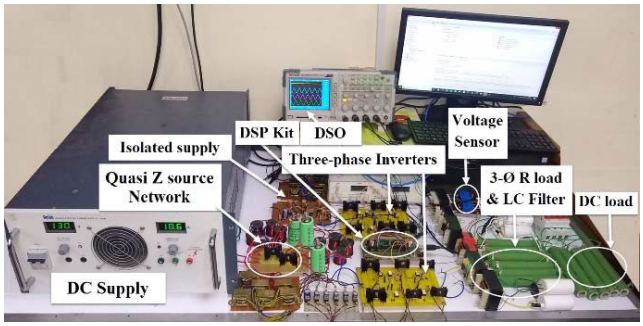

FIGURE 10. Photograph of the experimental setup.

TABLE 5. Proposed converters parameter.

Parameter	Rating
Power P	2.18 kW (for parallel)
	2.02 kW (for series)
Input voltage v_{in}	130 V (for parallel)
	130 V (for series)
Inductor ($L_1 = L_2$)	5 mH
Capacitor ($C_1 = C_2 = C_{DC}$)	470 uF
Switching frequency f_s	10 kHz
DC load resistance R_{DC}	100 Ω
AC load resistance R_{AC}	20 Ω
Filter inductor L_f	2 mH
Filter capacitor C_f	10 uF
Switches (IGW25N120H3FKSA1)	1200 V, 50 A
Diode (IDWD10G120C5XKSA1)	1200 V, 34 A

of 60 V (peak) at a frequency of 60 Hz. The input voltage is 130 V, and the desired DC output voltage is 380 V. To achieve the 380 V DC output, both units maintain the same ST duty ratio ($D_{st} = 0.3289$). The duty signals are derived by comparing reference triangular waves with two constant DC signals (upper $v_{u(dc)}$ and lower $v_{l(dc)}$), which have a magnitude corresponding to $D_{st} = 0.3289$. For unit 1, the output voltage of 70 V (peak) at 50 Hz is obtained by comparing the reference triangular signals with three-phase sinusoidal modulating signals having a modulating index (m) of 0.37 and a frequency of 50 Hz. Conversely, for unit 2, the output voltage of 60 V (peak) at 60 Hz is obtained by comparing the reference signal with sinusoidal modulating signals having $m = 0.32$ and a frequency of 60 Hz. In this manner, the converter units can be operated at different voltages and frequencies to meet specific requirements. The proposed SLCHMOCs enable this flexibility without the need for additional front-end components, allowing the units to operate effectively together.

IV. VERIFICATION

For the experimental validation of the proposed converters, the researchers conducted tests with $n = 2$, representing two simultaneous AC outputs and one DC output. The block diagram of the overall implementation of the converters is presented in Fig. 9. In this setup, a 32-bit TMS320F28335 DSP, operating at a clock frequency of 150 MHz, is utilized to generate the gating signals for the converters. To ensure compatibility with the ADC pin of the DSP, which accepts only DC signals ranging from 0 to 3.3 V, it is more suitable to use an analog-to-digital converter (ADC). The parameters of the complete system can be found in Table 5. In the subsequent subsections, A and B, the steady-state and dynamic results of both the proposed parallel and series SLCHMOCs are comprehensively presented. Fig. 10 provides a visual depiction of the experimental setup, showcasing the implemented configuration for reference.

A. VALIDATION OF THE PROPOSED PARALLEL SLCHMOCs

The proposed parallel SLCHMOC*s* are tested for 2.18 kW with DC power (P_{DC}) 1444 W and AC power (P_{AC}) 735 W.

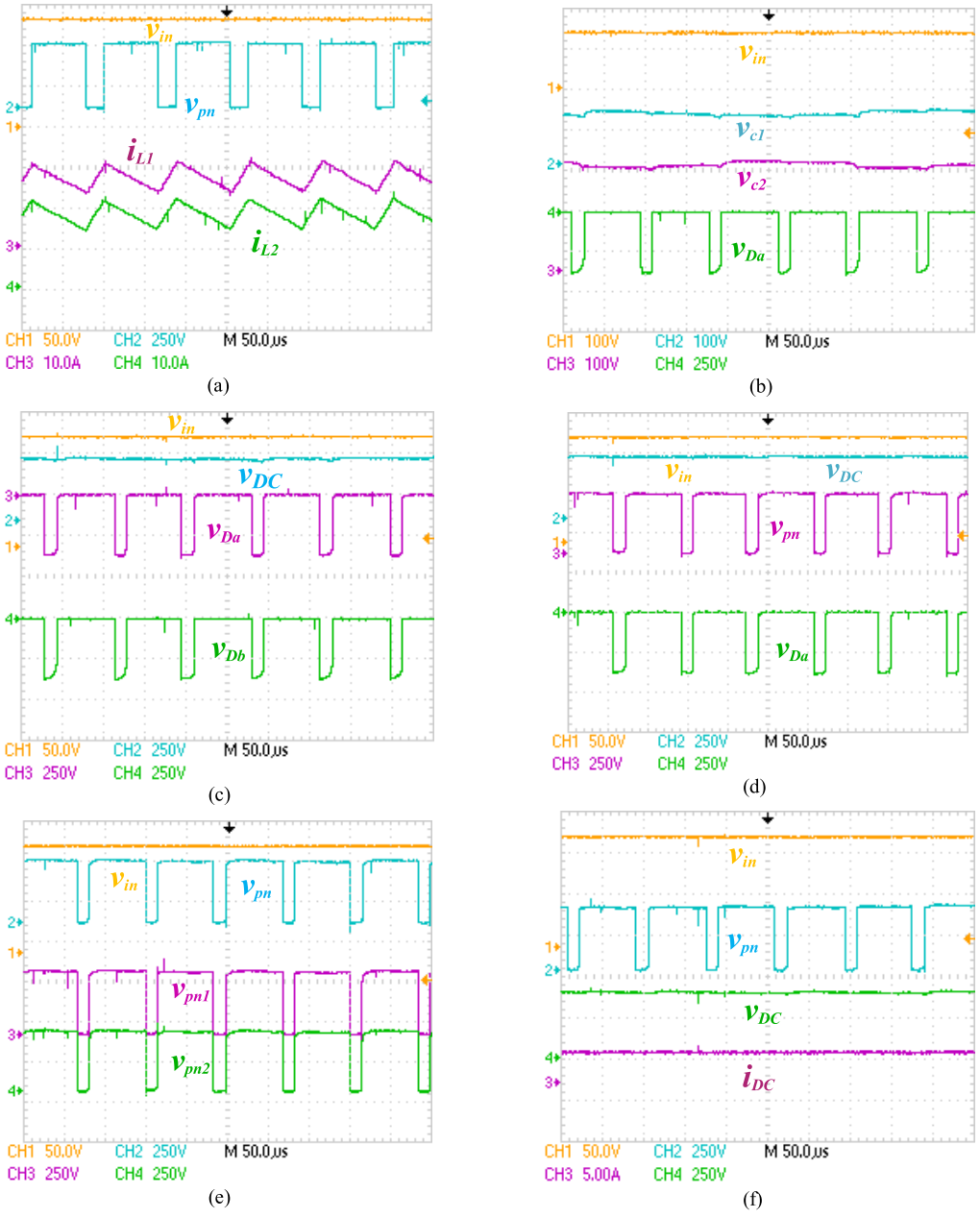

FIGURE 11. Steady-state result of the proposed parallel SLCHMOCS. (a) Inductor currents with v_{in} and v_{pn}. (b) Capacitor voltages with v_{in} and v_{Da}. (c) Diode voltages with v_{in} and v_{DC} (d) DC voltage with v_{pn} and v_{Da}. (e) Switch node voltages. (f) DC voltage and current.

1) STEADY-STATE RESULTS

In Figs. 11 and 12, the steady-state response of the proposed parallel SLCHMOCs are shown, considering an AC voltage reference $v_{\text{ref}} = 70$ V and a DC voltage reference $v_{\text{dcref}} = 380$ V. In Fig. 11(a), the input voltage v_{in} is depicted as 130 V, along with the switch node voltage v_{pn} at the theoretical value of 380 V. Additionally, the inductor currents i_{L1} and i_{L2} are shown, both equal to the input current i_{in} of 18.6 A. Fig. 11(b) illustrates the input voltage v_{in} at 130 V, along with the voltage across capacitors $C_1(v_{\text{c1}} = 125$ V) and $C_2(v_{\text{c2}} = 255$ V). Furthermore, it displays the switching voltage waveform of diode D_a (v_{Da}). During the NST state, diode D_{a} is forward-biased, resulting in a voltage of zero across it. Conversely, during the ST interval, diode D_{a} becomes reverse-biased, leading to a negative v_{Da}. In Fig. 11(c), the input voltage v_{in} at 130 V, the DC output voltage v_{DC} at 380 V, and the voltage waveforms across diodes D_{a} and D_{b} are shown. During the NST state, diode D_{b} is forward-biased, causing the voltage across it (v_{Db}) to be zero. Conversely, during the ST state, diode D_{b} becomes reverse-biased, resulting in a negative v_{Db}. Fig. 11(d) displays the switch node voltage v_{pn} along with the input voltage v_{in} at 130 V, the DC output voltage v_{DC}

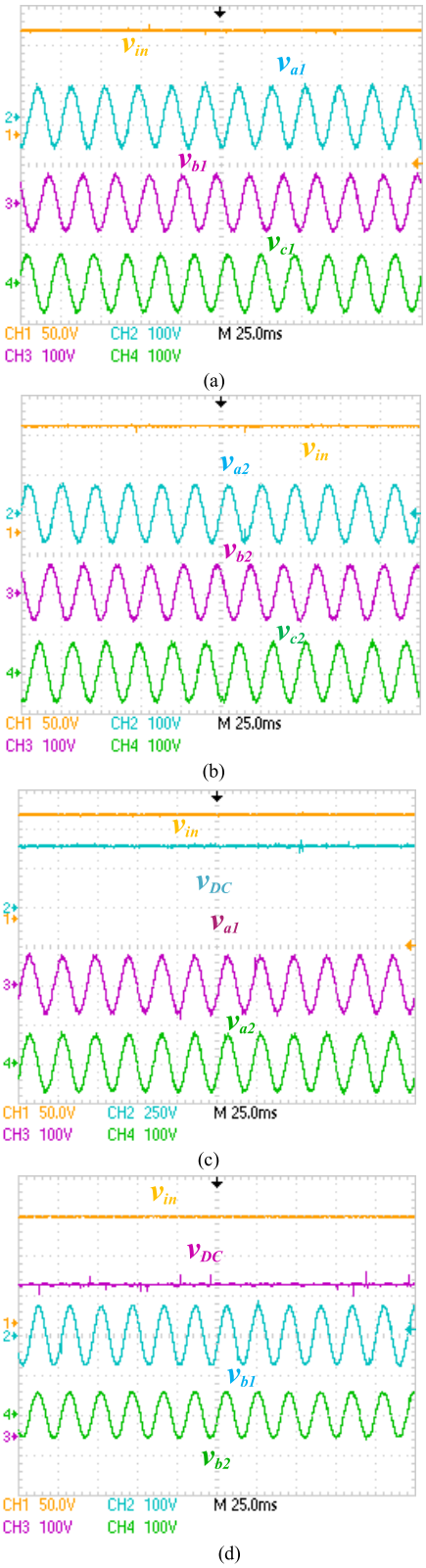

FIGURE 12. (a) Three-phase voltages of unit 1 with v_{in}. (b) Three-phase voltages of unit 2 with v_{in}. (c) Phase voltages of units 1 and 2 with v_{DC} at v_{ref} = 70 V. (d) Phase voltages of units 1 and 2 with v_{DC} at different v_{ref}.

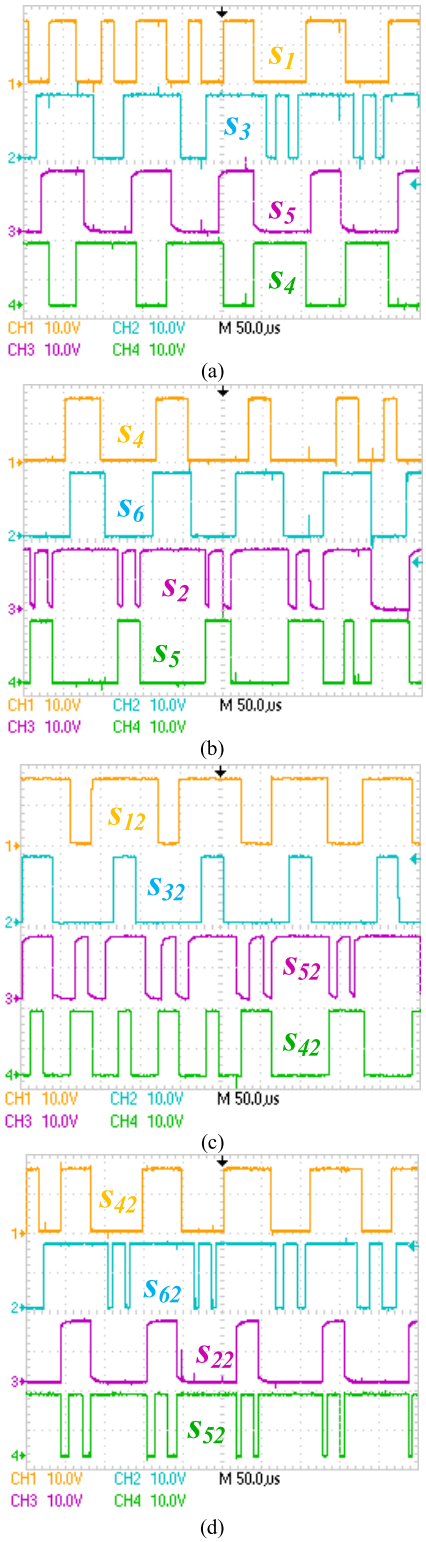

FIGURE 13. Hybrid PWM signals for (a) upper and (b) lower switches with S_4 and S_5 (c) upper and (d) lower switches with S_{42} and S_{52} of converter units 1and 2 of the proposed parallel SLCHMOC$_s$.

at 380 V, and the voltage waveform of diode D_a. In Fig. 11(e), the input voltage v_{in}, the switch node voltages of converter units 1 and 2, equal to $v_{pn1} = v_{pn2} = 380$ V are shown. This switch node voltage ($v_{pn1} = v_{pn2}$) matches the output voltage of the impedance source network (v_{pn}). Furthermore,

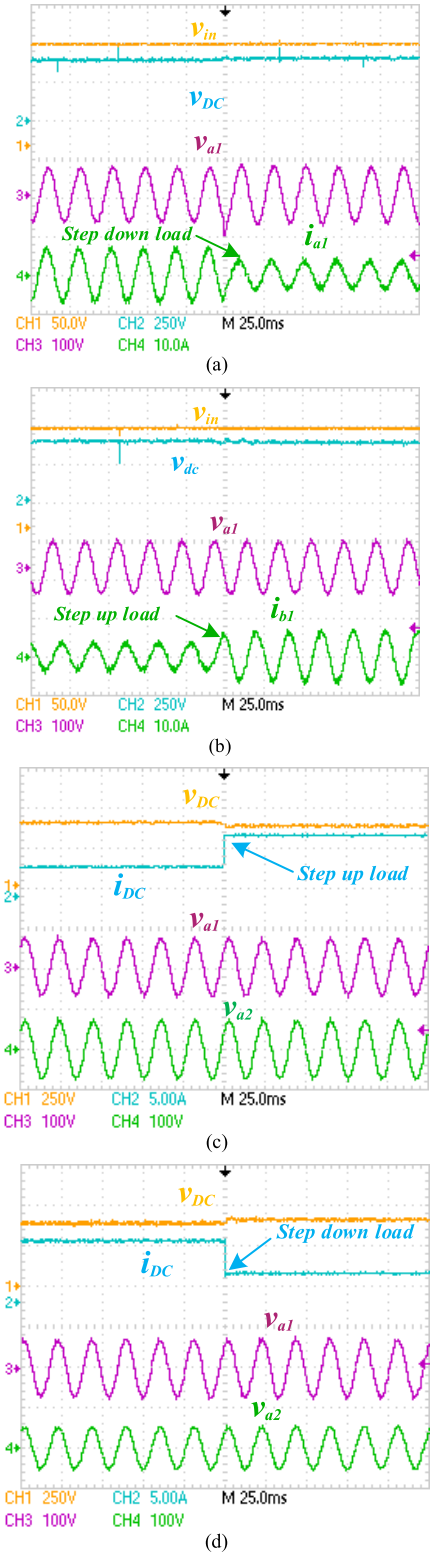

FIGURE 14. Dynamic results of the proposed parallel mode converters (a) Step down dynamics with v_{DC}. (b) Step up dynamics with v_{DC}. (c) Step up dynamics with phase voltages with equal v_{ref} for both units. (d) Step down dynamics with phase voltages with different v_{ref} for both units.

Fig. 11(f) shows the output DC voltage v_{DC} at 380 V, the output DC current i_{DC} at 3.8 A, along with the input voltage v_{in} and the switch node voltage v_{pn}. These values are presented considering a DC load resistance of 100 Ω.

Figs. 12(a) and (b) display the three-phase voltages of converter units 1 and 2, respectively, along with the input voltage $v_{\mathrm{in}} = 130$ V, which has a peak-peak magnitude of 140 V, while AC reference voltage v_{ref} is 70 V. It can be observed that all three-phases have the same magnitude of 140 V peak-peak and a phase difference of 120^0, indicating system stability and balance.

In Fig. 12(c), the phase a voltage (140 V peak-peak) of converter units 1 and 2 is shown, along with the input voltage v_{in} and the DC output voltage v_{DC}. Both units have a reference voltage (v_{ref}) of 70 V. Furthermore, Fig. 12(d) presents the DC output voltage v_{DC} at 380 V, the phase b voltage (140 V and 120 V peak-peak) for unit 1 and 2 at $v_{\mathrm{ref}} = 70$ V and 60 V, respectively, along with the input voltage v_{in}. The DC output voltage of 380 V is utilized in DC power distribution. Due to its relatively high magnitude, the use of efficient grounding and protection techniques is necessary to ensure proper safety and operation [29]. These figures demonstrate voltage characteristics and relationships in the converter system, revealing stability, balance, and output voltage levels. They highlight the importance of grounding and protection in high-voltage DC applications. These figures collectively provide a detailed and visual representation of the steady-state response of the parallel SLCHMOCs, depicting various voltage waveforms and their relationships under different operating conditions.

In Figs. 13(a) and (b), the hybrid PWM signals for the upper and lower side switching signals with s_4 and s_5 are depicted for converter unit 1. Additionally, Figs. 13(c) and (d) display the PWM signals for the upper and lower sides with switching signals s_{42} and s_{52} for converter unit 2 during parallel operation of the proposed converters.

2) DYNAMIC RESULTS

The dynamic response of the proposed converters for DC and AC load transients is presented in Fig. 14. In Figs. 14(a) and (b), the AC load changes (step-down and step-up) are demonstrated for converter unit 1. In the step-down scenario (Fig. 14(a)), where the load current decreases from 14 A (peak-peak) to 7 A, the voltage of phase a (v_{a1}) shows a slight increase and quickly returns to its original position within one cycle. The DC output voltage (v_{DC}) remains unaffected by this load change. Similarly, in the step-up case (Fig. 14(b)), where the load current increases from 7 A to 14 A, the corresponding voltage of phase a (v_{a1}) slightly decreases and quickly restores to its original position within one cycle, while the DC output voltage (v_{DC}) remains stable. These observations indicate the stability and excellent dynamic response of the system with the proposed converter. Fig. 14(c) illustrates a step-up load change in the DC network, where the phase a voltage (140 V peak-peak) of converter units 1 and 2 is depicted, with v_{ref} set at 70 V and v_{dcref} at 380 V. As the DC load current is varied from 3.8 A to 7.6 A, there is a slight decrease in v_{DC}, which then quickly returns to its original position within one cycle. In Fig. 14(d),

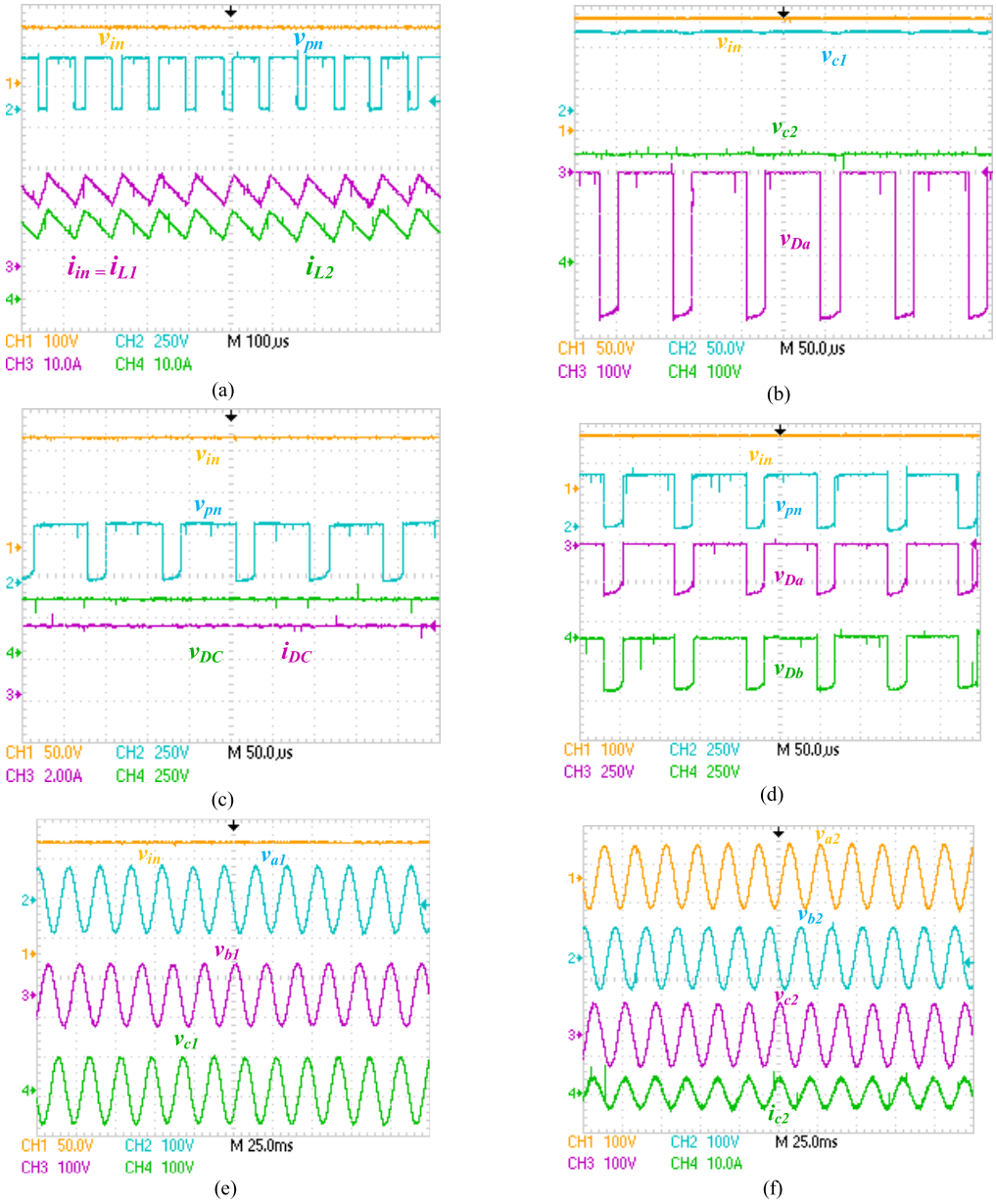

FIGURE 15. Presents the steady-state performance of the proposed series SLCHMOC$_S$. It includes various subplots: (a) shows the inductor currents with input voltages v_{in} and v_{pn}, (b) displays the capacitor voltages with v_{in} and v_{Da}, (c) illustrates the DC voltage (v_{DC}) and current (i_{DC}) with v_{pn} and v_{in}, (d) presents the diode voltages with v_{pn}. and v_{in}, (e) exhibits the three-phase voltages of unit 1 with v_{in}, and (f) three-phase voltages with phase c current (i_{c2}) of unit 2.

a step-down load change in the DC network is shown when both units have different reference voltages: $v_{\text{ref}} = 70$ V for unit 1 and $v_{\text{ref}} = 50$ V for unit 2. Despite the DC load current decreasing from 7.6 A to 3.8 A, the phase *a* voltage (v_{a1}, v_{a2}) and the DC output voltage (v_{DC}) remain constant at 140 V, 100 V (peak-peak), and 380 V, respectively. This behaviour confirms the stability and favourable dynamic response of the proposed converter. In summary, the proposed converter system demonstrates stable and excellent dynamic response characteristics, as depicted in Fig. 14.

B. VALIDATION OF THE PROPOSED SERIES SLCHMOC$_S$

The suggested series SLCHMOCs have been tested and confirmed to handle a power of 2.02 kW when supplied with an input voltage (v_{in}) of 130 V. The DC power output (P_{DC}) is measured at 1057 W, while the corresponding AC power output (P_{AC}) is recorded as 960 W.

1) STEADY-STATE RESULT

Fig. 15. presents the steady-state outcomes of the proposed series SLCHMOCs. Both converter units operate with a

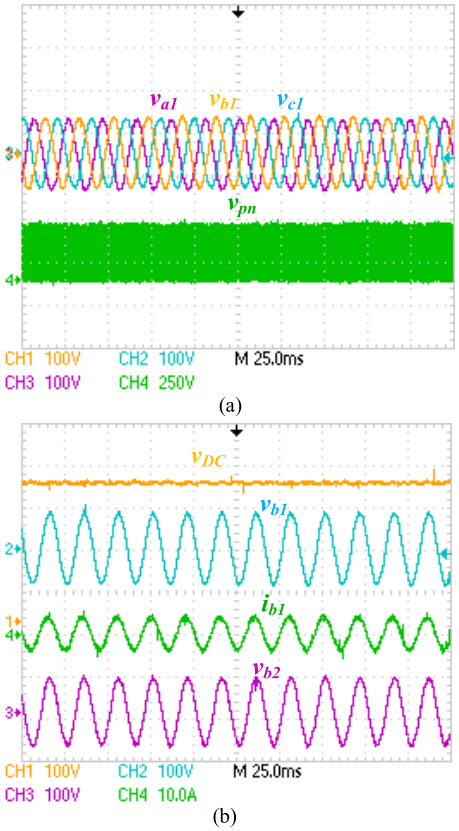

FIGURE 16. Shows (a) three-phase voltages of converter unit 1 with v_{pn}. (b) Phase b voltages and current of converter units 1 and 2 with V_{DC}.

reference voltage of 80 V. In Fig. 15(a), the input voltage (v_{in}) is 130 V, the switch node voltage ($v_{\rm pn}$) is 325 V, and the inductor currents (i_{L1} and i_{L2}) are measured at 17.3 A, which is also the input current ($i_{\rm in}$). The charging and discharging of the inductor currents are equal since $i_{L1} = i_{L2}$.

Fig. 15(b) displays $v_{\rm in} = 130$ V, capacitor voltages ($v_{\rm C1}$ and $v_{\rm C2}$) at 97 V and 227 V, and the diode voltage ($v_{\rm Da}$) at 325 V. During the ST (switched on) state, the diode is reverse biased, while it is forward biased during the NST (switched off) state. In Fig. 15(c), the input voltage ($v_{\rm in}$), switch node voltage ($v_{\rm pn}$) at 325 V, DC output voltage ($v_{\rm DC}$) at 325 V, and current ($i_{\rm DC}$) at 3.25 A are depicted. This particular DC voltage level is selected as it is considered optimal for a DC microgrid. As the DC network and $v_{\rm pn}$ are in parallel, $v_{\rm DC} = v_{\rm pn} = 325$ V. Fig. 15(d) shows the diode voltages ($v_{\rm Da}$ and $v_{\rm Db} = 325$ V) and switch node voltage ($v_{\rm pn} = 325$ V), along with the input voltage ($v_{\rm in}$) at 130 V. During the ST state, $v_{\rm pn} = 0$ V, and the diodes $D_{\rm a}$ and $D_{\rm b}$ are reverse biased, resulting in negative voltage across them ($v_{\rm Da}$ and $v_{\rm Db} = -325$ V). Conversely, during the NST state, the diodes are forward-biased, causing the voltage across them to be zero ($v_{\rm Da}$ and $v_{\rm Db} = 0$ V), while $v_{\rm pn} = 325$ V. Fig. 15(e) illustrates the input voltage ($v_{\rm in}$) at 130 V and the three-phase voltages of unit 1. It can be observed that the three-phase voltages of converter units 1 and 2 measure 160 V (peak-to-peak), with a reference voltage of 80 V. All three-phase voltages are 120^0 apart from each other and remain balanced. Fig. 15(f) demonstrates the three-phase voltages of unit 2 alongside the phase c current ($i_{\rm c2}$). In a resistive load scenario, it is noticeable that $v_{\rm c2}$ and $i_{\rm c2}$ are in the same phase. The phase voltages $v_{\rm a2}$ and $v_{\rm b2}$ have a voltage magnitude of 160 V (peak-to-peak) and a current magnitude of 8 A (peak-to-peak), considering an AC load resistance ($R_{\rm AC}$) of 20 Ω and a reference voltage ($v_{\rm ref}$) of 80V.

In Fig. 16(a), the three-phase voltages of converter unit 1 are depicted, accompanied by the switch node voltage ($v_{\rm pn}$) at 325 V. Fig. 16(b) illustrates $v_{\rm DC}$ at 325 V, along with the phase b voltage ($v_{\rm b1}$ and $v_{\rm b2}$) and current ($i_{\rm b1}$) for converter units 1 and 2. The voltage and current magnitudes are measured at 160 V and 8 A peak-to-peak, respectively, considering a reference voltage ($v_{\rm ref}$) of 80 V. As the load is resistive, phase voltages $v_{\rm b1}$, $v_{\rm b2}$, and current $i_{\rm b1}$ exhibit a 0-degree phase displacement with each other.

C. VERIFICATION OF THE INDEPENDENT OPERATION OF THE PROPOSED SLCHMOC$_{\rm S}$ UNITS FOR DIFFERENT VOLTAGES AND FREQUENCIES

This subsection demonstrates the independent operation of multiple converter units in the proposed parallel SLCHMOCs, catering to different voltage and frequency requirements. The steady-state simulation results for one sample case of the parallel SLCHMOCs are presented in Fig. 17, with unit 1 configured for a voltage requirement of 70 V at 50 Hz, and unit 2 operating at 60 V and 60 Hz. Fig. 17(a) shows the input DC voltage ($v_{\rm in} = 130$ V), capacitor voltages ($v_{\rm c1}$ and $v_{\rm c2}$), and the input DC current (equivalent to the current in inductor L_1, $i_{\rm L1}$). Fig. 17(b) displays the current in inductor L_2, the switch node voltage ($v_{\rm pn}$), and the voltages across diodes D_a ($v_{\rm Da}$) and D_b ($v_{\rm Db}$). In Fig. 17(c), the output DC voltage ($v_{\rm DC} = 380$ V), output DC current ($i_{\rm DC} = 3.8$ A for a DC load resistance of 100 Ω), and the three-phase output voltages of unit 1 (peaking at 70 V, 50 Hz) are illustrated. Fig. 17(d) shows the three-phase output currents of unit 1 (peaking at 3.5 A with 20 Ω/phase 3.0 A with 20 Ω/phase loads). From the results presented in Figs. 17(c) and (d), it is evident that the period of the AC output voltage and current waveform for unit 1 is 0.02 s (corresponding to a frequency of 50 Hz), while for unit 2, it is 0.0167 s (corresponding to a frequency of 60 Hz). The results demonstrate that the converter units operate independently, catering to different voltage and frequency requirements.

D. EFFICIENCY AND POWER LOSS ANALYSIS OF THE PROPOSED SLCHMOCS

Efficiency analysis has been conducted for both the proposed parallel and series SLCHMOCs. The analysis details are provided below.

1) PROPOSED PARALLEL SLCHMOCS

Fig. 18(a) illustrates the efficiency versus total load power curve of the parallel SLCHMOCs, where the DC load power is variable while the AC load power remains constant. Fig. 18(b) presents the efficiency curve when the AC load

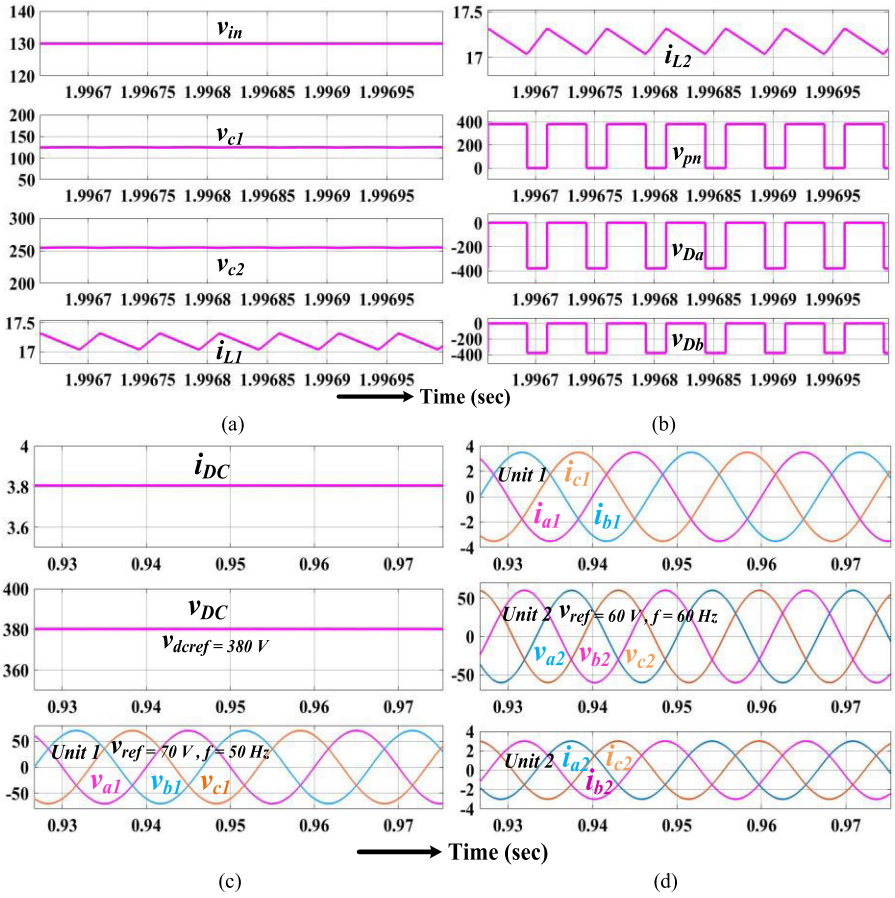

FIGURE 17. Depicts the steady-state simulation results of the proposed parallel SLCHMOC$_S$. (a) shows the input voltage (v_{in}), capacitor voltages (v_{C1} and v_{C2}), and inductor current (i_{L1}). (b) displays the inductor current (i_{L2}), switch node voltage (v_{pn}), and diode voltages (v_{Da} and v_{Db}), (c) presents the output DC current and voltage (v_{DC} and i_{DC}) alongside the three-phase voltages of unit 1. (d) illustrates the three-phase load currents of unit 1, as well as the three-phase voltages and load currents of unit 2, with $v_{dcref} = 380$ V, $v_{acref} = 70$ V, 50 Hz (unit 1), and 60 V, 60 Hz (unit 2).

power is variable while the DC load power is kept constant. As depicted in Figs. 18(a) and (b), the implemented prototype achieves an efficiency of 90.01% at a power level of 2.18 kW.

2) PROPOSED SERIES SLCHMOCS

Likewise, it can be observed from Fig. 19(a) and (b) that the developed prototype of the proposed series SLCHMOCs achieves an efficiency of 89.95% at a power level of 2.02 kW.

3) EFFICIENCY ANALYSIS FOR INCREASING NUMBER OF CONVERTER UNITS

The efficiency versus load curve for different numbers of converter units ($n = 2$, 3, and 4) was obtained through simulations and is presented in Fig. 20. It can be observed from Fig. 20 that the efficiency of the proposed converters slightly decreases with an increase in the number of units. Here are some important points regarding the efficiency analysis for a greater number of units in the proposed converters:

1. Increasing the number of units leads to higher current/voltage stresses at the front-end inductors and capacitors. However, since the DC resistance (DCR) of the inductors (5 mH) and the equivalent series resistance (ESR) of the capacitors (470 μF) are typically very small (in the milliohm range), the increase in current at the front-end components does not contribute significantly to losses.
2. Additionally, as the number of switches increases with more converter units, there will be higher switching losses, resulting in a reduction in efficiency. However, if separate independent converters are connected in series/parallel to achieve the same number of outputs obtained from the proposed converters, the number of switches remains the same in both cases. Therefore, the switching losses between both schemes will be comparable.

Considering the above points, it is evident that the efficiency is not significantly compromised with an increase in the number of units in the proposed SLCHMOCs.

4) EFFICIENCY COMPARATIVE ANALYSIS

To assess the effectiveness of the suggested SLCHMOCs in comparison to other counterparts, a comprehensive

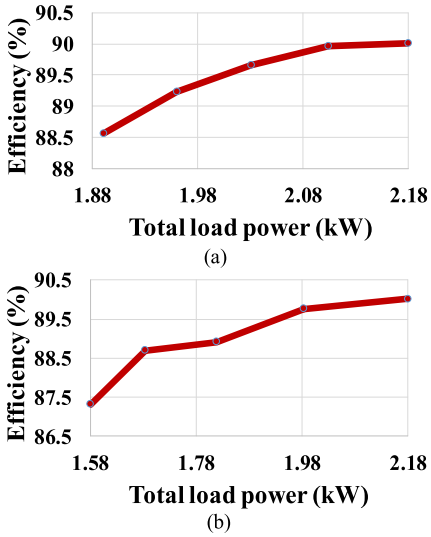

FIGURE 18. Illustrates the efficiency versus the total load power curve for parallel SLCHMOCs. The graph is divided into two parts: (a) representing variable DC and constant AC power and (b) representing variable AC and constant DC power.

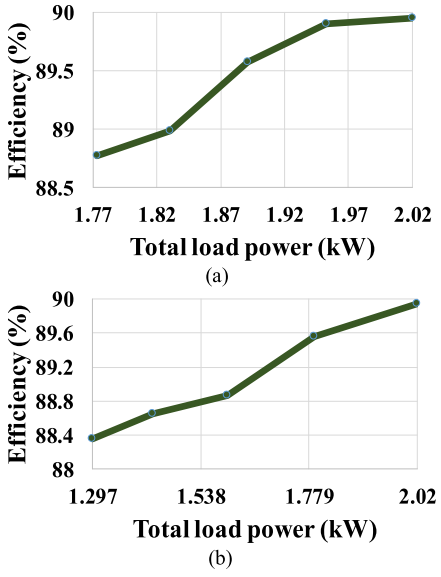

FIGURE 19. Displays the efficiency plotted against the total load power curve for series SLCHMOCs. It includes two sections: (a) variable DC and constant AC power, and (b) variable AC and constant DC power.

comparison table (Table 6) has been compiled, juxtaposing the proposed configurations with closely related hybrid converter topologies. Notably, the efficiency analysis reveals that the suggested SLCHMOCs exhibit a competitive efficiency when compared to their counterparts.

The examination of Table 6 underscores that the efficiencies of CFSI [16], QSBI$_s$ [17], single-phase SSI [19], and BDHC [22] are inferior to those of the proposed topologies. Meanwhile, one converter, IHC [18] demonstrate higher efficiency than the proposed SLCHMOCs. It is essential to note, however, that the proposed SLCHMOCs possess distinct advantages over these converters.

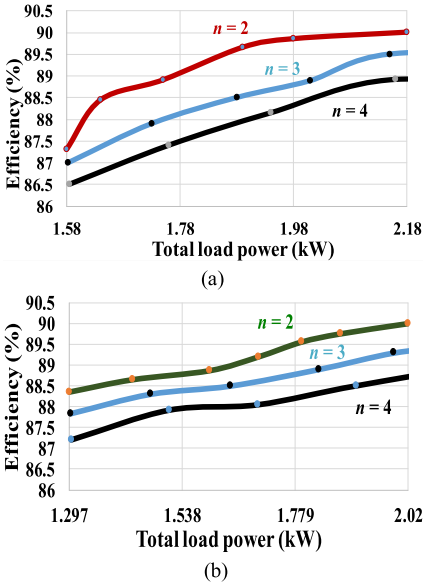

FIGURE 20. Depicts the efficiency versus total load power curve for parallel SLCHMOCs. In (a), the curve represents the efficiency under conditions of variable DC and constant AC power, while in (b), it shows the efficiency with variable AC and constant DC power.

In particular, the converters [18] is characterized by having a sole DC and a single-phase AC output, whereas the proposed SLCHMOCs excel by offering concurrent multiple series or parallel three-phase AC outputs alongside a DC output. This versatility in output configurations enhances the applicability and functionality of the proposed SLCHMOCs, showcasing their potential advantages in diverse applications.

5) POWER LOSS ANALYSIS OF THE PROPOSED SLCHMOCS

Figs. 21(a) and (b) present the power loss distribution among the components used in the parallel and series SLCHMOCs of the proposed converters. The distribution of power loss among the components is determined based on the methodology described in the reference [30].

The overall loss in the system comprises losses associated with switches and passive components such as inductors, capacitors, and diodes. These losses are evaluated by considering the non-idealities and standard parameters of the components obtained from datasheets, along with measurements of voltages and currents. Formulas and calculations described in reference [30] are employed to quantify the losses accurately.

As per Table 5, 1 GBT IGW25N120H3FKSA1 is used for developing the prototype. The electrical parameters of the IGW25N120H3FKSA1 are E_{on} = 2.6mJ, E_{off} = 1.7mJ and forward voltage drop v_{FD} =1.5 V (max). The diode IDWD10G120C5XKSA1 has a forward voltage drop of 1.45 V (max) when the current flowing is 18.6 A. To calculate the power loss, the following parasitic values are employed: $r_L = 0.105\ \Omega$, $r_{C1} = r_{C2} = r_{CDC} = 0.103\ \Omega$. Additionally, IGBT on-resistance r_{on} is set at 16 mΩ, diode forward series resistance $r_D = 13\ \text{m}\Omega$, a forward voltage drop $v_{FD} = 1.45$ V.

TABLE 6. Comparative analysis of efficiency of previously reported and proposed converters.

Hybrid Converter	Maximum efficiency (%)
CFSI [16]	82.6
qSBI$_s$ [17]	83.67
IHC [18]	91.32
single phase SSI [19]	83
BDHC [22]	88.1
Proposed SLCHMOCs	90.01

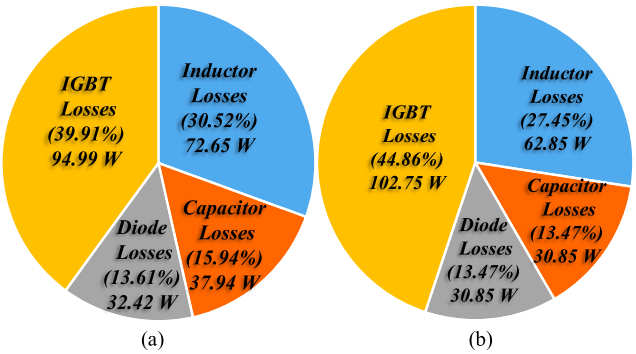

FIGURE 21. Illustrates the distribution of power losses for both parallel and series SLCHMOCs. In (a), the power loss distribution for parallel SLCHMOCs is shown, while in (b), the power loss distribution for series SLCHMOCs is presented.

From the steady state performance results, the output power in parallel SLCHMOCs ($P_T = P_{DC} + P_{AC}$) can be calculated as 380*3.8+3*2*49.5*2.48 = 2180 W. The input power to the converter is 130*I_L = 130*18.6 = 2418 W. The inductor ESR losses were found to be 72.65 W, capacitor ESR losses 37.94 W, diode losses 32.42 W and IGBT losses 94.99 W. Similarly, for series SLCHMOCs, the total output power = 2020 W and input power to the converter = 2249 W. the inductor ESR losses were found to be 62.85 W, capacitor ESR losses 32.55 W, diode losses 30.85 W and IGBT losses 102.75 W, shown in Figs. 21(a) and (b).

The total losses calculated using the basic method, which involves computing the difference between input power and output power from experimental results, are compared and found to be in good agreement with the losses calculated using the methodology outlined in reference [30].

This verification ensures the reliability and consistency of the power loss calculations in both the basic method and the method described in the reference [30].

The power loss calculations are based on the following assumptions:

1) The switches are represented using an ideal model, which includes a forward resistance (r_S) and a collector-to-emitter saturation voltage ($v_{CE(on)}$).
2) Diodes are represented using an ideal switch model, which includes a forward series resistance (r_D) and a forward voltage drop (v_{FD}).
3) The system accounts for the winding DC resistance (DCR) of inductors (r_L) and the equivalent series resistance (ESR) of capacitors (r_C).
4) The analysis includes the collector-to-emitter current of switches (i_{CE}), the anode-to-cathode current of diodes (i_D), the current through inductors (i_L) and the current through capacitors (i_C).
5) Inductor current ripples are neglected in the calculations.

Losses in switches (IGBTs):

The calculation of conduction losses in the inverter bridge switches is performed as follows:

$$P_{Cond\_S} = \frac{1}{T_s}\int_0^{T_s}\left(v_{CE(on)}i_{C(avg)} + r_S i^2_{C(rms)}\right)dt$$

The switching loss is calculated as

$$P^{on,off}_{Switch\_S} = \frac{1}{T_s}\int_0^{t_{on}+t_{off}} (v_{CE}\,(t)\,i_C(t))\,dt$$

Total power losses of the inverter switches are calculated as

$$P_{Total\_S} = 12\left(P_{Cond\_S} + P^{on,off}_{Switch\_S}\right)$$

Losses in Diodes:

The conduction losses of diodes are calculated as

$$P_{Cond\_D} = \frac{1}{T_s}\int_0^{T_s}\left(v_{FD}i_{D(avg)} + r_D i^2_{D(rms)}\right)dt$$

Generally, turn-on switching losses of diodes are negligible. The turn-off switching losses of diodes are calculated as

$$P^{off}_{Swicth\_D} = \frac{2}{T_s}\int_0^{t_{off}} v_D\,(t) i_D\,(t)\,dt$$

Losses in inductors:

Core and winding losses are part of the power losses of inductors. For pulse width modulated converters, the core losses are often insignificant. Inductors' winding resistances (r_L) determine the winding losses, which are calculated as

$$P_{wind\_L} = r_L i^2_{L(rms)}$$

Losses in capacitors:

The power losses of the capacitors depend on the equivalent series resistances (r_C) and are calculated as

$$P_{rC} = \frac{1}{T_s}\int_0^{T_s} r_C i^2_C dt$$

The overall loss is theoretically calculated by the addition of the above break-up of losses.

The experimental efficiencies depicted in Figs. 18 and 19 indicate a relatively moderate level, approximately 90.01% and 89.95% respectively. These results can be attributed to the presence of the ST (shoot-through) state in the proposed

converters, as well as suboptimal choices of passive and active components in the experimental setup. When the ST duty cycle is long to achieve high voltage gain, power losses in passive components, active elements, and semiconductor devices tend to increase significantly. To enhance efficiency, it is imperative to carefully select semiconductor devices, passive components, and appropriately design printed circuit boards, thereby mitigating these losses and further improving overall efficiency.

E. APPLICATIONS OF THE PROPOSED CONVERTERS

1. As the proposed converters are capable of supplying regulated multiple three-phase AC and single DC outputs simultaneously in a single stage. Its outputs can be used in the hybrid microgrid, renewables, uninterrupted power supplies, and industrial AC/DC loads.
2. The outputs of the proposed converters can be used in variable voltage/current and constant voltage/current applications with different frequencies of 50 and 60 Hz.
3. The three-phase AC outputs can be used in the electric arc furnace used in steelmaking and refining of ores.
4. The DC output voltage $v_{DC} = 380$ V has been used in DC power distribution. Since the voltage is relatively large, it necessitates the use of highly efficient grounding and protection techniques [29].
5. In the series SLCHMOCs, the DC output voltage of 325 V is equal to the peak of the AC phase voltage. The dc-link voltage of a standard single-phase power supply with diode bridge input stages is 325 V. As a result, existing supplies will work with this DC voltage level [29].
6. As all the outputs of the proposed converters can be independently regulated, therefore, the DC output voltage 380 V and 325 V can be step-down to 230 V. The existing AC system's root mean square value is the same as 230 V. As a result, if this voltage level is employed, the resistive loads (mainly heating) rated to run on the present AC system do not need to be changed.

V. CONCLUSION

This paper introduces a parallel-series SLCHMOC$_S$ utilizing switched impedance that offers multiple simultaneous AC outputs along with a boost DC output. The parallel SLCHMOCs generate n number of regulated AC voltage outputs with the same voltage but different load currents, along with one boost DC output. Similarly, the series SLCHMOCs produce n number of AC outputs with the same load current but different voltages, including one boost DC output, all within a single stage. To operate the proposed SLCHMOCs, a hybrid PWM technique is employed, which ensures simple implementation, rapid dynamic response, and high robustness. The proposed SLCHMOCs feature higher power density, lower weight, volume, and cost compared to multi-stage architectures. Additionally, they eliminate the need for extra regulators or adapters, allowing the outputs to meet multiple loads demand simultaneously. These outputs are suitable for three-phase industrial loads, renewable energy systems, uninterrupted power supplies, and can be integrated into hybrid microgrids. The paper includes detailed mathematical modeling, steady-state and dynamic analysis to investigate the characteristics of the proposed SLCHMOCs. Furthermore, prototypes with power ratings of 2.18 kW and 2.02 kW are developed to validate their performance. The measured efficiencies of the proposed parallel and series SLCHMOCs are 90.01% and 89.95% respectively.

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