RESEARCH ARTICLE

A Novel Structure Between WL Spaces to Improve the Retention Characteristics in 3D NAND Flash

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ABSTRACT As NAND flash evolved from two-dimensional (2D) to three-dimensional (3D), all cells have been changed to share a charge trap layer (CTL). This change has a lateral charge spreading effect, which is the trapped charge spreading laterally. This lateral charge spreading effect causes a major problem in NAND flash reliability. In this study, we introduce a new structure that can improve lateral charge spreading by defining a new parameter called 'intercell CTL thickness' and modifying the CTL structure in the WL spaces. When the intercell CTL thickness decreases, the ISPP slope remains relatively constant up to a certain thickness, indicating that program efficiency does not decrease until that critical point. However, as the intercell CTL thickness decreases, the current also decreases, which can be explained by the screen effect and dielectric constant reduction. As for the thickness of the CTL, which is the trap nitride thickness, it decreases while the oxide thickness increases. As a result, it causes a decrease in the total dielectric constant, resulting a decrease in cell current. In addition, as the physical CTL thickness decreases, more charges will be trapped in the same V_{TH} condition. More charges strengthen the screen effect on the electric field, causing a decrease in cell current. In this study, we will discuss the retention characteristics of this novel structure, investigate the window characteristics between lateral charge spreading with cell current, and propose the optimal point.

INDEX TERMS 3D NAND, lateral charge spreading, charge trap layer, intercell CTL thickness, ISPP slope, cell current, dielectric constant, screen effect.

I. INTRODUCTION

NAND flash memory has evolved from 2D NAND flash to 3D NAND flash, with higher capacity [1], [2], [3]. In addition to high capacity, 3D NAND flash has more advantages such as improved program efficiency and reduced interference [4], [5], [6]. However, unlike 2D NAND, 3D NAND has a structure in which the CTL is shared between all cells [7], [8]. This shared CTL structure causes several problems because the neighboring cells are connected. First, charges are trapped in the word line (WL) space region [9], [10]. This causes a screen effect that shields the electric field, which decreases cell current [10]. Furthermore, more than 200 layers of stacked cells in 3D NAND flash, the reduction in cell current becomes a significant issue [11], [12]. In addition, this

structure has an issue where trapped charges spread over time [13], [14], [15], [16]. These problems caused by the transition to 3D NAND raise issues with reliability, which leads to an important challenge [3], [17], [18]. In this study, we introduce a modified 3D NAND device structure by changing the shape of the CTL between WL spaces with reduced CTL thickness. This advanced novel structure is expected to decrease lateral charge spreading. In addition, to find the optimization point for this modified CTL thickness, we introduce a parameter called 'intercell CTL thickness'. By observing the ISPP slope and cell current with intercell CTL thickness variation, we identified the optimization thickness point for retention characteristics.

II. DEVICE STRUCTURE

Figure 1(a) shows a simulated structure of conventional 3D NAND flash. The simulated device has a three-dimensional

The associate editor coordinating the review of this manuscript and approving it for publication was Giambattista Gruosso.

TABLE 1. Conditions for device simulation.

	Erase	Program	Retention	Read
Selected cell	-18 V	18 V	0 V	-5 ∼ 12 V
Unselected cell	0 V	6 V	0 V	6 V
B/L	0 V	0 V	0 V	0 ∼ 1 V
Time	5×10^{-2} s	3×10^{-3} s	1×10^{3} s	-
Temperature	-	-	300 K	-

structure, and the figure shows a cross-sectional view of the 3D structure cut vertically. Tungsten was used for the gate. The gate length and WL space length are 25 nm and 25 nm, respectively. The thicknesses of the tunneling oxide, charge trap nitride, and blocking oxide (ONO) are 5 nm, 7 nm, and 7 nm, respectively. The thickness of the polysilicon channel is 10 nm. The mesh consists of 2 nm hexahedral structure for the smallest area. Figure 1(c) shows the novel structure of this 3D NAND flash and defines the intercell CTL thickness. This parameter represents the thickness of the charge trap layer in the WL space, which is the inter-cell region, and it is reduced from 7 nm to 1 nm. In other words, when the intercell CTL thickness is 7 nm, the device retains the structure of conventional 3D NAND flash as shown in Figure 1(b). While in the case of a 1 nm intercell CTL, the thickness is shown in Figure 1(c). The device consists of three cells. The source and drain doping concentration are n-type 2×10^{18} cm^{-3}, and the polysilicon channel doping concentration is p-type 5×10^{18} cm^{-3}. The erase, program, retention, and read conditions of the device are described in Table 1. The physical parameters of the materials were referenced from previous studies [19], [20], [21], [22]. In this study, the constant current method was used to extract threshold voltage at $I_D = 1\mu A$ [23]. The simulations were conducted using Synopsys' Sentaurus technology computer-aided design (TCAD). A nonlocal tunneling (NLT) model was applied to the tunneling oxide and polysilicon channel for program/erase operations, and the Shockley Read Hall (SRH) model was applied [24], [25].

III. RESULTS AND DISCUSSION

In this study, the intercell CTL thickness was reduced from 7 nm to 1 nm as shown in Figure 1(b). The primary purpose of this novel structure is to mitigate the lateral charge spreading. The first thing to check is how much lateral spreading has occurred. Figure 2 shows the distribution of trapped electrons in CTL and the retention characteristics after 1000 s at 300 K. In the case of Figure 2(a), the intercell CTL thickness is 7 nm, while in the case of Figure 2(b), the intercell CTL thickness is 1 nm. The same positions in Figure 2(a) and Figure 2(b) are set as point A and point B. It shows that the point A has more charge than point B.

Figure 3 shows the actual number of trapped electrons at points A and B. In the case of point A, it shows a charge of 10^{12} C/cm^3, while point B shows a charge of 10^9 C/cm^3.
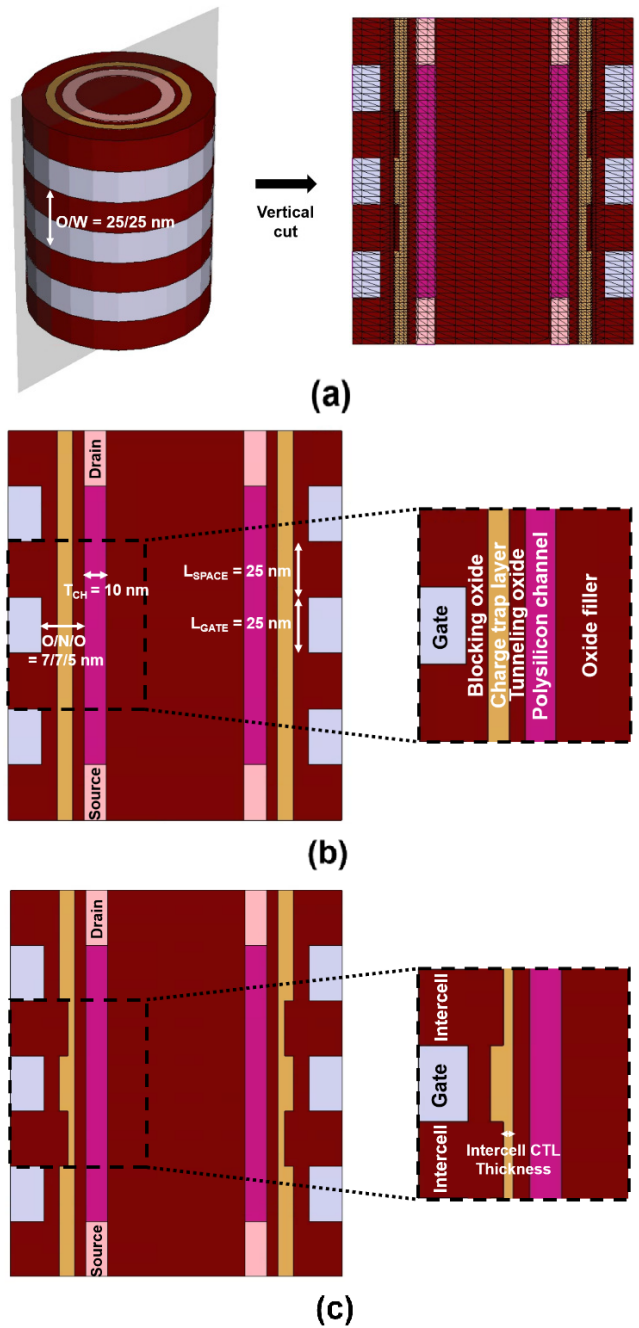

FIGURE 1. Cross-sectional view of the simulated 3D device with (a) hexahedral mesh structure with a minimum size of 2 nm (b) 7 nm intercell CTL thickness, (c) 3 nm intercell CTL thickness.

This means that the electrons spread out more for the intercell CTL thickness of 7 nm than 1 nm. Figure 4 shows the ΔV_{TH} depending on retention from 0 s to 10^3 s at 300 K, and Figure 5 shows V_{TH} difference(= ΔV_{TH}) between at 0 s and 1,000 s [26]. It indicates that ΔV_{TH} decreases as the intercell CTL thickness decreases. In other words, ΔV_{TH} for the thinner intercell CTL thickness decreased with less lateral charge spreading. This can be explained by the diffusion transport model as follows [14], [15], [27] as shown
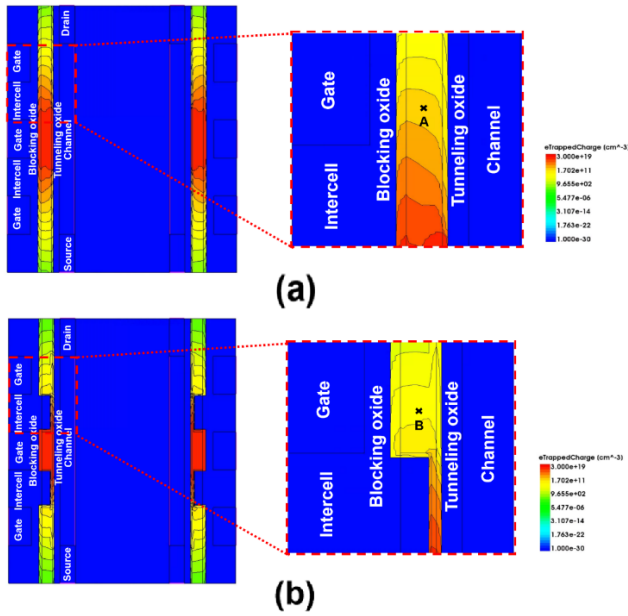
FIGURE 2. Trapped electron distribution in CTL after retention to 1,000 s at 300 K of 3D NAND device structure with (a) 7 nm intercell CTL thickness with point A, (b) 1 nm intercell CTL thickness with point B. Points A and B are discussed in Figure 3.
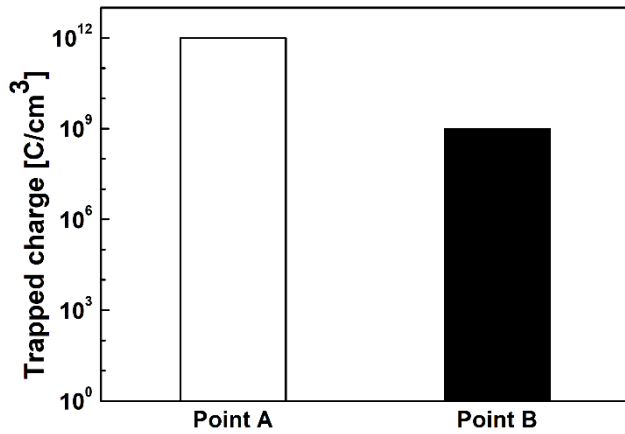

FIGURE 3. Comparison of trapped charge at point A and point B of Figure 2.

FIGURE 4. V_{TH} difference(= ΔV_{TH}) in the variation of retention time from 0 s to 1,000 s at 300 K and intercell CTL thickness from 1 nm to 7 nm respectively. The selected cell was programmed as V_{TH} = 3 V and other cells were programmed as V_{TH} = −1 V in the initial state. When the intercell CTL thickness is thinner, the V_{TH} difference decreases, resulting in the reduction of lateral charge spreading.

FIGURE 5. V_{TH} difference(= ΔV_{TH}) between 1,000 s and 0 s at 300 K. (inset: Transfer curves in the variation of intercell CTL thickness, from 1 nm to 7 nm. V_{TH} was targeted to 3 V at 0 s in all intercell CTL thicknesses).

in Figure 6. The 1 nm intercell CTL in Figure 6(b) shows a more challenging obstacle to the lateral diffusion of the trapped electrons compared to the 7 nm intercell CTL due to the narrow path [28].

Figure 7 shows the incremental step pulse programming (ISPP) slope characteristics. It was confirmed that the slope increased significantly until the CTL thickness reached 2 nm, but saturated starting from 3 nm as shown in Figure 7. This is because decreasing the charge trap layer thickness physically limits the amount for the trapped charge [29], [30]. From this simulation result it was identified that the trap layer thickness is 3 nm for the limit. Therefore, there is no loss in terms of program efficiency up to 3 nm, when the ISPP slope remains relatively constant [31], [32].
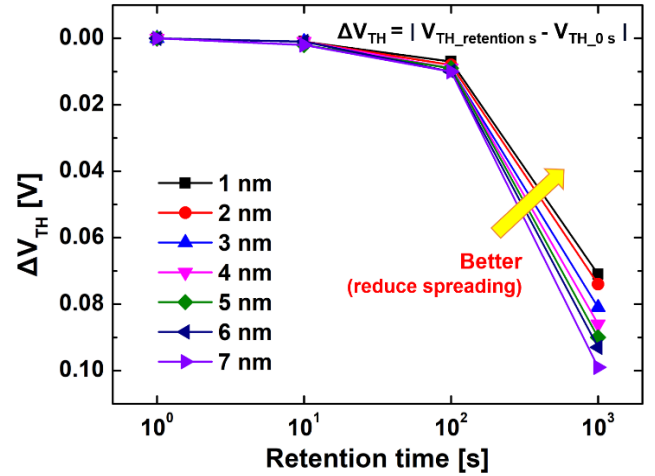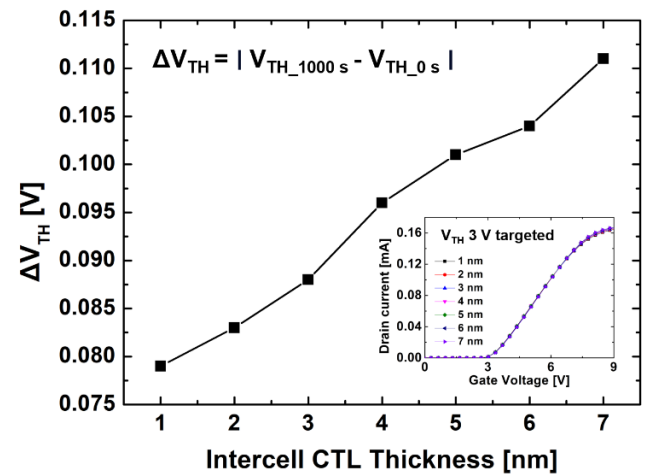
Figure 8 shows the cell current characteristics depending on the intercell CTL thickness before and after retention. It was observed that the current decreases for the thinner intercell CTL in both cases. However, 1,000 s retention characteristics show that the cell current increases, which is due to the decrease in V_{TH} caused by lateral charge spreading [15]. The decrease in current by the reduction in intercell CTL thickness can be explained by two mechanisms as follows.

First, it can be explained by the screen effect [10], [33]. Figure 9 compares the amount of trapped charge for a programmed cell (V_{TH} = 3 V) at 1 nm and 7 nm intercell CTL thickness, which shows more electrons are trapped with a thinner CTL thickness at the same V_{TH} target. It means that the screen effect increases due to stronger shielding electric
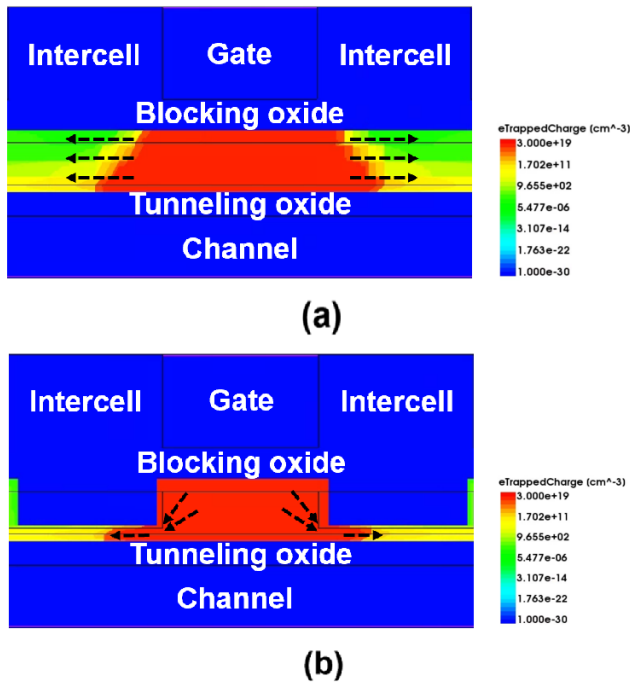
FIGURE 6. Diffusion transport mechanism of trapped electrons in 3D NAND devices with (a) 7 nm intercell CTL thickness, (b) 1 nm intercell CTL thickness. The narrow path in CTL reduces charge diffusion.
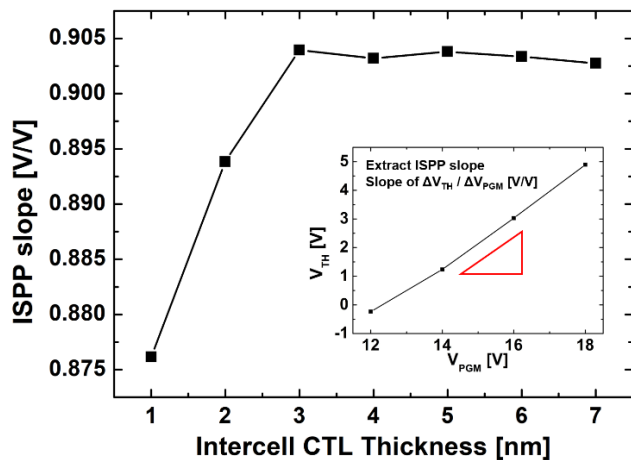

FIGURE 7. ISPP slope in the variation of intercell CTL thickness, from 1 nm to 7 nm (inset: ISPP slope extraction to measure slope of ΔV_{TH} divided by ΔV_{PGM}, when V_{PGM} varied from 12 V to 18 V).

FIGURE 8. Cell current at 0 s Initial state and 1,000 s retention state in the variation of intercell CTL thickness, from 1 nm to 7 nm.

FIGURE 9. Trapped charge in charge trap layer in intercell CTL thickness 1 nm and 7 nm. V_{TH} was the same targeted at 3 V.

field [10]. Therefore, this screen effect results in a decrease in current [10], [33].

Second, the variation of nitride thickness causes current differences. Figure 10 shows intercell CTL thicknesses of 7 nm and 1 nm, respectively. In the case of the 7 nm intercell CTL thickness, there is more nitride with a dielectric constant ($\varepsilon = 7.5$) compared to the oxide with a dielectric constant ($\varepsilon = 3.9$). As a result, thicker nitride makes a higher capacitance value, indicating more cell current [34]. Therefore, the cell current of 7 nm intercell CTL thickness should increase.
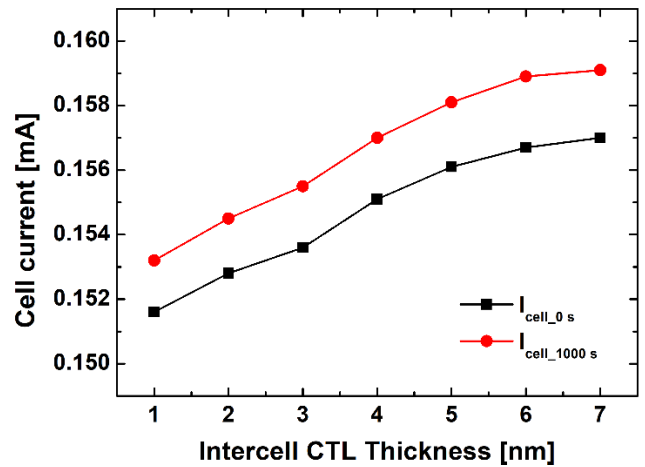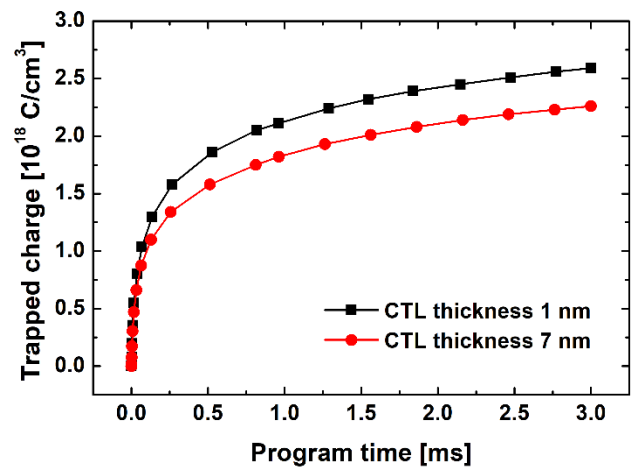
This reduction in cell current in 3D NAND flash with more than 200 layers of stacked cells can makes a significant issue [11], [12]. Therefore, there is a tradeoff relationship between the decreasing of intercell CTL thickness, which can mitigate lateral charge spreading, and the decrease in cell current. Furthermore, including ISPP slope, these several factors show window characteristics indicating the presence of an optimization point.

Figure 11 shows the tradeoff between cell current and the parameter ΔV_{TH}, which is a measure of lateral charge spreading in Figure 5. For the thinner intercell CTL, lateral charge spreading was reduced and the cell current decreased in Figure 5 and Figure 8 respectively. This shows the intercell CTL thickness window characteristics and means that the optimization point exists in this range. A range of 3-4 nm in this specific structure can also be regarded as the optimization point for retention and current since the ISPP slope shows a relatively constant characteristic up to 3 nm, as shown in Figure 7.
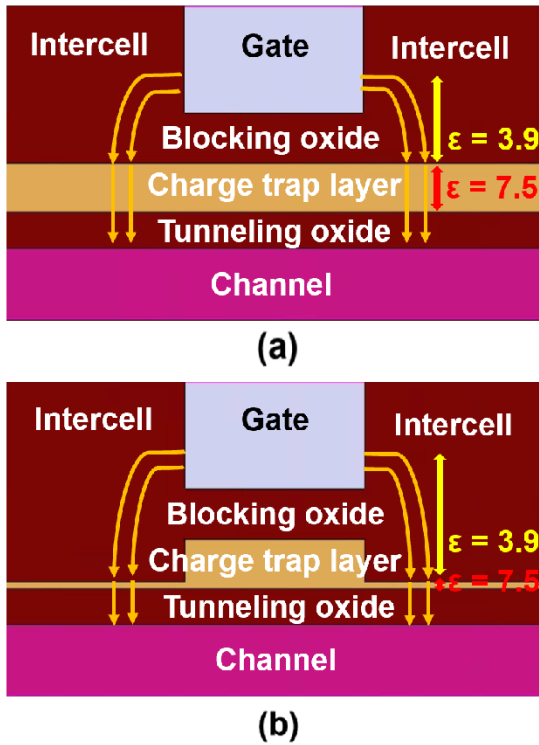
FIGURE 10. Fringing field and difference of dielectric constant at oxide ($\varepsilon = 3.9$) and nitride ($\varepsilon = 7.5$) region in 3D NAND device with (a) 7 nm intercell CTL thickness, (b) 1 nm intercell CTL thickness.
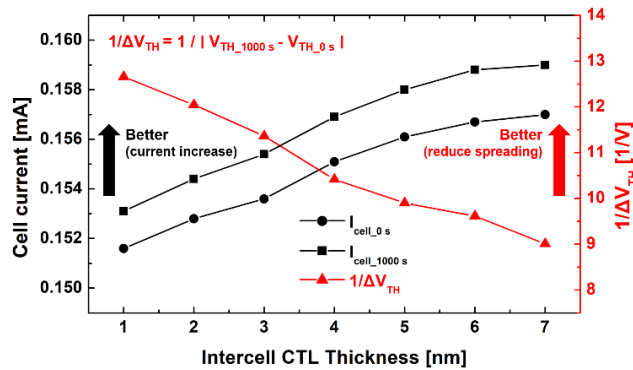

FIGURE 11. Cell current and retention characteristics in the variation of intercell CTL thickness, from 1 nm to 7 nm.

IV. CONCLUSION

In this study, a novel structure was introduced by modifying the intercell CTL thickness to mitigate lateral charge spreading. The retention characteristics, cell current, and ISPP slope were discussed in the variation of intercell CTL thickness. As the intercell CTL thickness decreases, lateral charge spreading caused by the diffusion transport mechanism is reduced. The cell current, however, also decreases with the reduction of intercell CTL thickness by the increase in the screen effect from the increased trapped electrons and the reduction in dielectric constant. The ISPP slope shows a sharp decrease from the critical point due to the physical limitation in the thickness of the CTL. Therefore, program efficiency is not degraded before the intercell CTL thickness reaches the critical value. In conclusion, considering these characteristics, we suggested an optimal point for the intercell CTL thickness, and the novel structure provided higher reliability and reduced lateral charge spreading with less degradation of cell current and higher program efficiency by finding the optimization point.

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