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## RESEARCH ARTICLE

# New Power Interface Based on Multi-Dimensional Golden Section Search Algorithm for Power-Hardware-in-the-Loop Applications

JUAN CONSTANTINE, KUO LUNG LIAN<sup>ID</sup>, (Senior Member, IEEE),  
YOU FANG FAN, (Student Member, IEEE), CHU YING XIAO, AND ZHAO-PENG HE

Department of Electrical Engineering, National Taiwan University of Science and Technology, Taipei 106335, Taiwan

Corresponding author: Kuo Lung Lian (ryanlian@gapps.ntust.edu.tw)

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**ABSTRACT** Power-Hardware-in-the-Loop (PHIL) is a kind of real-time simulation, capable of exchanging not just low-voltage, low current signals, but the power required by the power device under test (PDuT). PHIL requires a PDuT to be connected to a real-time digital power network simulator via a power interface (PI). There have been quite a few PIs proposed in the past. Among them, the ideal transformer model (ITM) is the most commonly used due to its ease of implementation. Other PIs such as partial circuit duplication and damping impedance can be considered as an extended version of the ITM. These PIs need to follow a strict impedance ratio between PDuT and the rest of the system prior to the PHIL implementation, which could be a tedious and difficult task. This paper proposed a new PI for PHIL based on multi-dimensional golden section search algorithm, which can eliminate such a constraint. The proposed method has been shown to have wider stability regions when PDuT is a passive device or active one such as an inverter based resource. Moreover, dynamic responses of the proposed method are similar to those of the ITM under stable conditions. The validity of the proposed method has been justified with offline simulation and experimental PHIL setups.

**INDEX TERMS** Real-time simulation, power hardware-in-the-loop (PHIL), golden section search (GSS), Gauss-Seidel, power amplifier.

## I. INTRODUCTION

Due to the need for clean energy in the world and the commitment to meet net zero emissions, the installation of renewable energy (RE) sources to the grid has greatly increased. Moreover, new devices that facilitates realization of smart grids are also proliferating. Nevertheless, it is economically infeasible and may impose hazards to the system and personnels to test these devices by directly connecting them to a power network. Furthermore, the increasing complexity of these devices requires more comprehensive tests for system

compatibility and reliability. Offline simulation requires detailed model of the equipment, which may not be available or not provided by the manufacturer. Moreover, offline simulation fails to capture some of the actual interaction such as oscillations of controller of the hardware as reported in [1].

Real-time simulation (RTS) allows a real device to interact with a real-time simulator. In general, there are three types of RTS, which are rapid control prototyping (RCP), hardware-in-the-loop (HIL) or controller hardware-in-the-loop (CHIL), and power-hardware-in-the-loop (PHIL) [2]. RCP is used when an emulated controller interacts with a real device (the plant) [3]. HIL simulation, on the other hand, is employed where the controller is a real device and the plant is modelled

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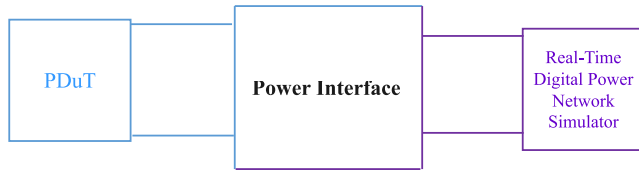


FIGURE 1. Basic PHIL concept.

usually by a digital real-time simulator [4]. Thus, the purpose of HIL simulation usually is to investigate the performance of a controller of an equipment, rather than the entire equipment itself, under various conditions. To simulate how a real power hardware device interact with a power network, PHIL is usually used. PHIL is a natural extension of HIL, in which the real-time simulation environment is capable of exchanging not just low-voltage, low current signals, but the power required by the power device under test (PDuT). PHIL allows power engineers to study how a real PDuT may interact with the power network without connecting to a real power network. Moreover, the detailed model of the PDuT is generally not needed in PHIL since PDuT itself is part of the simulation.

Fig. 1 shows the basic conceptual diagram of PHIL where a power PDuT is connected to a real time digital power network simulator (RTDPNS) via a power interface (PI). The PI is essential for achieving accurate simulation results and achieving stability of PHIL systems. There have been quite a few interfaces proposed in the past. This includes the ideal transformer model (ITM), time-variant first order approximation (TVFOA), transmission line model (TLM), partial circuit duplication (PCD), and damping impedance method (DIM). Among them, the ITM is the most commonly used due to its ease of implementation [5], [6]. The problem of the ITM is that the ratio between the RTDPNS and PDuT impedances needs to be maintained in order to preserve stability. This imposes practical difficulty as one needs to precisely determine, prior to PHIL implementation, the impedance of the PDuT, which could be a tedious and difficult task [7]. The PCD and DIM can be considered as extended models of the ITM. The PCD adds an extra linking impedance in both the RTDPNS and PDuT to increase the region of stability. However, this introduces inaccuracies due to extra power losses. The DIM is a generalization of the ITM and PCD. It has a linking impedance similar to the PCD and includes a damping impedance [8]. The DIM is stable as long as the damping impedance matches the impedance of the PDuT. Similar to the ITM, it is challenging to know the exact PDuT impedance, particularly when the PDuT is a non-linear devices such as inverter-based resources (IBRs). Reference [9] presents the wideband identification method to estimate the impedance of the PDuT. The practical challenge of this approach is to maintain the small-signal condition and at the same time, guarantee a measurable perturbation within the frequency range of interest. Moreover, uncertainty components such as sensors and analogue-to-digital converter (ADC) may affect the result

of impedance identification. TLM has been well-known for the RTS communities. It is commonly used to separate different computations tasks across different domains. For instance, a transmission line model is employed in the RTDS simulator [10] when a power electronic device modeled in the small-time step domain is connected to a power network, modeled in a larger time step (typically  $50 \mu\text{s}$ ). Although the TLM has been proposed to be used in PHIL, it is seldomly used in practical PHIL applications [11] because a real resistor must be added on the PDuT side to represent the line's characteristic impedance, which incurs extra power losses and decreases output voltage range. Tremblay et al. [11] have modified TLM for PHIL applications by adding a high-speed control loop between the sending and receiving ends of the transmission line. Nevertheless, such a new interface leads itself to an ITM form, which again requires a strict impedance ratio between PDuT and rest of the system (ROS) to maintain stability. The TVFOA algorithm is based on the assumption that a PDuT can be modeled as a time-varying first-order linear system (RL or RC circuit) [12]. As reported in [13], TVFOA may show larger error and even instability at high frequency; thus, it is rarely used for PHIL.

This paper proposes a new power interface for PHIL, which can eliminate most of the above mentioned problems. Different from most of the existing power interfaces, which are mainly based on Gauss-Seidel iteration (which will be explained in Section II), the proposed method integrates RTDPNS and PDuT by the proposed multiple-dimensional golden section search (GSS). Thus, the impedance ratio constraint of IMA is not applicable to the proposed method. The contributions of the paper are listed as follows:

- 1) The proposed method, comparable to the ITM, is easy to be implemented and it does not need to add any linking nor damping impedance to improve stability.
- 2) The proposed PI can still maintain stability even if the impedance ratio of the ITM is violated. Thus, the user does not need to know the impedance of the PDuT prior to implementing PHIL.
- 3) The proposed PI has wider stability region, compared to the ITM, allowing it to be used in more PHIL applications.
- 4) The proposed method is inherently stable, and does not lead to unconverged results, endangering system and personnels.

The organization of the rest of the paper is as follows: Section II describes how ITM works and its inherent problems. Section III presents the proposed method and how it is implemented in PHIL applications. Section IV demonstrates the superior performance of the proposed method via simulation and experiments. Finally, a conclusion is given in Section V.

## II. ITM INTERFACE

The PI in Fig. 1 can be implemented as shown in Fig. 2 [14]. The RTDPNS is used to simulate the rest of the system

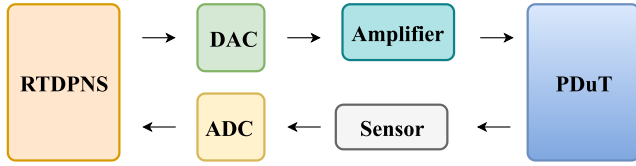


FIGURE 2. The power interface of PHIL.

(ROS) and needs to run in real-time with fixed time-step. As pointed out in [15], there are a few processors that can be used as simulators. These include PC based, FPGA based, supercomputer based and custom processor based simulators. The power amplifiers (PA) can be realized using switched-mode amplifiers, linear amplifiers, and generators. Switched mode amplifiers are commonly used for PHIL applications ranging from small-scale up to mega watts range [1], [16], [17]. Linear amplifiers have higher bandwidths as compared to switched mode PAs. However, linear amplifiers are limited to low power range. The generator-type amplifiers typically uses synchronous generators driven by a dc or ac motors, which are used for low and medium power range. In this paper, we have chosen the switched-mode power amplifier as the PA for the PHIL.

Fig. 3 illustrates one way of how Fig. 2 can be realized for the PHIL setup. Fig. 3 contains the same key components of Fig. 2, including digital-to-analogue converters (DAC), ADC, sensors, PA, PDUt, and RTDPNS. Note that  $Z_{TL}$  represents the impedance of the line that is connected between the PDUt and the PA. This is included for completeness. Nevertheless, the line is usually short and its impedance can be neglected.

Here, we assumed that the PA behaves as a controlled current source (CCS). Similar analysis can be done for a controlled voltage source (CVS). Reference [18] provides a comprehensive analysis.

To have a successful PHIL simulation, the PA needs to behave as the power network to be modeled. To achieve this, the hardware circuit needs to iteratively interact with the software circuits (or virtual circuits) in the RTDPNS. Fig. 3 shows how the hardware circuits interact with the virtual circuits in the RTDPNS for the ITM method.

Since CCS is assumed, the PA is current regulated [19]. As shown in Fig. 3,  $I_{ref}^{(i)}$ , where  $i$  is 0 initially, is set to regulate the current of the hardware circuit ( $I_1$ ) at  $I_{ref}^{(i)}$ . Then, the voltage at the terminal of PDUt ( $V_t^{(i)}$ ) is sensed via a voltage sensor and an ADC and is sent to the virtual circuit. The sensed voltage is set to the equivalent voltage source, representing the PDUt in the virtual circuit. The resulting current flowing through the virtual circuit ( $I_2$ ) will be sensed via a DAC and sent to the current controller of PA to update  $I_{ref}^{(i)}$  and  $i = i + 1$ . The above steps will be repeatedly continuously, and after a few iterations, the terminal voltages and currents of the hardware circuit converge to those of the virtual circuit. This is when the PDUt can be regarded as physically connecting to the RTDPNS. Such an iteration is

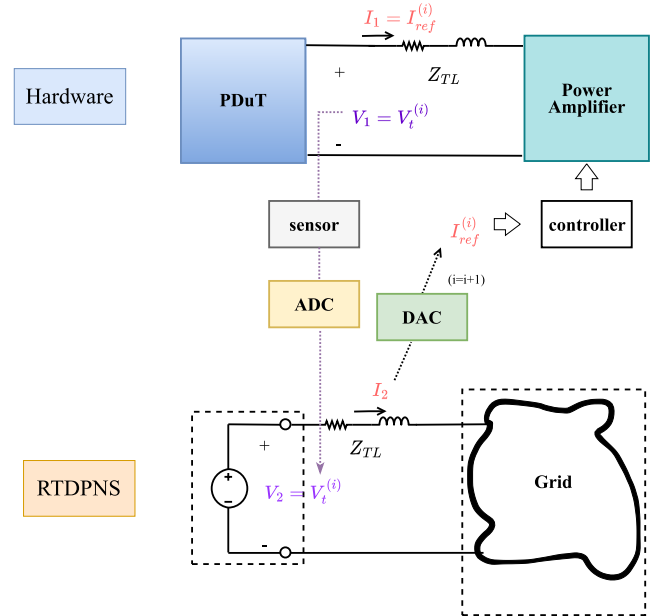


FIGURE 3. System diagram of the ITM method.

in fact a Gauss-Seidel iteration. This is evident if we regard the hardware and virtual circuits to be two different functions. As a new value is obtained from one function (circuit), it is immediately used in the next function (circuit) to determine another value [20], [21].

Fig. 3 can be represented by Fig. 4 whose PI is modeled by an ideal transformer. To simplify the analysis, we assume that the PDUt is represented as an impedance,  $Z_L$ , and  $Z_{TL}$  is negligible. The ROS is represented by its Thevenin equivalent circuit ( $V_g$  and  $Z_s$  in Fig. 4) in the RTDPNS. Fig. 5 shows the equivalent block diagram of Fig. 4 and its open-loop transfer function,  $G_{op}$  is given by:

$$G_{op} = \frac{Z_L}{Z_s} e^{-sT_D} F_{PA}(s) \quad (1)$$

where  $T_D$  is the total delay time of the loop and  $F_{PA}$  is the transfer function of the PA. According to [22],  $T_D$  may include the computation needed for the RTDPNS ( $T_{comp}$ ), the communication time for ADC and DAC ( $T_{comm}$ ), the time delay introduced by the switched-mode PA ( $T_{PA}$ ), and phase shifts due to the feedback filters, which equivalently can be regarded as a time delay (denoted as  $T_{filt}$ ) [22]. The transfer function of the filter is denoted as  $F_{filt}(s)$ . Note that  $T_{PA}$  is constituted by one sample period due to the discrete behaviour and half-time step due to the pulse-width modulator. Thus,  $T_{PA}$  is equal to  $1.5T_{samp}$  [22], where  $T_{samp}$  is the sample period of the digital controller of the PA.

From (1), it can be seen that under ideal condition where delays are neglected and the transfer function of PA is 1, (2) needs to be satisfied. Violation of such a constraint leads to instability of the PHIL setup.

$$|Z_L/Z_s| < 1 \quad (2)$$

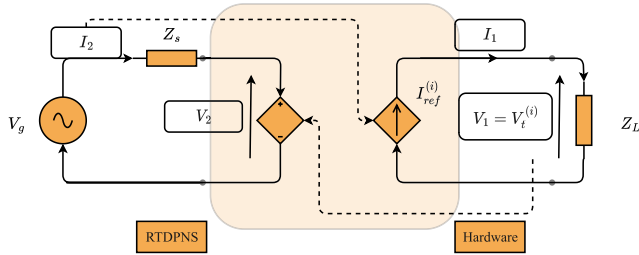


FIGURE 4. ITM (current-type).

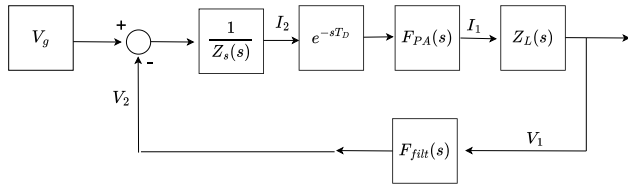


FIGURE 5. Transfer function of the ITM (current type).

Note that for voltage type ITM, \$|Z\_L/Z\_s| > 1\$ needs to be obeyed instead for maintaining stability. Moreover, it should be emphasized that (2) is only applicable to passive elements and cannot be generalized to any type of PDuT.

### III. PROPOSED PHIL INTERFACE

#### A. FORMULATION

As mentioned in Section II, ITM employs Gauss-Seidel iteration method to integrate the software and hardware parts of PHIL. As seen from Fig. 3, the conversion between voltage and current across different domains inherently lead to the impedance constraint of the stability. Consequently, we proposed to formulate the PHIL setup as the following: Unlike the ITM, the PDuT is modeled as an equivalent current source in the proposed configuration, as shown in Fig. 6. The GSS optimizer in Fig. 6 is implemented in a real-time simulator to carry out the proposed GSS optimization algorithm, which will be delineated in the next subsection. The GSS optimizer sends out the current reference, \$I\_{ref}^{(i)}\$ in two paths — one is directly to the current source model in the RTDPNS and the other is via DAC to the current controller of the PA, as shown in Fig. 6. The resulting terminal voltage of the PDuT, \$V\_{t1}^{(i)}\$ is sensed via a voltage sensor and an ADC, and is sent to the GSS optimizer. Similarly, the voltage across the equivalent current source model, \$V\_{t2}^{(i)}\$ in the RTDPNS is directly sent to the GSS optimizer. If the initialized value of \$I\_{ref}^{(i)}\$ is indeed the true value of the current in the PHIL, the voltage difference between both ends, \$V\_1 - V\_2\$, as shown in Fig. 6 should be minimized, which can be written as (3).

$$\text{Min}\{V_{t2}^{(i)} - V_{t1}^{(i)}\}. \quad (3)$$

Alternatively, (4) can be written for the convergence condition.

$$\left| \frac{V_{t2}^{(i)} - V_{t1}^{(i)}}{V_{t1}^{(i)}} \right| \leq \varepsilon, \quad (4)$$

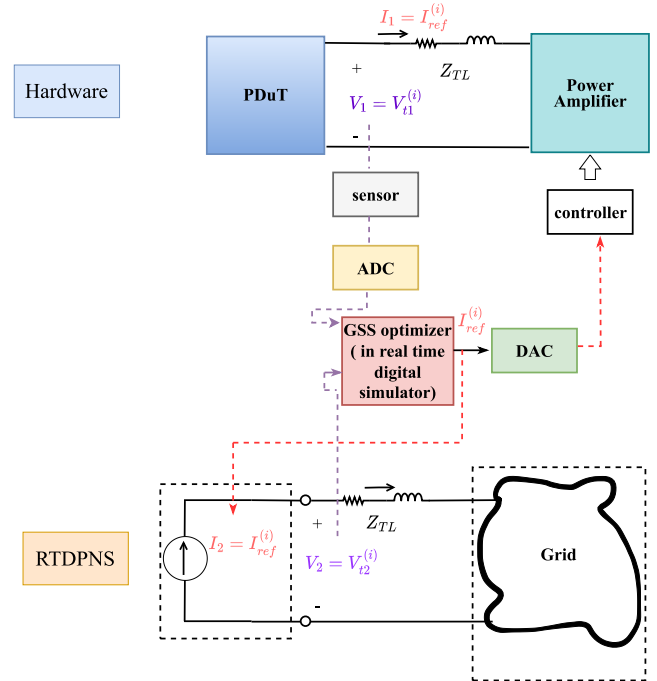


FIGURE 6. System diagram of the proposed method.

where \$\varepsilon\$ is a tolerance value. Note that if the tolerance value is too small, it takes a longer time to reach to the final solution while if it is too large, it converges prematurely. \$\varepsilon\$ in our setup was set to 1%.

#### B. ITERATION METHOD

GSS is one of the fastest direct search algorithms [23] to find the minimum or maximum value of a function. For the PHIL applications, GSS is to find the minimum of a function. The algorithm works by iteratively narrowing down an interval where the minimum of the function lies. At each iteration, the algorithm evaluates the function at two points within the interval and then chooses a new interval that is either to the left or right of the current interval, depending on which point had a higher function value. The ratio of the current boundary length to the new one is always the same, and this ratio is the golden ratio, which is approximately 0.618. This property of the algorithm ensures that the interval is always divided into two parts in a way that is optimal in terms of minimizing the number of function evaluations required to find the minimum. Fig. 7 illustrates how a one-dimensional GSS works. It starts with two initial guesses, \$x\_l\$ (lower guess) and \$x\_u\$ (upper guess), which bracket the minimum of \$f(x)\$. Next, two interior points \$x\_1\$ and \$x\_2\$ are chosen according to the golden ratio,

$$x_1 = x_l + d, \quad (5)$$

$$x_2 = x_u - d, \quad (6)$$

where

$$d = R(x_u - x_l), \quad (7)$$

$$R = \frac{\sqrt{5} - 1}{2}(x_u - x_l). \quad (8)$$

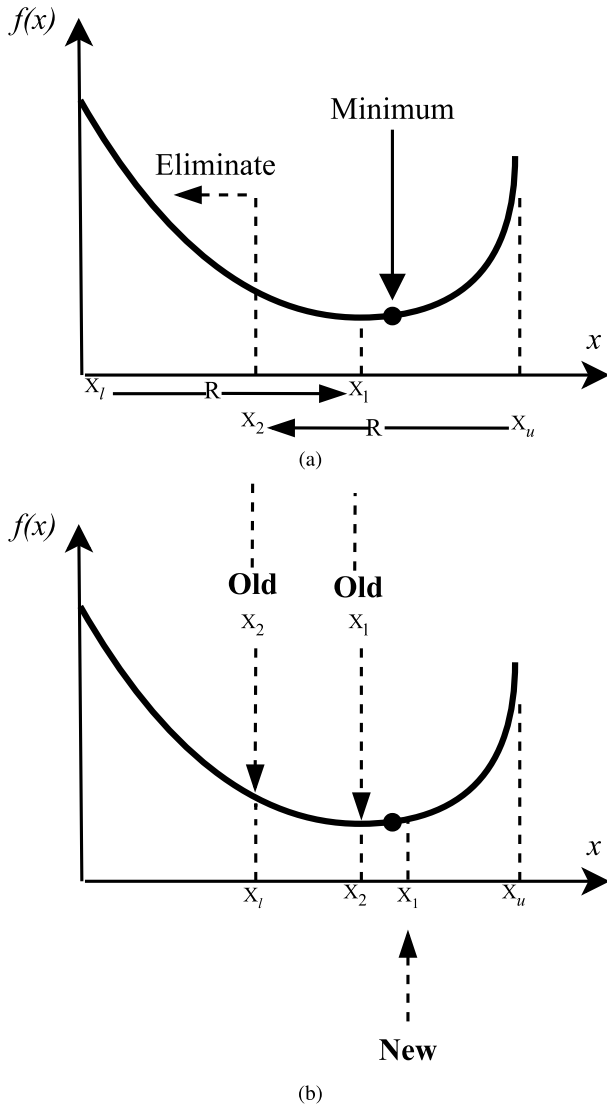


FIGURE 7. 1-D GSS: (a) region elimination, (b) update of the intermediate values.

As shown in Fig. 7, if  $f(x_1) < f(x_2)$ ,  $x_2$  becomes the new lower limit and  $x_1$  becomes the new  $x_2$ . On the other hand, if  $f(x_2) < f(x_1)$ ,  $x_1$  becomes the new upper limit and  $x_2$  becomes the new  $x_1$ .

Since our current control for the power amplifier is based on d-q frame current control, the formulation for the GSS needs to be extended to two dimensions. In other words,  $I_{ref}^{(i)}$ , which is a current reference vector in the a-b-c reference frame, needs to be converted into its d-q reference frame counterpart, which is  $I_{ref,d}$  and  $I_{ref,q}$  as shown in Fig. 8.

Thus, instead of two initial guess values, four initial boundary values need to be specified, and they are  $x_l$ ,  $x_u$ ,  $y_l$ , and  $y_u$ , as shown in Fig. 9. The intermediate points are also four, which are A ( $x_1, y_1$ ), B ( $x_2, y_1$ ), C ( $x_1, y_2$ ), and D ( $x_2, y_2$ ). Re-arranging (5) and (6) and extending them to the y-coordinate, the values of  $x_1$ ,  $x_2$ ,  $y_1$ , and  $y_2$  can be obtained:

$$x_1 = x_l + (1 - R)(x_u - x_l) \quad (9)$$

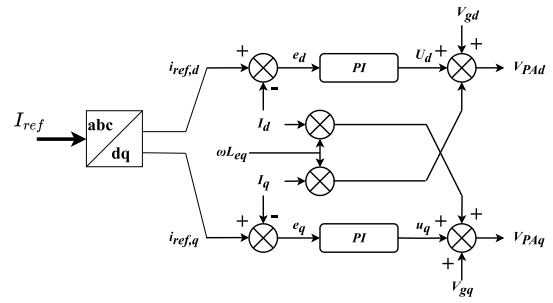


FIGURE 8. The current control of PA in the d-q frame.

$$x_2 = x_l + (R)(x_u - x_l) \quad (10)$$

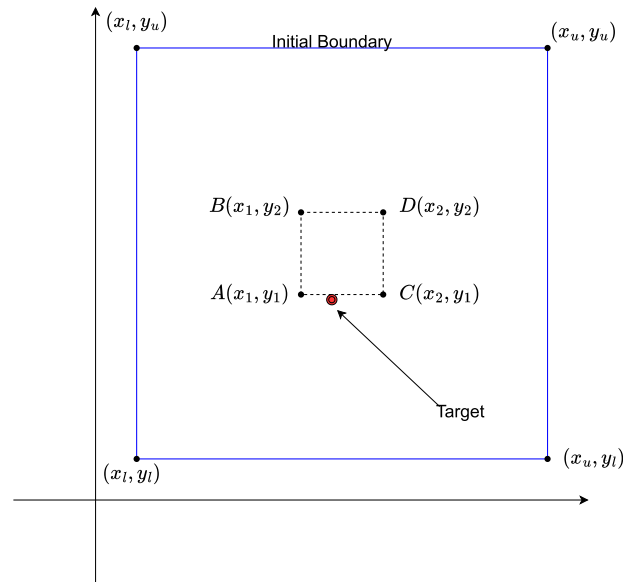
$$y_1 = y_l + (1 - R)(y_u - y_l) \quad (11)$$

$$y_2 = Y_l + (R)(y_u - y_l) \quad (12)$$

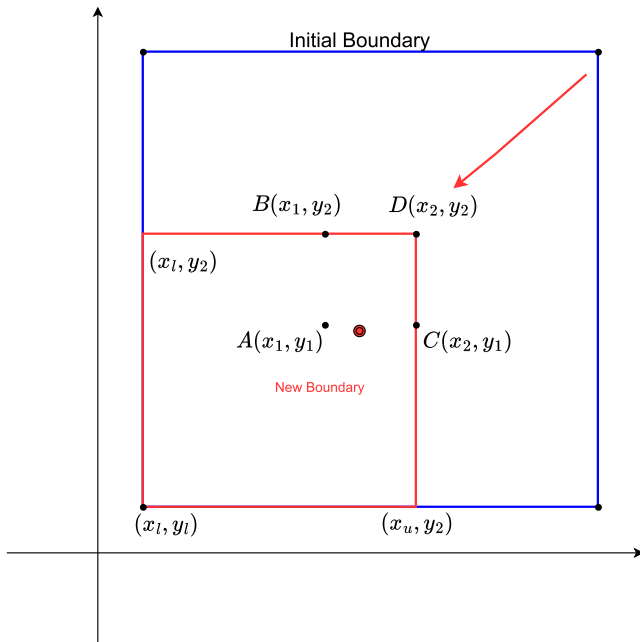
Assuming that point A is closest to the target optimum value, as shown in Fig. 9 (a),  $f(A)$  is the minimum among the intermediate points. Thus, the target value will not lie in  $x_2 < x < x_u$  and  $y_2 < y < y_u$ . Consequently, the new boundary is formed by  $(x_l, y_2)$ ,  $(x_l, y_l)$ ,  $(x_2, y_l)$ , and point D, as shown in Fig. 9 (b). The process of eliminating region keeps continuing until the target value is reached, as shown in Fig. 9 (c).

#### IV. VALIDATION

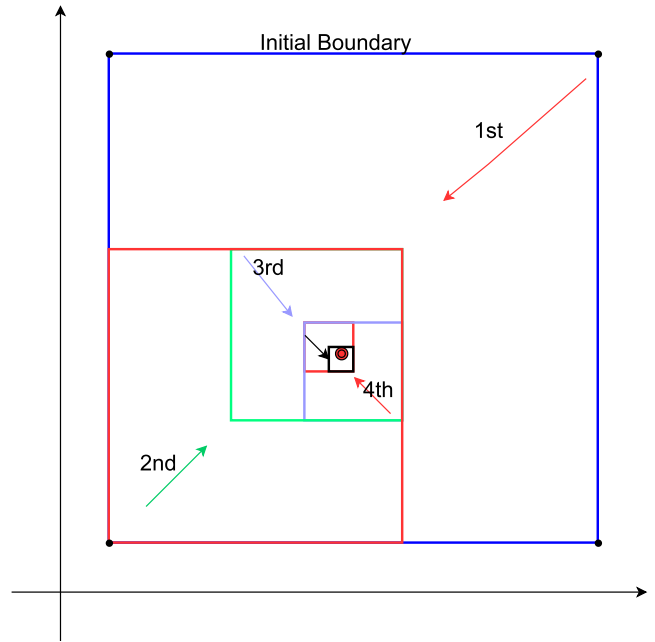
We have constructed two platforms for model validation. The first one is offline PHIL simulation. The entire system is built in Matlab/Simulink, where the time step emulating the hardware circuit is  $1 \mu s$  and the time step for RTDPNS and the digital controller of the power amplifier is  $50 \mu s$ . On the other hand the second platform is the experimental PHIL and Fig. 10 shows the actual setup. The controller is implemented in OP4512 from OPAL-RT. The GSS optimizer and the RTDPNS are implemented in SCALEXIO of dSPACE whereas the switched-mode power converter from SEMIKRON is used for PA and its switching frequency ( $f_{sw}$ ) is set to be 10 kHz. The time step for both controller and RTDPNS are  $50 \mu s$ . The time step for the GSS optimizer is set to be 7 ms. This is because it takes time for the current to reach the steady-state value. Thus, the current reference cannot be updated instantaneously. For our PHIL setup, a duration of 7 ms is inserted to ensure that all the current trajectories reach the steady-state before the reference is changed. We have considered four cases. In the first three cases, the PDuT is a passive device whose impedance is  $Z_L = R_L + j\omega L_L$ , as shown in Fig. 11. The PA is a voltage source converter (VSC) with LCL filters whose parameters are listed in Table 2. For the last case, the PDuT is an inverter based resource (IBR). The power system modeled in the RDPNS in all four cases is represented by the Thevenin equivalent whose impedance is  $R_s + j\omega L_s$ .



(a)



(b)



(c)

**FIGURE 9. Golden section step illustration: (a) Initialisation (b) First step (c) The rest of the steps.**

**A. CASE 1:  $L_S > L_L$**

For this case, we set  $L_S$  and  $L_L$  to be 5 mH and 1 mH, respectively. These values are chosen because they are readily available off-shelf for experimental implementation. As listed in Table 2, a minimum of delay time present in the experimental PHIL setup is 152.5  $\mu$ s. Note that  $T_{filt}$  is compensated by adding a phase angle in the Park transformation, as done in [24] and [25]. We vary the values of  $R_S$  and  $R_L$  from 0.1  $\Omega$  to 20  $\Omega$  in discrete manner and plot the stability regions (the region enclosed by

dashed lines) of ITM and the proposed method, as shown in Fig. 12 and 13, respectively. Different from the ITM, the proposed method does not readily yield an analytical transfer function. Consequently, we obtained the stability regions by numerically plotting closed-loop Nyquist plots of the PHIL setup whose input is subjected to small-signal perturbations via offline simulations. Fig. 12 shows that for ITM, most of the stable region is when  $R_S > R_L$  (i.e. region R2 in Fig. 12). Due to the feedback filters whose transfer function is  $\frac{1}{(0.002s+1)}$ , the stability at the region 1,

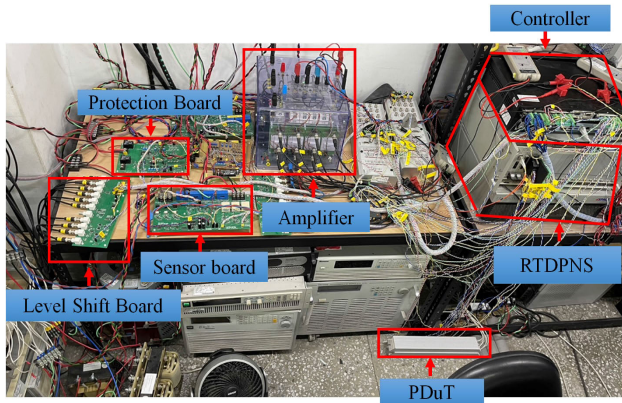


FIGURE 10. The setup of experimental PHIL.

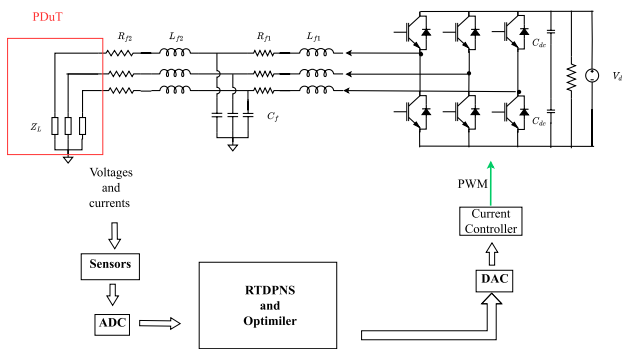


FIGURE 11. The PHIL setup whose PDuT is a passive device.

TABLE 1. Parameter values used in PHIL simulations.

Parameters	Values
$R_{f1}$	1 $\Omega$
$L_{f1}$	5 mH
$R_{f2}$	1 $\Omega$
$L_{f2}$	10 mH
$C_f$	1 $\mu$ F
$C_{dc}$	2200 $\mu$ F
$V_{dc}$	200 V
$f_{sw}$	10 kHz
$F_{filt}(s)$	$\frac{1}{(0.002s+1)}$

$R_L$  can be maintained. This is evident from the closed-loop Nyquist plots shown in Fig. 14 (a) and (b). Fig. 14 (a) shows that the system is unstable when the value of  $R_s$  is 2  $\Omega$  and  $R_L$  is 5  $\Omega$  without feedback filters because the origin is enclosed in the closed-loop Nyquist plot. On the other hand, Fig. 14 (b) shows that the system is stable when the feedback filter is included. As Fig. 13 indicates, the proposed method is stable regardless of the values of  $R_s$  and  $R_L$ , and the stability region is much larger than that of Fig. 12. As an example, Fig. 15 shows the closed-loop Nyquist plots of the three points indicated in Fig. 13. All these three figures show that they are stable because the origins are not encircled.

Figs. 16 shows the PHIL results based on offline simulation for ITM and proposed method when  $R_s = 15 \Omega$  and  $R_L =$

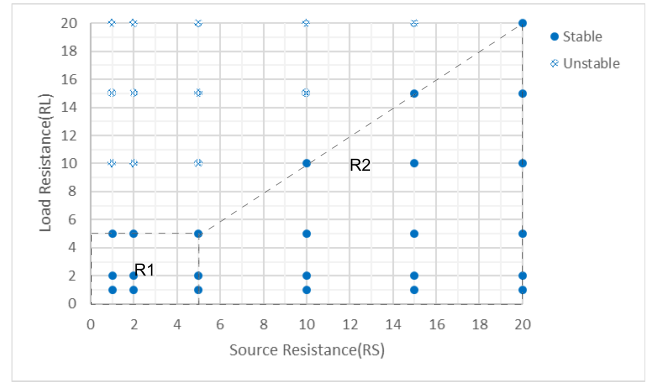


FIGURE 12. Stability region of ITM for case 1.

10  $\Omega$ . The initial conditions setting for the ITM and the proposed method are as follows: For the ITM,  $I_{ref,d}^{(0)}$  and  $I_{ref,q}^{(0)}$  are both set to 0.1 A. For the proposed method, the initial boundary  $x_l$  and  $y_l$  are set to 0.1 A whereas  $x_u$  and  $y_u$  are set to  $-10$  A. Note that magnitude of 10 A is the maximum current limit for this experimental setup. Since such a case is stable for both the ITM and the proposed method as seen in Figs. 12 and 13, offline PHIL simulation results indicate that the currents measured at the hardware circuits,  $I_d$  and  $I_q$  from the ITM and proposed method, converge to the true solutions, as shown in Fig. 16, which are obtained from dividing the source voltage ( $V_g = 110\sin(377t)$ ) by the total impedance value. Nevertheless, as shown in Fig. 16, ITM has a large negative overshoot and is more oscillatory as compared to the proposed method when the PA is turned on. Fig. 17 shows the difference between the true values and the converged results of ITM and the proposed method at the steady state. The figure shows that the proposed method is comparable with ITM in terms of accuracy.

Fig. 18 shows the experimental PHIL results when  $R_s = 15 \Omega$  and  $R_L = 10 \Omega$ . The ITM results are more oscillatory than those of the proposed method before  $t = 0.17$  s after PA is turned on, which is evident from Fig. 18. Moreover, Fig. 18 (b) shows a negative overshoot also occurs in the ITM. Nevertheless, some discrepancies exist between Figs. 16 and 18, which are resulted from that the real setup has higher damping effect. In addition, as reported in [22], in a real PHIL setup, there exist variable delays such as the wait time of the simulator to respond to the new value of the input from the hardware circuits at the beginning of the next time step, which can also contribute to the discrepancy. Fig. 19 shows the difference between the true values and the converged results of ITM and the proposed method at the steady state. The figure shows that the experimental results yield higher error, which is reasonable due to component and time delay uncertainties and distortions present in the experiment. Nevertheless, the proposed method yields slightly better results as the error for  $I_d$  of the proposed method is slightly lower than that of the ITM while the error for  $I_q$  for both methods is comparable.

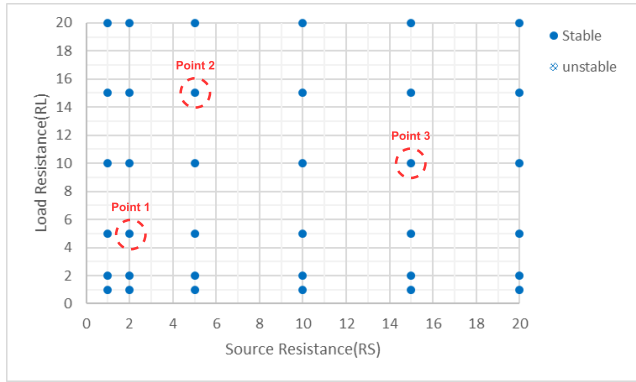
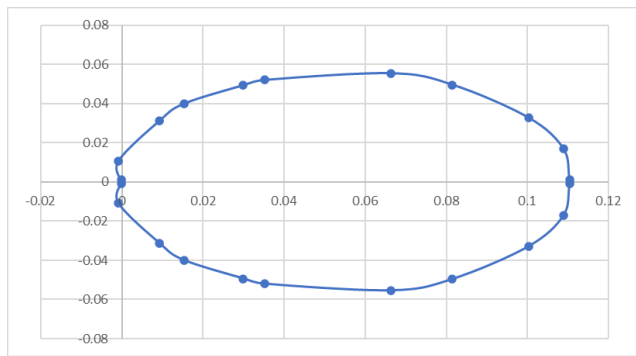
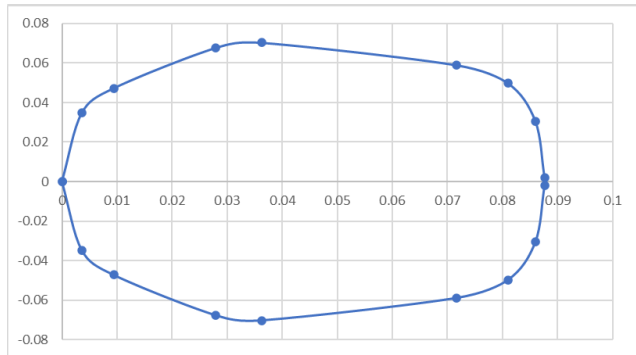


FIGURE 13. Stability region of the proposed method for cases 1, 2, and 4.



(a)



(b)

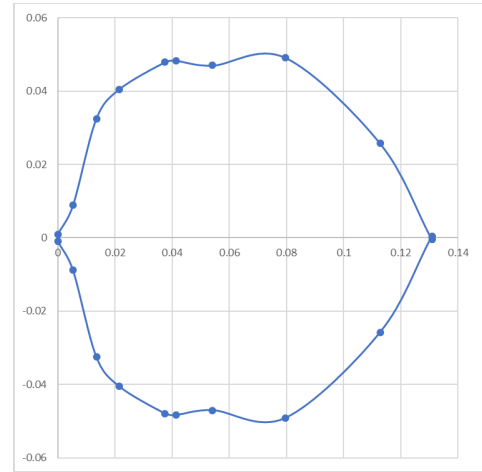
FIGURE 14. Closed-Loop Nyquist plots for ITM: (a) without the feedback filter; (b) with the feedback filter.

TABLE 2. Various delay times for the PHIL setup.

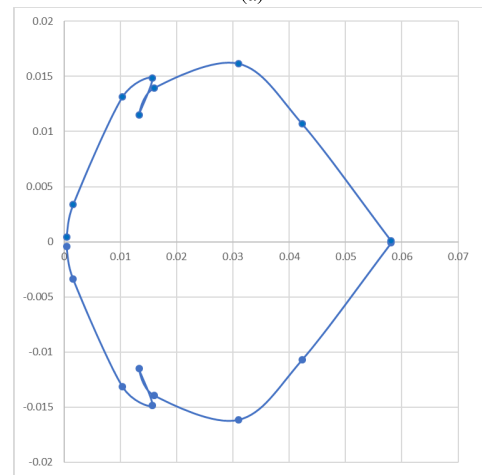
Delay Types	Values
$T_{comp}$	50 $\mu s$
$T_{comm}$	2.5 $\mu s$
$T_{PA}$	100 $\mu s$

**B. CASE 2:  $L_S < L_L$**

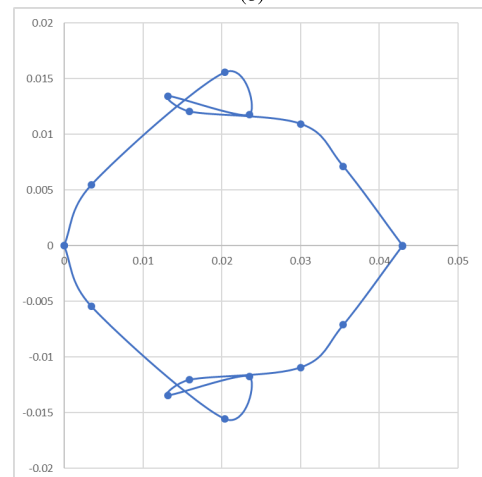
For this case, we set  $L_S$  and  $L_L$  to be 1 mH and 5 mH. We vary the values of  $R_S$  and  $R_L$  from 0.1  $\Omega$  to 20  $\Omega$  and plot the stability region (enclosed by dashed lines) of ITM as shown in Fig. 20. As figure indicates the stability region is much smaller than that of Fig. 20. This is because a large



(a)



(b)

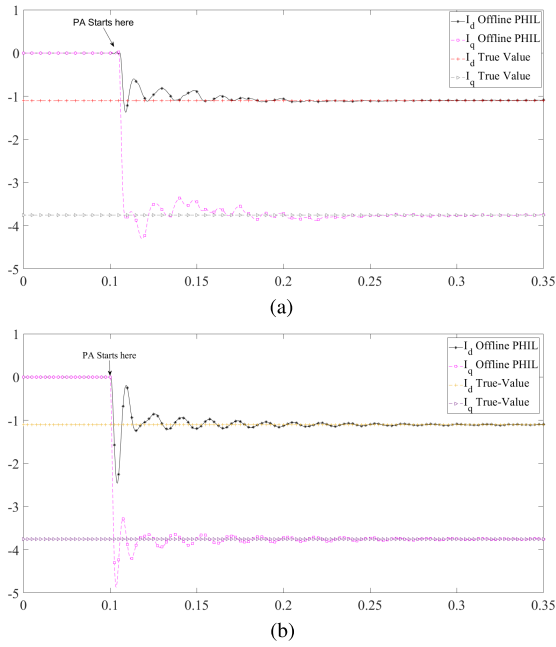


(c)

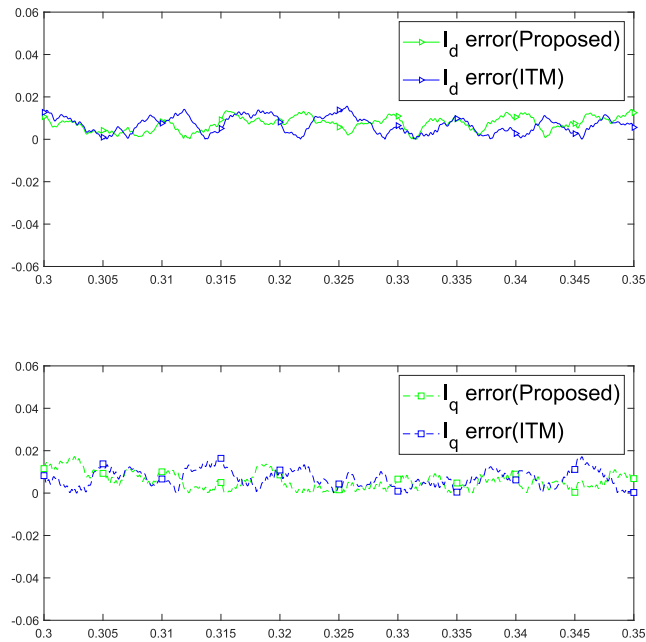
FIGURE 15. Closed-Loop Nyquist plots for the proposed method: (a) point 1 in Fig. 13; (b) point 2 in Fig. 13; (c) point 3 in Fig. 13.

portion of the region is  $R_S < R_L$ , violating (2). For the proposed method, similar to Case 1, the system is stable (the region enclosed by dashed lines) regardless of the values of  $R_S$  and  $R_L$ , as shown in Fig. 13. This is validated by



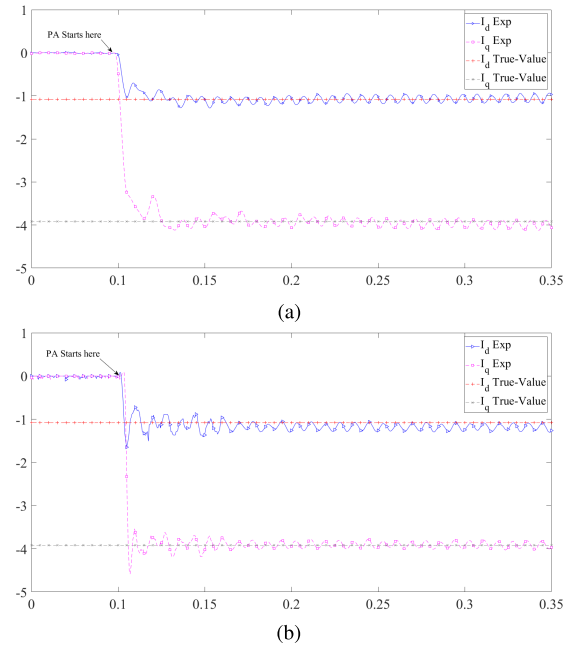


**FIGURE 16.** The current flowing through the PDuT (Offline PHIL) when  $(R_s, L_s, R_L, L_L) = (15 \Omega, 5 \text{ mH}, 10 \Omega, 1 \text{ mH})$ : (a) The proposed method; (b) ITM.

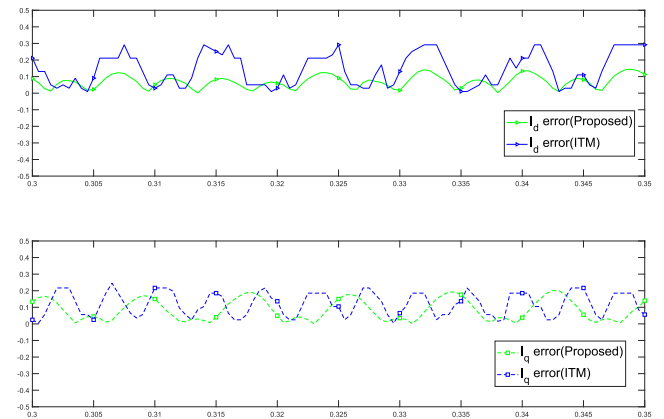


**FIGURE 17.** The difference between true values and the converged results (Offline simulation).

choosing  $R_s$  and  $R_L$  to be  $0.1 \Omega$  and  $15 \Omega$ , respectively. Offline PHIL simulation results indicate that the proposed method can still converge to the true value while the ITM leads to instability, as shown in Fig. 21. Similar results are confirmed by experiments, as shown in Fig. 22. Note that the amplitude of the current for Fig. 22 (b) is smaller than that of Fig. 21 (b) due to the more damping effect of the real PHIL



**FIGURE 18.** The current flowing through the PDuT (Experimental PHIL) when  $(R_s, L_s, R_L, L_L) = (15 \Omega, 5 \text{ mH}, 10 \Omega, 1 \text{ mH})$ : (a) The proposed method; (b) ITM.



**FIGURE 19.** The difference between true values and the converged results (Experiment).

setup. The slight discrepancies between Figs. 21 (a) and 22 (a) may be also due to the factor of the variable delays in the real PHIL setup as mentioned in Section IV-A.

### C. CASE 3: DYNAMIC RESPONSE

This section investigates the dynamic response of the proposed method. For the dynamic case, an additional condition is required for the proposed method to detect the change of states. (13) is the equation for detecting the change of state. If the condition holds, the initial boundary will be re-initialized to search for the new operating state.

$$\frac{|P_n - P_{n-1}|}{P_n} \leq \epsilon, \quad n = 1, 2, 3, \dots \quad (13)$$

where  $\epsilon$  is a tolerance value, and is set to 10%.

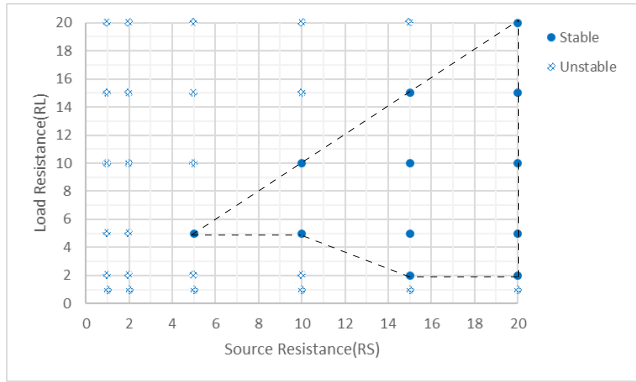


FIGURE 20. Stability Region of ITM for case 2.

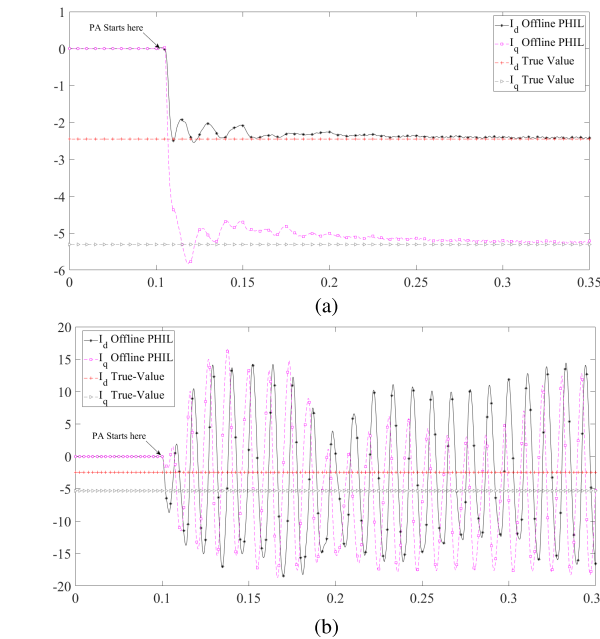


FIGURE 21. The current flowing through the PDuT (Offline PHIL) when  $(R_S, L_S, R_L, L_L) = (0.1 \Omega, 1 \text{ mH}, 15 \Omega, 5 \text{ mH})$ : (a) The proposed method; (b) ITM.

Fig. 23 shows the current trajectories when the PDuT is changed from the half to the full load for the proposed method. Fig. 24, on the other hand, shows the dynamic current response of the ITM when subjected to the same stable condition. Comparing both figures, one sees that the proposed method yields similar dynamic trajectories of the ITM, demonstrating that the dynamic responses are well reproduced by the proposed method.

**D. CASE 4: AN IBR AS A POWER DEVICE UNDER TEST**

Fig. 25 shows the PHIL setup for an IBR serving as the PDuT. This IBR, which can be regarded as a typical storage device, consists of a VSC whose dc side is connected to a dc source and its ac impedance is  $R_L + j\omega L_L$ . The switching frequency for the IBR is set to 5 kHz. The controller of the IBR, denoted as controller 2, is adapted from the ac voltage

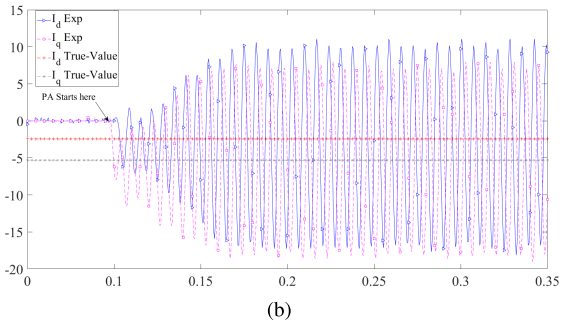
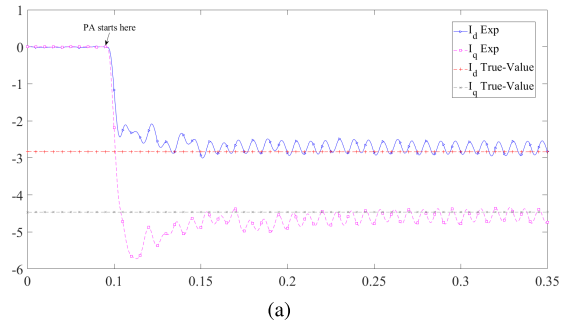


FIGURE 22. The current flowing through the PDuT (Experimental PHIL) when  $(R_S, L_S, R_L, L_L) = (0.1 \Omega, 1 \text{ mH}, 15 \Omega, 5 \text{ mH})$ : (a) The proposed method; (b) ITM.

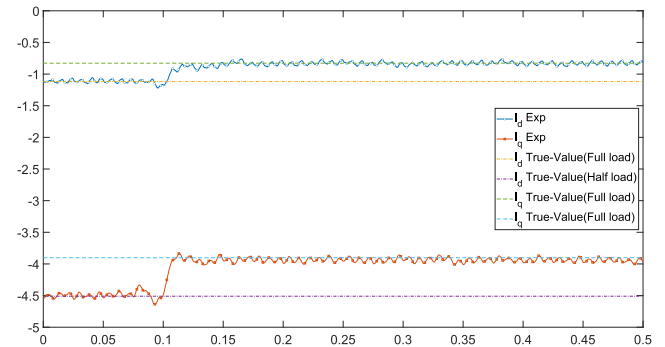


FIGURE 23. Transient response of GSS.

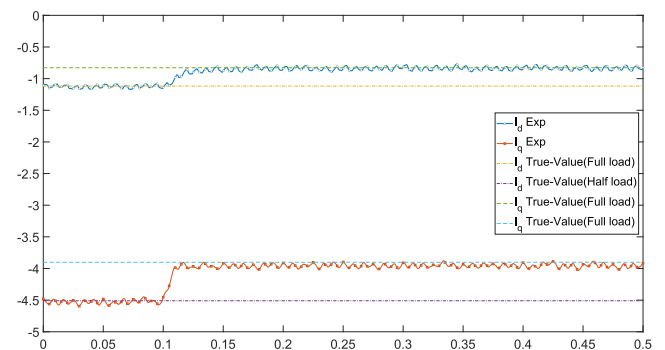


FIGURE 24. Transient response of ITM.

controller from [26]. The parameters of an IBR that may influence the overall stability of the PHIL include the control algorithms, control parameters of the IBR, the values of  $R_L$

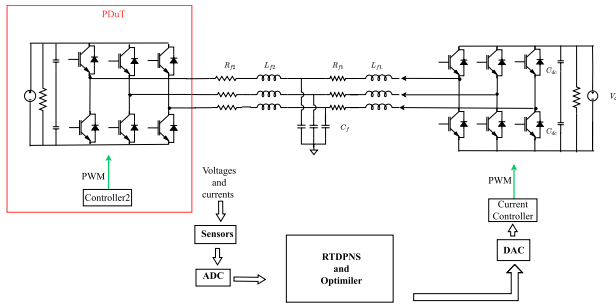


FIGURE 25. The PHIL setp whose PDUt is an IBR.

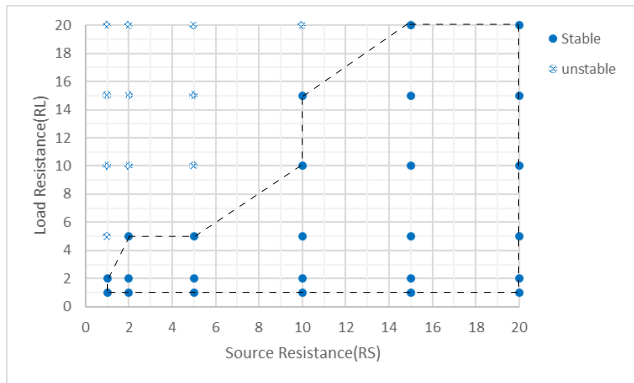


FIGURE 26. Stability Region of ITM for IBR.

and  $L_L$  of the IBR, and the source impedance. It is beyond the scope of this paper to investigate how each parameter affect the stability region. Instead, similar to what we have done for Cases 1 and 2, we varied the values of  $R_L$  and  $R_S$  while all other parameters remained fixed, and compared the stability regions of ITM and the proposed method. Fig. 26 shows the stability region of ITM, which is obtained by plotting its closed-loop Nyquist plots for each combination of  $R_S$  and  $R_L$  when  $L_S$  and  $L_L$  are set to 5 mH and 10 mH, respectively as in Case 1. It can be seen that the stability region shown in Fig. 26 is different from its passive counterpart as shown in Fig. 12. On the other hand, the stability region of the proposed method for the IBR case is still the same as that in Fig. 13.

V. CONCLUSION

This paper proposes a new power interface for PHIL, which can eliminate the stability constraints imposed by other power interfaces such as ITM, PCD, and DIM. This stability constraint is an impedance ratio between the ROS and PDUt, which needs to be maintained in order to preserve stability. This imposes practical difficulty as one needs to precisely determine, prior to PHIL implementation, the impedance of the PDUt, which could be a tedious and difficult task. The proposed method extends one dimensional GSS to multiple-dimensional GSS for PHIL applications. The proposed method does not require to convert current from the software part to the voltage from the hardware part. Thus, unlike ITM, it can maintain stability regardless the values

of the source impedance and the impedance of the PDUt. Offline and experimental PHIL results have confirmed that the proposed method has larger stability regions, compared to the ITM.

REFERENCES

- [1] P. C. Kotsampopoulos, F. Lehfuss, G. F. Lauss, B. Bletterie, and N. D. Hatziaargyriou, "The limitations of digital simulation and the advantages of PHIL testing in studying distributed generation provision of ancillary services," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5502–5515, Sep. 2015.
- [2] M. D. O. Faruque, T. Strasser, G. Lauss, V. Jalili-Marandi, P. Forsyth, C. Dufour, V. Dinavahi, A. Monti, P. Kotsampopoulos, J. A. Martinez, K. Strunz, M. Saeedifard, X. Wang, D. Shearer, and M. Paolone, "Real-time simulation technologies for power systems design, testing, and analysis," *IEEE Power Energy Technol. Syst. J.*, vol. 2, no. 2, pp. 63–73, Jun. 2015.
- [3] G. Huang, X. Wu, F. Guo, L. Yu, and W.-A. Zhang, "DEID-based control of networked rapid control prototyping system: Design and applications," *IEEE Trans. Ind. Electron.*, vol. 70, no. 1, pp. 1047–1056, Jan. 2023.
- [4] K. L. Lian and P. W. Lehn, "Real-time simulation of voltage source converters based on time average method," *IEEE Trans. Power Syst.*, vol. 20, no. 1, pp. 110–118, Feb. 2005.
- [5] W. Ren, M. Steurer, and T. L. Baldwin, "Improve the stability and the accuracy of power hardware-in-the-loop simulation by selecting appropriate interface algorithms," *IEEE Trans. Ind. Appl.*, vol. 44, no. 4, pp. 1286–1294, Jul. 2008.
- [6] S. Resch, J. Friedrich, T. Wagner, G. Mehlmann, and M. Luther, "Stability analysis of power hardware-in-the-loop simulations for grid applications," *Electronics*, vol. 11, no. 1, p. 7, Dec. 2021. [Online]. Available: <https://www.mdpi.com/2079-9292/11/1/7>
- [7] M. Pokharel and C. N. M. Ho, "Stability analysis of power hardware-in-the-loop architecture with solar inverter," *IEEE Trans. Ind. Electron.*, vol. 68, no. 5, pp. 4309–4319, May 2021.
- [8] B. Li, Z. Xu, S. Wang, L. Han, and D. Xu, "Interface algorithm design for power hardware-in-the-loop emulation of modular multilevel converter within high-voltage direct current systems," *IEEE Trans. Ind. Electron.*, vol. 68, no. 12, pp. 12206–12217, Dec. 2021.
- [9] A. Riccobono, E. Liegmann, M. Pau, F. Ponci, and A. Monti, "Online parametric identification of power impedances to improve stability and accuracy of power hardware-in-the-loop simulations," *IEEE Trans. Instrum. Meas.*, vol. 66, no. 9, pp. 2247–2257, Sep. 2017.
- [10] L. Qi, J. Langston, M. Steurer, and A. Sundaram, "Implementation and validation of a five-level STATCOM model in the RTDS small time-step environment," in *Proc. IEEE Power Energy Soc. Gen. Meeting*, Jul. 2009, pp. 1–6.
- [11] O. Tremblay, D. Rimorov, R. Gagnon, and H. Fortin-Blanchette, "A multi-time-step transmission line interface for power hardware-in-the-loop simulators," *IEEE Trans. Energy Convers.*, vol. 35, no. 1, pp. 539–548, Mar. 2020.
- [12] A. Monti, H. Figueroa, S. Lentijo, X. Wu, and R. Dougal, "Interface issues in hardware-in-the-loop simulation," in *Proc. IEEE Electric Ship Technol. Symp.*, Jul. 2005, pp. 39–45.
- [13] W. Ren, "Accuracy evaluation of power hardware-in-the-loop (PHIL) simulation," Ph.D. dissertation, Florida State Univ., 2007.
- [14] J. Ihrens, S. Möws, L. Wilkening, T. A. Kern, and C. Becker, "The impact of time delays for power hardware-in-the-loop investigations," *Energies*, vol. 14, no. 11, p. 3154, May 2021. [Online]. Available: <https://www.mdpi.com/1996-1073/14/11/3154>
- [15] G. F. Lauss, M. O. Faruque, K. Schoder, C. Dufour, A. Viehweider, and J. Langston, "Characteristics and design of power hardware-in-the-loop simulations for electrical power systems," *IEEE Trans. Ind. Electron.*, vol. 63, no. 1, pp. 406–417, Jan. 2016.
- [16] J. Sun, C. Yin, J. Gong, Y. Chen, Z. Liao, and X. Zha, "A stable and fast-transient performance switched-mode power amplifier for a power hardware in the loop (PHIL) system," *Energies*, vol. 10, no. 10, p. 1569, Oct. 2017. [Online]. Available: <https://www.mdpi.com/1996-1073/10/10/1569>
- [17] N. D. Marks, W. Y. Kong, and D. S. Birt, "Stability of a switched mode power amplifier interface for power hardware-in-the-loop," *IEEE Trans. Ind. Electron.*, vol. 65, no. 11, pp. 8445–8454, Nov. 2018.

- [18] G. Lauss, Z. Feng, M. H. Syed, A. Kontou, A. D. Paola, A. Paspatis, and P. Kotsampopoulos, "A framework for sensitivity analysis of real-time power hardware-in-the-loop (PHIL) systems," *IEEE Access*, vol. 10, pp. 101305–101318, 2022.
- [19] M. Muhammad, H. Behrends, S. Geißendörfer, K. V. Maydell, and C. Agert, "Power hardware-in-the-loop: Response of power components in real-time grid simulation environment," *Energies*, vol. 14, no. 3, p. 593, Jan. 2021. [Online]. Available: <https://www.mdpi.com/1996-1073/14/3/593>
- [20] S. Chapra and R. Canale, *Numerical Methods for Engineers*. New York, NY, USA: McGraw-Hill, 2014.
- [21] R. K. L. Lian, R. K. Subroto, V. Andrean, and B. H. Lin, *Harmonic Modeling of Voltage Source Converters Using Basic Numerical Methods*. USA: IEEE Press, 2021.
- [22] E. Guillo-Sansano, M. H. Syed, A. J. Roscoe, G. M. Burt, and F. Coffele, "Characterization of time delay in power hardware in the loop setups," *IEEE Trans. Ind. Electron.*, vol. 68, no. 3, pp. 2703–2713, Mar. 2021.
- [23] G. S. Rani, S. Jayan, and K. V. Nagaraja, "An extension of golden section algorithm for n-variable functions with MATLAB code," *IOP Conf. Ser., Mater. Sci. Eng.*, vol. 577, no. 1, Nov. 2019, Art. no. 012175.
- [24] S. Zhang, Y. Ma, L. Yang, F. Wang, and L. M. Tolbert, "Development of a hybrid emulation platform based on RTDS and reconfigurable power converter-based testbed," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2016, pp. 3121–3127.
- [25] G. Li, S. Jiang, Y. Xin, Z. Wang, L. Wang, X. Wu, and X. Li, "An improved DIM interface algorithm for the MMC-HVDC power hardware-in-the-loop simulation system," *Int. J. Electr. Power Energy Syst.*, vol. 99, pp. 69–78, Jul. 2018. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S0142061517319014>
- [26] M. Amin and M. Molinas, "A gray-box method for stability and controller parameter estimation in HVDC-connected wind farms based on nonparametric impedance," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 1872–1882, Mar. 2019.



**KUO LUNG LIAN** (Senior Member, IEEE) received the B.A.Sc. (Hons.), M.A.Sc., and Ph.D. degrees in electrical engineering from the University of Toronto, Toronto, ON, Canada, in 2001, 2003, and 2007, respectively. From October 2007 to January 2009, he was a Visiting Research Scientist with the Central Research Institute of Electric Power Industry, Japan. He is currently a Professor with the National Taiwan University of Science and Technology, Taipei, Taiwan. He was a recipient of the 2023 Delta Young Technology Scholar Award. He served as the Chairperson for the IAS at Taipei Chapter, from 2019 to 2021. He is an Associate Editor of IEEE Access, IEEE Transactions on Power Delivery, and *Journal of Contemporary Issues in Education* (JCIE).



**YOU FANG FAN** (Student Member, IEEE) received the B.Eng. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 2020. He is currently pursuing the M.S. degree with the Department of Electrical Engineering, National Taiwan University of Science and Technology, Taipei, Taiwan.



**CHU YING XIAO** is currently pursuing the M.S. degree with the Department of Electrical Engineering, National Taiwan University of Science and Technology, Taipei, Taiwan.



**JUAN CONSTANTINE** received the B.Eng. degree from Swiss German University, Indonesia, in 2015. He is currently pursuing the master's degree in electrical engineering with the National Taiwan University of Science and Technology, Taipei, Taiwan.



**ZHAO-PENG HE** is currently pursuing the M.S. degree with the Department of Electrical Engineering, National Taiwan University of Science and Technology, Taipei, Taiwan.

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