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RESEARCH ARTICLE

Implementation Decentralized Space Vector PWM Method for Multilevel Multiphase Converters

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ABSTRACT In the field of power electronics research, the expansion of the number of phases and voltage levels in power converters may pose several challenges for central processors. In the space vector pulse width modulation (SVPWM) method, the microprocessor must simultaneously calculate the multi-vector switching and the corresponding switching time based on complex computational algorithms. The complexity of the algorithm flowchart tends to increase significantly as the number of phases and voltage levels increase. This problem can be easily solved in decentralized controlled power converters. The decentralized control structure and method allow cells to divide themselves into tasks based on limited information exchange with neighboring cells. This study presents a decentralized control topology for a multilevel multiphase power converter (MMPC) using the SVPWM method. Depending on the number of active cells, each cell exchanges information with its neighbors, determining the exact switching vector and switching time. Using this approach, the requirements for computing power and processing speed of the cells are significantly reduced. Digital signal processing (DSP) TMS320F28379D is used as a controller of cells to verify the proposed structure and method in addition to simulation results using on MATLAB/Simulink software.

INDEX TERMS Multicellular converter, multilevel multiphase power converter, decentralized control, space vector pulse width modulation, decentralized power converters, dynamic reconfiguration, multicell serial-parallel converters.

LIST OF ABBREVIATIONS

AC	Alternating current.
CPWM	Carrier pulse width modulation.
DC	Direct current.
DSP	Digital signal processing.
FFT	Fast fourier transform.
dSPACE	Digital signal processing and control engineering.
IGBT	Insulated gate bipolar transistor.
MMPC	Multilevel multiphase power converter.
NPC	Neutral point clamped.
PWM	Pulse width modulation.
SVPWM	Space vector pulse width modulation.
THD	Total harmonic distortion.

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I. INTRODUCTION

The technology of MMPC is increasingly perfected to improve power quality, reduce harmonics on the power grid, reduce switching losses, reduce switching voltage, reduce voltage stress, high-voltage modulation with voltage-limited components [1], increase electromagnetic compatibility, and increase equipment performance. The modular structure of power converters has been an inevitable development trend of power converters in medium and large power applications [2], [3]. In this case, the number of modules that the central processor has to manage and control is large, monitoring and controlling the voltage between the modules [4], [5], monitoring and controlling the current between phases [6], performing power quality enhancement algorithms, and providing appropriate pulse width modulation (PWM) signals for modules [7]. This is a difficult problem when implementing the MMPC. In addition, in some applications, if one

or several modules need to stop working, possibly owing to damage or operational optimization, the MMPCs need to re-establish connections, and it is necessary to adjust the control program of the module to match the number of modules that are still in operation; this process requires the system to stop working and can take a long time to adjust.

The carrier pulse width modulation (CPWM) method has been widely deployed in MMPC [8]. Multilevel CPWM techniques can be mentioned as phase shift, phase disposition, phase opposition disposition, alternative phase opposition disposition, ... The biggest advantage of CPWM technique is easy implementation [9], [10]. This advantage becomes even more pronounced as the number of phases of the power converter increases because this technique controls each phase separately. Therefore, the implementation of CPWM in multiphase converters is simple. However, the CPWM method is implemented based on analog modulation technology and there is no common algorithm for all configurations.

In multilevel modulation, the SVPWM technique simultaneously processes all signals as an overall process [11]. Therefore, the SVPWM method stands out for its ability to optimize switching states, which is suitable when deployed on digital microchips [12]. The SVPWM method has proven to be effective, providing numerous performance-enhancing benefits in single-phase and three-phase systems. In general, the multilevel SVPWM modulation algorithm and method are calculated based on a given configuration with a predetermined number of modules in each phase and a predetermined number of phases, and they do not change during the operation [13]. The SVPWM method is used as a switching pulse modulation algorithm in 3-phase [14], 5-phase [15], 6-phase [13], dual-six-phase [16], and dual-three-phase applications [17].In addition to the main task of providing flexible switching solutions for insulated gate bipolar transistor (IGBT) switches, research on the SVPWM method focuses on solving the following problems: voltage balance of capacitors in a multilevel neutral point clamped (NPC) inverter model [18], balance voltage between modules in multilevel multiphase power converters [19], reduction of common mode voltage [20], reduction of total harmonic distortion (THD) [15], reducing switching loss, solving the problem when the power converter works in over-modulation. Recently, the core value of the SVPWM method has been enhanced by finding a general implementation for multilevel multiphase power converters. The multiphase, multilevel modulation algorithm can be applied to inverters with any number of phases and levels. However, this topic has not been extensively studied or published. Therefore, this is a potential research direction and has many applications.

Studies [21], [22] presented a modulation technique for multilevel multiphase power converters, which converts the multilevel multiphase problem to a 2-level multiphase platform. The switching vectors and switching time are adjusted to multiphase, multilevel space based on the results of 2-level multiphase calculation. Currently, no commercial digital signal processor has sufficient built-in pulse width modulation units to drive all the switches. Typically, multiphase multilevel power converters are controlled by combining a field programmable gate array (FPGA) and digital signal processing and control engineering (dSPACE) [22]. In addition to generating PWM signals for all switches, the processor also has to connect a lot of feedback signals about voltage and current, although the connection ability, the calculation speed of the FPGA, and dSPACE is quite high, when the number levels and phases of the system increase, this is also a matter of concern and consideration.

The idea of dividing the execution duties of the central processor can be easily solved using decentralized control structures in the power converters. The main concerns for decentralized power converters were the ability to accurately modulate the required voltage, system startup time, and reconfiguration time when changing the configuration. Dynamic architecture, reliability in operation and control, the ability to connect modules according to the flexible power and voltage needs of the applications... Recent studies have focused on three models of decentralized power converter control:

- First, the controller is divided into main and sub-controllers or local and central controllers [23], [24]. When using this structure, the advantage is that the controllers are divided into execution tasks, thereby reducing the amount of computation of the modules compared to using a central processor. However, when it is necessary to change the structure or expand the system, the power converter must stop working, reestablish many connections and modify the program of the modules.

- Second, the modules of the decentralized power converter use the collected voltage and current analysis results of the module to generate an appropriate PWM signal for the module itself [25], [26]. The advantage of this structure is that the modules are completely decentralized, and there is no need to establish any communication information. However, the implementation algorithm in the modules is relatively complex and can only be applied to some IGBT connection models.

- Third, the cell calculation algorithm is implemented based on the limited information exchanged between two neighboring cells [27], [28], [29]. Cells of decentralized power converters can operate on their own based on the exchange of a limited number of signals, which quickly proves to be highly efficient and easy to scale to the number of levels and phases. A carrier pulse width modulation method was developed in this study. Based on the information exchanged with neighboring cells, the task of each cell is to synthesize its own carrier with the appropriate frequency and amplitude. The information needed for the cell to synthesize the carrier can be the carrier amplitude [30], carrier phase angle [31], [32], cell location [30], total cells [30].

Meanwhile, decentralized power converters using the SVPWM method have not been fully researched or published.

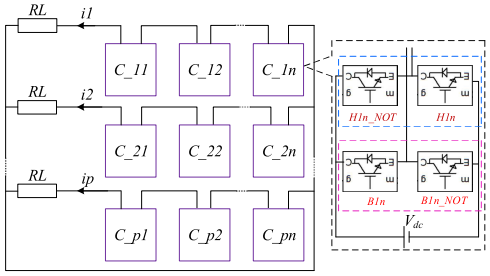
Studying [33], [34], the cell determines its own position using the phase angle shift algorithm, which calculates its own switching vectors and appropriate switching times in a multilevel single-phase decentralized power converter. In general, the study [34] presented the SVPWM method for decentralized control multilevel power converters, where the switching vector and switching time are calculated based on the location information of the cell. The results show that it is possible to apply SVPWM to decentralized power converters. According to the research results, based on the number of modules present in each phase, the number of phases of the system, modulation voltage, and SVPWM algorithm of the cells generate all the switching vectors and switching times of the cells. Then, based on the information of the cell's position in the phases and the position in a phase, the cells choose the appropriate switching vectors and switching times. Thus, the computational volume of the cells is still very large, limiting the superiority of decentralized power converters, and it is necessary to adjust the algorithm to simplify the program execution of each cell.

This paper presented the structure and method of SVPWM for decentralized multiphase and multilevel power converters. The tasks performed for the cells were divided according to the arrangement of the cells in the phases and the positions of the cells in each phase. Each cell uses a cascade full-bridge model with a fixed direct current (DC) voltage source. The output alternating current (AC) voltage is the sum of the voltages of the active cells in the system. This study demonstrates the effectiveness of reducing the execution workload of each cell compared to the case of using a central processor. In addition, when changing the number of cells in each phase or changing the number of phases to suit the application, the proposed structure and method allow the system to automatically correct the structure without having to stop. The remaining content of this research is organized as follows. Section II presents a proposed configuration and SVPWM method for a decentralized multilevel multiphase converter: proposing the DSVPWM algorithm, building a program implementation flow chart for each cell, comparing and evaluating calculation ability between the two traditional CPWM method and the proposed DSVPWM method. In section III, the verifications include: system configuration, response of output voltage and load current according to reference voltage, system response when simulated dynamic restructuring occurs. In section IV, the proposals will be verified through an experimental model using DSPs as cell controllers. Finally, Section V concludes the work.

II. PROPOSED CONFIGURATION AND SVPWM METHOD FOR MULTILEVEL MULTIPHASE CONVERTERS

A. PROPOSED DSVPWM ALGORITHM

The multilevel multiphase power converter is introduced as shown in Fig. 1, which includes p phase, each phase consists of n cell cascade full bridge in series. Fig. 2 shows the control connection diagram between the cells of the proposed multilevel multiphase inverter. The inputs and outputs of the cell



(a) Principal circuit. (b) Cell.

FIGURE 1. Multilevel multiphase cascade full bridge power converter.

TABLE 1. Input and output of cell controller with DSVPWM method.

Symbol	Parameter
EN	Enable
V_{m_in}	Received signal modulation voltage from primary cell
F_{m_in}	Received modulation frequency from the previous cell
θ_{H-1}	Index from cell n-1 in a phase
θ_{H+1}	Index from cell n+1 in a phase
θ_{V-1}	Index from cell n-1 in a column
θ_{V+1}	Index from cell n+1 in a column
clk_{in}	Received synchronous clock pulse from primary cell
V_{m_out}	Transmitted signal modulation voltage to next cell
F_{m_out}	Transmitted modulation frequency to the next cell
clk_{out}	Transmitted synchronous clock pulse to other cells
θ_{H_n}	Index to adjacent cells in the same phase
θ_{V_n}	Index to adjacent cells in the same column
$S1$	The control signal IGBT B of cell n
$\overline{S1}$	The control signal IGBT B_NOT of cell n
$S2$	The control signal IGBT H of cell n
$\overline{S2}$	The control signal IGBT H_NOT of cell n

controller are listed in Table 1. In the proposed decentralized control structure, the cells determine their location in the system. The phase angle shift algorithm (1) was used to determine the position of the cells in each phase. To ensure that the phase-angle shift algorithm can be implemented, the initial phase angle at the starting time of the cells is 180°, and the phase angle of the first cell is zero. The total cell N_{cp} in each phase was calculated using (2). After a few iterations, the phase angle θ_H of the cells automatically stabilizes, ensuring that the phase difference of the two cells $\Delta\theta_H$ complies with equation (3). Then, the position of the cells i_n in phase is determined by (4). where operator $round(x)$ rounds each element of x to the nearest integer.

$$\begin{cases} \theta_H^{k+1} = \theta_H^k + K\left(\theta_H^{\sim k+1} - \theta_H^k\right), \; with\, K \le 0.67 \\ \theta_H^{\sim k+1} = mod\left\{\theta_{H+1}^k + 0.5mod \right. \\ \left.\left[\left(\theta_{H-1}^k - \theta_{H+1}^k, 360\right), 360\right]\right\} \end{cases} \quad (1)$$

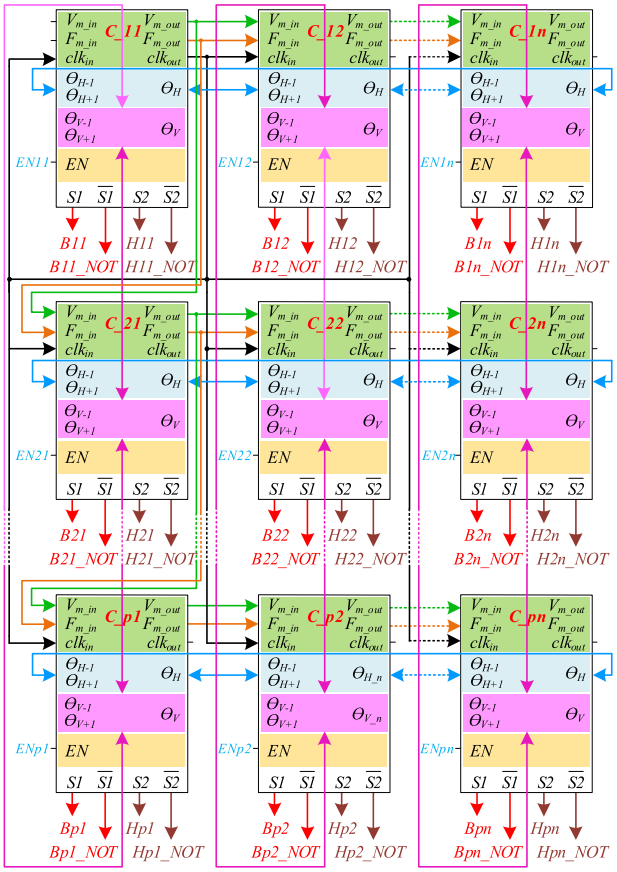


FIGURE 2. Decentralized control connection between cells with DSVPWM algorithm for MMPC.

$$N_{cp}^k = round\left\{360/\left[0.5mod\left(\theta_{H-1}^k - \theta_{H+1}^k, 360\right)\right]\right\} \quad (2)$$

$$\Delta\theta_H = 0.5mod(\theta_{H-1}^k - \theta_{H+1}^k, 360) = \frac{360}{N_{cp}} \quad (3)$$

$$i_n^k = round\left(\frac{360}{\theta_H^k N_{cp}^k}\right) + 1 \quad (4)$$

A similar process and algorithm (5) were applied to determine the position of the phase and the total number of phases of the system. The initial phase angle of the cells was 180°, and the initial phase angle of the cells in the first phase was fixed at 0. The total phases of the MMPC are determined by Equation (6), and the position of the phase is defined by Equation (7).

$$\begin{cases} \theta_v^{k+1} = \theta_v^k + K\left(\theta_v^{\sim k+1} - \theta_v^k\right), \ with\, K \le 0.67 \\ \theta_v^{\sim k+1} = mod\left\{\theta_{v+1}^k + 0.5mod\right. \\ \left.\left[\left(\theta_{v-1}^k - \theta_{v+1}^k, 360\right), 360\right]\right\} \end{cases} \quad (5)$$

$$p^k = round\left\{360/\left[0.5mod\left(\theta_{v-1}^k - \theta_{v+1}^k, 360\right)\right]\right\} \quad (6)$$

$$i_p^k = round\left(\frac{360}{\theta_v^k p^k}\right) + 1 \quad (7)$$

The multilevel multiphase reference voltage v_{ref} of the inverter has the form as shown in (8):

$$v_{ref}^k = V_m sin\{\omega t + [2\pi(l-1)/p^k]\} \quad (8)$$

where $l = 1, 2, 3, \ldots, p$; p is the total phase of the DC/AC converter. For the multilevel modulation technique, the modulation voltage can be an integer of the input voltage V_{dc} for each cell, as shown in Equation (9).

$$v_r^k = \frac{v_{ref}^k}{V_{dc}} = \left[\, v_{r1}^k,\ v_{r2}^k,\ \ldots,\ v_{rp}^k \,\right]^T \quad (9)$$

The multilevel multiphase reference voltage vector can be decomposed into the sum of its integer and fractional parts (10) and (11). The operator *floor(x)* rounds the elements of x to the nearest integer towards minus infinity. v_{fs} vector is created from v_f vector by arranging the elements of v_f in the descending orders, as shown in (12).

$$v_i^k = floor(v_r^k) \quad (10)$$

$$v_f^k = v_r^k - v_i^k \quad (11)$$

$$v_{fs}^k = sort(v_f^k) = \left[\, v_{fs1}^k,\ v_{fs2}^k,\ \ldots,\ v_{fsp}^k \,\right]^T \quad (12)$$

Initialize matrix A with one row, $(p+1)$ column as shown in (13). The first element of matrix A has a value of 0, and the remaining elements are determined using Equation (14).

$$A^k = \left[\, 0\ \ A_2^k\ \ A_3^k\ \ \ldots\ \ A_p^k\ \ A_{p+1}^k \,\right] \quad (13)$$

$$A_g^k = \begin{cases} 1 & if\ \left[v_f\left(i_p^k, 1\right)\right] = v_{fs}(g,1) \\ 0 & if\ \left[v_f\left(i_p^k, 1\right)\right] \neq v_{fs}(g,1) \end{cases}$$
$$with\, g = 2\ to\ p+1 \quad (14)$$

The switching vector of 2-level modulation is obtained by solving Equation (15), with the coefficient matrix D described by Equation (16).

$$v_d^k = A^k D^k = \left[\, v_{d1}^k\ v_{d2}^k\ \cdots\ v_{d(p+1)}^k \,\right] \quad (15)$$

$$D^k = \begin{bmatrix} 1 & 1 & \ldots & 1 \\ 0 & 1 & \ldots & 1 \\ \ldots & \ldots & \ldots & 1 \\ 0 & 0 & \ldots & 1 \end{bmatrix} \quad (16)$$

The switching vectors v_s can be calculated by adding the integer part of the reference phase voltage $v_i(i_p, 1)$ to the displacement vectors according to (17).

$$v_s^k = v_d^k + v_i^k(i_p^k, 1) = \left[\, v_{s1}^k\ v_{s2}^k\ \cdots\ v_{s(p+1)}^k \,\right] \quad (17)$$

Calculate the switching times t_s corresponding to each switching vector, from the components of v_{fs}, by using (18)-(22).

$$t_s^k = \left[\, t_{s1}^k\ t_{s2}^k\ \cdots\ t_{s(p+1)}^k \,\right] \quad (18)$$

$$\sum_{u=1}^{u=p+1} t_{su}^k = 1 \quad (19)$$

$$t_{s1}^{k} = 1 - v_{fs}^{k}(1,1) \tag{20}$$

$$t_{p+1}^{k} = v_{fs}^{k}(p+1,1) \tag{21}$$

$$t_{j}^{k} = v_{fs}^{k}(j-1,1) - v_{fs}^{k}(j,1) \quad with\, j = 2\ to\ p \tag{22}$$

$$v_{smax}^{k} = max\left(v_{s}^{k}\right) \tag{23}$$

$$B = \begin{cases} 0 & if\ v_{smax}^{k} < 0 \\ 1 & if\ \left(v_{smax}^{k} > 0\right)\ and\ \left(v_{smax}^{k} \neq i_{n}^{k}\right) \\ PWM(t_{s}^{k}) & if\ \left(v_{smax}^{k} > 0\right)\ and\ \left(v_{smax}^{k} = i_{n}^{k}\right) \end{cases} \tag{24}$$

$$H = \begin{cases} 1 & if\ v_{smax}^{k} > 0 \\ 0 & if\ \left(v_{smax}^{k} \leq 0\right)\ and\ \left(v_{smax}^{k} \neq -i_{n}^{k}\right) \\ PWM(t_{s}) & if\ \left(v_{smax}^{k} \leq 0\right)\ and\ \left(v_{smax}^{k} = -i_{n}^{k}\right) \end{cases} \tag{25}$$

The function max(x) (23) is used to find the maximum value of the elements in the switching vector v_s. The signal that controls the IGBT switches of each cell, as shown in Fig. 1b, and is determined by Equation (24) and (25). If the control signal is zero, the equivalent IGBT is in the non-conducting state; if the control signal is 1, the IGBT equivalent is in the conduction state.

In addition to the two states 0 and 1, the IGBT switches with switching time t_s as illustrated in Fig. 3; t_{on} and t_{off} times are calculated by (26) and (27).

$$t_{on} = \sum_{u=1}^{u=p+1} t_{su}\ \ if\ (v_{su}^{k} = v_{smax}^{k}) \tag{26}$$

$$t_{off} = 1 - t_{on} \tag{27}$$

For example, at 0.013s, a four-phase power converter, with each phase consisting of four cells in series, is illustrated with a reference voltage of 380V, frequency of 50Hz. By executing the algorithm in the first cell of phase b, the results are presented as follows (28)-(35). The PWM signal of cell *C_21* at 0.013s is prdesented in Fig. 4 and Table 2.

$$v_r = \begin{bmatrix} -3.0743 & -2.2336 & 3.0743 & 2.2336 \end{bmatrix}^T \tag{28}$$

$$v_i = \begin{bmatrix} -4 & -3 & 3 & 2 \end{bmatrix}^T \tag{29}$$

$$v_f = \begin{bmatrix} 0.9257 & 0.7664 & 0.0743 & 0.2336 \end{bmatrix}^T \tag{30}$$

$$v_{fs} = \begin{bmatrix} 0.9257 & 0.7664 & 0.2336 & 0.0743 \end{bmatrix}^T \tag{31}$$

$$A = \begin{bmatrix} 0 & 0 & 1 & 0 & 0 \end{bmatrix} \tag{32}$$

$$v_d = \begin{bmatrix} 0 & 0 & 1 & 1 & 1 \end{bmatrix} \tag{33}$$

$$v_s = v_d + v_i(2,1) = v_d + (-3) = \begin{bmatrix} -3 & -3 & -2 & -2 & -2 \end{bmatrix} \tag{34}$$

$$t_s = \begin{bmatrix} 0.0743 & 0.1593 & 0.5328 & 0.1593 & 0.0743 \end{bmatrix} \tag{35}$$

B. FLOWCHART OF ALGORITHMS AND CONTROL METHODS

The modulation process for determining the switching pulse and the corresponding switching time in each cell was performed according to the algorithm diagram shown in Fig. 5. At startup, the computation of the cells was executed with the initial conditions listed in Fig. 5(a). In the structures of the decentralized control system in general and in the multilevel multiphase power converter structure proposed in Fig. 2, so that the cell controllers in the system can operate synchronously, it is possible to generate the necessary switching pulses because a synchronous clock is applied to all cells. In the proposed control structure and method, all the active cells have equal roles and can be selected as the primary cell. In this study, cell *C_11* is selected as the primary cell.

In addition to providing synchronous clock to all cells in the system, cell *C_11* also provides amplitude and frequency of modulated voltage to all first cells of each phase (*C_21* to *C_p1*, p is the phase number of the MMPC). For the remaining cells, V_m and F_m will be transmitted to all cells in each phase, respectively, as shown in Fig. 5(b) presentation. The proposed structure and method for MMPC, the system can automatically adjust the operation when adding or removing cells in the same row or any column (make sure the system has at least 3 phases left, in each phase has at least 3 cells left). During operation, the system must ensure that the number of cells in the phases is equal. Depending on the state of the *EN* signal, the specified cell will be active or deactivated as shown in Fig. 5(c). In the case of $EN = 0$, the cell will stop working and follow the diagram as shown in Fig. 5(d), the phase angles transmitted to the cell will be bypassed in rows or columns, switching signal IBGT $B = 1$ and $H = 0$, the cell's contribution to the output voltage is 0V.

When a cell is working, Fig. 5(e) shows an executable program that determines the phase angle of cells in a phase according to expression (1), the total cells in a phase according to equation (2), the angle cell phase according to the vertical distribution based on expression (5), the total phases present in the system according to expression (6), the position

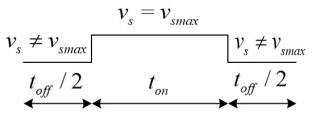


FIGURE 3. Trigger signal.

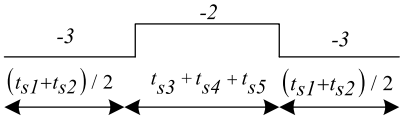


FIGURE 4. Trigger signal of cell *C_21* at 0.013 seconds.

TABLE 2. The switching vector and the switching time of cell C_21 at 0.013 seconds.

Switching vectors	Switching times
v_{s1} = -3	t_{s1} = 0.0743
v_{s2} = -3	t_{s2} = 0.1593
v_{s3} = -2	t_{s3} = 0.5328
v_{s4} = -2	t_{s4} = 0.1593
v_{s5} = -2	t_{s5} = 0.0743

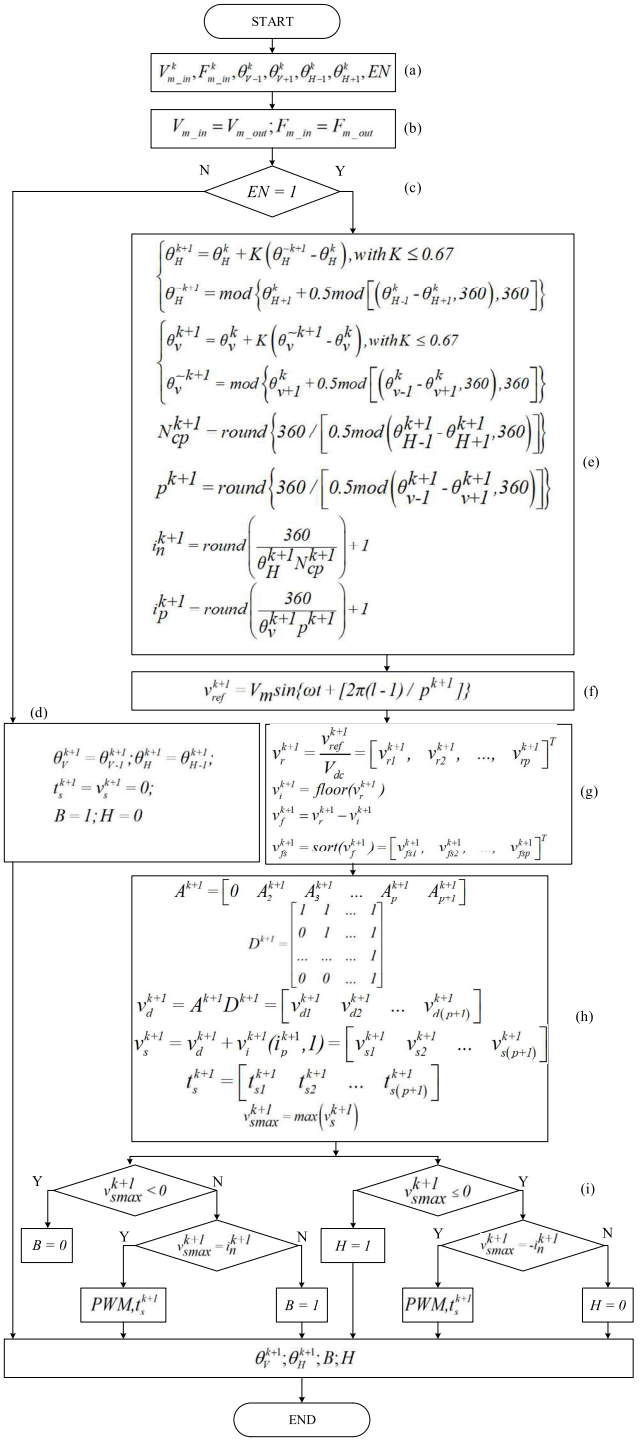


FIGURE 5. Algorithm flowchart of cell.

of the cell in a phase according to equation (3), and the position of the phase in the system according to expression (7). The multiphase reference voltages of the cells were synthesized based on the received signal V_m, F_m, and the phase number, as shown in Fig. 5(f). Fig. 5(g) converts the multilevel calculation problem to a 2-level space according to Equations (9), (10), (11), and (12). The switching vectors and corresponding switching times are calculated according to (13)-(23), as shown in Fig. 5(h). Finally, Fig. 5(i) shows the switching state of each cell's IGBT switch.

TABLE 3. Compare cell execution workload between SVPWM and DSVPWM method.

Parameter	SVPWM	DSVPWM
v_{ref}	v_{ref} is an p-by-1 matrix	v_{ref} is an p-by-1 matrix.
	$N_{c1} = p$	$N_{d1} = p$
v_r	v_r is an p-by-1 matrix	v_r is an p-by-1 matrix
	$N_{c2} = p$	$N_{d2} = p$
v_{fs}	v_{fs} is an $(p+1)$-by-1 matrix	v_{fs} is an p-by-1 matrix
	$N_{c3} = p+1$	$N_{d3} = p$
v_d	P is an $(p+1)$-by-$(p+1)$ matrix	A is an 1-by-$(p+1)$ matrix
	$N_{c4} = (p+1)^2$	$N_{d4} = (p+1)$
	Permutation matrix P $N_{c5} = (p+1)^2$	$N_{d5} = 0$
	v_d is the product of two matrices $(p+1)$-by-$(p+1)$	v_d is the matrix product of 1-by-$(p+1)$ and $(p+1)$-by-$(p+1)$
	$N_{c6} = \frac{7}{8}(p+1)^3$	$N_{d6} = \frac{7}{8}(p+1)^2$
	$N_{c7} = \frac{7}{8}(p+1)^2(p-1) + \frac{9}{2}(p+1)^2$	$N_{d7} = \frac{7}{8}(p+1)(p-1) + \frac{5}{4}(p+1)^2 + \frac{13}{4}(p+1)$
	v_d is an p-by-$(p+1)$ matrix	v_d is a 1-by-$(p+1)$ matrix
v_s	v_s is the sum of two matrices p-by-$(p+1)$	v_s is the sum of two matrices 1-by-$(p+1)$
	$N_{c8} = p(p+1)$	$N_{d8} = p+1$
	v_s is an p-by-$(p+1)$ matrix	v_s is a 1-by-$(p+1)$ matrix
t_s	t_s is an p-by-$(p+1)$ matrix	t_s is a 1-by-$(p+1)$ matrix
	$N_{c9} = p(p+1)$	$N_{d9} = p+1$

The DSVPWM method is essentially a process of modulating the voltage of each cell through separate switching vectors. where m is the ratio of the reference voltage peak amplitude to the V_{dc} voltage of each cell as shown in Equation (36). If the harmonic criteria are not considered, the range of m values in the MMPC satisfies Equation (37). For example, in the case of an MMPC with four cells in series in a phase, m is in the range $0 \le m \le 4$.

$$m = \frac{V_m}{V_{dc}} \tag{36}$$

$$0 \le m \le i_n \tag{37}$$

C. COMPARE EXECUTION WORKLOAD BETWEEN SVPWM AND DSVPWM METHOD

The workload of the cells to be executed when using the DSVPWM method is significantly reduced compared to that when using the SVPWM method for the centralized controller. Usually, centralized controllers using SVPWM compute all vectors and switching times in an overall process. If the number levels and phases of the MMPC increase, this

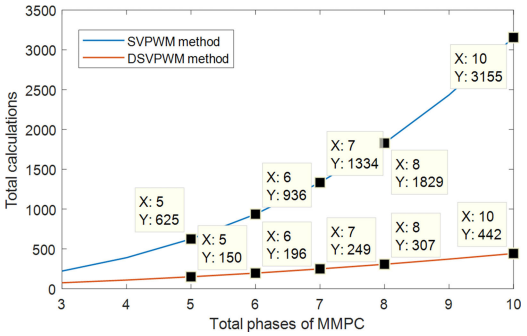


FIGURE 6. Position of four cells in phase a. X is total phase of MMPC; Y is total calculations.

increases the computational volume and processing speed of the microcontrollers. Specifically, for a system with p phases, each phase has n cells, and vector v_d is calculated by multiplying two matrices $(p+1)$-by-$(p+1)$. Compared with the proposed DSVPWM method, v_d obtained by performing the calculation of expression (15) is only matrix multiplication 1-by-$p+1$ by $(p+1)$-by-$(p+1)$. According to Strassen [35], multiplying matrix $A(x,y)$ by matrix $B(y,z)$, the required number of multiplications N_{mul} and additions N_{add} is given by (38) and (39).

$$N_{mul} = \frac{7}{8}xyz \tag{38}$$

$$N_{add} = \frac{7}{8}x(y-2)z + \frac{5}{4}xy + \frac{5}{4}yz + \frac{8}{4}xz \tag{39}$$

The process of finding vectors v_d in the proposed algorithm will have a reduced number of multiplications $(p+1)$ times compared with the centralized control method. The computational volume in the process of generating PWM signals of the central controller and the decentralized method proposed in this study are compared and presented in detail in Table 3. The total calculations of the two methods are summarized by Equation (40) and (41). Where N_c is the total number of calculations when applying the centralized control algorithm, and N_d is the total number of calculations when applying the decentralized control algorithm. Fig. 6 shows the relationship of between N_c and N_d when the total phase of the power converter is in the survey range of 3-10. For example, when $p = 10$, then $N_c = 3155$, $N_d = 442$; the decentralized power converter has 7.14 times reduction in computation volume.

$$N_c = \sum_{i=1}^{i=9} N_{ci} \tag{40}$$

$$N_d = \sum_{i=1}^{i=9} N_{di} \tag{41}$$

III. SIMULATION RESULTS

The DSVPWM algorithm for MMPC was simulated and validated using the MATLAB/Simulink software. The four phases 1, 2, 3, 4, and 9-level output voltage systems are modulated by a 4-phase model, and each phase connected in series consists of 4 cell cascade full bridge. The parameters used to verify the simulation results are presented in Table 4. The simulation results demonstrate and evaluate the general characteristics of the implementation of the SVPWM method for the MMPC sets. Simulation analyses will evaluate the configuration of the system in the case of start-up and dynamic reconstruction when adding or removing a few cells, and evaluate the voltage contribution of each cell to the input voltage.

TABLE 4. Simulation parameters.

Parameter	Symbol	Unit	Value
Output inductor	L	H	0.0001
Load resistor	R	Ω	100
Voltage source of each cell	V_{dc}	V	100
Switching frequency	f_{sw}	Hz	10000
Sampling time	T_s	s	1e-6
Modulation voltage amplitude	V_m	V	380
Modulation frequency	F_m	Hz	50

A. SYSTEM CONFIGURATION TIME

The vectors and the corresponding switching time of each cell are calculated based on the results of the cell positioning process, number of active cells in a phase, number of phases, and position of the phases in the MMPC. The number of time steps required to configure the system successfully depends on the number of cells in a phase and the number of phases present in the MMPC. Algorithms (1)-(4) and (5)-(7) are similar; comparing the total number of phases in the system and the total number of cells in a phase, the system configuration time is calculated for the case where there are more total cells in a loop. The MMPC is built on MATLAB/Simulink, which has four phases: four cells in each phase, the position information of the cells in phase a, and the stability of column 1 with the value established after three steps, as shown in Fig. 7. The time required for all cells to determine the required information tended to increase with the number of active cells. The system configuration time was evaluated by a simulation model of the system with three to 50 active cells in a loop. N_t is the maximum value of N_{cp} and p as expressed in Equation (42). After conducting the approximate linearization according to the quadratic function, Equation (43) presents the number of iterations required for the system to be successfully configured by linearizing the survey data according to the cubic function; the deviation of the linearization function has a maximum value of 2.5478. Fig. 8 shows the number of time steps required for the system to determine the location and total number of cells. The time for the system to establish cell location information and the total cells was calculated according to equation (44).

$$N_t = max\left(N_{cp}, p\right) \tag{42}$$

$$N_c = 0.0010533N_t^3 + 0.38422N_t^2 - 1.5647N_t + 3.469 \tag{43}$$

$$T_{configuration} = N_c.T_s \tag{44}$$

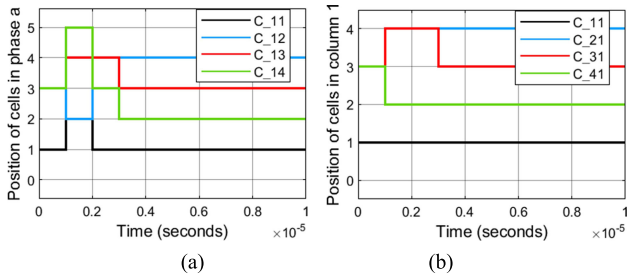


FIGURE 7. Position of the four cells in phase a and in column 1.

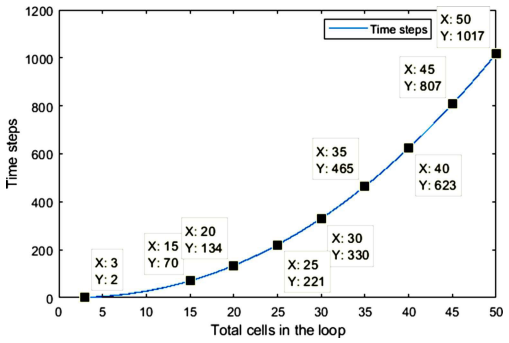


FIGURE 8. The number of time steps for cell's position to be stable. X: the total cells in the loop; Y: the number of time steps.

B. EVALUATE THE DYNAMIC RECONFIGURATION PROCESS

Fig. 9 shows the operating assumption of the MMPC. When all the cells of the four phases in the system are active, after three steps, the position of cells in one phase and the position of the phases have reached a steady state. From the simulation results shown in Fig. 10, cell *C_11* has a position of 1, cell *C_12* has a position of 4, cell *C_13* has a position of 3, and cell *C_14* has a position of 2 in phase *a* of the power converter. The reference voltage is 380V, the modulation factor $m = 3.8$, and the reference frequency is 50Hz, the PWM signal of the cells in phase *a* corresponding to the determined location is presented in Fig. 11. The positions of cells in the phases are algorithmically (1), (2), and (3) position-adjusted. During the operation, when adjusting the system structure by adding or removing a few cells, the teta angle of each cell was adjusted between 0^o and 360^o. This allows all cells in the phases to be able to customize their position in the overall single phase, but still ensures joint division of the voltage contribution to the load as required. If there are four cells in a phase, when starting cell *C_11* has a position of 1, but maybe under a different operating condition, cell *C_11* will have a value other than 1. The maximum number of levels of the output voltage was 9. In this study, the phase position does not change during the operation; this is achieved by fixing the teta angle of the first cell in a column to zero when implementing algorithms (4), (5), and (6).

With the proposed DSVPWM modulation method, the system must always ensure that the number of cells in each phase is equal. The structure of decentralized controlled power converters can be flexibly adjusted. With the proposed

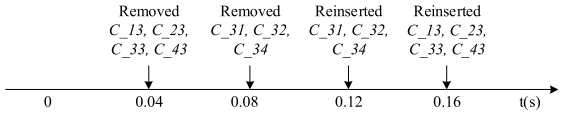


FIGURE 9. Simulation process.

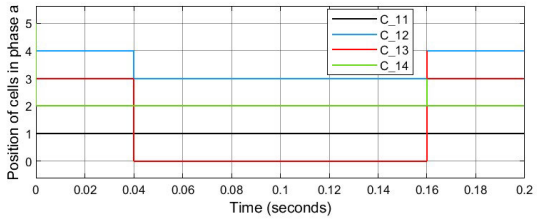


FIGURE 10. Position of four cells in phase a.

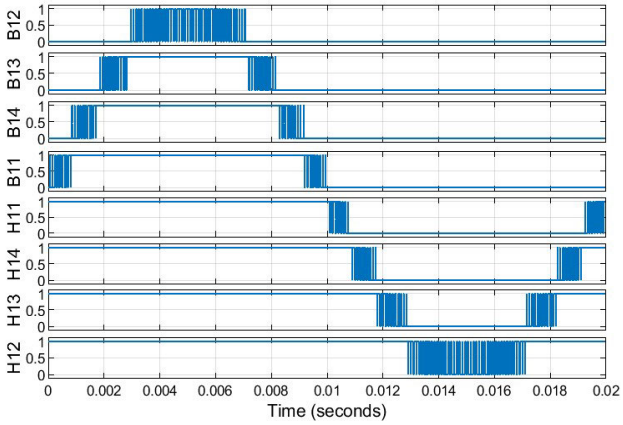


FIGURE 11. The PWM signals of cells in phase a for one cycle.

decentralized structure, any cell in the system is established to communicate with four neighboring cells. For example, cell *C_22* communicates with four cells: *C_12*, *C_23*, *C_21*, and *C_32*. When some cells are added or removed from the system, the power converter does not need to stop working; thus, the old communications are adjusted, and new communications are established. In this study, when a cell stops working, the signal to that cell is bypassed horizontally and vertically to verify the ability to self-adjust the dynamic structure. The DSVPWM method for MMPC is considered operable when the cells self-adjust their positions in phase and in columns, precisely modulate the required PWM signals, and precisely modulate the reference voltage. Fig. 12-14 presented the response of position, voltage, and load current in the case of the simulated system structure adjusted according to Fig. 9. Specifically:

- At the time 0.04 seconds, an assumption is established with the *EN* signal of the cells in column 3 as *C_13*, *C_23*, *C_33*, and *C_43* being zero. In each phase, the remaining three cells operated. For example, in phase 1, three cells, *C_11*, C_12, and *C_14*, automatically adjust their position, as shown in Fig. 12. Similar results were obtained in phases 2, 2, and 4 of the system. Because the loops determine the

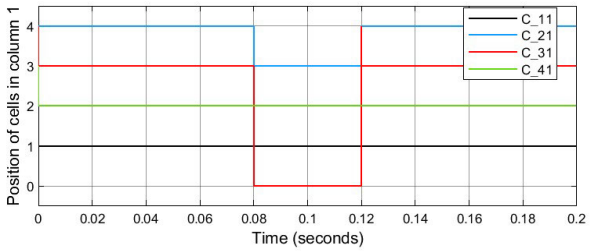


FIGURE 12. Position of cells in column 1.

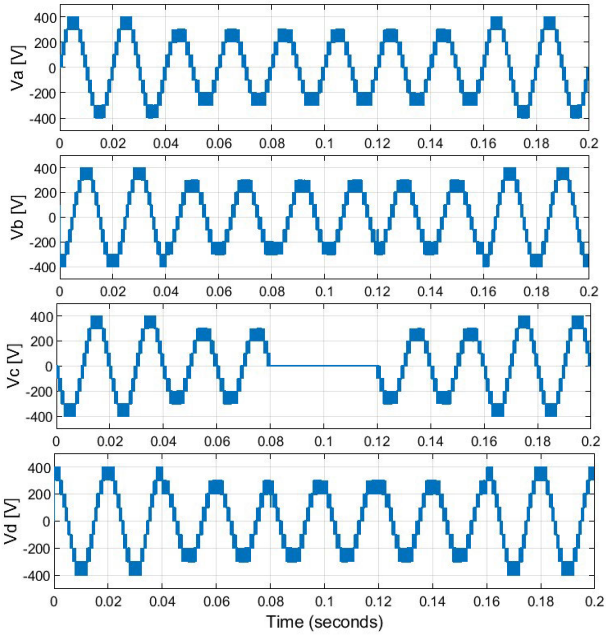


FIGURE 13. Output voltage.

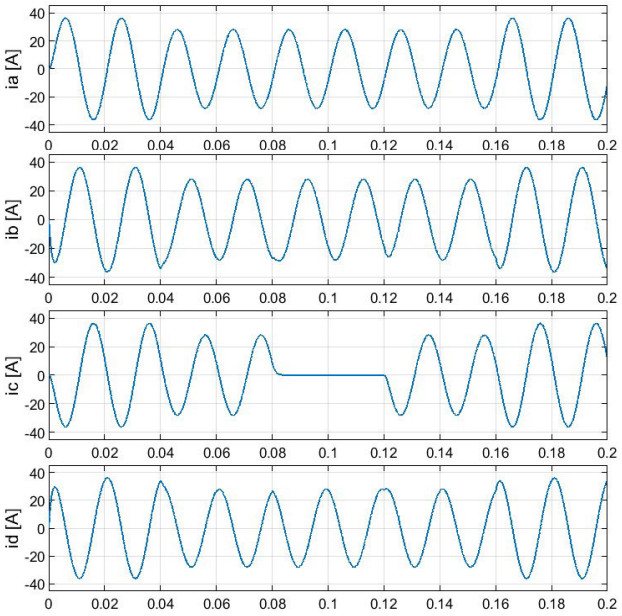


FIGURE 14. Load current.

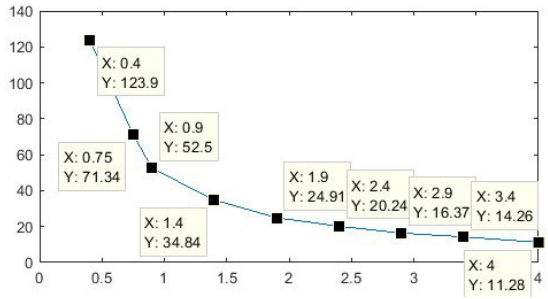


FIGURE 15. Relationship THD and modulation index; X: the modulation index; Y: the THD value.

cell's position in the phases independently of each other, the cell positions within the phases have a random value in the population of a phase. The positions of cells *C_11* is 1, *C_12* has the position of 3, *C_14* has the position of 2. The configuration of the column-based loops does not change; therefore, the column-based cell location information does not change. The reference voltage peak amplitude automatically adjusted by the system was 300V, the modulation index was 3. The output phase voltage is the voltage contribution of the three active cells, the output four phase voltage comprises seven levels.

- The phase number change of the power converter is evaluated in the period from 0.08s to 0.12s. For example, phase c of the system including 3 cells *C_31*, *C_32*, *C_34* is removed from the system at 0.08 seconds; This problem leads to a loop that determines the total number of phases, the positions of cells in the same column are adjusted. Figure 12 shows the new position of cell *C_11* as 1, cell position *C_21* as 3, cell position *C_41* as 2, and the discarded cell *C_31* at position 0. In this phase, the loops of phases 1, 2 and 4 do not change; therefore, the cell position information in a phase will not change; The voltages of phases *a*, *b*, and *d* have seven response levels according to the reference signal; the voltage of phase *c* voltage is 0. At the end of the cycle, at 0.12 seconds, cells in phase 3 are restored to operation, vertical position information is reset, and phase *c* voltage is restored to the correct voltage reference.

- At 0.16 seconds, the cells in column 3 are reinserted. The position of the cells in the horizontal direction of all phases was adjusted, the output voltage ensured the contribution of four cells in each phase, and the output voltage reached nine levels.

Fig. 15 shows the relationship between the THD value and the modulation index. The survey evaluated the sinusoidal distortion of the voltage in the frequency range of 0 to 20 kHz and the output voltage was of good quality, meeting the grid connection requirements.

C. EVALUATION OF POWER LOSS OF THE INVERTER

In order to have a more general assessment of the proposals, this study examined the power loss and compared it with classical methods (CPWM and SVPWM). Total power loss is mainly due to two components: switching loss and conduction loss. Survey data obtained on the thermal model of Plecs

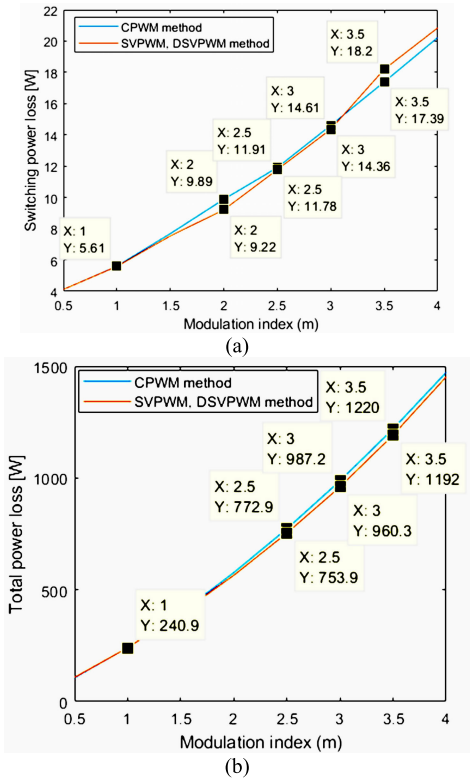


FIGURE 16. Power loss analysis of CPWM, SVPWM and DSVPWM method of four phases, nine level cascade inverter; a) switching power loss; b) total power loss. X: the modulation index; Y: the power loss.

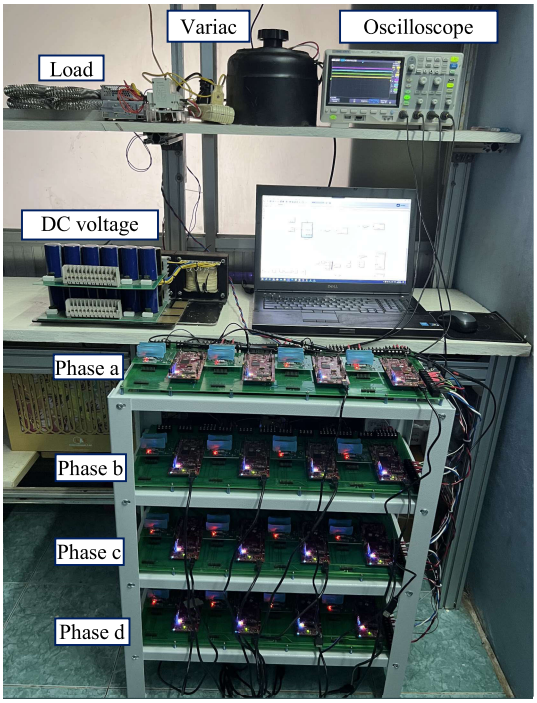


FIGURE 17. Experimental prototype of MMPC with DSVPWM method.

software shows that the power losses caused by switching and conduction have similar values with the SVPWM and DSVPWM methods. The IGBT component investigated is IGW25N120H3 from Infineon manufacturer. And the total power loss of the proposed DSVPWM method is lower than that of the CPWM method. The detailed comparison results are shown in Fig. 16, Fig. 16a presented the switching loss and Fig. 16b presented the total power loss of the inverter according to the modulation index.

TABLE 5. Experimental parameters.

Symbol	Parametter	Unit	Value
V_{dc}	DC voltage	V	30
R	Load resistor	Ω	100
L	Output inductor	H	0.0036
f_{sw}	Switching frequency	kHz	10
T_s	Sampling time	s	5e-5
m	Modulation index		3.4
F_m	Frequency modulation	Hz	50

IV. EXPERIMENTAL RESULTS

The proposals for the configuration, control method, and DSVPWM modulation algorithm are verified by a low-power experimental model. As shown in Fig. 17, the settings for the experiment include control cells, DC power, and load. Experimental parameters of MMPC with algorithm DSVPWM are shown in Table 5; The DC voltage of each cell was 30V, and a resistor with a value of 100Ω connected in series with inductor L with an inductance of 0.0036H was used as the load for each phase.

The experimental model built to evaluate the proposed algorithm included four phases, each with four cells. With such a structure, a comprehensive assessment of the structure and control methods presented in Section III is conducted. Fig. 18 shows the control connection of the MMPC using the DSVPWM method. Each cell included the following:

- One power driver circuit using MORNSUN QP12W08S-37.

- One cascade full bridge circuit consisting of 4 IGBTs using GW40N120KD.

- A TMS320F28379D DSP was used as the cell controller. The control program of the cells was built on the platform of MATLAB/Simulink software; the Code Composer Studio program was used to compile and load programs for DSPs.

The number and function of the signal pins used by each cell are shown in Table 6. Cells exchange information horizontally and vertically with neighboring cells via asynchronous serial communication (SCI) protocol. In the proposed structure, *C_11* is the primary cell. By creating and using signal buses according to SCI standards, cells can communicate with each other with the least number of communication channel commands, thereby reducing signal loss during transmission. This is a significant improvement over the communication methods used in this study [30].

Cell *C_11* transmits the amplitude and frequency reference signal of the voltage to be modulated through the cells in column 1 of cells *C_12*, *C_13*, *C_14*. To synchronize the voltage reference signal, the synchronous clock generated from the GPIO 04 pin of cell *C_11* is propagated to the GPIO 15 pin of all the remaining cells, including itself in the MMPC.

TABLE 6. Function pins of DSP.

Symbol	Pin on DSP	Function
EN	GPIO 25	Enable
Communication in a phase	SCIB (GPIO 18)	Receive θ_{H_n+1} angle signal from front cell in the same phase
	SCIB (GPIO 19)	Transmit the signals to the next cell in the same phase: - Modulation voltage amplitude V_m - Frequency modulation voltage F_m - θ_{H_n} angle
	SCIA (GPIO 9)	Transmit the θ_{H_n} angle signal to the rear cell in the same phase
	SCIA (GPIO 8)	Receive signals transmitted from the rear cell in the same phase: - Modulation voltage amplitude V_m - Frequency modulation voltage F_m - θ_{H_n-1} angle
Communication in a column	SCID (GPIO 105)	Receive signals transmitted from the front cell in the same column: - Modulation voltage amplitude V_m - Frequency modulation voltage F_m - θ_{V_n+1} angle
	SCID (GPIO 104)	Transmit the θ_{V_n} angle signal to the front cell in the same column
	SCIC (GPIO 56)	Transmit the signals to the rear cell in the same column: - Modulation voltage amplitude V_m - Frequency modulation voltage F_m - θ_{V_n} angle
	SCIC (GPIO 139)	Receive θ_{V_n-1} angle signal from rear cell in the same column
clk_{in}	GPIO 14	Received synchronous clock pulse PWM from primary cell
	GPIO 15	Received synchronous clock pulse of the reference voltage from primary cell
clk_{out}	GPIO 06	Transmitted synchronous clock pulse PWM to others cell
	GPIO 04	Transmitted synchronous clock pulse of the reference voltage to others cell
B_{pn}	GPIO 0	The control signal IGBT *B* of cell *pn*
B_{pn}_NOT	GPIO 1	The control signal IGBT *B_NOT* of cell *pn*
H_{pn}	GPIO 2	The control signal IGBT *H* of cell *pn*
H_{pn}_NOT	GPIO 3	The control signal IGBT *H_NOT* of cell *pn*

The cells calculate the appropriate switching pulses once the voltage reference signal is synthesized, based on information about the specified system architecture. To synchronize the PWM signal of the cells, a synchronization pulse generated from the GPIO 06 pin of cell *C_11* is transmitted to the GPIO 14 pin of all remaining cells, including itself in the MMPC system.

A. STEADY-STATE OPERATION

The results were analyzed and evaluated when a full 4-cell MMPC power converter was activated. At the local controllers of each cell, the analog output signal pins DACA and DACB were interpolated to observe the position of the

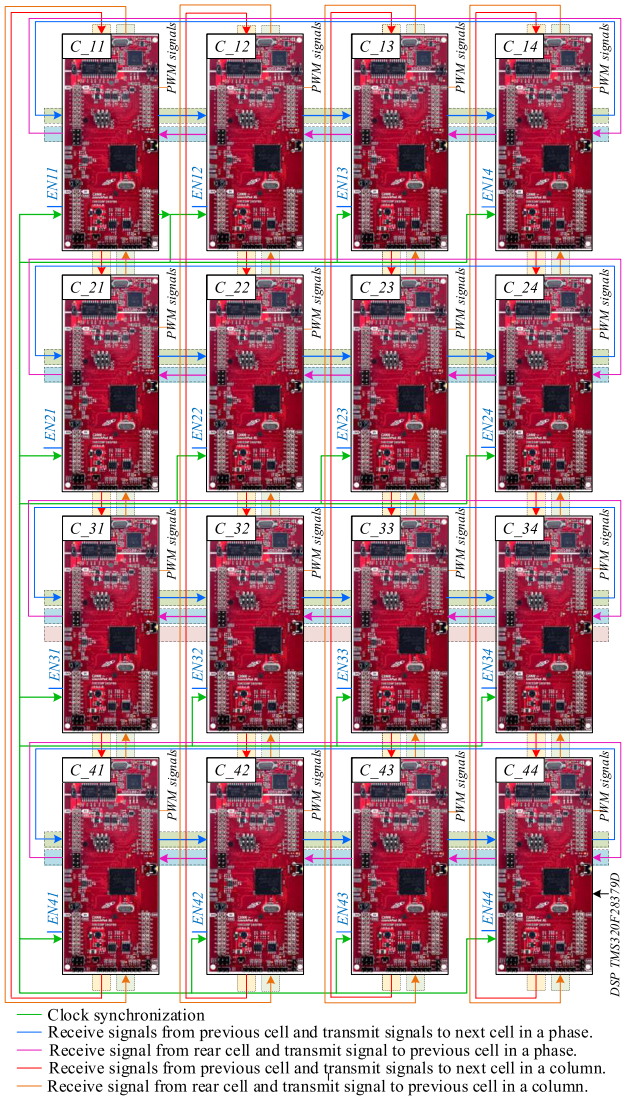
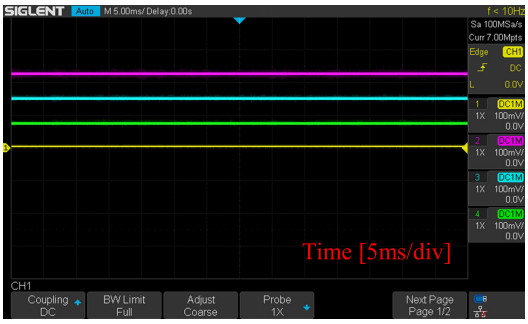
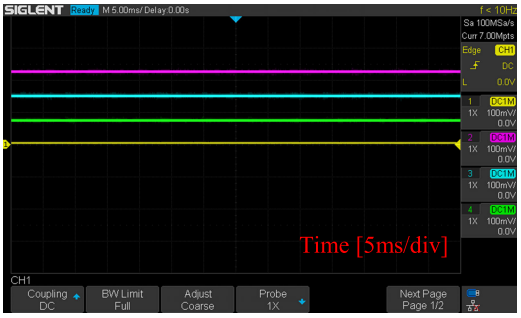


FIGURE 18. Establish experimental communication between cells in MMPC using DSVPWM method.

corresponding cell in the phases and columns. Fig. 19 shows the position arrangement of the cells in phase *a* (Fig. 19(a)) and column 2 (Fig. 19(b)). The positions of cells *C_11*, *C_12*, *C_13*, and *C_14* in phase *a*: *cell_11* is at position 1, cell *C_12* is at position 4, cell *C_13* is at position 3, cell_14 is at position 2. The positions of cells *C_12*, *C_22*, *C_32*, and *C_42* in column 2; cell *C_12* at position 1; cell_22 at position 4; cell *C_32* at position 3; and cell *C_42* at position 2. Communication between cells is performed using SCI communication blocks built in the MATLAB/Simulink library [36], and the study did not consider the data transmission and reception speeds of the proposed methods. With the experimental model method and structure, the cell controllers exchange information and reach a stable state, the cells will locate themselves in rows and columns; With the proposals in this article, locating cells in the structure is the basis for cells to synthesize their own vectors and switching times. The modulated PWM control signal for each cell is shown in Fig. 20. The four corresponding

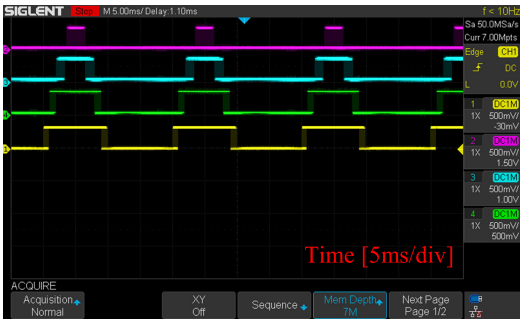


(a)

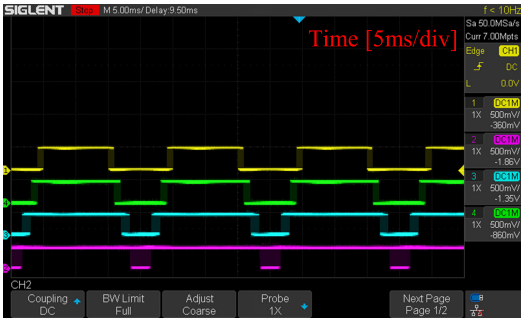


(b)

FIGURE 19. Position of cells in MMPC using DSVPWM method; a) Position of four cells *C_11*, *C_12*, *C_13*, *C_14* in phase a (yellow color: *C_11*, purple color: *C_12*, blue color: *C_13*, green color: *C_14*); b) Position of four cells *C_12*, *C_22*, *C_32*, *C_42* in column 2 (yellow color: *C_12*, purple color: *C_22*, blue color: *C_32*, green color: *C_42*).



(a)



(b)

FIGURE 20. PWM signals of cells *C_11*, *C_12*, *C_13*, *C_14* using DSVPWM method (yellow color: *C_11*, purple color: *C_12*, blue color: *C_13*, green color: *C_14*); a) PWM B signals; b) PWM H signals.

PWM *B* signal outputs of the GPIO 0 are shown in Fig. 20(a). The four corresponding PWM *H* signal outputs of GPIO 2 are

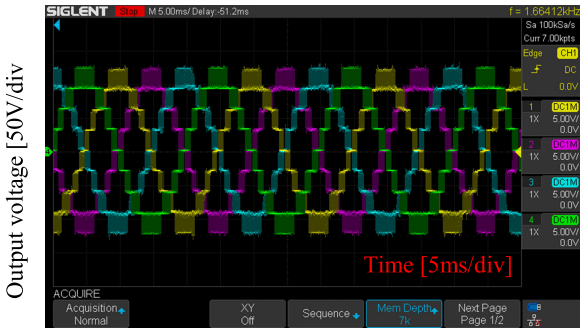
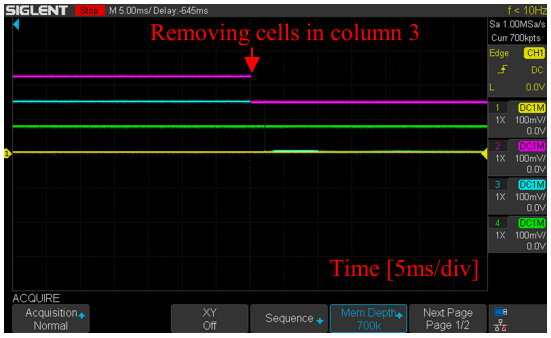
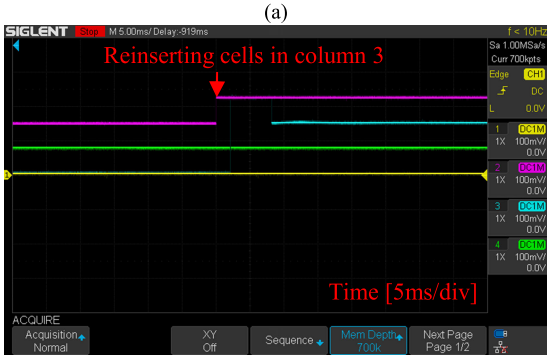


FIGURE 21. Output phase voltage waveform of MMPC using DSVPWM method when the system has 4 × 4 cells.



(a)



(b)

FIGURE 22. Position of cells in phase a of MMPC using DSVPWM method (yellow color: *C_11*, purple color: *C_12*, blue color: *C_13*, green color: *C_14*); a) when removing cells in column 3; b) when reinserting the cells in column 3.

shown in Fig. 20(b). The external DC power supply voltage of each cell is 30V, which helps reduce the voltage current capacitor balancing problem in some applications, meaning the single-level voltage of the inverter is also 30V; With a high modulation factor $m = 3.4$, the control algorithm takes full advantage of the voltage of all 4 cells; As a result, the output voltage reaches 9 levels; The voltage between levels is 30V as shown in Fig. 21.

By comparison to centralized controllers, the decentralized control structure and method proposed in this study requires the establishment of column and row control communications. Simulation settings and original experiments show that the cell-to-cell communication process can be easily deployed and operated. Expanding the number of levels and phases of MMPCs will reduce the complexity of

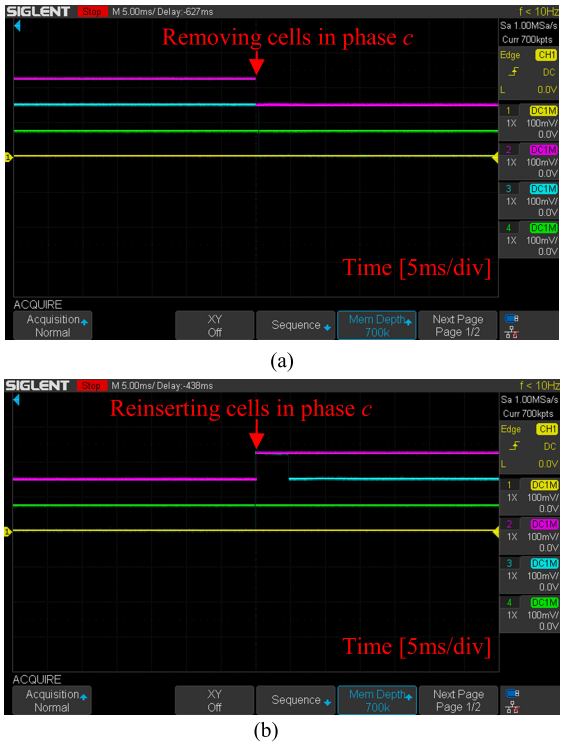


FIGURE 23. In case column 3 has been removed, position the cells in column 2 of the MMPC using the DSVPWM method (yellow color: *C_12*, purple color: *C_22*, blue color: *C_32*, green color: *C_42*); a) when removing cells in phase *c*; b) when reinserting the cells in phase *c*.

decentralized controllers compared to central controllers in connection and control.

B. CONVERTER RECONFIGURATION

Within this experimental limit, the removal or activation a cell is performed via the *EN* signal pin (GPIO 25) of each cell. By emulating a cell that stops working, the row phase angles of the incoming cell (SCIB GPIO 18 and SCIA GPIO 8) are bypassed via the output signal pin (SCIA GPIO 9 and SCIB GPIO 19), and the column phase angles incoming transmissions (SCID GPIO 105 and SCIC GPIO 56) will be bypassed via the output pins (SCID GPIO 104 and SCIC GPIO 139).

The ability to automatically adjust to adapt to the remaining number of activated cells in the MMPC was tested in turn according to the hypothetical process: the system operates with all cells; remove cells *C_13*, *C_23*, *C_33*, *C_43*; remove cells *C_31*, *C_32*, *C_34*; restore operation of cells *C_31*, *C_32*, *C_34*; and restore operation for cells *C_13*, *C_23*, *C_33*, *C_43*. The total active cells and the position of active cells in each row and column are automatically recalibrated as shown in Fig. 22 and Fig. 23, where the position and total active cells are interpolated from the phase angle in rows and columns using algorithms (1) and (5). In this study, the coefficient K was chosen to be 0.66 for both the row and column phase angle interleaving algorithms. The cells in the row require approximately 2ms to establish a new steady state

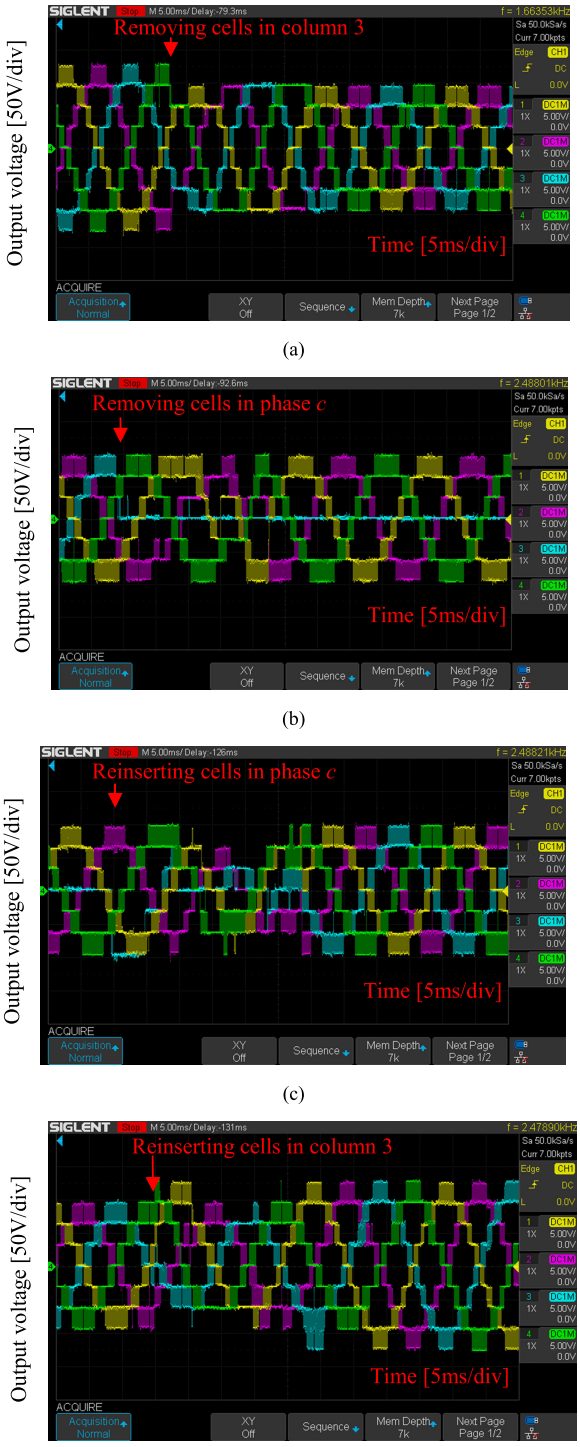


FIGURE 24. Output phase voltage when changing structure (yellow color: phase *a*, purple color: phase *b*, blue color: phase *c*, green color: phase *d*; a) when removing cells in column 3 of the system has 4 cells in a phase; b) when removing cells in phase *c* of the system has 3 cells in a phase; c) when reinserting cells in phase *c* of the system has 3 cells in a phase; d) when reinserting cells in column 3 of the system has 3 cells in a phase.

when the cell is removed as shown in Fig. 22(a). Meanwhile, the system required 8ms for the cells in phase *a* to recover, as shown in Fig. 22(b).

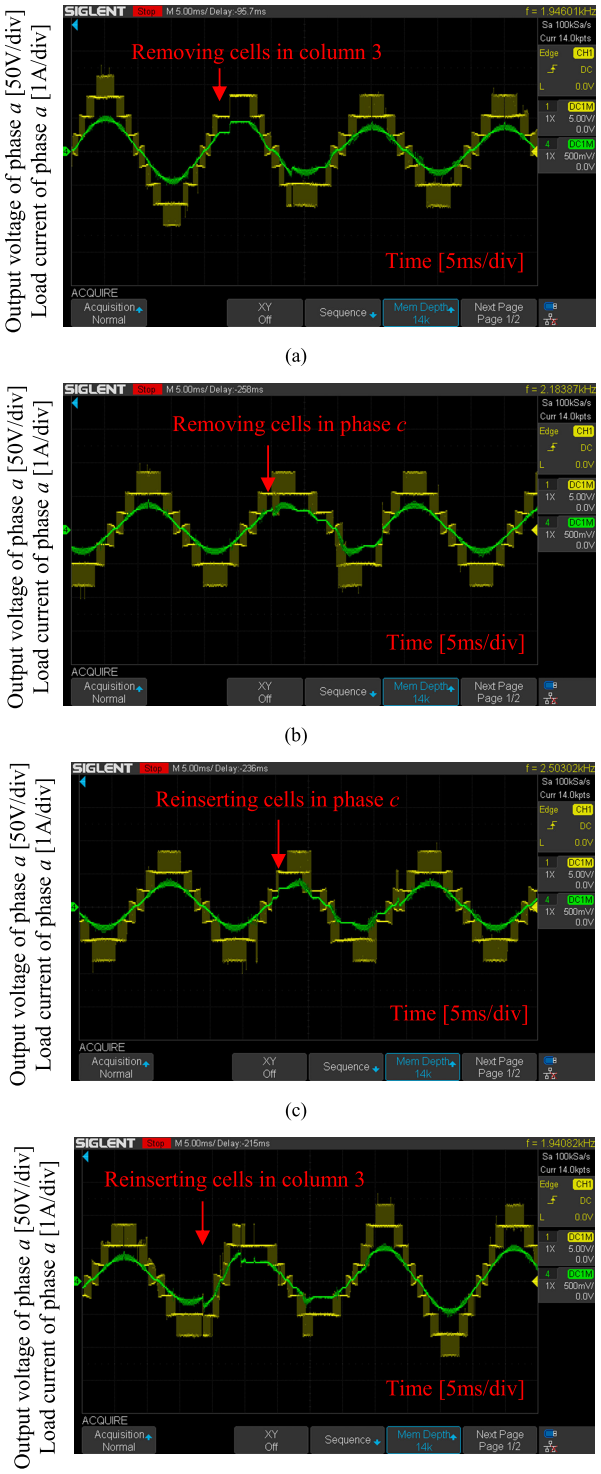


FIGURE 25. Output voltage and load current of phase a when changing structure (yellow color: output voltage of phase a; green color: load current; a) when removing cells in column 3 of the system has 4 cells in a phase; b) when removing cells in phase c of the system has 3 cells in a phase; c) when reinserting cells in phase c of the system has 3 cells in a phase; d) when reinserting cells in column 3 of the system has 3 cells in a phase.

When the cells in column 3 are removed, Fig. 23 shows the repositioning process of cells in column 2 when phase

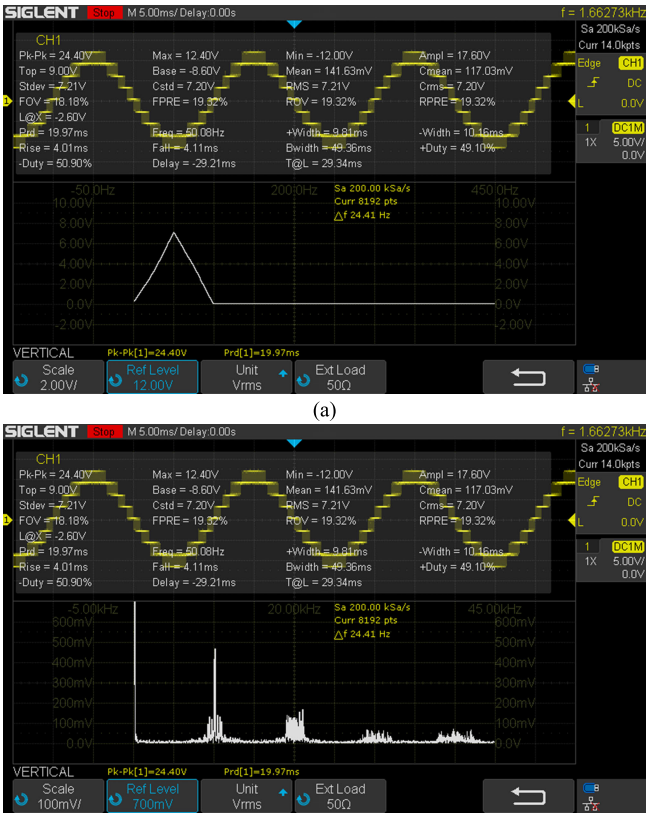


FIGURE 26. FFT analysis of single-phase voltage: (a) spectrum of 9 first harmonics; (b) spectrum of 900 harmonics.

c is removed and operation is restored; According to the measurement results on the oscilloscope, the transient times are 0.5ms and 4.5ms respectively.

Fig. 24 shows the four-phase voltage waveform of the inverter when changing the MMPC structure, which was conducted by changing one column or row at a time. According to (37) to limit the modulation coefficient according to the number of activated cells in a phase, after removing the 3rd cell of each phase, the remaining three cells are activated, and based on the total number of active cells in the row that the primary cell aggregates, cell *C_11* automatically adjusts the modulation factor to a maximum value of 3 (within the limits of this test); the output voltage has seven levels; the voltage at each level is 30V.

When deactivated, the voltage of the cell contributing to the load was 0V, and the control signal of the GPIO signal pins 0 and 2 of the cells was 0. As shown in Fig. 24(a) shows, because the cells in column 3 stop operating, the 4-phase voltage is changed from nine levels to seven levels after about 27ms. The 4-phase voltage of the inverter is modulated with a maximum modulation coefficient corresponding to three cells of each phase. In this experiment, the modulation coefficient was set as 3. The voltage phase-difference angle between the four branches did not change. The corresponding phase-difference angle when there are four cells in one phase is 90°. In the case of adjusting each phase with

three active cells, Fig. 24(b) shows the voltage adjustment of the four phases when the cells of phase *c* stop operating, which requires a time of 23ms. The phase voltages were maintained at seven levels, the voltage levels were stable at 30V, and the voltage phase difference angle between phases was adjusted to 120°, satisfying formula (8). Meanwhile, the process of restoring the operation of phase c and column 3, requires a period of 30ms as shown in Fig. 24(c) and Fig. 24(d), respectively. Experiments show that the voltage of the inverter phases can be automatically adjusted according to the total number of activated cells in the phases and columns. Fig. 25 shows the voltage and current of phase *a* in the case of a regulated inverter structure.

For decentralized power converters, the cells automatically determine the voltage contribution to the load voltage synthesis, which is made possible by switching the PWM signals of each self-aggregating cell. This voltage- dispersion contribution can be one of the factors affecting the output voltage THD index. Therefore, the output voltage THD index corresponding to the control method and structure of the decentralized power converters must be paid attention and considered. The results of the single-phase voltage fast Fourier transform (FFT) analysis of the load were shown on a Siglent SDS1104X oscilloscope. Analytical results were evaluated in the frequency range of 0 to 450Hz and 0 to 45kHz was shown in Fig. 26. The results of the spectrum analysis at a frequency 50Hz, voltage had an effective value 72.1V and a frequency of 50.08Hz. Comparing the modulation coefficient and reference frequency, the output voltage deviation corresponds to -0.035% amplitude and 0.16% frequency. At a switching frequency of 10kHz, the harmonics have an amplitude of 4.6V and gradually decrease at frequencies that are multiples of the 10kHz frequency.

V. CONCLUSION

This study has used the SVPWM method for decentralized control of multilevel multiphase power converters. The cells exchanged with neighboring cells, correctly calculated vectors and corresponding switching times in the case of a stable configuration or dynamically adjusted as needed. The proposed method and structure show that the process of searching for switching vectors and the switching time is faster than when using a centralized controller. By verifying the simulation and experimental results, the proposed method can be considered a general method for multilevel, multiphase modulation of power converters. The highlight of the proposal is that it is possible to modulate the output voltage with any number of levels and phases to meet diverse applications such as multiphase motor control and energy conversion on electrical systems.

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REFERENCES

[1] Y. Jin, Q. Xiao, C. Dong, H. Jia, Y. Mu, B. Xie, Y. Ji, S. K. Chaudhary, and R. Teodorescu, "A novel submodule voltage balancing scheme for modular multilevel cascade converter—Double-star chopper-cells (MMCC-DSCC) based STATCOM," *IEEE Access*, vol. 7, pp. 83058–83073, 2019, doi: 10.1109/ACCESS.2019.2924609.

[2] D. Jiao, Q. Huang, and A. Q. Huang, "Evaluation of medium voltage SiC flying capacitor converter and modular multilevel converter," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Oct. 2020, pp. 4386–4392, doi: 10.1109/ECCE44975.2020.9235758.

[3] V. Hofmann and M.-M. Bakran, "A capacitor voltage balancing algorithm for hybrid modular multilevel converters in HVDC applications," in *Proc. IEEE 12th Int. Conf. Power Electron. Drive Syst. (PEDS)*, Dec. 2017, pp. 691–696, doi: 10.1109/PEDS.2017.8289176.

[4] P. Hu, R. Teodorescu, S. Wang, S. Li, and J. M. Guerrero, "A currentless sorting and selection-based capacitor-voltage-balancing method for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1022–1025, Feb. 2019, doi: 10.1109/TPEL.2018.2850360.

[5] A. Ghazanfari and Y. A. I. Mohamed, "A hierarchical permutation cyclic coding strategy for sensorless capacitor voltage balancing in modular multilevel converters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 576–588, Jun. 2016, doi: 10.1109/JESTPE.2015.2460672.

[6] H. Liu, K. Ma, P. C. Loh, and F. Blaabjerg, "A sensorless control method for capacitor voltage balance and circulating current suppression of modular multilevel converter," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2015, pp. 6376–6384, doi: 10.1109/ECCE.2015.7310553.

[7] W. Li, L.-A. Grégoire, and J. Bélanger, "A modular multilevel converter pulse generation and capacitor voltage balance method optimized for FPGA implementation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 5, pp. 2859–2867, May 2015, doi: 10.1109/TIE.2014.2362879.

[8] F. Sasongko and H. Akagi, "Low-switching-frequency operation of a modular multilevel DSCC converter with phase-shifted rotating-carrier PWM," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5058–5069, Jul. 2017, doi: 10.1109/TPEL.2016.2608912.

[9] S. Busquets-Monge, R. Griñó, J. Nicolas-Apruzzese, and J. Bordonau, "Decoupled DC-link capacitor voltage control of DC–AC multilevel multileg converters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 3, pp. 1344–1349, Mar. 2016, doi: 10.1109/TIE.2015.2495295.

[10] S. Kouro, M. Angulo, J. Rodriguez, and J. Pontt, "Multicarrier PWM with DC-link ripple feedforward for multilevel inverters," in *Proc. 12th Int. Power Electron. Motion Control Conf.*, Aug. 2006, vol. 23, no. 1, pp. 234–239, doi: 10.1109/EPEPEMC.2006.4778405.

[11] K. Li and C. Zhao, "New technologies of modular multilevel converter for VSC-HVDC application," in *Proc. Asia–Pacific Power Energy Eng. Conf.*, Mar. 2010, pp. 1–4, doi: 10.1109/APPEEC.2010.5449237.

[12] T. Trivedi, P. Agarwal, R. Jadeja, and P. Bhatt, "FPGA based implementation of simplified space vector PWM algorithm for multilevel inverter fed induction motor drives," *Int. J. Electr. Comput. Eng.*, vol. 9, no. 8, pp. 922–927, 2015, doi: 10.5281/zenodo.1108909.

[13] E. A. R. E. Ariff, O. Dordevic, and M. Jones, "A space vector PWM technique for a three-level symmetrical six-phase drive," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8396–8405, Nov. 2017, doi: 10.1109/TIE.2017.2703668.

[14] N.-Y. Dai, M.-C. Wong, Y.-H. Chen, and Y.-D. Han, "A 3-D generalized direct PWM algorithm for multilevel converters," *IEEE Power Electron Lett.*, vol. 3, no. 3, pp. 85–88, Sep. 2005, doi: 10.1109/LPEL.2005.855112.

[15] M. B. Booin and M. Cheraghi, "THD minimization in a five-phase five-level VSI using a novel SVPWM technique," in *Proc. 10th Int. Power Electron., Drive Syst. Technol. Conf. (PEDSTC)*, Feb. 2019, pp. 285–290, doi: 10.1109/PEDSTC.2019.8697810.

[16] F. Patkar, E. Levi, and M. Jones, "A six-phase multilevel space vector PWM algorithm for a dual-inverter supplied drive," in *Proc. 6th IET Int. Conf. Power Electron., Mach. Drives (PEMD)*, Mar. 2012, pp. 1–5, doi: 10.1049/cp.2012.0245.

[17] K. Marouani, L. Baghli, D. Hadiouche, A. Kheloui, and A. Rezzoug, "Discontinuous SVPWM techniques for double star induction motor drive control," in *Proc. 32nd Annu. Conf. IEEE Ind. Electron.*, Nov. 2006, pp. 902–907, doi: 10.1109/iecon.2006.347288.

[18] J. Lyu, W. Hu, F. Wu, K. Yao, and J. Wu, "A neutral-point voltage balance controller for the equivalent SVPWM strategy of NPC three-level inverters," *J. Power Electron.*, vol. 16, no. 6, pp. 2109–2118, Nov. 2016, doi: 10.6113/jpe.2016.16.6.2109.

[19] A. Dekka, B. Wu, N. R. Zargari, and R. L. Fuentes, "A space-vector PWM-based voltage-balancing approach with reduced current sensors for modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2734–2745, May 2016, doi: 10.1109/TIE.2016.2514346.
[20] V. Padhee, A. K. Sahoo, and N. Mohan, "SVPWM technique with varying DC-link voltage for common mode voltage reduction in an indirect matrix converter," in *Proc. IEEE Energy Convers. Congr. Exposit. (ECCE)*, Sep. 2015, pp. 875–881, doi: 10.1109/ECCE.2015.7309780.
[21] O. Lopez, J. Alvarez, J. Doval-Gandoy, F. Freijedo, A. Nogueiras, and C. M. Penalver, "Multilevel multiphase space vector PWM algorithm applied to three-phase converters," in *Proc. 34th Annu. Conf. IEEE Ind. Electron.*, Nov. 2008, vol. 55, no. 5, pp. 3290–3295, doi: 10.1109/IECON.2008.4758487.
[22] J. Alvarez, Ó. Lopez, F. D. Freijedo, and J. Doval-Gandoy, "Digital parameterizable VHDL module for multilevel multiphase space vector PWM," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 3946–3957, Sep. 2011, doi: 10.1109/TIE.2010.2100334.
[23] B. Xu, H. Tu, Y. Du, H. Yu, H. Liang, and S. Lukic, "A distributed control architecture for cascaded H-bridge converter with integrated battery energy storage," *IEEE Trans. Ind. Appl.*, vol. 57, no. 1, pp. 845–856, Jan. 2021, doi: 10.1109/TIA.2020.3039430.
[24] J. Liu, W. Yao, Z. Lu, L. Du, and Y. Ji, "A distributed control structure and synchronization method for complex converter based on CAN," in *Proc. IEEE Southern Power Electron. Conf. (SPEC)*, Dec. 2017, pp. 1–6, doi: 10.1109/SPEC.2017.8333646.
[25] M. Sinha, J. Poon, B. B. Johnson, M. Rodriguez, and S. V. Dhople, "Decentralized interleaving of parallel-connected buck converters," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4993–5006, May 2019, doi: 10.1109/TPEL.2018.2868756.
[26] S. Dutta, R. Mallik, B. Majmunovic, S. Mukherjee, G.-S. Seo, D. Maksimovic, and B. Johnson, "Decentralized carrier interleaving in cascaded multilevel DC-AC converters," in *Proc. 20th Workshop Control Model. Power Electron. (COMPEL)*, Jun. 2019, pp. 1–6, doi: 10.1109/COMPEL.2019.8769699.
[27] H. Gao and Y. Wang, "On phase response function based decentralized phase desynchronization," *IEEE Trans. Signal Process.*, vol. 65, no. 21, pp. 5564–5577, Nov. 2017, doi: 10.1109/TSP.2017.2733452.
[28] S. I. Seleme, L. Grégoire, M. Cousineau, and P. Ladoux, "Modular control with carrier auto-interleaving and capacitor-oltage balancing for MMCs," *IET Power Electron.*, vol. 12, no. 4, pp. 817–828, Apr. 2019, doi: 10.1049/iet-pel.2018.5096.
[29] L.-A. Grégoire, M. Cousineau, S. I. Seleme, and P. Ladoux, "Real-time simulation of interleaved converters with decentralized control," *Renew. Energy Power Quality J.*, vol. 1, no. 14, pp. 268–273, May 2016, doi: 10.24084/repqj14.287.
[30] Q. D. Phan, G. Gateau, P. C. Nguyen, M. Cousineau, H. P. To, B. A. Nguyen, L. Veit, R. De Milly, and M. M. Hillesheim, "A fast, decentralized, self-aligned carrier method for multicellular converters," *Appl. Sci.*, vol. 11, no. 1, p. 137, Dec. 2020, doi: 10.3390/app11010137.
[31] G. Gateau, P. Q. Dung, M. Cousineau, P. U. T. Do, and L. H. Nhan, "Digital implementation of decentralized control for multilevel converter," in *Proc. Int. Conf. Syst. Sci. Eng. (ICSSE)*, Jul. 2017, pp. 558–562, doi: 10.1109/ICSSE.2017.8030937.
[32] Q. D. Phan, G. Gateau, M. T. Nguyen, and M. Cousineau, "2D decentralized interleaving principle for multicell serial–parallel converters," in *Proc. IEEE 13th Int. Conf. Power Electron. Drive Syst. (PEDS)*, Jul. 2019, pp. 1–7, doi: 10.1109/PEDS44367.2019.8998840.
[33] P. C. Nguyen, Q. D. Phan, and D. T. Nguyen, "A new decentralized space vector PWM method for multilevel single-phase full bridge converters," *Energies*, vol. 15, no. 3, p. 1010, Jan. 2022, doi: 10.3390/en15031010.
[34] P. C. Nguyen and Q. D. Phan, "The development of decentralized space vector PWM method for multilevel multiphase converters," in *Proc. IEEE 8th Int. Conf. Commun. Electron. (ICCE)*, Jan. 2021, pp. 163–168, doi: 10.1109/ICCE48956.2021.9352119.
[35] B. Johansson and E. Osterberg, "Algorithms for large matrix multiplications: Assessment of Strassen's algorithm," School Eng. Sci., KTH Roy. Inst. Technol., Stockholm, Sweden, Tech. Rep., 2018.
[36] S. Elert, "Programming possibilities using MATLAB simulink embedded coder on the example of data analysis from ahrs module," *J. Phys., Conf. Ser.*, vol. 1507, no. 8, Mar. 2020, Art. no. 082042, doi: 10.1088/1742-6596/1507/8/082042.

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