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RESEARCH ARTICLE

Current-Voltage Modeling of DRAM Cell Transistor Using Genetic Algorithm and Deep Learning

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ABSTRACT Accurate current-voltage (*I-V*) modeling based on the Berkeley short-channel insulated-gate field-effect transistor model (BSIM) is pivotal for integrated circuit simulation. However, the current BSIM model does not support a buried-channel-array transistor (BCAT), which is the structure of the state-of-the-art commercial dynamic random access memory (DRAM) cell transistor. In this work, we propose an intelligent *I-V* modeling technique that combines genetic algorithm (GA) and deep learning (DL). This hybrid technique facilitates both optimization of BSIM parameter and accurate *I-V* modeling, even for devices not originally supported by BSIM. Additionally, we extended application of the DL to model one of the principal degradation mechanisms of transistor, the hot-carrier degradation (HCD). The successful modeling results of *I-V* characteristic and device degradation demonstrated that devices not supported by BSIM can be accurately modeled for integrated circuit simulations.

INDEX TERMS BSIM-CMG, deep learning, genetic algorithm, I-V modeling, compact modeling, BCAT, DRAM cell transistor, HCD.

I. INTRODUCTION

Accurate and fast current-voltage (*I-V*) modeling is essential for integrated circuit simulation. The Berkely short-channel insulated-gate field-effect transistor model (BSIM) has been widely used in the semiconductor industry over the past few decades. Accurate *I-V* modeling necessitates the extraction and optimization of over 100 distinct parameters.

To address these challenges, researchers have delved into various optimization-based techniques for parameter extraction, including the application of genetic algorithms (GA) [1], [2], [3] and the implementation of deep learning methodologies (DL) [4], [5], [6], [7], [8], [9].

The GA, grounded in the principles of natural selection and genetics, serves as a sophisticated approach to identifying an optimal set of parameters. The DL techniques, employing deep neural networks, can determine the values of each parameter through the training *I-V* data. However,

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a fundamental constraint of these methods is that they can only be applied to semiconductor devices that are supported by the BSIM model.

A buried-channel-array transistor (BCAT) having a saddle-fin and buried-gate structure has been employed in state-of-the-art dynamic random access memory (DRAM) technology [10], [11], [12]. Nonetheless, the lack of support from BSIM makes it challenging to accurately model the *I-V* characteristics of these advanced DRAM cell transistors.

In addition, the *I-V* characteristics of physical transistors varies under environmental factors such as operating temperature, device degradation, and so on. Especially, modeling of device degradation mechanism is becoming more important and critical in *I-V* characteristic as devices scaling.

There are known mechanisms that affects the devices *I-V* characteristics such as hot-carrier degradation (HCD), negative bias thermal instability (NBTI), positive bias thermal instability (PBTI), time dependent dielectric breakdown (TDDB) [13], [14], [15], [16], [17]. However, conventional BSIM models encounter challenges in precisely forecasting these phenomena.

To enhance model precision, the utilization of look-up tables can be considered [18]. Nevertheless, it is noteworthy that look-up tables come with the drawback of necessitating a substantial amount of model parameters and *I-V* data sampling. Furthermore, interpolation based on look-up tables is vulnerable to data noise.

To overcome these challenges, we have proposed an *I-V* modeling approach that enables BSIM-based circuit simulation even for semiconductor devices not supported by BSIM. Our proposed modeling technique, carried out through a two-step integration of the GA and the DL, proved to be a successful model for DRAM cell transistor. Also, we extended our modeling technique to the HCD that is one of the principal degradation mechanisms.

TABLE 1. BSIM-CMG parameters values optimized through the GA.

Parameters	ETAMOB	KSATIV	CDSC	UA	DROUT
Default Value	2	1.0	$7.0\text{x}10^{-3}$ [Fm^{-2}]	0.3	1.06
Optimized Value	4.0	0.67	$3.66\text{x}10^{-7}$ [Fm^{-2}]	$1.08\text{x}10^{-9}$	50.0

II. *I-V* MODELING USING GA AND DL

Fig. 1 illustrates the model implementation of BCAT for circuit simulation. The drain current of BCAT can be modeled based on a conventional transistor and an add-on current source as follows:

$$I_{\text{D,model(GA+DL)}} = I_{\text{D,BSIM(GA)}} \times \varepsilon_{\text{(DL)}}. \quad (1)$$

Here, $I_{\text{D,BSIM(GA)}}$ refers to the transistor current modeled by BSIM, and its BSIM parameters are determined using the GA. $\varepsilon_{\text{(DL)}}$ is a correction function that depends

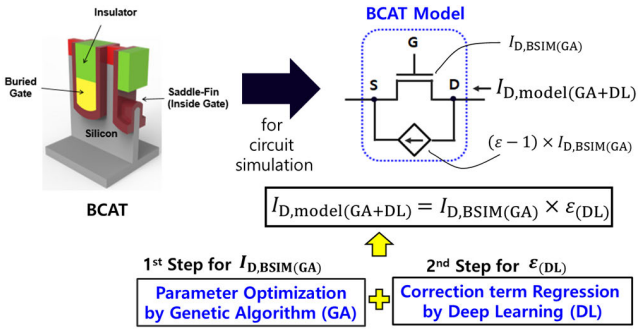

FIGURE 1. *I – V* model implementation of BCAT for circuit simulation.

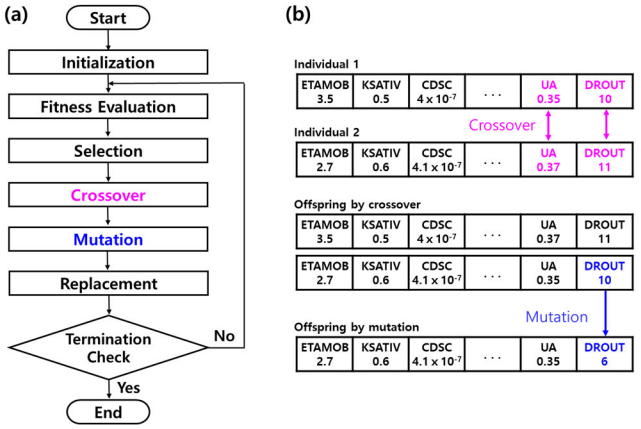

FIGURE 2. (a) A flow chart of GA. (b) Crossover and mutation during the GA optimization of BSIM parameter.

on the gate-source voltage (V_{GS}) and drain-source voltage (V_{DS}) [19]. This bias-dependent correction function $\varepsilon_{\text{(DL)}}$ is determined using the DL. In summary, the proposed method involves two stages.

In the first stage, BSIM parameter optimization is performed by the GA. Here, we used BSIM-CMG model with a FinFET that closely resembles the BCAT structure [20]. In the next stage, a current source is introduced to reduce the error arising from disparities between the BSIM-CMG model and the actual BCAT characteristics. This current source function is determined through regression using the DL.

Table. 1 represents some of the key BSIM-CMG parameters determined through the GA. The GA is a popular optimization technique inspired by the process of natural selection. It has been widely utilized in various domains to solve optimization problems. As illustrated in Fig. 2(a), the algorithm operates through several stages, as follows:

1. Initialization: The algorithm commences by initializing a population of possible solutions (BSIM-CMG parameter sets). We generated a total of 1000 individuals as the initial population.

2. Fitness evaluation: In the fitness evaluation step, the fitness scores of each individual in the population is calculated. The fitness score is an indicator of how closely the modeling results resemble the target values. Fitness score of each individual in the population is evaluated by fitness

function:

$$\text{fitness score} = \sum_{V_{GS}, V_{DS}} \frac{\left|\log_{10} I_{D,BSIM(GA)} - \log_{10} I_{D,measured}\right|}{\left|\log_{10} I_{D,measured}\right|} \tag{2}$$

where, $I_{D,BSIM(GA)}$ is a drain current from BSIM-CMG model, and $I_{D,measured}$ is the measured drain current. The fitness score is calculated across the V_{GS} or V_{DS} range according to the *I-V* graphs.

3. Selection: Based on the fitness score, individuals are selected for reproduction. Here, the tournament selection function was used (the selection tournament size = 2). Firstly, we sort all of the individuals according to the fitness scores. Then, the selection process was carried out on the top 50 % of individuals.

4. Crossover: Selected individuals undergo crossover to create offspring. The BSIM-CMG parameter values of the selected two individuals are transformed into binary information that can be called genes. Then, two genetic information segments are crossed over around the midpoint of the genetic information, resulting in the creation of two offspring individuals.

This process involves exchanging portions of two individuals as shown in Fig. 2(b). Therefore, two offspring individuals are generated from the two parent individuals, and selection and crossover are repeated until the specified population size is reached.

5. Mutation: To maintain genetic diversity within the population, right after the crossover, some of the offspring may undergo mutation. This operation introduces small, random changes to the individual's genetic material as shown in Fig. 2(b). The mutation rate was set to be 0.1 %.

6. Replacement: The individuals are replaced to the offspring from previous population. Additionally, we preserved 4 % best individuals from the previous population for enhancing the performance of the GA.

7. Termination check: The algorithm checks whether a certain termination criterion has been met. If a certain termination criterion, such as a generation iteration or fitness scores, is met, the GA will be terminated. If the termination criterion is not met, the fitness scores of the offspring will be calculated, and the above process will be repeated.

Fig. 3(a) illustrates the result of parameter optimization for BSIM-CMG based on the GA. The minimum value of fitness score decreases as generation progress. We used the BSIM-CMG parameters of the individual with the lowest fitness score of the GA as the optimal BSIM-CMG parameter. Fig. 3(b) shows the *I-V* characteristics of measurement result and obtained by the BSIM-CMG model with default parameter and optimal parameter. The GA based BSIM-CMG model show the feasibility of modelling BCAT current characteristics.

However, there is mismatch between measurement and the GA based BSIM-CMG model. Because there is limitation on

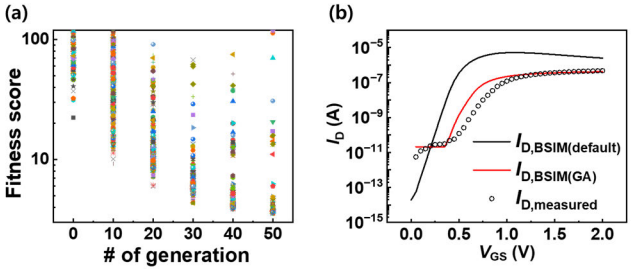

FIGURE 3. (a) Fitness score versus the number of evolution generations. (b) The modeling result of the transfer characteristics through GA as the first step.

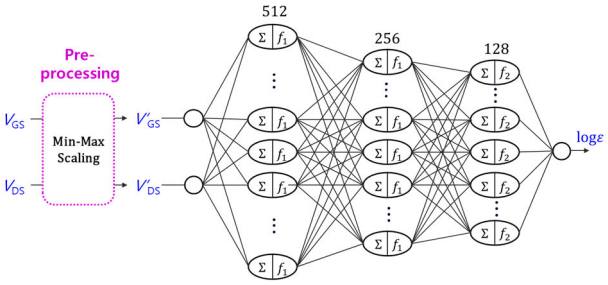

FIGURE 4. Deep neural network used in this work for DL.

the GA based BSIM-CMG model, the DL was implemented to correct the modeling mismatch.

Fig. 4 shows the fully connected deep neural network (DNN) architecture used in this work. The proposed DNN has two input neurons (V'_{GS}, V'_{DS}) and one output neuron ($\log_{10}\varepsilon_{(DL)}$). Input neurons are transformed by preprocessing the input parameters with min-max scaling. The neural network comprises three hidden layers, utilizing the leaky ReLU (f_1) and hyperbolic tangent (f_2) functions as activation functions. The $\varepsilon_{(DL)}$ values span a very wide range from 0.1 to 10, so in order to bring them within the range representable by the artificial neural network's output, we have set $\log_{10}\varepsilon_{(DL)}$, as the target output.

The cost function J is defined as the average root mean square relative errors in drain current, transconductance and output conductance ($E(I_D)$, $E(g_m)$ and $E(g_{ds})$):

$$J = \sqrt{25 \times E(I_D)^2 + E(g_m)^2 + E(g_{ds})^2} \tag{3}$$

where $E(I_D)$, $E(g_m)$ and $E(g_{ds})$ are given by

$$E\left(I_D\right) = \frac{1}{k}\sum_{i=1}^{k}\left[\left(\log_{10}\frac{I^{(i)}_{D,model(GA+DL)}}{I^{(i)}_{D,measured}}\right)^2 + A \times \left(I^{(i)}_{D,model(GA+DL)} - I^{(i)}_{D,measured}\right)^2\right], \tag{4}$$

$$E(g_m) = \frac{1}{k}\sum_{i=1}^{k}\left|B \times \left(g^{(i)}_{m,model(GA+DL)} - g^{(i)}_{m,measured}\right)\right|, \tag{5}$$

$$E(g_{ds}) = \frac{1}{k}\sum_{i=1}^{k}\left|B \times \left(g^{(i)}_{ds,model(GA+DL)} - g^{(i)}_{ds,measured}\right)\right| \tag{6}$$

TABLE 2. Comparison of measurement and modeling results for HCD.

Stress time (s)	Measured				Modeling			
	V_{TH} (V)	Subthreshold swing (mV/dec)	$g_{m.max}$ (μA/V)	I_{ON} (μA)	V_{TH} (V)	Subthreshold swing (mV/dec)	$g_{m.max}$ (μA/V)	I_{ON} (μA)
0	0.94	280	1.45	0.986	-	-	-	-
1	0.94	300	1.45	0.968	0.94	290	1.4415	0.968
10	0.94	250	1.35	0.958	0.94	290	1.4385	0.958
20	0.94	300	1.35	0.948	0.94	290	1.4360	0.948
50	0.94	270	1.55	0.944	0.94	290	1.4090	0.942
100	0.94	290	1.40	0.927	0.94	300	1.5020	0.927
200	0.94	280	1.50	0.918	0.94	300	1.3680	0.918
500	0.94	310	1.30	0.886	0.94	300	1.3175	0.886
1000	0.94	280	1.20	0.859	0.94	300	1.2230	0.856
2000	0.94	290	1.15	0.828	0.94	300	1.1575	0.828

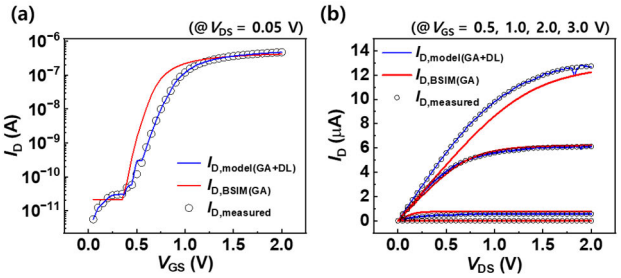

FIGURE 5. The modeling results of (a) the transfer characteristics and (b) the output characteristics.

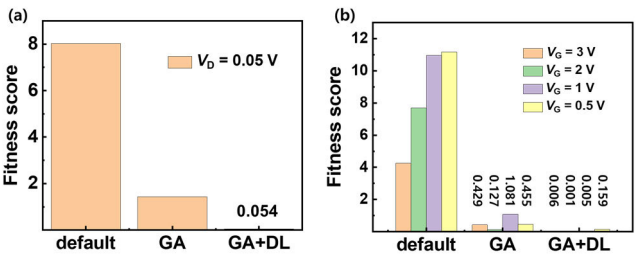

FIGURE 6. The fitness scores at each (a) the transfer characteristics curve and (b) the output characteristics curve.

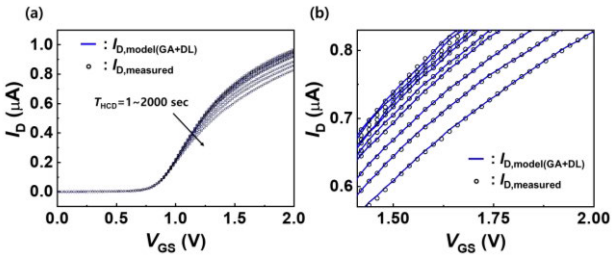

FIGURE 7. (a) The modeling results of HCD degradation. (b) A magnified graph of the voltage range 1.25∼2.00 V in Fig. (a).

where k is the training set sample size and A and B are scale factors for the error calculation.

The neural network is trained with a dataset of (V_{GS}, V_{DS} and $I_{D,measured}$) with V_{GS} and V_{DS} range from 0 V to 2.0 V with 50 mV increment. Then, we evaluate the accuracy of the trained neural network using a test dataset that has the same voltage ranges but smaller voltage increments of 5 mV. Pytorch with AdaDelta [21] optimization was used for training. AdaDelta optimization is a stochastic gradient descent method that uses adaptive learning rates per dimension to overcome the challenges of continuously decaying learning rates during training and the requirement for manually selecting a global learning rate.

Fig. 5 illustrates the *I-V* modeling results of BCAT using the proposed model. The *I-V* characteristics obtained by the proposed model exhibit a closer match to the measurement results, especially include the off-current region in Fig. 5(a), with lower fitness scores compared to the GA results.

Fig. 6 shows the fitness scores of each modeling results. As the steps progressed, the fitness scores significantly decreased for both the transfer characteristics curve and the output characteristics curve at all V_{GS} bias. At first, the fitness score of the $I_{D,BSIM(default)}$ model in the transfer characteristics curve at V_{DS} = 0.05 V was 8.026 and the fitness score of the output characteristics curve at V_{GS} = 3.0 V is 4.248. After using the GA, The fitness scores of the $I_{D,BSIM(GA)}$ model in the transfer characteristics curve and the output characteristics curve were reduced to 1.439 and 0.429 respectively. Finally, when incorporating both the GA and the DL for further refinement, the fitness scores for the $I_{D,model(GA+DL)}$ model were observed to be 0.054 in the transfer characteristics curve and 0.006 in the output characteristics curve.

III. MODELING EXTENSION TO THE HOT CARRIER DEGRADATION BY ADDING INPUT VARIABLES

In general, the *I-V* characteristics of real transistors exhibit variations in response to different environmental factors such as operating temperature, device degradation, and so on.

By including various parameters in addition to V_{GS} and V_{DS} as input parameters for the DL model, it becomes possible to perform *I-V* modeling under a wide range of environmental scenarios. By incorporating the HCD stress duration (T_{HCD}) as an input parameter, we successfully modeled the *I-V* characteristics of HCD in BCAT under various stress durations. The stress voltage is $V_{GS} = V_{DS} = 2.5$ V, with the stress duration ranging from 1 to 2000 sec. We used the same neural network as illustrated in Fig. 4.

Fig. 7 depicts the modeling results of the BCAT affected by HCD. Table 2 compares the measured values and modeling results for key electrical characteristics. V_{TH} was calculated by current constant method at $I_D = 0.1$ μA. I_{ON} is defined as I_D at $V_{GS} = 2.0$ V and $V_{DS} = 0.05$ V. Subthreshold swing (SS) was extracted within the range of I_D varying from 1 nA to 100 nA.

In summary, our proposed *I-V* modeling technique can be extended to various situations. It's worth noting that if the number of input parameters increases to represent multiple situations simultaneously, a modification to a larger and deeper neural network may be necessary. Furthermore, while this study only conducted *I-V* modeling for a single device, it is necessary to conduct additional research on probabilistically predicting the characteristics of devices based on the mass data of many devices.

IV. CONCLUSION

In this study, we proposed a transistor *I-V* modeling approach that sequentially utilizes the GA and the DL. The proposed method has the advantage of enabling circuit simulation based on accurate *I-V* modeling for next-generation devices that are not supported by BSIM. By using state-of-the-art commercial DRAM transistors (BCAT), we successfully verified the proposed modeling. Furthermore, this modeling technique can be expanded to various device modeling applications, including device degradation such as HCD.

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REFERENCES

[1] Y. Li and Y.-Y. Cho, "Intelligent BSIM4 model parameter extraction for sub-100 nm MOSFET era," *Jpn. J. Appl. Phys.*, vol. 43, no. 4S, p. 1717, Apr. 2004, doi: 10.1143/jjap.43.1717.

[2] Q. Zhou, W. Yao, W. Wu, X. Li, Z. Zhu, and G. Gildenblat, "Parameter extraction for the PSP MOSFET model by the combination of genetic and Levenberg–Marquardt algorithms," in *Proc. IEEE Int. Conf. Microelectronic Test Struct.*, Mar. 2009, pp. 137–142, doi: 10.1109/ICMTS.2009.4814627.

[3] R. Menozzi, A. Piazzi, and F. Contini, "Small-signal modeling for microwave FET linear circuits based on a genetic algorithm," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 43, no. 10, pp. 839–847, Oct. 1996.

[4] M.-Y. Kao, F. Chavez, S. Khandelwal, and C. Hu, "Deep learning-based BSIM-CMG parameter extraction for 10-nm FinFET," *IEEE Trans. Electron Devices*, vol. 69, no. 8, pp. 4765–4768, Aug. 2022, doi: 10.1109/TED.2022.3181536.

[5] F. Chavez, D. T. Davis, N. C. Miller, and S. Khandelwal, "Deep learning-based ASM-HEMT I–V parameter extraction," *IEEE Electron Device Lett.*, vol. 43, no. 10, pp. 1633–1636, Oct. 2022, doi: 10.1109/LED.2022.3197800.

[6] J. Wang, Y.-H. Kim, J. Ryu, C. Jeong, W. Choi, and D. Kim, "Artificial neural network-based compact modeling methodology for advanced transistors," *IEEE Trans. Electron Devices*, vol. 68, no. 3, pp. 1318–1325, Mar. 2021, doi: 10.1109/TED.2020.3048918.

[7] K. Mehta and H.-Y. Wong, "Prediction of FinFET current-voltage and capacitance-voltage curves using machine learning with autoencoder," *IEEE Electron Device Lett.*, vol. 42, no. 2, pp. 136–139, Feb. 2021, doi: 10.1109/LED.2020.3045064.

[8] M. Li, O. Irsoy, C. Cardie, and H. G. Xing, "Physics-inspired neural networks for efficient device compact modeling," *IEEE J. Explor. Solid-State Comput. Devices Circuits*, vol. 2, pp. 44–49, 2016, doi: 10.1109/JXCDC.2016.2636161.

[9] L. Zhang and M. Chan, "Artificial neural network design for compact modeling of generic transistors," *J. Comput. Electron.*, vol. 16, no. 3, pp. 825–832, Sep. 2017, doi: 10.1007/s10825-017-0984-9.

[10] K. Kim, "From the future Si technology perspective: Challenges and opportunities," in *IEDM Tech. Dig.*, Dec. 2010, pp. 1.1.1–1.1.9, doi: 10.1109/IEDM.2010.5703274.

[11] J. M. Park, Y. S. Hwang, S.-W. Kim, S. Y. Han, J. S. Park, J. Kim, J. W. Seo, B. S. Kim, S. H. Shin, C. H. Cho, S. W. Nam, H. S. Hong, K. P. Lee, G. Y. Jin, and E. S. Jung, "20 nm DRAM: A new beginning of another revolution," in *IEDM Tech. Dig.*, Dec. 2015, p. 26, doi: 10.1109/IEDM.2015.7409774.

[12] S. Jeon, J. Choi, H.-c. Jung, S. Kim, and T. Lee, "Investigation on the local variation in BCAT process for DRAM technology," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Monterey, CA, USA, Apr. 2017, pp. FA-4.1–FA-4.2, doi: 10.1109/IRPS.2017.7936374.

[13] J. Park, N. Lee, G.-J. Kim, H.-S. Choi, D. H. Kim, C. Kim, M. Kang, and Y. Kim, "Impact ionization and hot-carrier degradation in saddle-fin and buried-gate transistor of dynamic random access memory at cryogenic temperature," *IEEE Electron Device Lett.*, vol. 42, no. 5, pp. 653–656, May 2021, doi: 10.1109/LED.2021.3067109.

[14] S. Mahapatra and U. Sharma, "A review of hot carrier degradation in n-channel MOSFETs—Part I: Physical mechanism," *IEEE Trans. Electron Devices*, vol. 67, no. 7, pp. 2660–2671, Jul. 2020, doi: 10.1109/TED.2020.2994302.

[15] S. Mahapatra and U. Sharma, "A review of hot carrier degradation in n-channel MOSFETs—Part II: Technology scaling," *IEEE Trans. Electron Devices*, vol. 67, no. 7, pp. 2672–2681, Jul. 2020, doi: 10.1109/TED.2020.2994301.

[16] J. Keane, X. Wang, D. Persaud, and C. H. Kim, "An all-in-one silicon odometer for separately monitoring HCI, BTI, and TDDB," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 817–829, Apr. 2010, doi: 10.1109/JSSC.2010.2040125.

[17] A. Kerber, A. Vayshenker, D. Lipp, T. Nigam, and E. Cartier, "Impact of charge trapping on the voltage acceleration of TDDB in metal gate/high-k n-channel MOSFETs," in *Proc. IEEE Int. Rel. Phys. Symp.*, Anaheim, CA, USA, May 2010, pp. 369–372, doi: 10.1109/IRPS.2010.5488803.

[18] P. G. A. Jespers and B. Murmann, *Systematic Design Analog CMOS Circuits*, Cambridge, U.K.: Cambridge Univ. Press, 2017.

[19] M.-Y. Kao, H. Kam, and C. Hu, "Deep-Learning-Assisted physics-driven MOSFET current-voltage modeling," *IEEE Electron Device Lett.*, vol. 43, no. 6, pp. 974–977, Jun. 2022, doi: 10.1109/LED.2022.3168243.

[20] J. P. Duarte, "BSIM-CMG: Standard FinFET compact model for advanced circuit design," in *Proc. 41st Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2015, pp. 196–201, doi: 10.1109/ESSCIRC.2015.7313862.

[21] M. D. Zeiler, "ADADELTA: An adaptive learning rate method," 2012, *arXiv:1212.5701*.

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