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RESEARCH ARTICLE

A Very Large-Scale Integration (VLSI) Chip Design for Abnormal Heartbeat Detection Using a Data-Shifting Neural Network (DSNN)

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ABSTRACT In this paper, we propose a data-shifting neural network (DSNN) for the detection of abnormal heartbeats. Our study aims to identify six types of electrocardiogram (ECG) signals using the deep learning network. In order to enhance the detection accuracy, the DSNN is devised by doubling the input signal using a data shifting scheme so that the amount of information for training may be adequately sufficient. Although the computational time doubles, the accuracy can be improved. When implemented using the Taiwan Semiconductor Manufacturing Company (TSMC) $0.18-\mu m$ complementary metal oxide semiconductor (CMOS) process, the proposed DSNN chip has an operating frequency at 20 MHz with chip area of $0.619\ mm^2$ and maximum power dissipation $0.75\ mW$. As a result, the proposed DSNN can substantially increase detection accuracy for the task of ECG heartbeat classification. Results obtained after applying the proposed circuit to the ECG signals drawn from the MIT-BIH arrhythmia database showed that it achieved a detection rate of 97.17% with a small chip area, suggesting that it may be suitable for wearable or portable devices in healthcare.

INDEX TERMS Very-large-scale integration implementation (VLSI), electrocardiogram (ECG), convolutional neural network (CNN), data-shifting neural network (DSNN).

I. INTRODUCTION

The human body produces a variety of physiological signals that can be diagnostically useful. Among all the physiological signals of interest, an electrocardiogram (ECG) has been considered a simple, reliable, well-known, and well-defined one. Since an ECG signal provides vital information about the heart's electrical activity resulting from the cardiac muscle conduction and abnormal ECG signals can be indicative of various cardiac disorders, it can be employed for identifying abnormal cardiac rhythms and for investigating cardiac diseases or heart rate variability (HRV) [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13]. In particular, the prevention of sudden cardiac deaths (SCD) essentially requires quick and accurate identification of the arrhythmias from ECG recordings since arrhythmias are often the underlying cause of SCD, and thus making their early detection is crucial for timely intervention. In fact, in order to achieve the goal of efficient and accurate classification of cardiac arrhythmias using ECG data, there are a number of previous researches in literature proposing a variety of approaches for the task of arrhythmia detection

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[5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17]. Among these, some were developed for the detection of life-threatening arrhythmias, such as premature ventricular contractions (PVCs), ventricular fibrillation (VF) and ventricular tachycardia (VT) [5], [6], [7], [8], [9], [10], [11], [12], [13], but only software simulation results were reported in their studies.

In general, real-time detection with high accuracy helps cardiologists classify the abnormality correctly on a timely basis, leading to targeted and effective treatment strategies. In this aspect, some researchers have proposed very large-scale integration (VLSI) circuit design-based approaches aiming at detecting the abnormal ECG signals in a real-time manner [14]- [17]. Lee et al. have proposed a low-power system-on-chip (SoC) platform for ECG signal acquisition and classification system [14]. Their design focuses on low-power operation, with long battery life for body-end circuits and low power consumption for receiving-end circuits. It achieves high accuracy in beat detection and ECG classification. Another example of VLSI chip design is proposed for the prediction of ventricular arrhythmia using a unique set of ECG features and a naive Bayes classifier [15]. It is a fully integrated ECG signal processor with adaptive techniques and a naive Bayes classifier. It offers reasonable power consumption and area, but only achieves a modest accuracy of 86% for ventricular arrhythmia prediction. In addition, in recent years deep learning networks have attracted great attention and thus increasingly applied in the field of ECG analysis, including the detection of abnormal ECG signals. One common approach for ECG analysis using deep learning is to use convolutional neural networks (CNNs) to automatically learn relevant features from the ECG signal. The CNN can be trained on a large dataset of ECG signals with labeled abnormalities, allowing it to learn to recognize patterns in the signals that are indicative of cardiac arrhythmias. As a result, once a deep learning model is trained, it can be used to classify ECG signals into a number of arrhythmic events. In such aspects of applications, VLSI implementations of CNN-based techniques for abnormal heartbeat detection were proposed in previous studies in literature [16] and [17]. The results obtained from these works have shown that the hardware realization of CNN for ECG heartbeat classification may achieve high speed, small area, and low power dissipation with a high detection rate, thus improving early detection and timely treatment of cardiac disorders. Ultimately, it is important to note that the choice among all these chip designs would depend on specific requirements such as power constraints, accuracy targets, available process technology, and the trade-offs between accuracy and implementation complexity.

In fact, the motivation behind researching VLSI chip design for ECG-based abnormal heartbeat detection is driven by the perpetual quest to enhance medical diagnostics' efficiency and precision. While a number of researchers have made commendable strides in the past, the continuous evolution of technology and the rising demand for compact, energy-efficient, and accurate solutions necessitate ongoing exploration of novel techniques. The significance of this study lies in the critical role VLSI chip design plays in healthcare technology, crucial for seamlessly integrating abnormal heartbeat detection into portable and wearable devices, potentially revolutionizing healthcare by enabling continuous monitoring and timely interventions. The pursuit of miniaturization aligns with personalized medicine's trend, accommodating unobtrusive health monitoring and potential implantable solutions, expanding continuous cardiac monitoring. Emphasizing accuracy, researchers aim to develop chips that not only meet clinical accuracy requirements but also surpass existing solutions, advancing the state-of-the-art. In a broader context, the societal impact is substantial, promising effective treatment, lives saved, reduced healthcare costs, and contributing to sustainability through power-efficient designs. In essence, this research embodies an unwavering commitment to technological innovation, aiming to usher in a new era of efficient, accurate, and accessible cardiac monitoring for individual well-being and the broader healthcare ecosystem.

In this study, we propose a novel data-shifting neural network (DSNN) that can provide a real-time detection of abnormal heartbeat with high accuracy. In general, our proposed work offers several advantages over the previous works. First, the proposed work achieves high classification accuracy while occupying a relatively smaller area, making it more compact compared to the previous works as proposed by [16] and [17]. In addition, the proposed DSNN circuit consumes only $0.75mW$ of power, which is significantly lower than both circuits as proposed by [16] and [17]. Also, although the proposed work operates at a lower frequency of $20MHz$ compared to [16] and [17], it still offers a reasonable operating frequency for ECG abnormal heartbeat classification. On the other hand, this work fits into the framework of translational medicine [18], [19]. In the context of translational medicine, the novel DSNN represents a significant breakthrough since it is designed to revolutionize the real-time detection of abnormal heartbeats by offering accuracy and speed. The proposed DSNN leverages deep learning techniques to swiftly analyze vast amounts of medical data, instantly identifying irregular cardiac rhythms. This innovation holds tremendous potential for early diagnosis and intervention in cardiac conditions, ultimately improving patient outcomes and paving the way for more effective healthcare practices. DSNN exemplifies the seamless integration of technology into the medical field, translating scientific advancements into tangible benefits for patients and healthcare providers.

In summary, the main contributions of this study involve introducing a novel DSNN for real-time detection of abnormal heartbeat with high accuracy. This innovation provides several advantages over previous works, such as notably achieving superior classification accuracy within a more compact design and exhibiting remarkable energy efficiency. Also, despite operating at a lower frequency of 20 MHz, the

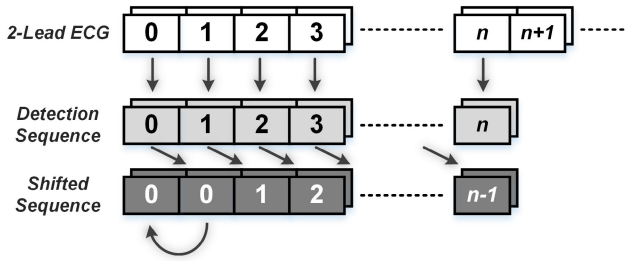


FIGURE 1. The proposed data-shifting scheme. Here, a shifted sequence results from shifting the original detection sequence of length n to the right by one sample. As a result, both the detection and shifted sequences are used as inputs into the DSNN for training and testing.

proposed DSNN circuit maintains a reasonable operating frequency for ECG abnormal heartbeat classification. Overall, the study presents a novel and efficient approach to real-time abnormal heartbeat detection, offering advancements in accuracy, compactness, and power efficiency compared to existing methods. This paper is organized as follows. The proposed DSNN and its architecture is described in Section II. Section III provides descriptions of a performance evaluation and discussion. Finally, this paper is briefly concluded in Section IV.

II. PROPOSED DATA-SHIFTING NEURAL NETWORK (DSNN) AND ITS ARCHITECTURE

The DSNN architecture is a scheme designed for the classification of ECG heartbeats. The flowchart of the proposed DSNN is illustrated in Figure 2. In general, it utilizes a data-shifting technique to enhance detection accuracy while minimizing the increase in circuit area. The architecture mainly consists of several key components, including a data-shifting scheme to expand the training and testing signals, a CNN as the main structure of the DSNN, and a voting circuit for making the decision at the classification stage of the ECG heartbeat detection. All these components and their functions are described as follows.

Here, we presented a data-shifting scheme, referred to as DSNN as described previously, that doubles the number of training and testing signals, as depicted in Fig. 1. Observing Fig. 1, one may see that a 2-lead ECG signal is separated into a number of n-point detection sequences. In this study, n was set to 24. A shifted sequence can result from shifting the original detection sequence either to the right or to the left by one or more samples. The number of right shifts can be adjusted to an arbitrary number (typically 1), and left shifts can also be accepted. Finally, both the detection and shifted sequences are then used as inputs into the DSNN for training and testing. Although this would cause the computational time to be doubled, due to the slow sampling rate of the ECG signal the requirement of real-time analysis can be still adequately met. In addition, for the hardware part in our proposed study, we only added a voting circuit to the end of the CNN circuit so the overall circuit area only increases slightly. Note that there are three convolutional layers and two fully connected (FC) layers included to form the main structure of the CNN, as depicted in Fig. 3. Also, it is revealed from Fig. 3 that the second FC layer is followed by a voter. Note that here the voter would compare the two maximal probabilities of the softmax outputs obtained by applying the detection and shifted sequences as inputs into the CNN, respectively, and then vote for the type of the ECG heartbeat corresponding to the higher probability of the two. As a result, a higher detection accuracy may be thus achieved by the proposed DSNN at the expense of a little bit of increase in circuit area.

In addition, the size of the input ECG data is 2×24 since there are two ECG leads and the ECG sequence length is 24. It should be noted that when an ECG sequence is input into the CNN, two-dimensional (2D) convolution calculations of three 1×7 filters in the first layer are performed and then followed by the 1×2 max pooling process. Then, a 1×1 filtering process in the second layer is performed. Afterward, similar to the first layer, in the third layer, 2D convolution calculations of three 1×7 filters are performed and then followed by a 1×3 max pooling. Finally, the learned feature maps are flattened as 6 nodes and then fed into a fully connected neural network with an input layer consisting of 14 nodes and an output layer of 6 nodes (since there are six types of ECG heartbeats to be classified). Table 1 provides a listing of the total number of filter coefficients or parameters required for each layer of the CNN as proposed in our study.

Details about the network layers, activation functions, loss function, and training methodology are listed in the following.

- The neural network architecture comprises three convolutional layers interspersed with two max-pooling layers, followed by a flattening layer and two dense layers.
- The activation functions used in the convolutional and dense layers are 'ReLU', while the final output layer employs a 'softmax' activation for multi-class classification.
- The model's loss function is categorical cross entropy, suitable for multi-class categorization tasks.
- For training, the model uses the Adam algorithm optimizer, running for 2, 000 epochs with a batch size of 48.
- A 20% validation split is incorporated during training to assess model performance on unseen data while shuffling ensures diverse data exposure in each epoch.

This study utilizes the MIT-BIH database [20] for neural network training and testing. The MIT-BIH Arrhythmia Database is a widely-adopted dataset for studying cardiac arrhythmias. It encompasses ECG recordings from 48 subjects, each approximately 30 minutes long. Expert cardiologists have annotated this dataset, identifying various arrhythmia types. We specifically selected normal heartbeats and those showing five different arrhythmias. Each ECG was extracted with two leads and 24 sample points at a sampling

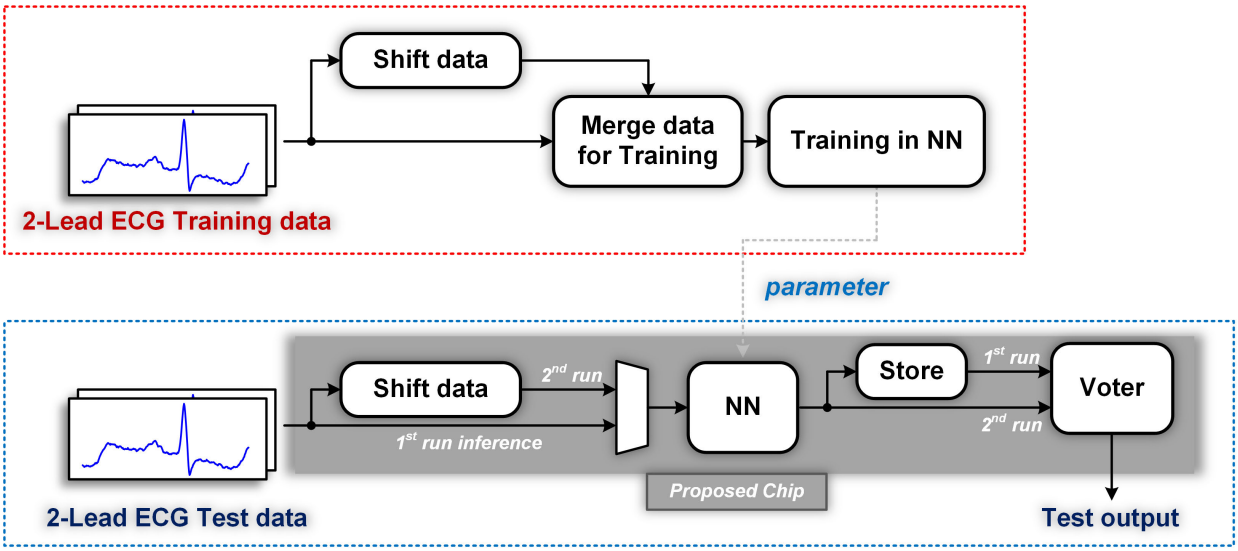


FIGURE 2. The flowchart of the proposed DSNN.

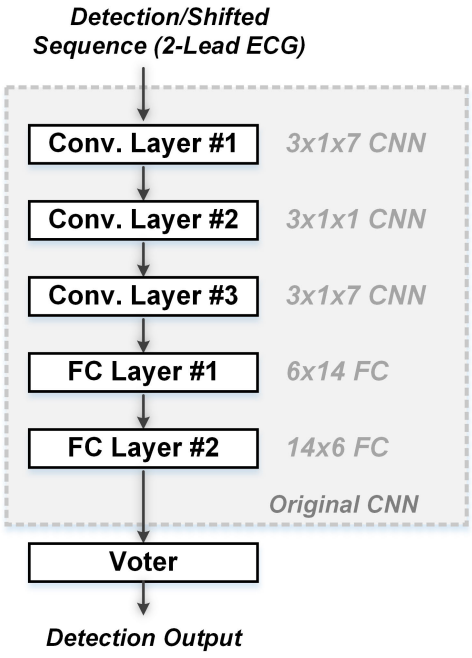


FIGURE 3. The schematic block diagram of the proposed DSNN.

frequency of 360Hz. Thus, if our neural network is applied to another database with a different sampling frequency or real-time ECG measurements, it only requires re-sampling to a 360Hz frequency and extracting based on the R-peak for 24 sample points for compatibility.

Fig. 4 illustrates the comprehensive architecture of the proposed DSNN. Upon examining Fig. 4, it is evident that the 1×7 filters were efficiently implemented using a singular multiplier and one adder, resulting in substantial savings in the circuit area. The Fully Connected (FC) layer similarly employs a single multiplier and adder to perform the 6×14 and 14×6 matrix multiplications, leading to a further reduction in circuit footprint. Moreover, each layer of the circuit operates using a single multiply-accumulate (MAC) unit, which adds significantly to its compactness. The entire architecture, consisting of five convolutional layers and two fully connected layers, only requires five multipliers, five adders, and five registers, fulfilling the design objective of a small circuit area. The MaxPooling module is implemented by utilizing registers and comparators, as shown in Figure 5. Specifically, a 1×2 MaxPooling configuration employs one register and one comparator, whereas a 1×3 MaxPooling setup necessitates two registers and two comparators to function effectively. The final stage introduces a voting circuit, which decides between the two maximum results derived from the softmax outputs of the detection and shifted sequences, respectively, thereby casting a vote for the ECG heartbeat type. The addition of this voter circuit can effectively enhance overall detection accuracy. This concept could be extended to the identification processes in all similar signal-processing scenarios. This design approach allows

TABLE 1. A listing of the total number of filter coefficients or parameters required for each layer of the proposed CNN.

Type	Filter Shape	Input Size	Parameter
Conv. Layer (ReLU) #1	$3 \times 1 \times 7$	2×24	21
Maxpooling	1×2	$3 \times 2 \times 18$	0
Conv. Layer (ReLU) #2	$1 \times 1 \times 1$	$3 \times 2 \times 9$	3
Conv. Layer (ReLU) #3	$3 \times 1 \times 7$	$1 \times 2 \times 9$	21
Maxpooling	1×3	$3 \times 2 \times 3$	0
Flatten		$1 \times 1 \times 6$	0
FC Layer (ReLU) #1	14	$1 \times 1 \times 6$	84
FC Layer #2	6	$1 \times 1 \times 14$	84
Softmax	Classifier	$1 \times 1 \times 6$	0
Total			213

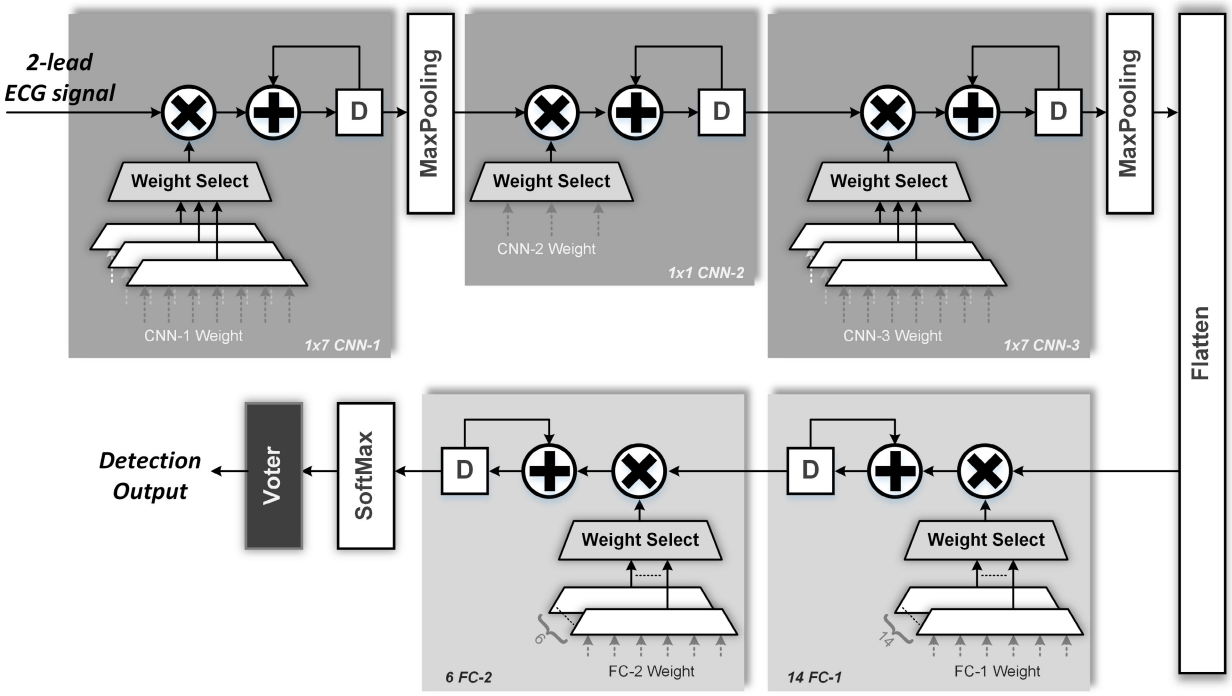


FIGURE 4. The circuit architecture of the proposed DSNN.

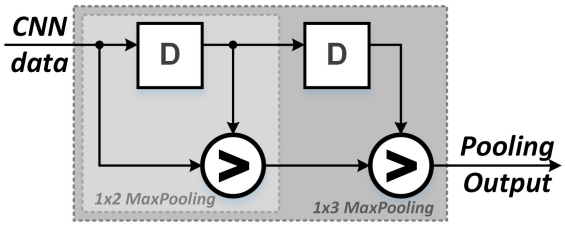


FIGURE 5. The architecture of the proposed MaxPooling module.

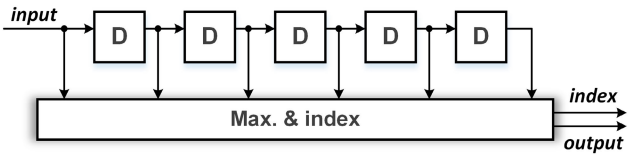


FIGURE 6. The architecture of the proposed SoftMax module.

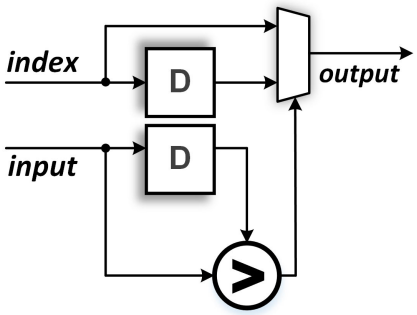


FIGURE 7. The architecture of the proposed Voter module.

TABLE 2. Chip Characteristics of the proposed DSNN chip.

Process Technology	TSMC CMOS 0.18-μm
Supply Voltage	1.8 V
Clock Frequency	20 MHz
Core Area	$790 \times 783\ \mu m^2$
Power Consumption	0.75 mW @ 20 MHz
Accuracy	97.17%

the proposed DSNN architecture to markedly minimize the circuit area while significantly boosting detection precision. The architectures of the SoftMax and Voter circuits are illustrated in Figures 6 and 7, respectively.

III. RESULTS AND DISCUSSION

A. VLSI IMPLEMENTATION

To verify performance, the chip of the proposed DSNN core was implemented using the TSMC $0.18-\mu m$ CMOS process technology. The Synopsys Design Compiler was used to synthesize the RTL code, and the Cadence Innovus was then used for placement and routing. The proposed DSNN core was operated at a frequency of $20MHz$ with a power consumption of $0.75\ mW$. The gate count was $8.6K$. Fig. 8 provides both the core layout and photomicrograph of the proposed DSNN core, and the chip characteristics are addressed in Table 2.

This study has discussed both circuit efficiency and recognition accuracy. Table 3 presents the data from simulations of our designed DSNN network, indicating the impact of adding varying numbers of FC layers after the Flatten layer.

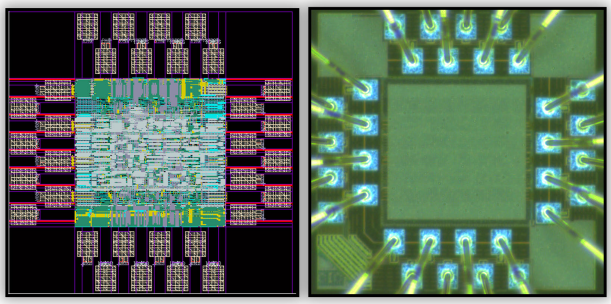


FIGURE 8. The core layout and photomicrograph of the proposed DSNN chip.

TABLE 3. A comparison of different FC layers between circuit performance and accuracy.

FC Layers	0	1*	2	3	4
Gate Counts	5.0K	8.6K	10.0K	11.4K	12.8K
Power	0.7mW	0.75mW	0.82mW	0.88mW	0.95mW
Param #	81	213	409	605	801
Accuracy	94.6	97.17	97.2	95.6	96.1

*: Propsoed DSNN.

TABLE 4. A comparison between the characteristics of circuits obtained from the designs with and without the use of the data-shifting scheme.

Design	Power	Freq.	Gate Counts	Accuracy
CNN w/o shifted	$0.73mW$	20MHz	8.41K	96.73%
CNN w/ shifted	$0.75mW$	20MHz	8.60K	97.17%

Table 3 shows that as the number of FC layers increases, the circuit area, power consumption, and the required network parameters all increase. However, the recognition accuracy does not improve correspondingly. This could potentially be due to an excessive number of neural network parameters. Thus, the neural network adopted in this research can be deemed efficient in terms of circuit performance.

B. PERFORMANCE EVALUATION AND COMPARATIVE ANALYSIS

In order to understand the contribution of the data-shifting scheme, a simple performance comparison between the characteristics of circuits obtained from the designs with and without the use of the data-shifting scheme is shown in Table 4. It is revealed from Table 4 that the data-shifting scheme design achieves a classification accuracy over 97.17%, which is a bit superior to the accuracy of 96.73% achieved by the design without the scheme. This indicates that the data-shifting scheme contributes to improved accuracy in abnormal heartbeat classification by only slightly increasing the number of gate counts. Meanwhile, incorporating the data-shifting scheme may not significantly impact power efficiency; that is, the data-shifting scheme design demonstrates clear advantages in terms of achieving higher classification accuracy while maintaining comparable power consumption. Therefore, the data-shifting scheme proves to be an effective approach for enhancing the performance of the circuit in ECG abnormal heartbeat classification.

In addition, Table 5 provides a performance comparison among a number of existing works, including the proposed DSNN. From this comparison, it is evident that the proposed work offers several advantages over the previous works. First, the proposed work achieves the highest classification accuracy of 97.17% compared to the other works, indicating better performance in abnormal heartbeat classification. Note that the results were produced by applying the proposed DSNN circuit to the ECG data drawn from the MIT-BIH arrhythmia database. Secondly, the proposed work occupies a relatively smaller area of 0.619 mm^2, making it more compact compared to the works as proposed by [16] and [17]. This is advantageous for integration and overall system design. Thirdly, the proposed DSNN circuit consumes only 0.75 mW of power, which is significantly lower than both circuits as proposed by [16] and [17]. This lower power consumption can contribute to energy efficiency and extended battery life in practical applications. Also, it should be noted that the smallest chip area and power dissipation are both achieved by the circuit as proposed by [15], but this might be because it was implemented using 65 $-$ nm technology. On the other hand, it can achieve only a modest detection accuracy at 86% which is the lowest of all these works. Furthermore, while the proposed work operates at a lower frequency of 20MHz compared to [16] and [17], it still offers a reasonable operating frequency for ECG abnormal heartbeat classification. Higher frequencies may not be necessary for this specific application, making the proposed work more power-efficient.

According to the performance evaluation as described above, one may see that the DSNN represents a significant advancement in the field of abnormal heartbeat detection, offering several potential advantages when compared to all the previously established methods [14], [15], [16], [17]. To establish the superiority of the DSNN approach and its potential benefits, a comparative analysis is further conducted as follows. While being able to provide real-time detection of abnormal heartbeats with comparably high accuracy, in comparison to Lee et al.'s SoC platform [14], the proposed DSNN achieves minimal hardware overheads so it may be more cost-effective, easily deployable, and suitable for integration into existing healthcare infrastructure. In addition, the DSNN also outperforms existing methods, especially the naive Bayes classifier used in the VLSI chip design for ventricular arrhythmia prediction [15]. This is because DSNN leverages deep learning techniques, allowing it to automatically learn intricate features from ECG signals. This surpasses the traditional naive Bayes classifier's limitations and can adapt to a broader range of arrhythmia patterns and patient profiles. Moreover, DSNN's hardware efficiency, even after being fabricated into a real chip, promises high-speed processing, small area utilization, and low power consumption, potentially outperforming existing VLSI implementations as proposed in [16] and [17]. To sum up, the proposed DSNN stands out from a number of existing studies by offering real-time abnormal heartbeat detection with high accuracy,

TABLE 5. A performance comparison of the proposed abnormal heartbeat detection chip with a number of other existing works.

Method	[15]	[16]	[17]	**DSNN**
Technology	$65nm$	$90nm$	$0.18\mu m$	$0.18\mu m$
Accuracy	86%	95.14%	94.94%	97.17%
Voltage (V)	1.0V	1.0V	1.8V	1.8V
Gate Counts	N/A	23.6K	14K	8.6K
Core Area (mm^2)	0.112	0.67	0.73	0.619
Frequency	10 KHz	125 MHz	66.6 Hz	20 MHz
Power	2.79 μW	4.18 mW	3.1 mW	0.75 mW

TABLE 6. The numbers of ECG segments used for training and testing processes for each type of ECG heartbeats.

Item	Diseases	Codename	# of train	# of test	Total
1	Normal Beat	N	4,000	500	4,500
2	Left Bundle Branch Block Beat	L	4,000	500	4,500
3	Right Bundle Branch Block Beat	R	4,000	500	4,500
4	Premature Ventricular Contraction	V	4,000	500	4,500
5	Atrial Premature Beat	A	4,000	500	4,500
6	Paced Beat	/	4,000	500	4,500
Total Heartbeats			24,000	3,000	27,000

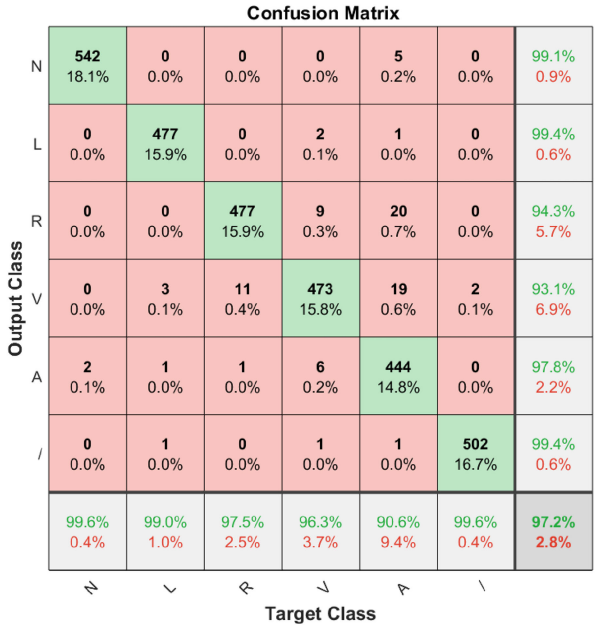
minimal hardware overheads, and cost-effectiveness. Not only ensure easy deployment and integration into existing healthcare infrastructure, DSNN surpasses existing methods by employing deep learning, enabling automatic learning of intricate ECG features, and adapting to a broader range of arrhythmia patterns. Also, DSNN's hardware efficiency promises superior speed, compact area utilization, and low power consumption, potentially outperforming existing VLSI implementations.

C. ACCURACY ANALYSIS AND DISCUSSION

Table 6 provides the numbers of ECG segments used for training and testing processes, respectively, for each type of ECG heartbeat. To assess the efficiency of the proposed chip in ECG classification, we implemented a 6 × 6 confusion matrix, as demonstrated in Table 7. Generally, this confusion matrix juxtaposes the actual labeled values against the predictions made by our suggested DSNN model, where each row represents the predicted values for the heartbeat label corresponding to that row. Table 7 displays the detection outcomes acquired from the chip for all six labeled ECG heartbeats. A glance at Table 7 reveals that the detection results achieved by our proposed chip across all ECG events could substantially exceed 90% accuracy. This suggests that our CNN chip might be effectively utilized in wearable healthcare monitoring devices.

Moreover, note that in the DSNN circuit architecture of this study, although recognition accuracy can be effectively improved with a slight increase in the circuit area, the computation time is doubled. However, this increase in computation time has minimal impact on ECG signals. Given that the operating frequency of the circuit is 20MHz, and the sampling frequency of the ECG signal is approximately 360Hz, a single DSNN computation can be completed before capturing the next 24 sample points of the ECG. This

TABLE 7. Detection results for all the six labeled ECG heart beats.



suggests that the DSNN does not compromise computational efficiency.

Furthermore, it should be also noted that real-world deployment of wearable ECG-based arrhythmia detectors faces challenges like variations in ECG signal quality due to factors like electrode placement, motion artifacts, and skin conditions. Noise, including environmental interference and muscle artifacts, can affect signal accuracy. Ensuring adaptability to diverse patient populations, as ECG patterns vary among individuals, is crucial. Overcoming these challenges necessitates robust signal processing techniques, noise reduction algorithms, and machine learning models trained on diverse datasets. Additionally, achieving user comfort,

data security, and efficient power management are essential for successful adoption and reliable arrhythmia detection.

Overall, the proposed work demonstrates a balance among power consumption, circuit area, operating frequency, and classification accuracy, making it a promising advancement in VLSI circuit design for abnormal heartbeat classification.

IV. CONCLUSION

In this paper, a novel DSNN for the detection of abnormal heartbeats is proposed. It is revealed from our study that the DSNN employs a data-shifting scheme to improve abnormal heartbeat detection accuracy. By utilizing shifted sequences and incorporating a CNN structure, FC layers, and a voting circuit, it achieves an enhanced classification performance. The architecture optimizes the circuit area by utilizing specific optimizations for the filters and matrix multiplications, ensuring efficient hardware implementation while maintaining high detection accuracy. The proposed DSNN chip was implemented using the TSMC $0.18-\mu m$ CMOS process. According to the chip characteristics our proposed DSNN chip manifests itself as a substantially small-area and high-speed design, in comparison to a number of previous works. In addition, it is also revealed from the numerical experimental results that the proposed chip can achieve 97.17% in overall detection accuracy for identifying six types of ECG heartbeats drawn from the MIT-BIH arrhythmia database. We believe our design would empower cardiologists to provide timely interventions, make precise diagnoses, assess risk levels, monitor treatments effectively, and plan long-term care strategies. These advantages make it an attractive proposition for improving cardiac healthcare and addressing the growing need for reliable, efficient, and accessible solutions in this domain, ultimately leading to improved patient outcomes, better quality of life, and reduced risks associated with cardiovascular events.

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