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RESEARCH ARTICLE

Open-Circuit Fault-Tolerant Method for Half-Bridge Switches of Three-Level Quasi-Switched Boost T-Type Inverter to Improve Voltage Gain

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ABSTRACT The three-level quasi-switched boost T-type inverter (3L-qSBT^{2}I) can feature buck-boost operating and shoot-through (ST) immunity with high voltage gain and low component voltage rating. In order to improve the reliability of 3L-qSBT^{2}I, this paper proposes an open-circuit fault-tolerant (OC-FT) method to solve OC faults of semiconductor devices. Under this approach, OC faults of half-bridge switches of the T^{2}I branch are addressed. To solve these faults, one extra normally-closed (NC) relay is integrated with the 3L-qSBT^{2}I, which connects neutral points of DC-link voltage and inverter side. In normal condition, this relay is closed and the inverter operates like a conventional 3L-qSBT^{2}I. In post-fault operation, this relay is opened and the inverter operates like a two-level inverter. A new two-level space vector modulation (SVM) scheme is introduced to control this inverter. Unlike any traditional OC-FT methods, in this proposed method, almost large voltage vectors are still used, in post-fault operating. Therefore, the voltage gain of the proposed method is increased compared to others. Comparison study and experimental results are presented to validate the proposed topology and FT method.

INDEX TERMS T-type inverter, quasi-switched boost, fault-tolerant, three-level inverter, open-circuit fault.

I. INTRODUCTION

Beside conventional two-stage inverters where a voltage-source inverter (VSI) is placed after a DC-DC boost converter, impedance-source inverters (ISIs) are attracted topologies [1], [2]. The ISIs can buck/boost output voltage in single-stage power conversion and immune to shoot-through (ST) state, which appears when all switches in any inverter branch are simultaneously gated on [1] and [2]. The first generation of ISIs is Z-source inverter (ZSI) which uses diodes, inductors and capacitors to construct impedance-source network [3]. In order to decrease capacitor voltage rating of ZSI and provide continuous input current, quasi-Z-source inverters (qZSIs) have been presented [4]. In ZSIs/qZSIs, boost factor, which is defined by ratio between DC-link voltage and input voltage, is $1/(1-2D)$, where D is ST duty ratio [3], [5]. Because ST state is inserted within zero vectors, the value of D is limited by $(1-M)$ where M is modulation index, $M \leq 1$ [3], [4], [5], [6]. As a result, the buck-boost operation of these topologies is inflexible to be controlled. Moreover, ST current, which goes through inverter side switches in ST state, is total currents of all inductor currents in impedance-source network [3], [4], [5], [6]. This ST current generates high conduction losses and switching losses of semiconductor devices and decreases system efficiency [7]. Quasi-switched boost inverters (qSBIs) were introduced to improve performance

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of ISIs compared to traditional ZSIs/qZSIs [7], [8]. Unlike ZSIs/qZSIs, qSBIs use more active switches, diodes and less inductors/capacitors than ZSIs/qZSIs [7], [8], [9]. Because of having extra switches in impedance-source network, the boost factor/voltage gain of qSBIs are very flexible to be controlled [8], [10], [11]. There are many studies reported for qSBIs to improve inductor current profile, boost factor, voltage gain and system efficiency [8], [10], [11]. Specially, three-level quasi-switched boost T-type inverter (3L-qSBT^{2}I) introduced many advantages than others [10], [11]. In literatures [10], [11], the boost factor of the inverter is defined as $2/(2-3D-D_0)$, where D_0 is extra duty ratio of boost-network switches, $D \leq D_0 \leq (1-D)$. The boost factor of the works in [10] and [11] can enhance to twice of that in ZSIs/qZSIs [10]. In literature [11], modulation index utilization is improved compared to [10], which directly enhances voltage gain and efficiency of the whole system. In summary, with benefit of high voltage gain, the qSBIs bring many advantages compared to ZSIs/qZSIs [11].

The ISIs are based on high switching frequency semiconductor devices. These devices are able to face with problems which are categorized into short-circuit faults (SCFs) and open-circuit faults (OCFs) [12]. In order to improve system reliability and stability, these problems should be taken into account [12], [13], [14]. The SCF is very serious because it generates a huge short-circuit (SC) current which goes through inverter branches [14]. This SC current can lead to the destruction of not only faulty components but also healthy parts of the system. Fortunately, with the help of impedance-source network, amplitude of SC current can be limited which ensures the safety of healthy parts of the system [14]. It gives more time for the inverter to address the SCF. Normally, the inverter is stopped whenever a SCF is diagnosed [14]. Unlike the SCF, the OCF has attracted much researchers [12], [13], [14], [15], [16], [17], [18]. Most of reports about fault-tolerant (FT) methods for OCFs were presented for 3L-T^{2}I following impedance-source networks [15], [16], [17], [18]. The OCFs of these ISIs are classified into two groups: 1) OCFs of semiconductor devices of impedance-source network, and 2) OCFs of inverter side switches. The first group of OCFs is completely done by using control methods presented in literature [17]. The second group of OCFs is divided into: 1) OCFs of half bridge switches ($F1$) and 3) OCFs of bi-directional switches or inner switches ($F2$). The simplest FT method for $F2$ introduces the faulty legs to operate like a two-level inverter with the help of healthy half-bridge switches [15], [16], [17]. The $F1$ is more serious than $F2$ [19], [20], [21], [22]. Commonly solutions for this fault are to use redundant inverter legs [19], [20]. Although they can recover amplitude of output load voltages/currents, they require more extra devices which increases weight and size of the whole system. Other solutions to reconfigure inverter under failure mode are to use FT pulse-width modulation (PWM) techniques [21], [22]. The conventional FT methods for $F1$ trigger off both upper/lower half-bridge switches of faulty phase and turn on inner-switches. Now, the faulty phase is always connected to neutral-point of DC-link voltage through healthy bi-directional switches. The phase angles of references of healthy phases are modified compared to normal operating to recover sinusoidal waveforms at output load voltage/current. The main drawback of these PWM-based solutions is that amplitude of output load voltages and currents are decreased to 1/2 that of normal condition [15], [16], [17], [18], [21], [22]. Note that the value 1/2 mentioned above is true when output load voltages are calculated as $1/\sqrt{3}MBV_{dc}$, in normal condition, where B and V_{dc} are defined as boost factor and input voltage of the inverter. When applying conventional sinusoidal-PWM method in normal operation, the value of decrement under faulty condition is $1/\sqrt{3}$. With the help of buck/boost operation of ISIs, the decrement of output voltages can be addressed by increasing DC-link voltage [15], [16], [17], [18]. However, it leads to increase component voltage ratings, under faulty condition.

This paper will present a new space-vector modulation (SVM) FT method for $F1$ to increase voltage gain of the 3L-qSBT^{2}I under faulty condition. One extra normally-closed (NC) relay is added to the neutral-points of the inverter to implement the proposed FT method. When the $F1$ occurs, this NC relay is opened, and the inverter operates like a two-level qSBI. The operating of faulty half-bridge switch is replaced by healthy half-bridge switches and bi-directional switches. As a result, most large voltage vectors are still ensured by using proposed method during post-fault operating. Therefore, the voltage gain of the proposed method is enhanced in comparison with traditional FT methods. Under this SVM strategy, the inverter can obtain following advantages.

1) The proposed method can ensure the operation of the inverter under OCF of half-bridge switches without decrement of output load voltage/current amplitude.

2) This approach can increase voltage gain of the inverter to at least $2/\sqrt{3}$ times compared to existing FT methods.

3) This method can improve component voltage ratings such as capacitor/semiconductor voltage stresses in comparison with previous FT methods.

The rest of this paper has seven sections which will detail the operation of the 3L-qSBT^{2}I under the proposed FT method and highlight its benefits. In section II, the control methods and steady-state analysis under normal and failure modes of $F1$ have been presented. Section III and IV introduce design guidelines and small signal analysis of the 3L-qSBT^{2}I. Base on small-signal models, the comments on stability of the system are presented. Power loss contribution of the proposed inverter is investigated in section V. Comparison study about voltage gain and component voltage ratings has been attached in section VI. Simulation and experimental results are presented in section VII to verify the accuracy of the proposed FT method. The summary of this paper is presented in section VIII.

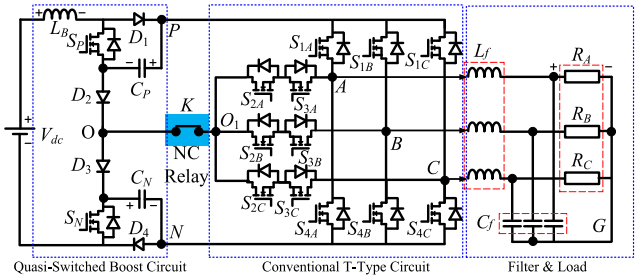

FIGURE 1. Proposed topology of 3L-qSBT^{2}I.

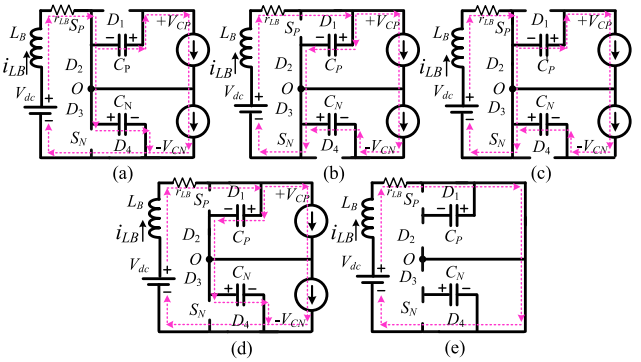

FIGURE 2. Operating modes of 3L-qSBT^{2}I under normal condition. (a)-(d) non-ST modes 1 – 4, (e) ST mode.

II. THREE-LEVEL QUASI-SWITCHED BOOST T-TYPE INVERTER (3L-qSBT^{2}I) AND PROPOSED FAULT-TOLERANT METHOD FOR HALF-BRIDGE SWITCHES

The topology of 3L-qSBT^{2}I is drawn in Fig. 1, which includes qSB circuit following by 3L-T^{2}I. In this topology, one NC relay K is added between qSB circuit and inverter side to feature FT characteristic. The qSB network is constructed by one inductor L_B, two capacitors C_P, C_N, two active switches S_P, S_N and four diodes $D_1 - D_4$. The conventional 3L-T^{2}I consists of three inverter legs, each leg is constructed by four switches $S_{1X} - S_{4X}$ $(X = A, B, C)$. Operating of the proposed inverter in normal and post-fault operation are detail below.

A. NORMAL OPERATION OF 3L-QSBT^{2}I

Under normal operating, the NC relay K is closed, which connects points "O" and "O_1" of the proposed 3L-qSBT^{2}I, as shown in Fig. 1. The inverter side has three-level output voltages which are $+V_{CP}$, 0-V, and $-V_{CN}$. Value $+V_{CP}$ is created at output voltage V_{XO} when point "P" of the qSB network is clamped to terminal "X" through switch S_{1X}. This state is called state [P]. Similarly, when switches S_{2X} and S_{3X} are simultaneously gated on, state [O] is generated which is value 0-V of V_{XO}. Value $-V_{CN}$ of V_{XO} is represented by state [N] which is generated by triggering on switch S_{4X}. Note that switches S_{2X} and S_{3X} are respectively turned on in state [P] and [N] without affecting output voltage.

Buck/boost operation of qSB network is controlled by two active switches S_P, S_N, and ST state of inverter side which is classified into five operating modes, as shown in Figs. 2(a) – 2(e). In non-ST modes 1 – 4, the inverter side operates like any conventional 3L-T^{2}I. When inverter side operates under ST mode, the output pole voltage V_{XO} is zero. So, this ST state is only appeared within zero vectors [OOO], [PPP], or [NNN]. As a result, ST duty ratio D is limited by $(1 - M)$, where M is modulation index, $M \leq 1$. The operation of 3L-qSBT^{2}I under normal condition has been detailed in [10] and [17]. In short, capacitor voltages V_{CP}, V_{CN} and boost factor B are defined as follows.

$$\begin{cases} V_{CP} = V_{CN} = \dfrac{V_{dc}}{2 - 3D - D_0} \\ B = \dfrac{V_{PN}}{V_{dc}} = \dfrac{V_{CP} + V_{CN}}{V_{dc}} = \dfrac{2}{2 - 3D - D_0} \end{cases} \tag{1}$$

where D_0 is extra duty ratio of switches S_P and S_N of qSB circuit.

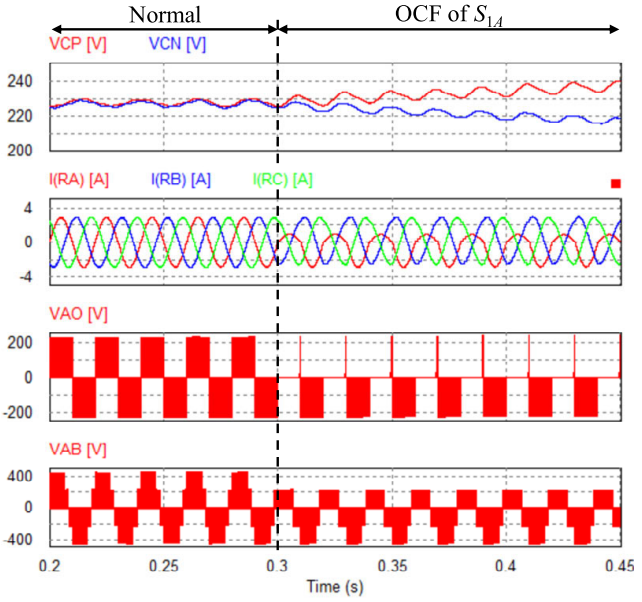

FIGURE 3. Simulation results of 3L-qSBT^{2}I under OCF of S_{1A} with 450-V of V_{PN}, 56-Ω resistor load. From top to bottom: Capacitor voltages V_{CP}, V_{CN}, output load currents I_{RX} $(X = A, B, C)$, output pole voltage V_{AO}, and output line-to-line voltage V_{AB}.

Conventional sinusoidal-PWM method has been used to controlled the inverter side, in normal operation. So, peak output load voltage $\hat{V}_{XG}$ and the voltage gain G of the inverter are defined as follows.

$$\begin{cases} \hat{V}_{XG} = M\dfrac{V_{PN}}{2} = \dfrac{MV_{dc}}{2 - 3D - D_0} \\ G = \dfrac{\hat{V}_{XG}}{V_{dc}/2} = \dfrac{2M}{2 - 3D - D_0} \end{cases} \tag{2}$$

B. FT METHOD FOR 3L-QSBT^{2}I TO SOLVE OCF AT S_{1A}

In 3L-qSBT^{2}I, OCFs are able to occur at boost switches S_P, S_N or inverter side half-bridge switches S_{1X}/S_{4X} or bi-directional switches S_{2X}/S_{3X}. This paper only focuses on OCFs at half-bridge switches S_{1X}/S_{4X}. The other OCFs are

completely addressed by previous studies [15], [16], [17], [18]. Because 3L-T^{2}I is symmetrical, the OCF of S_{1A} is considered in this section. The OCFs occurring at other half-bridge switches can be addressed by the same way as OCF of S_{1A}.

The simulation results for case of S_{1A} OCF under 450-V of DC link voltage and 56-Ω of three-phase resistive load are illustrated in Fig. 3. When the OCF occurs at switch S_{1A}, the value $+V_{PN}/2$ of output pole voltage V_{AO} represented by state [P] cannot be obtained. In positive half cycle of output load current, state [P] is replaced by state [O] because switch S_{2A} is gated on. As a result, amplitude of output load current is significantly decreased, in positive half cycle, as shown in Fig. 3. The OCF of S_{1A} also generates unbalanced capacitor voltages and significant distortion of output line-to-line voltage V_{AB}, as illustrated in Fig. 3.

In order to solve this OCF, the proposed method opens NC relay K during post-fault operating. So, in this time interval, the output voltage V_{XO} has only two-values $+V_{PN}/2$ and $-V_{PN}/2$ represented by states [P] and [N]. It is evident that states [P] and [N] of healthy phases (phases B and C) are still generated by the same way as normal condition by using two healthy switches S_{1X} and S_{4X}. In faulty phase (phase A), state [N] is still created by turning on switch S_{4A}. While, state [P] is created with the help of bi-directional switches S_{2X}, S_{3X} and state [P] of other healthy phases. For example, if the inverter operates under voltage vector [PNP], switches S_{4B} and S_{1C} are triggered on at the same time. State [P] of phase C is connected to phase A by triggering on bidirectional switches S_{2A}, S_{3A}, S_{2C}, and S_{3C}, as shown in Fig. 4.

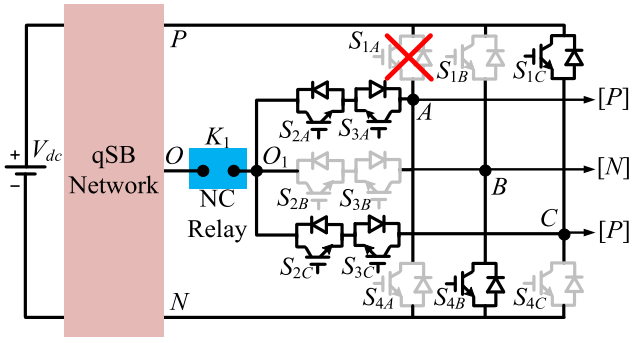

FIGURE 4. Operation of inverter under vector [PNP] with proposed FT method.

It can be seen that the state [P] of phase A is just ensured by state [P] of other healthy phases. As a result, voltage vector [PNN] is not obtained in this FT method because both phases B and C operate under state [N]. Space vector diagram (SVD) for the proposed FT method is depicted in Fig. 5. Note that vector [FFF] represents ST state of inverter side which is created by turning on all switches of 3L-T^{2}I. The SVD is divided into five sectors (I – V). In this section, dwell-time calculation and switching pattern selection are detailed. Sectors I and II are considered to be analyzed. Other sectors can be done by the same way as sector II.

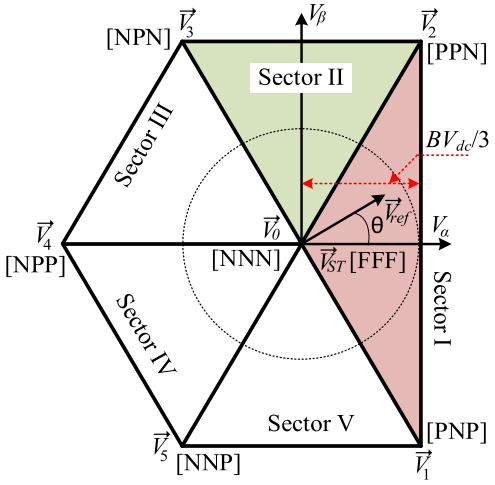

FIGURE 5. SVD of the proposed FT method for OCF at S_{1A}.

TABLE 1. Dwell-time calculation for proposed method.

Sector	Dwell-times
I	$t_1 = MT\sin(\pi/3-\theta)/\sqrt{3}; t_2 = MT\sin(\theta+\pi/3)/\sqrt{3}$ $t_0 = T-t_1-t_2-t_D$
II	$t_2 = MT\sin(2\pi/3-\theta)/\sqrt{3}; t_3 = MT\sin(\theta-\pi/3)/\sqrt{3}$ $t_0 = T-t_2-t_3-t_D$
III	$t_3 = MT\sin(\pi-\theta)/\sqrt{3}; t_4 = MT\sin(\theta-2\pi/3)/\sqrt{3}$ $t_0 = T-t_3-t_4-t_D$
IV	$t_4 = MT\sin(4\pi/3-\theta)/\sqrt{3}; t_5 = MT\sin(\theta-\pi)/\sqrt{3}$ $t_0 = T-t_4-t_5-t_D$
V	$t_5 = MT\sin(5\pi/3-\theta)/\sqrt{3}; t_1 = MT\sin(\theta-4\pi/3)/\sqrt{3}$ $t_0 = T-t_1-t_5-t_D$

C. DWELL-TIME CALCULATION

If the top of reference vector $\vec{V}_{ref}$ falls in sector I, four voltage vectors $\vec{V}_{ST}$, $\vec{V}_0$, $\vec{V}_1$, $\vec{V}_2$ are utilized to synthesize the reference vector. Relationship between these vectors is expressed as:

$$\begin{cases} \vec{V}_{ref} = \left(\vec{V}_{ST}t_D + \vec{V}_0 t_0 + \vec{V}_1 t_1 + \vec{V}_2 t_2\right)/T \\ T = t_D + t_0 + t_1 + t_2 \end{cases} \tag{3}$$

where t_D, t_0, t_1, t_2 are on-times of candidate voltage vectors $\vec{V}_{ST}$, $\vec{V}_0$, $\vec{V}_1$, $\vec{V}_2$, and T is sample time.

These voltage vectors are defined as follows.

$$\begin{cases} \vec{V}_{ref} = M\left|\vec{V}_{ref}\right|_{\max} e^{j\theta} \\ \vec{V}_0 = \vec{V}_{ST} = 0 \\ \vec{V}_1 = 2/3BV_{dc}e^{-j\pi/3} \\ \vec{V}_2 = 2/3BV_{dc}e^{j\pi/3} \end{cases} \tag{4}$$

where M is modulation index and $M \leq 1$; B is boost-factor which is defined in (1), and $\left|\vec{V}_{ref}\right|_{\max}$ is maximum amplitude

of reference vector which is defined below.

$$\left|\vec{V}_{ref}\right|_{\max} = BV_{dc}/3 \tag{5}$$

Substituting (4) and (5) into (3), the dwell-times of these candidate voltage vectors are expressed as follows.

$$\begin{cases} t_1 = MT\sin(\pi/3-\theta)/\sqrt{3} \\ t_2 = MT\sin(\theta+\pi/3)/\sqrt{3} \\ t_0 = T - t_1 - t_2 - t_D \end{cases} \tag{6}$$

Similar to sector I, if the reference vector is in sector II, four vectors $\vec{V}_{ST}$, $\vec{V}_0$, $\vec{V}_1$, $\vec{V}_3$ are used to obtain reference vector, and following equation is obtained.

$$\begin{cases} \vec{V}_{ref} = \left(\vec{V}_{ST}t_D + \vec{V}_0 t_0 + \vec{V}_2 t_2 + \vec{V}_3 t_3\right)/T \\ T = t_D + t_0 + t_2 + t_3 \end{cases} \tag{7}$$

where t_3 is dwell-time of voltage vector $\vec{V}_3$.

The voltage vector $\vec{V}_3$ in (7) is expressed as follow.

$$\vec{V}_3 = \frac{2}{3}BV_{dc}e^{j2\pi/3} \tag{8}$$

Based on (4), (5), (7), and (8) the dwell-times of these voltage vectors are calculated as follows.

$$\begin{cases} t_2 = MT\sin(2\pi/3-\theta)/\sqrt{3} \\ t_3 = MT\sin(\theta-\pi/3)/\sqrt{3} \\ t_0 = T - t_2 - t_3 - t_D \end{cases} \tag{9}$$

TABLE 2. Switching sequences for proposed FT method.

Sector	Switching pattern
I	[FFF]-[PNP]-[PPN]-[NNN]-[FFF] and return
II	[FFF]-[PPN]-[NPN]-[NNN]-[FFF] and return
III	[FFF]-[NPN]-[NPP]-[NNN]-[FFF] and return
IV	[FFF]-[NPP]-[NNP]-[NNN]-[FFF] and return
V	[FFF]-[NNP]-[PNP]-[NNN]-[FFF] and return

Dwell-time calculation for other sectors has been conducted by the same way as sector II. Table 1 summarizes dwell-times of candidate voltage vectors for proposed method. The minimum value of $(t_0 + t_D)$ is obtained in sector I. Based on (6), this minimum value is $(1-M)T$ which is obtained at phase angle $O = 0$ (rad). To ensure $t_0 \geq 0$, the maximum of ST duty ratio $D = t_D/T$ is limited as $(1-M)$.

D. SWITCHING PATTERN SELECTION

When location of reference vector is in sector I, switching sequence is selected as: [FFF]-[PNP]-[PPN]-[NNN]-[FFF] and return, which is presented in Fig. 6(a). PWM control signals of two switches S_P and S_N are also depicted in Fig. 6(a). The non-ST mode 3 is delayed by 90 degrees from ST mode to obtain good inductor current profile. In additional, duty ratios of switches S_P and S_N are also extended to D_0 to increase boost factor of the inverter. It should be evident that $D \leq D_0 \leq (1-D)$ [10], [11]. Similar to sector I, switching pattern

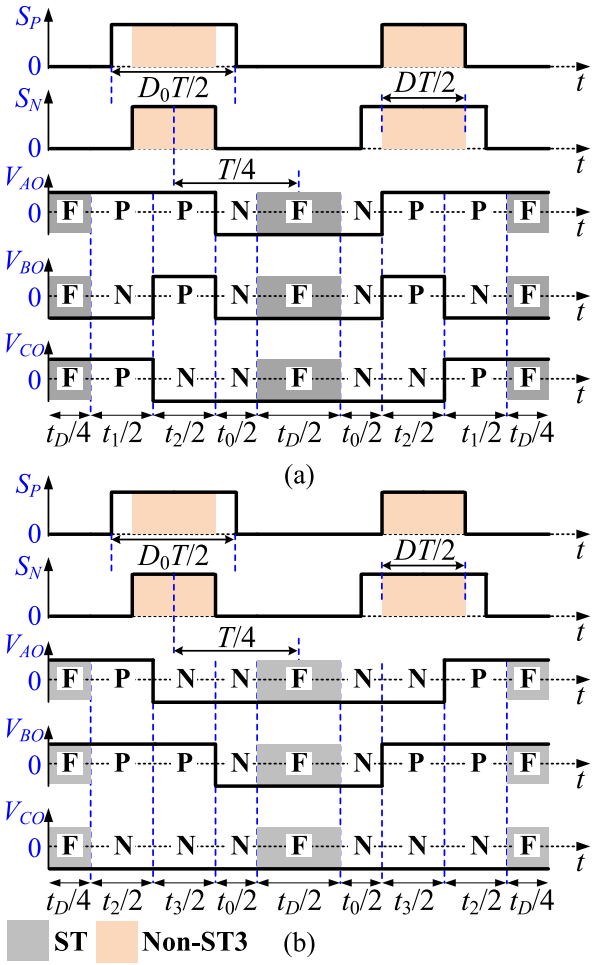

FIGURE 6. Switching patterns for sectors I and II, and control signals of two switches S_P and S_N.

for sector II is selected as [FFF]-[PPN]-[NPN]-[NNN]-[FFF] and return, which is shown in Fig. 6(b). The control signals of boost switches are the same as that in sector I. Switching sequences for other sectors are listed in Table 2.

E. STEADY-STATE ANALYSIS

In post-fault operation of the OCF at S_{1A}, the inverter has the same DC-DC operation compared to that in normal condition. Therefore, two capacitor voltages and boost factor of the inverter are still determined by (1). However, the peak-value of output phase voltage, now, equal to amplitude of reference vector, which is expressed as follow.

$$\hat{V}_{XG} = M\left|\vec{V}_{ref}\right|_{\max} = \frac{2MV_{dc}}{3\,(2-3D-D_0)} \tag{10}$$

The voltage gain of the inverter in post-fault operation is defined as follow.

$$G = \frac{\hat{V}_{XG}}{V_{dc}/2} = \frac{4M}{3\,(2-3D-D_0)} \tag{11}$$

When duty ratio D_0 obtains minimum value D, the voltage gain of the inverter is minimum. While, maximum value of

voltage gain G is achieved at value $(1-D)$ of coefficient D_0.

$$\begin{cases} G_{\min} = \dfrac{2M}{3\,(1-2D)} \\ G_{\max} = \dfrac{4M}{3\,(1-2D)} = 2G_{\min} \end{cases} \tag{12}$$

III. COMPONENT SELECTIONS

A. INDUCTOR AND CAPACITOR SELECTIONS

Key waveforms of the proposed inverter are presented in Fig. 7. The waveforms of inductor current are drawn in two cases: 1) $V_{dc} \geq V_{PN}/2$ denoted by $B \leq 2$, and 2) $V_{dc} < V_{PN}/2$ denoted by $B > 2$, as shown in Figs. 7(a) and 7(b), respectively. Based on (1), case 1 is achieved when $3D + D_0 \leq 1$, and case 2 is obtained when $3D + D_0 > 1$. For case 1, the inductor L_B stores energy in NST modes 1 – 3, and ST mode, as shown in Fig. 7(a). While, the inductor L_B only stores energy in NST mode 3 and ST mode, in case 2. Hence, the inductor L_B current ripple is calculated as follows.

$$\Delta I_{LB} = \begin{cases} \frac{V_{dc}(D+D_0-3DD_0-D_0^2)T}{L_B(4-6D-2D_0)}; \; when\, B \leq 2 \\ \frac{V_{dc}DT}{2L_B}; \; when\, B > 2 \end{cases} \tag{13}$$

The average value of inductor current is calculated as:

$$I_{LB} = \frac{P_O}{\eta\% V_{dc}} \tag{14}$$

where P_O denotes output power and $\eta\%$ is efficiency of the inverter.

The inductor L_B is chosen based on the condition $\Delta I_{LB} \leq x\% I_{LB}$, where $x\%$ is maximum value of inductor current ripple. Hence, value of inductor L_B is determined as follows.

$$L_B \geq \begin{cases} \frac{\eta\% V_{dc}^2(D+D_0-3DD_0-D_0^2)T}{x\% P_O(4-6D-2D_0)}; \; when\, B \leq 2 \\ \frac{\eta\% V_{dc}^2 DT}{2x\% P_O}; \; when\, B > 2 \end{cases} \tag{15}$$

The capacitor voltage ripples in two cases are similar, which are expressed as follows.

$$\Delta V_{Cj} = \frac{I_{PN} D_0 T}{2C_j}; \quad j = P,\, N \tag{16}$$

where I_{PN} represents equivalent current of inverter side. Similar to inductor selection, both capacitors are selected in term of $\Delta V_{Cj} \leq y\% V_{Cj}$, where $y\%$ is maximum acceptable capacitor voltage ripple. Based on (1) and (16), capacitances of C_P and C_N are determined as follows.

$$C_j \geq \frac{I_{PN} D_0 (2-3D-D_0) T}{2y\% V_{dc}}; \quad j = P, N \tag{17}$$

B. SWITCHING DEVICE SELECTIONS

All switches and diodes of qSB network are designed to block half of DC-link voltage, $V_{PN}/2$. While, all MOSFETs/IGBTs of inverter side are designed to block DC-link voltage, V_{PN}. Currents through all these switches/diodes are inductor current. The extra NC relay blocks half of DC-link voltage and carries inverter side current, I_{PN}.

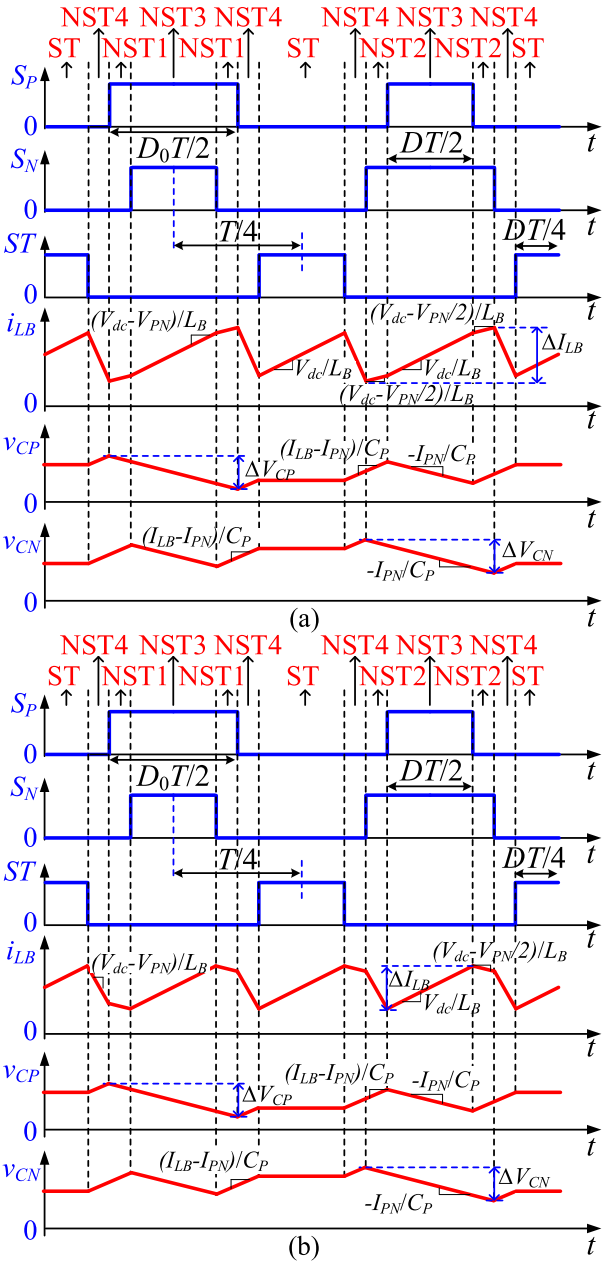

FIGURE 7. Key waveforms of the proposed inverter under (a) $B \leq 2$ and (b) $B > 2$.

IV. SMALL SIGNAL AND STABILITY ANALYSIS OF PROPOSED 3L-qSBT^{2}I

In order to analysis stability of the inverter, small signal analysis is presented. Because the proposed inverter is symmetrical, the operating of upper capacitor C_P and lower capacitor C_N are the same. Therefore, in small signal analysis, the C_P and C_N are called capacitors C, and their capacitor voltages are equal, $V_{CP} = V_{CN} = V_C$. Operating modes of the inverter are presented in Fig. 2. Series resistor r_{LB} has been added to inductor L_B to analyze small signal.

The average values of time intervals of non-ST modes 1 – 4 and ST mode are $(\bar{d}_0 - \bar{d})T/2$, $(\bar{d}_0 - \bar{d})T/2$, $\bar{d}T$,

$(1-\bar{d}_0-\bar{d})T$, $\bar{d}T$, respectively. Note that $\bar{d}$ and $\bar{d}_0$ are respectively average shoot-through (ST) duty ratio and extra duty ratios of S_P and S_N. The average values of inductor voltage $\bar{v}_{LB}$ and capacitor currents $\bar{i}_{CP}$ and $\bar{i}_{CN}$ in any switching period T are expressed as follows.

$$\bar{v}_{LB} = L_B\frac{d\bar{i}_{LB}}{dt} = \bar{v}_{dc} - \bar{v}_C\left(2-3\bar{d}-\bar{d}_0\right) - r_{LB}\bar{i}_{LB}, \quad (18)$$

$$\bar{i}_{CP} = \bar{i}_{CN} = C\frac{d\bar{v}_C}{dt} = \left(1-1.5\bar{d}-0.5\bar{d}_0\right)\bar{i}_{LB} - (1-\bar{d})\bar{i}_{PN}, \quad (19)$$

where $\bar{x}$ represents average model of signal x.

Assume that $\bar{x}$ is the sum of DC component X and AC small signal $\tilde{x}$, $\tilde{x} \ll X$. The (18) and (19) are rewritten as follows.

$$\begin{aligned} &L_B\frac{d\left(I_{LB}+\tilde{i}_{LB}\right)}{dt} \\ &= \left(V_{dc}+\tilde{v}_{dc}\right) \\ &\quad - \left(V_C+\tilde{v}_C\right)\left[2-3\left(D+\tilde{d}\right)-\left(D_0+\tilde{d}_0\right)\right] \\ &\quad - r_{LB}\left(I_{LB}+\tilde{i}_{LB}\right), \end{aligned} \quad (20)$$

$$\begin{aligned} &C\frac{d\left(V_C+\tilde{v}_C\right)}{dt} \\ &= -\left[1-\left(D+\tilde{d}\right)\right]\left(I_{PN}+\tilde{i}_{PN}\right) \\ &\quad + \left[1-1.5\left(D+\tilde{d}\right)-0.5\left(D_0+\tilde{d}_0\right)\right]\left(I_{LB}+\tilde{i}_{LB}\right), \end{aligned} \quad (21)$$

AC equations of (20) and (21) are presented as following equations.

$$\begin{aligned} &\left(L_Bs+r_{LB}\right)\tilde{i}_{LB} \\ &= \tilde{v}_{dc} - \left(2-3D-D_0\right)\tilde{v}_C \\ &\quad + 3V_C\tilde{d} + V_C\tilde{d}_0, \end{aligned} \quad (22)$$

$$\begin{aligned} Cs\tilde{v}_C &= 0.5\left(2-3D-D_0\right)\tilde{i}_{LB} \\ &\quad - 1.5I_L\tilde{d} - 0.5I_L\tilde{d}_0 - (1-D)\tilde{i}_{PN} + I_{PN}\tilde{d}, \end{aligned} \quad (23)$$

Similar to the works in [10] and [11], the output load voltages are controlled by controlling DC-link voltage V_{PN}. The DC-link voltage is controlled through two capacitor voltages using ST duty ratio D and extra duty ratio D_0. Similar to [10] and [11], the ST duty ratio D is fixed and the coefficient D_0 is used to control V_C. Based on (22) and (23), the transfer function $G(s) = \tilde{v}_C/\tilde{d}_0$ is expressed as follows. Note that this transfer function is constructed by setting $\tilde{v}_{dc} = 0$, $\tilde{d} = 0$, and $\tilde{i}_{PN} = 0$.

$$\begin{aligned} G(s) &= \frac{\tilde{v}_C}{\tilde{d}_0}\Bigg|_{\substack{\tilde{v}_{dc}=0\\ \tilde{d}=0\\ \tilde{i}_{PN}=0}} \\ &= \frac{-I_{LB}L_Bs + \left(2-3D-D_0\right)V_C - r_{LB}L_B}{2L_BCs^2 + 2r_{LB}Cs + \left(2-3D-D_0\right)^2}, \end{aligned} \quad (24)$$

In order to comment on the stability of the system, bode diagrams of the proposed inverter under normal and failure modes are drawn in Fig. 8. The parameters of L_B, r_{LB}, C, D, D_0 are listed in Table 3. Capacitor voltages V_C in normal and post-fault operating are 225-V and 300-V, respectively. With 1-kW output power, I_{LB} is determined as 5-A. It can be seen from Fig. 8, gain margin and phase margin of the system are negative. Hence, the inverter is unstable under normal and failure conditions. In general, to control the DC-link voltage, a proportional integral derivative (PID) controller must be used. With $k_p = 0.02$, $k_i = 1$, $k_d = 10^{-6}$, the system is stable with positive gain margin and phase margin, as shown in Fig. 8. Note that k_p, k_i, k_d are respectively proportional, integral and derivative coefficients of PID controller.

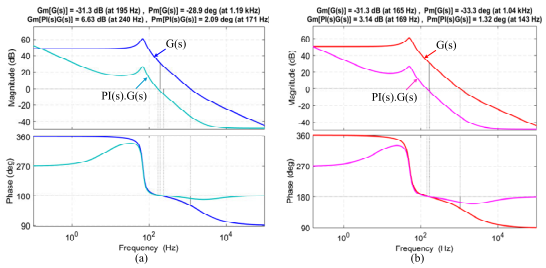

FIGURE 8. Bode diagrams of $G(s)$ and $PI(s)\bullet G(s)$ under (a) normal and (b) post-fault conditions.

TABLE 3. Simulation and experimental parameters.

Parameters/ Components		Values
DC input voltage	V_{dc}	200-V
AC output voltage	$V_{X,RMS}$	110-V_{RMS}
Modulation index	M	0.7 in normal, 0.78 in post-fault
ST duty ratio	D	0.28 in normal, 0.2 in post-fault
Extra duty ratio	D_0	0.28 in normal, 0.75 in post-fault
Line frequency	f_0	50 Hz
Switching frequency	f_s	5kHz – 10 kHz
Boost inductor	L_B	3 mH/20 A, r_{LB} = 0.5-Ω
Boost capacitors	C_P & C_N	B43640A9687M000, 680 µF/400 V, r_{esr}= 50-mΩ
LC filter	L_f & C_f	3 mH and 10 µF
Resistor load	R_X	56-Ω
Boost switches	S_P, S_N	C3M0075120, 1200-V, 30-A, $r_{DS,on}$ = 75-mΩ
Inverter side switches	$S_{1X}-S_{4X}$	12M1H060, 1200-V, 36-A, $r_{DS,on}$ = 60-mΩ
Diodes	D_1-D_4	60APF12, 1200-V, 60-A, V_F = 1.4-V
NC relay	K	BCH8-63, 400-V, 63-A, r_K = 30m Ω

V. POWER LOSS CALCULATION

Power loss of the inverter is divided into conduction losses and switching losses. The conduction losses of any devices (inductor, capacitors, relay and semiconductor devices) are calculated by square of device's current multiplied by the resistance of the component. The switching losses of proposed FT method are calculated as follows.

Switches S_P, S_N and diodes D_1-D_4 of qSB network have two switching events per switching period T. The switching voltages and currents of these switches are $V_{PN}/2$ and inductor current I_{LB}. Therefore, switching losses of these

semiconductor devices are calculated as follows.

$$P_{Sj,sw} = 2 \times \frac{1}{2}\frac{V_{PN}}{2} I_{LB} \frac{t_{ri} + t_{fu} + t_{ru} + t_{fi}}{T};\ j = P, N \quad (25)$$

$$P_{Dk,rr} = 2 \times \frac{V_{PN}}{2}\frac{Q_{rr}}{T};\quad k = 1 \div 4 \quad (26)$$

where $P_{Sj,sw}$ and $P_{Dk,rr}$ are respectively switching loss and reverse recovery loss of MOSFETs and diodes; t_{ri} and t_{fi} are current rise time and current fall time of MOSFETs; t_{ru} and t_{fu} are voltage rise time and voltage fall time of MOSFETs; Q_{rr} is reverse recovery charge of diodes.

In post-fault of S_{1A} OCF, switching losses and reverse recovery losses of switches S_{1B} and S_{4B} are respectively equal to that of switches S_{1C} and S_{4C}. Hence, switching losses and reverse recovery losses of S_{1B} and S_{4B} are taken into account. There are no switching losses for S_{1B} and S_{4B} in sector V because phase B is always clamped to state [N]. Assume that power factor is 1, the output current of phase B is determined by $i_{RB}(\omega) = I_{RB,peak} \cdot \sin(\omega - \pi/3 + \pi/2)$, where ω is phase angle of reference vector $\vec{V}_{ref}$. When $\pi/6 \le \omega \le \pi/3$, $i_{RB}(\omega) \ge 0$, locates in sector I, there are two switching events per switching period T for S_{1B} and body diode D_{4B} of S_{4B}. When $\pi/3 \le \omega \le 7\pi/6$, $i_{RB}(\omega) \ge 0$, $\vec{V}_{ref}$ locates in sectors II, III and IV. In any switching period T, there is one switching event for S_{1B} and D_{4B}. When $7\pi/6 \le \omega \le 4\pi/3$, $i_{RB}(\omega) \le 0$, there is one switching action per T at switch S_{4B} and body diode D_{1B}. However, when $-\pi/3 \le \omega \le \pi/6$, the $i_{RB}(\omega) \le 0$, there is two switching actions per T at switch S_{4B} and body diode D_{1B}. Switching currents of these devices are absolute value of $i_{RB}(\omega)$. Moreover, ST insertion generates one switching action for switch S_{1B} and S_{4B} in sectors II – IV, and two switching actions for only switch S_{1B} in sectors I and V. Switching current for ST state is $I_{LB}/2$ because there are two phases (phases B and C) carrying ST current I_{LB}. Switching voltages of these switches are DC-link voltage V_{PN}. The switching losses and reverse recovery losses of S_{1B} and S_{4B} are expressed as follows.

$$\begin{aligned} P_{S1B,sw} &= \frac{3}{2} \times \frac{1}{2} V_{PN} \frac{I_{LB}}{2} \frac{t_{ri} + t_{fu} + t_{ru} + t_{fi}}{T} \\ &+ \frac{1}{2\pi} \int_{\pi/6}^{7\pi/6} 2 \times \frac{1}{2} V_{PN} i_{RB}(\omega t) \frac{t_{ri} + t_{fu} + t_{ru} + t_{fi}}{T} d(\omega t) \\ &+ \frac{1}{2\pi} \int_{\pi/3}^{7\pi/6} \frac{1}{2} V_{PN} i_{RB}(\omega t) \frac{t_{ri} + t_{fu} + t_{ru} + t_{fi}}{T} d(\omega t) \end{aligned} \quad (27)$$

$$P_{D1B,rr} = \frac{1}{2\pi} \int_{7\pi/6}^{4\pi/3} V_{PN} \frac{Q_{rr}}{T} d(\omega t) + \frac{1}{2\pi} \int_{-\pi/3}^{\pi/6} 2 \times V_{PN} \frac{Q_{rr}}{T} d(\omega t) \quad (28)$$

$$\begin{aligned} P_{S4B,sw} &= \frac{1}{2} \times \frac{1}{2} V_{PN} \frac{I_{LB}}{2} \frac{t_{ri} + t_{fu} + t_{ru} + t_{fi}}{T} \\ &+ \frac{1}{2\pi} \int_{7\pi/6}^{4\pi/3} \frac{1}{2} V_{PN} |i_{RB}(\omega t)| \frac{t_{ri} + t_{fu} + t_{ru} + t_{fi}}{T} d(\omega t) \\ &+ \frac{1}{2\pi} \int_{-\pi/3}^{\pi/6} 2 \times \frac{1}{2} V_{PN} |i_{RB}(\omega t)| \frac{t_{ri} + t_{fu} + t_{ru} + t_{fi}}{T} d(\omega t) \end{aligned} \quad (29)$$

$$P_{D4B,rr} = \frac{1}{2\pi} \int_{\pi/6}^{\pi/3} 2 V_{PN} \frac{Q_{rr}}{T} d(\omega t) + \frac{1}{2\pi} \int_{\pi/3}^{7\pi/6} V_{PN} \frac{Q_{rr}}{T} d(\omega t) \quad (30)$$

In phase A, there is no switching loss for switch S_{4A} in sectors III and IV because phase A are always clamped to point N. In sectors I, II, and V, when $-\pi/2 \le \omega \le \pi/2$, $i_{RA}(\omega) \ge 0$, there is two switching events at body-diode of S_{4A}, in any switching period T. Moreover, the switching of V_{AO} between states [P] and [N] generates two switching events per T at switches S_{3B}, when $-\pi/3 \le \omega \le \pi/2$. In sector II and V, when $\pi/2 \le \omega \le 2\pi/3$ and $-2\pi/3 \le \omega \le -\pi/2$, $i_{RA}(\omega) \le 0$, the switching of V_{AO} creates two switching events at switch S_{4A}. There are two switching actions at body-diode D_{3B} when $\pi/2 \le \omega \le 2\pi/3$. The switching losses and reverse recovery losses of S_{3B}, S_{4A} and their body-diodes are expressed as follows. Note that switching loss and reverse recovery loss of S_{3C} and its body-diode are the same as S_{3B}. Switching voltages and currents of these switches are V_{PN} and $|i_{RA}(\omega)|$.

$$P_{S3B,sw} = \frac{1}{2\pi} \int_{-\pi/3}^{\pi/2} 2 \times \frac{1}{2} V_{PN} i_{RA}(\omega t) \frac{t_{ri} + t_{fu} + t_{ru} + t_{fi}}{T} d(\omega t) \quad (31)$$

$$P_{D3B,rr} = \frac{1}{2\pi} \int_{\pi/2}^{2\pi/3} 2 \times V_{PN} \frac{Q_{rr}}{T} d(\omega t) \quad (32)$$

$$\begin{aligned} P_{S4A,sw} &= \frac{1}{2\pi} \int_{\pi/2}^{2\pi/3} 2 \times \frac{1}{2} V_{PN} |i_{RA}(\omega t)| \frac{t_{ri} + t_{fu} + t_{ru} + t_{fi}}{T} d(\omega t) \\ &+ \frac{1}{2\pi} \int_{-2\pi/3}^{-\pi/2} 2 \times \frac{1}{2} V_{PN} |i_{RA}(\omega t)| \frac{t_{ri} + t_{fu} + t_{ru} + t_{fi}}{T} d(\omega t) \end{aligned} \quad (33)$$

$$P_{D4A,rr} = \frac{1}{2\pi} \int_{-\pi/2}^{\pi/2} 2 \times V_{PN} \frac{Q_{rr}}{T} d(\omega t) \quad (34)$$

Parameters of the proposed inverter used to calculate power loss are shown in Table 3. The power loss is analyzed under

TABLE 4. Overall comparison between proposed FT method and others under OCF of S_{1A}.

	3L-qZSI [15]	3L-qSBT^{2}I [16]	3L-qSBT^{2}I [17]	3L-qSBT^{2}I [18]	Proposed FT 3L-qSBT^{2}I
Boost factor, B	$1/(1-2D)$	$1/(1-2D)$	$2/(2-3D\text{-}D_0)$	$1/(1-2D)$	$2/(2-3D\text{-}D_0)$
Voltage gain, G	$MB/\sqrt{3}$	$MB/\sqrt{3}$	$MB/\sqrt{3}$	$2MB/\sqrt{3}$	$2MB/3$
Capacitor voltage stress, V_C/V_{dc} *	$(1-D)B/2$	$B/2$	$B/2$	B	$B/2$
Diode voltage stress, V_D/V_{dc}	$B/2$	$B/2$	$B/2$	B	$B/2$
Switch S_P/ S_N voltage stress, V_S/V_{dc}	NA	$B/2$	$B/2$	B	$B/2$
Switch S_{2X} voltage stress, V_{S2X}/V_{dc}	$B/2$	$B/2$	$B/2$	B	B
Switch S_{4X} voltage stress, V_{S4X}/V_{dc}	B	B	B	B	B
Inductors	4	1	1	1	1
Capacitors	4	2	2	2	2
Diodes	2	2	4	4	4
Boost switches	0	2	2	2	2
Unbalanced capacitor voltages	Yes	Yes	Yes	No	No
Output power	NA	200-W	1-kVA	900-W	1-kW

* only consider maximum value; NA: not applicable.

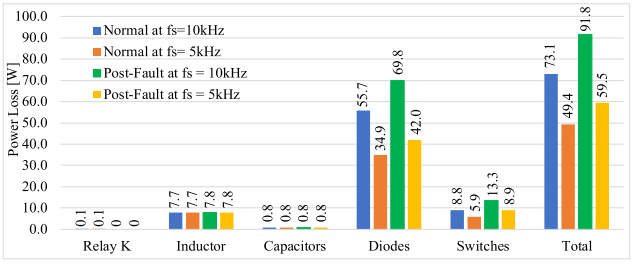

FIGURE 9. Power loss contribution of the proposed inverter under 200-V of V_{dc}, 110-V_{rms} of output load voltage and 1-kVA output power.

200-V input voltage and 110-V_{rms} output load voltages. Values of modulation index M, ST duty ratio D, and extra duty ratio D_0 for both normal and post-fault operating are listed in Table 3. With these parameters, DC-link voltage V_{PN} is boosted to 450-V in normal operation and 600-V in post-fault operation. The power loss contribution of the proposed inverter is shown in Fig. 9. This figure depicts that the power loss of the inverter under faulty conditions are higher than that in normal conditions. With 10-kHz switching frequency, total power loss of the inverter in normal operating is 73.1-W. While it is 91.8-W for case of post-fault operating with 10-kHz of switching frequency. This increment of power loss is because the switching losses of semiconductor devices in post-fault operating are higher than that in normal operating. As mentioned above, in post-fault condition, the DC-link voltage is 600-V while it is 450-V for normal condition. Moreover, the semiconductor devices of inverter side are switched at full-DC-link voltage in post-fault operating instead of half of DC-link voltage like normal condition. The increment of DC-link voltage and switching voltage are two main reasons which increase switching losses of devices. Efficiency of the inverter under normal conditions are calculated as 92.69% for 10-kHz of f_s, and 95.06% for 5-kHz of f_s. Under post-fault operation, efficiency of the proposed inverter is expressed as 90.82% for 10-kHz of f_s, and 94.05% for 5-kHz of f_s. It is clear that with higher loss, the inverter efficiency in post-fault operating is lower than that in normal condition.

VI. COMPARISON STUDY

The main contribution of the proposed FT inverter and control method is voltage gain improvement. Accordingly, voltage stresses of components are decreased. Some FT topologies based on impedance-source networks have been selected to compare with the proposed inverter to highlight these advantages. They are qSZI topology reported in [15], which is constructed by installing a qZS network before a conventional 3L-T^{2}I. The other FT topologies are 3L-qSBT^{2}I in [16], [17], and [18], which combine a qSB network and 3L-T^{2}I.

A. OVERALL COMPARISON

Overall comparison between these studies is listed in Table 4. In general, the qZS-based inverter has more passive components such as inductors and capacitors than qSB-based inverters. However, the qSB-based inverters have larger numbers of semiconductor devices. In detail, the qZSI used 4 inductors, which uses 3 more inductors than others. For number of capacitors, the qZSI has 2 more capacitors than qSBIs in [16], [17], and [18] and the proposed inverter. For semiconductor devices, the 3L-qSBT^{2}I reported in [16], [17], and [18] and the introduced topology have 2 more diodes and 2 more IGBTs/MOSFETs than qZSI in [15].

The FT methods in [15], [16], and [17] introduce healthy phases of the inverter to operate with a three-level output pole voltage. For example, when OCF occurs at switches S_{1A}/S_{4A}, phases B and C still generate three-level voltage states [P], [O], and [N] at output like normal operating. As a result, unbalancing of capacitor voltages causes distortion at output load voltages and currents. While, the unbalanced neutral-point voltage does not affect output voltage/current for the work in [18] and proposed inverter. It is because the work in [18] and the proposed FT method introduce the inverter to operate like a two-level inverter with two operating states [O] and [N] for [18], [P] and [N] for the proposed method.

B. VOLTAGE GAIN AND COMPONENT VOLTAGE STRESS COMPARISONS

Because these topologies are built based on impedance-source networks, the ST duty ratio D of inverter side is set

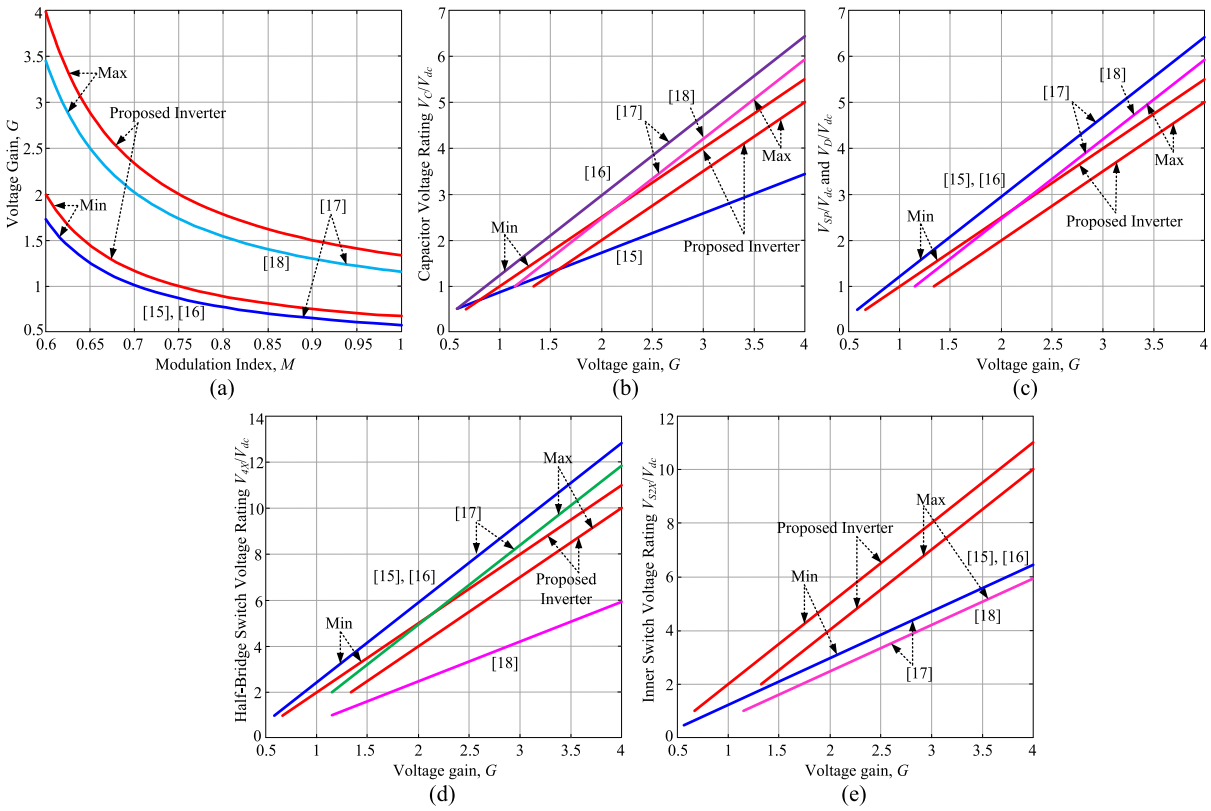

FIGURE 10. Comparison between proposed topology/method and others. (a) Modulation index *M* vs. voltage gain (*G*), (b) *Voltage gain (G)* vs. capacitor voltage stress, (c) *Voltage gain (G)* vs. boost switch/diode voltage stress, (d) *Voltage gain (G)* vs. half-bridge switch voltage stress, and (e) *Voltage gain (G)* vs. bi-directional switch voltage stress.

to $(1 - M)$ for all the works in [15], [16], [17], and [18] and the proposed inverter. For the work in [17] and the proposed method, two values of voltage gain G are considered in this section, which are minimum boost and maximum boost obtaining by setting values D and $(1 - D)$ for coefficient D_0. Comparison about voltage-gain and component voltage stresses are shown in Fig. 10. Among these topologies, the studies in [15] and [16], and minimum boost of the work in [17] have the smallest voltage gain, as shown in Fig. 10(a). The maximum boost of [17] and the work in [18] have higher voltage gain than [15], [16] and minimum boost of [17] and the proposed method. However, when applying maximum boost, the proposed inverter has highest voltage gain compared to others, as presented in Fig. 10(a). In detail, when adopting the same value M for all these works, the voltage gain G of the proposed method is $4M/[3(2M\text{-}1)]$. While the voltage gains of [15] and [16] are $M/[\sqrt{3}(2M - 1)]$, and the voltage gains of [17] and [18] are $2M/[\sqrt{3}(2M - 1)]$. It should be noted that these above values of voltage gains are obtained by applying maximum boost factors. It is clear that the proposed method can increase the voltage gain by $2/\sqrt{3}$ times than [17], [18] and $4/\sqrt{3}$ times than [15] and [16].

Because of having higher voltage gain, the proposed inverter has smaller component voltage stresses compared to others, as illustrated in Figs. 10(b) - 10(d). In detail, with value G of voltage gain, the proposed method requires value $3G/(6G\text{-}4)$ of modulation index M. The modulation indices of [15] and [16] are calculated as $3G/(6G - \sqrt{3})$. The modulation indices of [17] and [18] are expressed as $3G/(6G - 2\sqrt{3})$. It is clear that the proposed method has higher modulation index M compared to others. Meanwhile, the ST duty ratio D is maximized by $(1 - M)$. As a result, the proposed method requires smallest value of D compared to others. As listed in Table 4, having smaller value of D leads to have smaller value of boost factor B which causes capacitor and semiconductor voltage rating improvement, as shown in Figs. 10(b) – 10(d). The inverter in [15] has smallest capacitor voltage rating because it uses 4 capacitors instead of 2 capacitors in [16], [17], and [18], and the proposed inverter. In general, the voltage stresses of half-bridge switches of proposed inverter are also smaller than others, except FT method in [18], as presented in Fig. 10(d). The existing drawback of the proposed inverter is that it has higher voltage stresses of inner switches S_{2X}/S_{3X} of inverter side compared to other FT inverters, as illustrated in Fig. 10(e). It is common drawback of FT inverters which disconnect the neutral-point of DC-link with common-point of bi-directional switches, in post-fault operating [19], [20].

VII. SIMULATION AND EXPERIMENTAL RESULTS

A. SIMULATION RESULTS

Dynamic comparison between the proposed method and the work in [17] is presented in this section. The parameters used for simulation are listed in Table 3. In normal operating, both

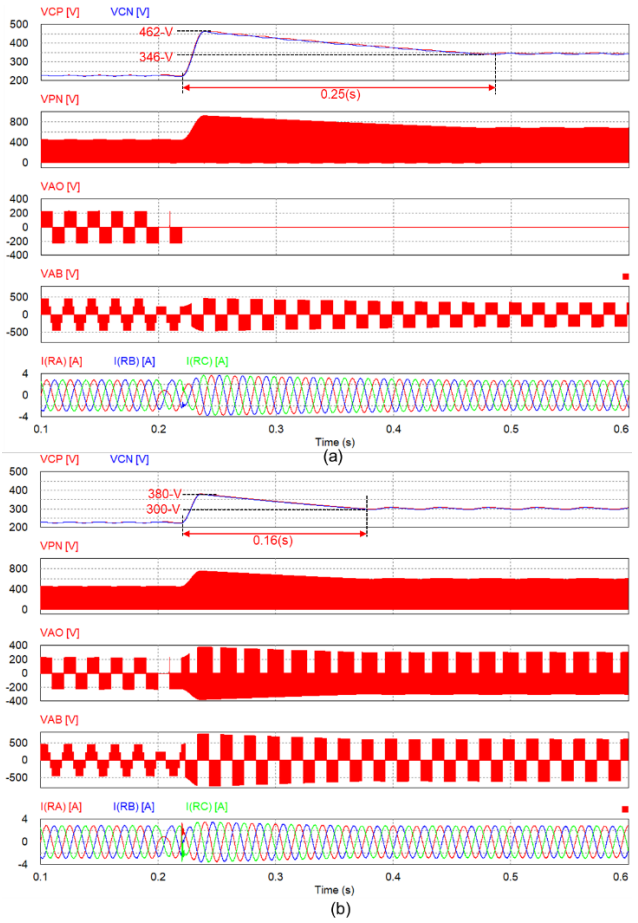

FIGURE 11. Simulation results of method in [17] and proposed method. (a) Method in [17], (b) proposed method.

the proposed method and the method in [17] are conducted with 0.7 of modulation index, 0.28 of ST duty ratio D, 0.28 of extra duty ratio D_0. Simulation results for these both methods are presented in Fig. 11.

In the simulation results, at $t = 0.2$(s), an OCF at switch S_{1A} is created. Assume that this OCF is detected at $t = 0.22$(s) and corresponding FT methods are activated to address this fault. Before $t = 0.2$(s), the inverters operate under normal condition with 225-V capacitor voltages and 450-V peak of DC-link voltage V_{PN}, as shown in Fig. 11. The output pole voltage V_{AO} has three voltage levels $+V_{CP}$, 0-V, and $-V_{CN}$. When OCF occurs at switch S_{1A}, the output voltages and currents are significantly distortion. When applying conventional FT method in [17], the inverter needs 346-V of capacitor voltages and 692-V of DC-link voltage V_{PN} at steady-state to recover amplitude of output load voltages/currents, as shown in Fig. 11(a). For method in the work [17], the modulation index M, ST duty ratio D, and extra duty ratio D_0 are respectively set to 0.78, 0.22, 0.76. Because of the increment of D and D_0 compared to that in normal operating, the capacitor voltages V_{CP} and V_{CN} and DC-link voltage V_{PN} have overshoot in transient time. Maximum values of capacitor voltages and DC-link voltage during transient time are respectively measured as 462-V and 924-V. This method needs 0.25(s) to obtain steady-state operating, as shown in Fig. 11(a).

For proposed method, the inverter needs 300-V of capacitor voltages and 600-V of DC-link voltage in post-fault operating to address OCF of S_{1A}. As a result, the modulation index M, ST duty ratio D, and extra duty ratio D_0 are set to 0.78, 0.2, and 0.75 respectively. Because of having smaller values of ST duty ratio D and extra duty ratio D_0, the proposed method has smaller capacitor voltages/DC-link voltage than [17]. According to simulation results shown in Fig. 11, the proposed method can decrease 13.3% capacitor voltages and DC-link voltage compared to method in [17]. The proposed method also has smaller peak-amplitude of DC-link voltage and capacitor voltages in transient time compared to method in [17]. It is measured that the peak values of V_{CP}/V_{CN} and V_{PN} are 380-V and 760-V, respectively. These values of capacitor voltages and DC-link voltage decrease 17.7% compared to that in method [17]. The introduced method also has smaller time duration to obtain steady-state operation than method in [17], which is measured as 0.16(s), as shown in Fig. 11(b).

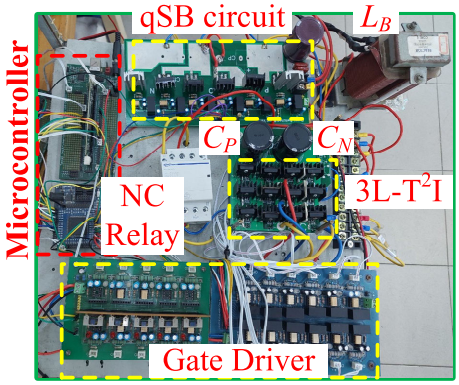

FIGURE 12. Photo of experimental prototype.

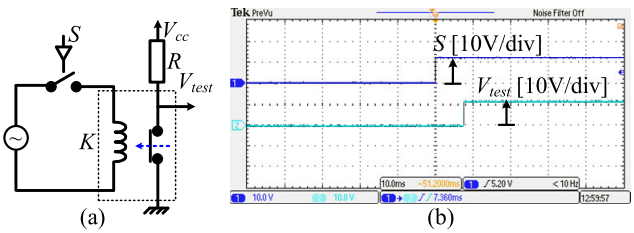

FIGURE 13. (a) Testing circuit of NC relay *K*, (b) experimental results.

B. EXPERIMENTAL RESULTS

The proposed FT method is further validated by using experimental prototype. The photo of laboratory prototype is depicted in Fig. 12. All MOSFETs 12M1H060 are applied for inverter side switches $S_{1X} - S_{4X}$. MOSFETs C3M0075120 are used for two switches S_P and S_N of qSB network. Isolated

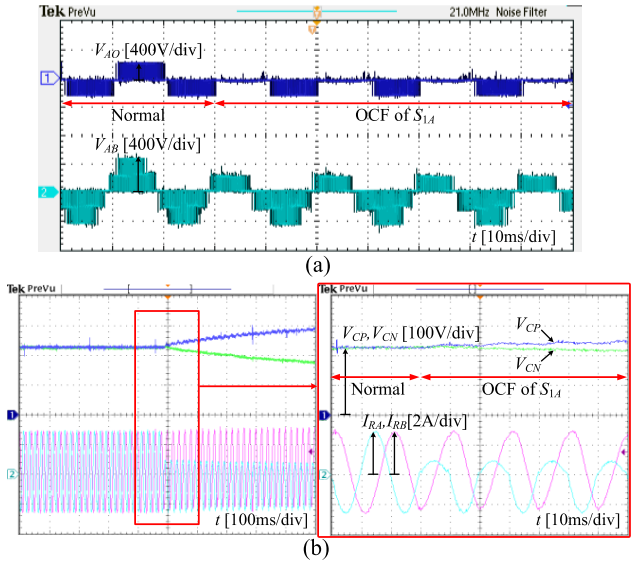

FIGURE 14. Experimental results without applying proposed FT method. From top to bottom: (a) output pole voltage V_{AO}, output line-to-line voltage V_{AB}, capacitor voltages V_{CP}, V_{CN}, output load currents I_{RA}, I_{RB}.

TABLE 5. Summary of experimental results.

	V_{CP}	V_{CN}	$V_{RA,RMS}$	$I_{RA,RMS}$	THD$_{VAB}$	THD$_{IRA}$
Normal	222-V	214-V	108-V	1.9-A	83%	0.64%
OCF of S_{1A}	-	-	-	-	119%	62.7%
Post-fault	300-V	271-V	105-V	1.85-A	140%	1.03%

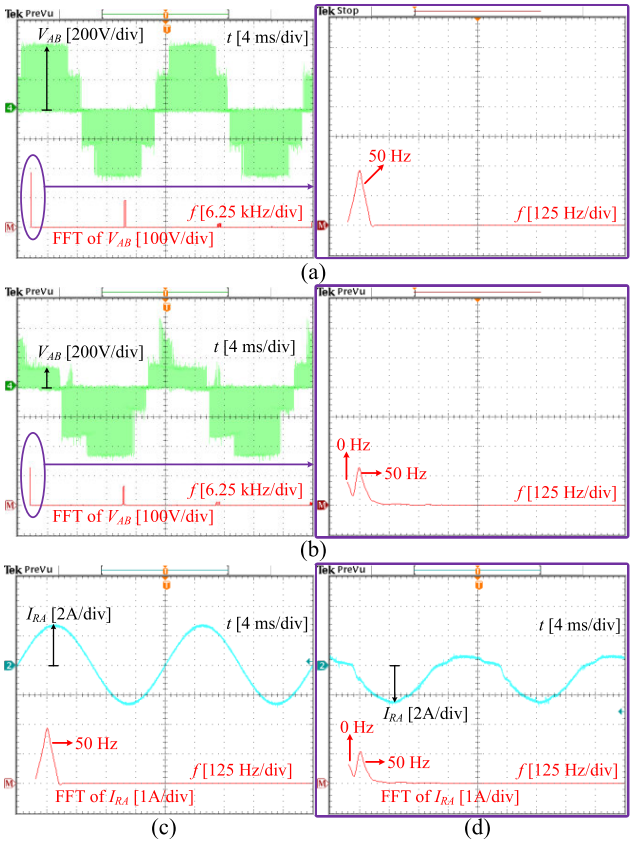

FIGURE 15. FFT spectra of V_{AB} and I_{RA} under normal and failure modes. (a), (c) Normal condition, (b), (d) faulty condition.

IC TLP250 are adopted to drive these MOSFETs. Diodes 60APF12 are installed for diodes D_1 – D_4 of impedance-source network. Microcontroller TMS320 F28335 and FPGA Cyclone II EP2C5T144C8 are used to generate control signals of inverter switches. BCH8-63 is used for NC relay K. In order to test the time to open relay K, testing circuit shown in Fig. 13(a) is built. Experimental results for this test are shown in Fig. 13(b). It shows that the time delay to open relay K is 7.36-ms. So, in experiment, the relay K is opened 7.36-ms before activating the proposed FT method. Because the experimental prototype is just built to verify the accuracy of the proposed method, so, values of output load currents are much smaller than rated current of NC relay K. In detail, the RMS values of output load current are 3-A$_{\text{RMS}}$ at 1-kVA, while the rated current of relay K is 63-A. Therefore, spark inside the relay during the opening transient is very small and can be ignored. In practice, there is no matter with the spark inside the relay during the opening transient when selecting the relay with rated current higher than output load currents.

The parameters used in experiment are listed in Table 3. Summary of experimental results is listed in Table 5. The DC input source is set as 200-V to test the proposed method. Under normal condition, three coefficients modulation index M, ST duty ratio D, and D_0 are selected as 0.7, 0.28, and 0.28. In this condition, two capacitor voltages are boosted to 222-V and 214-V. The RMS values of output load voltages and currents are measured as 108-V$_{\text{RMS}}$ and 1.9-A$_{\text{RMS}}$, respectively.

Experimental results of S_{1A} OCF are presented in Fig. 14. FFT spectra of output line-to-line volage V_{AB} and output load current I_{RA} under both normal and faulty conditions are shown in Fig. 15. It can be seen that when the OCF occurs at switch S_{1A}, two capacitor voltages are seriously unbalanced, as shown in Fig. 14(b). It results in distortion at output line-to-line voltage and output load current, as shown in Figs. 14(a) and 14(b). As shown in Figs. 15(a), and 15(c), under normal operation, THD values of V_{AB} and I_{RA} are measured as 83% and 0.64%. However, under faulty condition, these THD values are 119% and 62.7%, respectively. Moreover, unbalanced neutral-point voltage generates high amplitudes of DC components in V_{AB} and I_{RA}, which are denoted by 0-Hz components in FFT spectra of V_{AB} and I_{RA}, as depicted in Figs. 15(b) and 15(d).

Experimental results when applying proposed FT method are shown in Figs. 16 and 17. In post-fault operation, modulation index M, ST duty ratio D and duty ratio D_0 are selected as 0.78, 0.2, and 0.75, respectively. With these values of parameters, two capacitor voltages V_{CP} and V_{CN} are boosted to 300-V and 271-V, respectively, as listed in Table 5. As a result, the peak-value of DC-link voltage V_{PN} is increased compared to that in normal condition, as

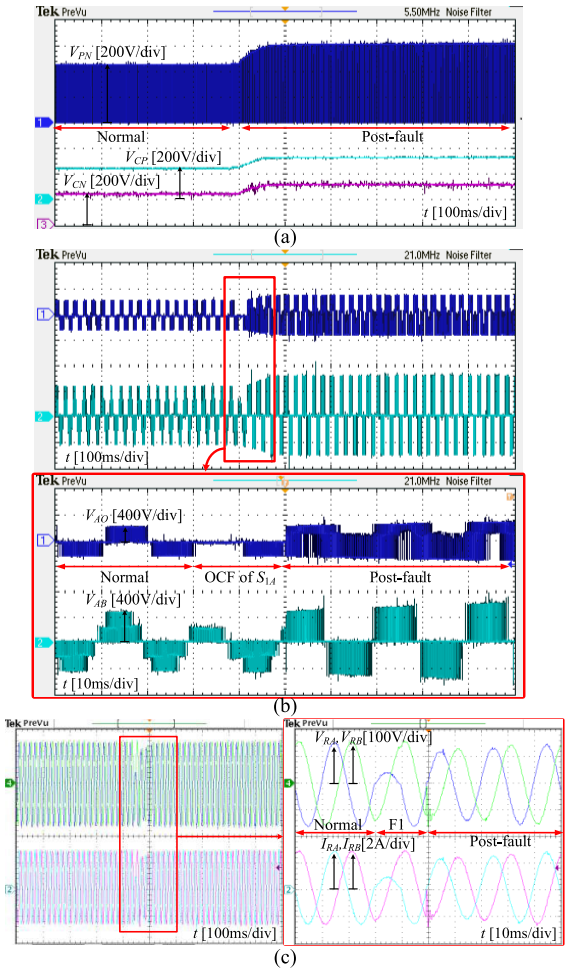

FIGURE 16. Experimental results when applying proposed FT method. From top to bottom: (a) DC-link voltage V_{PN}, capacitor voltages V_{CP}, V_{CN}, (b) output pole voltage V_{AO}, output line-to-line voltage V_{AB}, (c) output load voltages V_{RA}, V_{RB}, output load currents I_{RA}, I_{RB}.

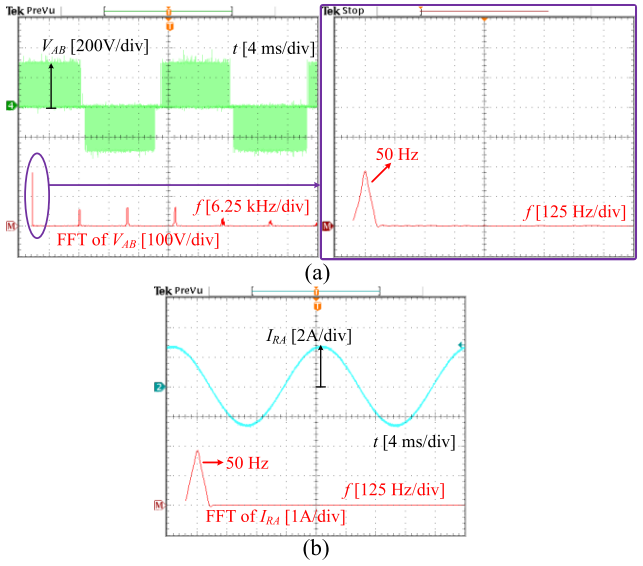

FIGURE 17. Experimental results of proposed FT methods (a) Output line-to-line voltage V_{AB} and its FFT spectra, (b) output load current I_{RA} and its FFT spectra.

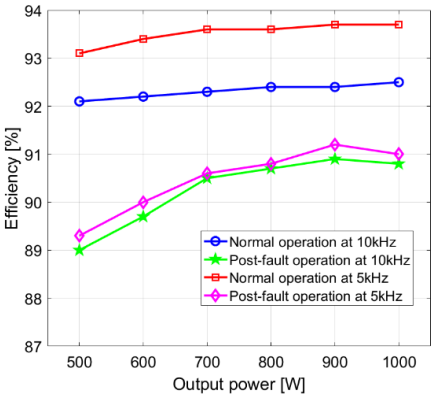

FIGURE 18. Efficiency of 3L-qSBT^{2}I under normal and post-fault operating.

presented in Fig. 16(a). Because of using ST state, the DC-link voltage waveform is varied from 0-V to peak-value of V_{PN}. The output load voltages and currents are recovered, as shown in Fig. 16(c). The RMS values of output load voltages and currents are measured as 105-V_{RMS} and 1.85-A_{RMS}, respectively. When applying introduced FT method, the amplitude of DC components of output line-to-line voltages and load currents are significantly reduced which are zero, approximately, as shown in FFT spectra in Fig. 17. In post-fault operating, the inverter operates with two-levels of output pole voltage V_{AO}, which are $\pm V_{PN}/2$, as shown in Figs. 16(b). As a result, the output line-to-line voltage has three voltage levels which are $+V_{PN}$, 0-V, and $-V_{PN}$, as shown in Figs. 16(b) and 17(a). Because of having smaller number of output voltage levels, in post-fault operating, THD values of V_{AB} and I_{RA} are higher than that in normal operation. These values are measured as 140% and 1.03%, as listed in Table 5. Although the THD of V_{AB} in post-fault operation is higher than that in faulty condition (119%), FFT spectra of V_{AB} has a very small amplitude of DC component in post-fault operation. As a result, THD of I_{RA} under post-fault operating (1.03%) is significantly reduced compared to that in faulty condition (62.7%), as listed in Table 5.

Efficiency of the inverter under normal and post-fault conditions is shown in Fig. 18. The results of efficiency are investigated under both 5-kHz and 10-kHz of switching frequency. It can be observed that when switching frequency is increased, the efficiency of system is decreased because switching losses of semiconductor devices are increased. In normal operating, the inverter obtains 92.5% and 93.7% peak-efficiency under 10-kHz and 5-kHz switching frequency, respectively. Under post-fault operating, the efficiency of the inverter is decreased compared to that in normal condition, as shown in Fig. 18. This decrement is because the conduction losses and switching losses of the inverter are increased, in post-fault operating. Firstly, in post-fault operating, the DC-link voltage of the inverter is increased from 436-V to 571-V, which increases switching voltage of semiconductor

devices. As a result, switching losses are increased. Secondly, the inverter side must turn on bidirectional switches S_{2A}, S_{3A} and switches $S_{1X} - S_{3X}$ $(X = B, C)$ of other healthy phases (see Fig. 4) to recover state [P] at faulty phase A. It results in increasing of conduction losses for this operating state. The efficiency decrement is the common drawback of FT methods [20], [21]. It is price paying for system reliability and stability.

VIII. CONCLUSION

This paper has presented a new topology of 3L-qSBT^{2}I with FT feature which can address OCF of half-bridge switches. Under this proposed FT method, the proposed 3L-qSBT^{2}I can achieve some advantages such as: 1) stepping-up/down output voltage from single input DC source, 2) ensuring output voltage under normal and failure modes of semiconductor devices, 3) improving voltage gain and component voltage stresses of the inverter under failure mode. Some comparisons about voltage gain and component voltage ratings have been included in this paper to highlight the contribution of the introduced FT method. Accordingly, the voltage gain of the inverter can be increased at least $2/\sqrt{3}$ times compared to previous FT mode for 3L-qSBT^{2}I. A 1-kVA experimental prototype is utilized to validate the accuracy of the proposed method. It is measured that the peak-efficiency of the inverter is 93.7%, under normal operating and 91% under faulty condition. In the future, optimal prototype of the proposed 3L-qSBT^{2}I will be built for grid-connected applications to increase performance of the whole systems under both normal and failure modes. With proposed FT method, the reliability and stability of the system are increased. It makes the inverter more suitable for some applications requiring uninterruptible power supply (UPS) characteristic.

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