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RESEARCH ARTICLE

4 × 4 bit Programmable Optical Memory Array With Digital Addressing Using Micro-Ring Resonators

ASSYLKHAN NURGALI[1], BIKASH NAKARMI[2], (Senior Member, IEEE), CARLO MOLARDI[3], (Senior Member, IEEE), AND IKECHI AUGUSTINE UKAEGBU[1,3], (Senior Member, IEEE)

[1]Integrated Device Solutions and Nanophotonics Laboratory, School of Engineering and Digital Sciences, Nazarbayev University, 010000 Astana, Kazakhstan
[2]Key Laboratory of Radar Imaging and Microwave Photonics, Ministry of Education, Nanjing University of Aeronautics and Astronautics, Nanjing 210016, China
[3]Electrical and Computer Engineering Department, School of Engineering and Digital Sciences, Nazarbayev University, 010000 Astana, Kazakhstan

Corresponding authors: Ikechi Augustine Ukaegbu (ikechi.ukaegbu@nu.edu.kz) and Bikash Nakarmi (bikash@nuaa.edu.cn)

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ABSTRACT The development of photonic integrated circuit (PIC) based computing systems requires efficient optical memory units, which can be challenging to implement due to the need for precise routing of optical signals. To address this challenge, we propose a 4 × 4 bit photonic non-volatile memory array system using micro ring resonators for fast and flexible memory addressing. The system uses phase change material (PCM) as a memory unit and implements wavelength division multiplexing (WDM) techniques to access memory cells through active and passive filtering by micro-ring resonators. Results show a system access speed of 30 Gbps with 50Mbps for erasing and 1.6Mbps for writing with accurate memory unit routing. This demonstration shows the potential for developing photonic non-volatile memory storage with reconfigurable memory addressing, which could facilitate the development of advanced PIC-based computing systems.

INDEX TERMS Optical memory, phase change material, wavelength division multiplexing, memory access, decoder.

I. INTRODUCTION

Over the years, photonic technologies and silicon photonics have been studied extensively for several applications in optical interconnects, sensing, digital photonics, and signal processing [1], [2]. This is due to their numerous advantages such as the ability to realize high component density, low electromagnetic interference, reduced crosstalk, high bandwidth, and low power consumption [3]. One of the significant advantages of silicon photonics is its compatibility with silicon microelectronic process. Thus, processing silicon photonics alongside the existing and mature CMOS technology, the cost of photonic devices would be drastically reduced and the integration level would greatly increase. With the increasing global demand for high-performance computing machines with multi-processors, optical interconnects, optical blocks and optical signal processing become essential as many processing units are grouped together on a single chip to meet Moore's demand curve [4]. In order to meet these demands, present electronics memory should provide greater amount of flexibility on electrical input/output bandwidth access time [5], which do not correspond with the present available on-chip computation rates [6]. This has given rise to the von Neumann bottleneck, which occurs as a result of information "traffic jam" between the processor and memory. Taking advantage of optical interconnects, routing signals between the processor and memory and vice versa is not optimal as this requires electrical-to-optical

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(E/O) and optical-to-electrical (O/E) conversions. Hence, there is need for on-chip photonic memory and memory access.

The electronics storage system, the RAM, has proven not to be capable of making pace with current trends of improvements in processing speeds [7]. Consequently, this will degrade the overall system as the present system cannot handle the memory bandwidth and requirement of less access time, and hence, forming a bottleneck, which is referred to as a ''Memory Wall'' [8]. To improve memory band access time, several works have been presented, employing the WDM technology [9], [10], [11]. However, these works either employ optoelectronic solutions [9] or implement several optical components [10], [11]. Hence there is a need for a full silicon photonics-based memory access solution employing WDM technology.

Phase change materials (PCM) are considered a promising option for implementing the next-generation memory devices due to their inherent optical and electrical properties [12]. The metastable crystalline and amorphous phases of PCM have distinct optical properties, and their phase transition can be controlled with optical and electric pulses. Additionally, their evanescent coupling with a waveguide allows them to overwrite the optical properties of the coupled section of the waveguide. This makes them ideal candidates for controlling the intensity of propagating light sources and implementing non-volatile memory in PICs [13], [14], [15]. Integrating non-volatile memories into a photonic circuit allows for the creation of photonic memory storage with multiple memory cells. However, directing optical signals to a specific memory location through the PIC requires complex procedures. One approach to solving this issue is to use wavelength division multiplexing (WDM), in which multiple wavelengths carry optical signals [16]. By integrating the memory unit with a micro-ring resonator (MRR), the memory unit only receives wavelengths at the resonance of the micro- ring resonator. This method was used by Feldmann et al, in 2019 [17] to build a 216-bit optical memory storage system, in which columns of the memory array were accessed with specific wavelengths. In [17], a waveguide with PCM was placed between two identical MRRs. In contrast, researchers in [18] and [19] placed PCM on top of a micro-ring cavity waveguide. The difference between placing it behind MRR and on top of MRR is that the former works as a weight in a linear flow system, while the latter controls resonance depth and width.

The idea of optical memory addressing with bit sequence, as well as building addressable storage is discussed in [20], [21], [22], [23], and [24]. Some of these works are based on using Mach-Zehnder Interferometer (MZI) for both role of decoder and memory cell [20], [21], [22], where authors used SOA-MZI as memory cell. In this type of memory cell, Semiconductor Optical Amplifier (SOA) sits on one branch of MZI. By controlling bias current of SOA, input signal amplified by SOA can introduce significant phase shift which can be introduced as memory state. Apart from them, Nakarmi et al. [23] used Single Mode Fabry-Pérot Laser Diode (SMFP-LD) as memory unit after decoder constructed from MZM modulators. Optical memory units also find application in building neural networks, as demonstrated by Feldmann et al. [24]. The tunability of PCM waveguides is utilized to determine the weights in the neural network. On the other hand, researchers in [25] used PCM attached to MRR, like in [17], as a non-volatile memory cell. In order to address cell, multi wavelength light inputs were sent to the storage, while multiple active MRRs filtered out unnecessary wavelengths. Overall, all of these models used WDM to address specific memory location, while efficiency and design footprint varied by designs.

In this work, we design a silicon photonics based reconfigurable memory system with memory addressing. The memory cells are integrated into a photonic integrated circuit (PIC) with a waveguide coupled to a PCM material. This enables information storage in the form of a change in optical properties, specifically the difference between the crystalline and amorphous phases. The phase change process can be accomplished by heating the PCM material with high-intensity optical pulses, which corresponds to the write/erase signal. In order to address a specific memory element, wavelength selective switch (WSS) and filtering with micro-ring resonators (MRRs) is utilized. This allows for the selection of individual memory cells within the array.

Differing from works in [20], [21], [22], and [23], this work seeks to maximize the number of memory cells in a compact space. While Narayan et al. [24] also based their design by maximizing storage, our objective is to maintain a constant optical light during the 'read' operation, with address selection performed using an electrical signal. In this approach, we identify the column element using WSS and activate/deactivate the selected row using an electrical signal.

The rest of the paper is organized as follows: Section II presents the integrated memory array structure and Section III describes the WDM-based memory array structure. Section IV presents the memory cell characteristics, while Section V describes the memory operation and analyzes the performance of the memory cell, as well as validating the memory access speed using transfer functions.

II. THE INTEGRATED MEMORY ARRAY STRUCTURE

Memory arrays are a fundamental component of digital electronics used for storing and retrieving digital information. They consist of memory cells arranged in a matrix structure, with each cell being identical and having a designated memory location. The memory cells are assigned to specific columns and row bitlines, allowing data to be delivered to or read from the array [25]. When working with memory arrays, the address decoder plays a critical role in enabling access to the memory cells. It accomplishes this by selecting a specific column or row based on the address input provided. With

a single address decoder that has N address input bits, it is possible to access up to 2^N columns or rows.

The development of memory arrays has seen the use of several types of memory units. Earlier on, read-only memories (ROM) were used, where data is programmed into the memory during fabrication, thus, making it impossible to rewrite. This was later improved with the introduction of programmable ROM (PROM), which allowed data in each MOSFET (memory cell) to be erased with ultraviolet light and then rewritten. Currently, the most widely used type of PROMs are electrically erasable programmable ROMs (EEPROM), where data erasure and writing can be done with electrical signals. The most popular type of EEPROMs today are flash memories, which have editing speeds that come close to those of volatile memories [26]. These can be classified into two types – NOR and NAND. In NOR type flash memory, information can only be erased in large block sizes or the entire memory array, while information in NAND can be erased on individual memory cells. The flexibility of NAND flash memory has made it the more commonly used type in modern technology. The proposed design in this work aims to replicate the functions of EEPROM using optical domain technology.

While the development of optical memory arrays and arithmetic units is in the early stages, they offer several advantages compared to electric storage memory units. One crucial advantage is the access speed to the memory element. In EEPROM, the access time is approximately 30-40 ns [27] and editing speed 7 us in newly proposed designs. On the other hand, the access time of optical memory arrays can be boosted up to 30 ps within the memory array, while memory editing takes around 250-600 ns [24]. These results show high speed operation potential in optical memory cells.

The memory addressing technique implemented in this work for different operations such as read/write, and erase is illustrated in Fig. 1. In Fig. 1, two 2 × 4 decoders are used for selecting the row (NAND Decoder) and column (AND Decoder) of the memory array. In the NAND decoder, all the outputs will be high except one output based upon the input combinations, whereas in the AND decoder, all outputs will be low except one output that is high. Based on the combination of decoders inputs (A, B), a particular row is selected, whereas depending on the inputs (C, D), a particular column is selected through the row activator and the WSS. When the decoder inputs A=0; B=1, the output Y2 is low, hence only bitline 1 is passed through the WSS and suppressing the optical inputs of bitline 0, bitline 2 and bitline 3. Thus, only the second row of memory array is selected for the operation. Every bitline consists of wavelengths of $\lambda 1$, $\lambda 2$, $\lambda 3$, and $\lambda 4$. On the other hand, based on the C and D inputs, one of the outputs of AND decoder will be logic high which selects the respective column of the selected row. When the column AND detector input values are C=1 and D=0, the O3 will be high, and as a result, only column three is selected. Hence, with the inputs of decoder A=0; B=1; C=1 and D = 0, the

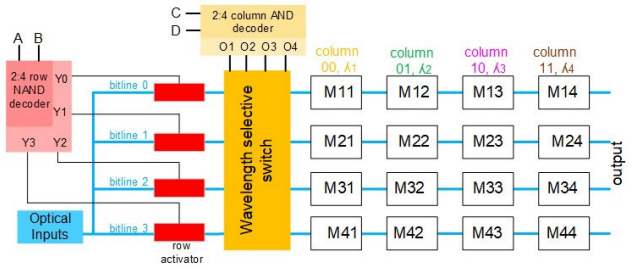

FIGURE 1. Addressing of memory array structure with wavelength selective switch. Mij are memory cells in the array. A, B, C, D - memory addressing signals.

memory location M23 is selected for the read, write and erase function.

Hence, memory locations of Mij will be accessed depending on the inputs of NAND and AND decoder where i refers for the output of the NAND decoder output with logic 0, Yi, and j refers for the AND output decoder, Oj with the logic 1. This configuration is designed so that the memory reading and writing is done in a particular column of the memory array with the only a specific wavelength, i.e., the column 1, column 2, column3 and column 4 can be accessed with only a specific wavelength, namely, $\lambda 1$, $\lambda 2$, $\lambda 3$, and $\lambda 4$, respectively.

III. WDM-BASED MEMORY ARRAY STRUCTURE

In Figure 1, NAND decoder is connected to row activators whereas AND decoder is connected directly to active MRRs in WSS, and memory cells in memory array. The structure of ROW activators connected to NAND decoder is illustrated in Fig. 2(a) with its working principle. Similarly, AND decoder connected to WSS that is responsible for passing only one wavelength belonging to a designated column in the memory array is described in Fig. 2(b). The process of chosen wavelength by WSS being selected by intended memory cell as well as its interaction with amorphous/crystalline state PCM is described in Fig.5(a).

The components for memory addressing using row and column selector are illustrated in Figure 2. The row addressing is achieved by controlling the absorption rate of the connecting waveguides using electro-optical modulation. This is depicted in Figure 2a, where the waveguide allows the propagating optical signal without absorption in the non-modulated state (Y = 0) and absorbs most of the signal in the modulated state (Y = 1). The modulated and unmodulated state is controlled through the NAND decoder inputs A, B. The electrical inputs of these active waveguides are obtained through the outputs of a NAND decoder. In this 2:4 NAND decoder, with any combinations of inputs A and B, all outputs will be logic 1 except for one output, which will be logic 0(refer to Table 1). As a result, three row waveguide sections will be modulated blocking the optical signals to pass through the waveguide leaving one unmodulated waveguide for

TABLE 1. 2:4 NAND decoder truth table.

A	B	Y_0	Y_1	Y_2	Y_3
0	0	**0**	1	1	1
0	1	1	**0**	1	1
1	0	1	1	**0**	1
1	1	1	1	1	**0**

TABLE 2. 2:4 AND decoder truth table.

C	D	O_0	O_1	O_2	O_3
0	0	**1**	0	0	0
0	1	0	**1**	0	0
1	0	0	0	**1**	0
1	1	0	0	0	**1**

uninterrupted propagation of light. Thus, the row connected with the low logic level output of the decoder is slected for the operation of memory read or write or erase function.Figure 2(b) illustrates column selector using the AND deoder and a wavelength selective switch (WSS). Figure 2(b) shows a single row and four column configuration where MRRs are connected to the optical input signal which are passed from the row selector and the output of the AND decoder. Since the decoder is AND decoder, only one output will be logic 1 and all outputs of decoder will be logic 0 as shown in Table 2. The logic 1 output of the decoder activate the MRR, and as a result, the respective MRR resonance shifts allowing the particular wavelength designed for resonance to pass through the MRR for the propagation. Whereas the MRRs with logic 0 operates normally by blocking the resonance frequency and passing all other wavelength. In Fig. 2(b) we observe the AND decoder output, O3, is logic high as a result the resonance of MRR R10 shifts from resonance wavelength $\lambda 3$ and allow to pass whereas all other MRRs blocks the wavelengths, $\lambda 1$, $\lambda 2$, and $\lambda 4$, which are the resonance frequency of respective MRRs, R00, R01 and R11, respectively. As a result, the output will be $\lambda 3$. The reason for using waveguide modulation for row and column addressing instead of PCM is high speed modulation, and switch limit of PCM materials [28].

The memory structure involving wavelength selection of a particular cell in a row is presented in Fig. 3. This arrangement features an incoming signal with wavelengths $\lambda 1$, $\lambda 2$, $\lambda 3$, and $\lambda 4$, alongside micro-ring resonators (MRRs) distinguished by radii R1-R4. These MRRs are designed to exhibit resonance conditions that permit only specific wavelengths to enter their cavities, with each of the four MRRs configured to resonate at one of $\lambda 1$-$\lambda 4$. By overlaying phase change material (PCM) onto these MRRs, individual optical memory units can be formed. In the amorphous phase, the signal of the chosen wavelength couples with the designated MRR, resulting in reduced output intensity. Conversely, in the crystalline phase, the MRR's extinction depth markedly decreases due

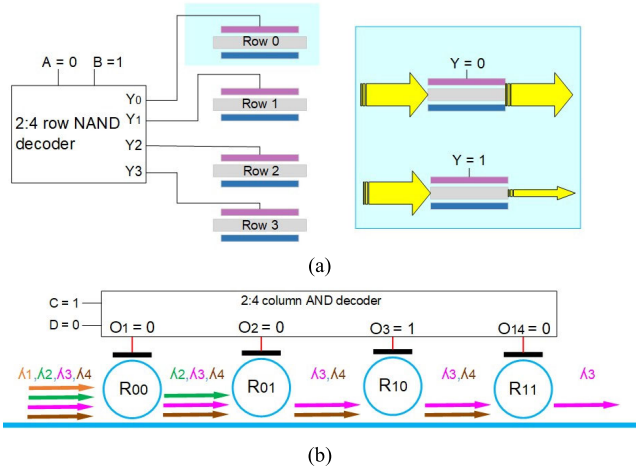

FIGURE 2. The structure of row (a) and column (b) selectors with their optical parts attached to decoders.

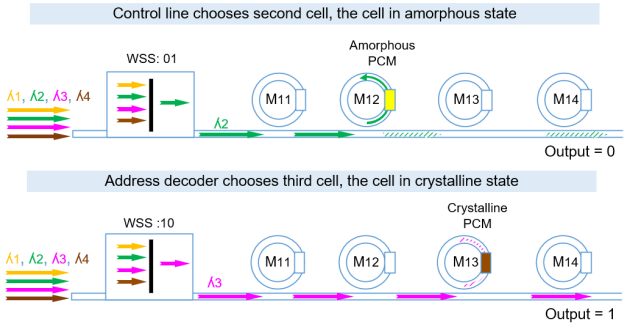

FIGURE 3. Structure of the proposed optical memory array.

to the undercoupling effect, caused by a significant rise in the PCM's absorption coefficient. Consequently, a substantial portion of the signal reaches the output without interacting with the MRR [29]. This methodology facilitates the retrieval of data from a specific memory cell at the output, with memory cell conditions corresponding to the HIGH - crystalline and LOW - amorphous states. This is displayed in Fig.3, the process is as follows: With the wavelength selective switch (WSS) choosing the second column cell and crystalline PCM, signal intensity at the output diminishes. In contrast, when the WSS selects the third column cell with crystalline PCM, a significant portion of light reaches the output.

The detailed illustration of the design of memory cells matrix with memory addressing technique is shown in Fig. 4a. The row activator and wavelength selective switch are used to address the specific memory location and based upon the read, write/erase pulse, a specific memory operation is carried out. The write pulse has wider pulse width with low power, whereas the erase signal has short pulse width with high power. In the configuration, the resonant frequencies of the non-modulated active MRRs are precisely engineered to align with the resonances of the MRRs integrated into

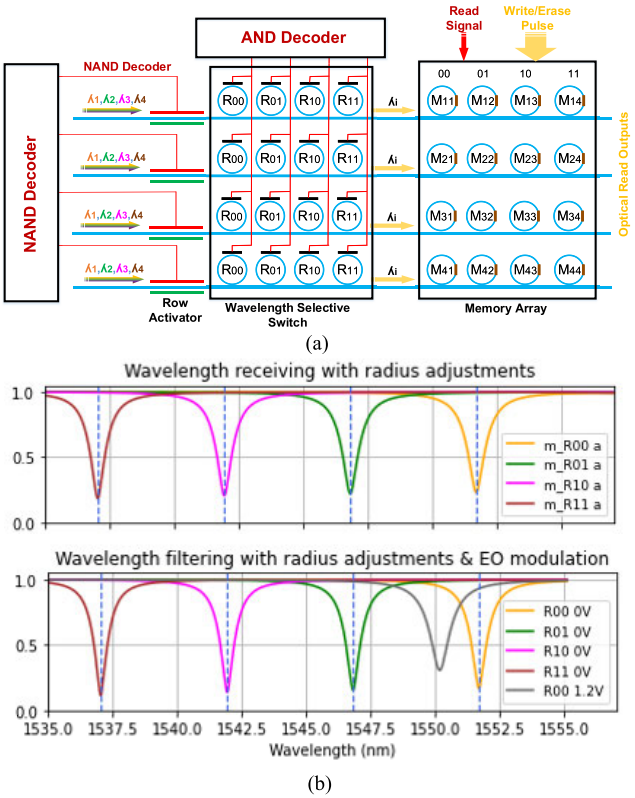

FIGURE 4. **(a) Schematic of a 4 × 4 optical memory array with address control via 4 active MRRs. (b) Spectrum of resonance states created by different length active MRRs at WSS part and matching resonances of memory array columns.**

the memory elements (Fig. 4b). As the signal containing four wavelengths corresponding to these resonances enters the system, all wavelengths are effectively filtered by coupling into the cavities of the non-modulated active MRRs. However, if any of these MRRs undergo modulation (R_{00} 1.2 V), it produces a resonance shift and signal at resonant wavelength passes through WSS section without coupling to MRRs in it. Subsequently, the selected wavelength interacts with the memory unit of an MRR whose resonance aligns with the signal's wavelength.

In the simulation, we used 1.2 a.u. modulation voltage to change the position of resonant state of each active MRR at WSS part. Regarding the selection of 4 specific wavelengths with even spacing, the radii of 3.84, 3.82, 3.8, and 3.78 um for MRRs at WSS part and memory array units were implemented. As for the row activators, we used 60 um long p-i-n doped waveguide that increases its waveguide loss drastically upon modulating with 2 a.u. voltage.

IV. MEMORY CELL CHARACTERISTICS

In this section, memory units based on PCM in MRRs are discussed. For the design of each memory cell, we propose the utilization of Germanium Antimony Tellurium, GeSbTe (GST), as the Phase Change Material (PCM) atop Micro-Ring Resonators (MRRs) within the memory array section. The optical properties of GST, as investigated and documented in [30], reveal refractive index values of 3.94 + i0.045 for the amorphous phase and 6.11 + i0.83 for the crystalline phase. While GST was chosen due to its favorable switching characteristics using optical pulses, it is important to acknowledge that a PCM featuring a substantial change in absorption index but minimal alteration in refractive index could offer smoother operational performance for this model. Fig. 5 showcases the effect of distinct GST (Germanium Antimony Tellurium) states on the optical properties of the Micro-Ring Resonator (MRR) memory cell through Lumerical simulations. In Fig. 5a, the amorphous phase of GST leads to decreased absorption and refractive index, thus preserving the MRR's pronounced extinction depth. Consequently, a substantial portion of the resonant wavelength signal at the coupling section efficiently couples into the ring cavity. Conversely, in the crystalline phase (Fig. 5b), reduced light coupling occurs due to under-coupling and resonance shift. These contrasting coupling behaviors and resonance characteristics between amorphous and crystalline GST are visually demonstrated in Fig. 5c, where MRRs containing amorphous and crystalline GST exhibit noticeable disparities in resonance depths. The operational signal bears a wavelength corresponding to the resonance of the MRR with PCM in the amorphous phase, thereby allowing light to couple into the MRR, resulting in diminished output intensity. Consequently, the phase transition from amorphous to crystalline is referred to as the 'write' process, leading to the restoration of output intensity, while the reverse is termed the 'erase' process.

In the simulation, rib waveguides were employed to enable electro-optic modulations. The waveguides had a consistent width of 0.4 um, ridge height of 0.15 um and a slab thickness of 0.08 um. At wavelength selection section, p-n junction with a concentration of $5^{*}10^{17}cm^{-3}$ was incorporated to the MRRs with radii of 4 um. The small radii and doped waveguides were used to enhance cavity losses. While active MRRs employed p-n type (Fig. 6a) waveguide modulation for the WSS, active waveguide at row selection used p-i-n structure (Fig. 6b) to pass signal uninterrupted during non-modulated state.

For the memory cell waveguide, a 10 nm thick GST layer measuring 1 um in length was positioned on the waveguide (Fig. 6c). To safeguard it from oxidation, a layer of Indium Tin Oxide (ITO) with identical dimensions was placed atop the GST layer, following the approach described in reference [29]. The dimensions of the GST layer were thoroughly selected to optimize the contrast change between phases and ensure a uniform phase transition along its length. The detailed model of the memory cell is displayed in Fig. 3a, with the direction of the erase/write signal.

V. MEMORY OPERATION

In the memory operation, data can be written to, erased or read from a selected memory cell. Memory cell selection as

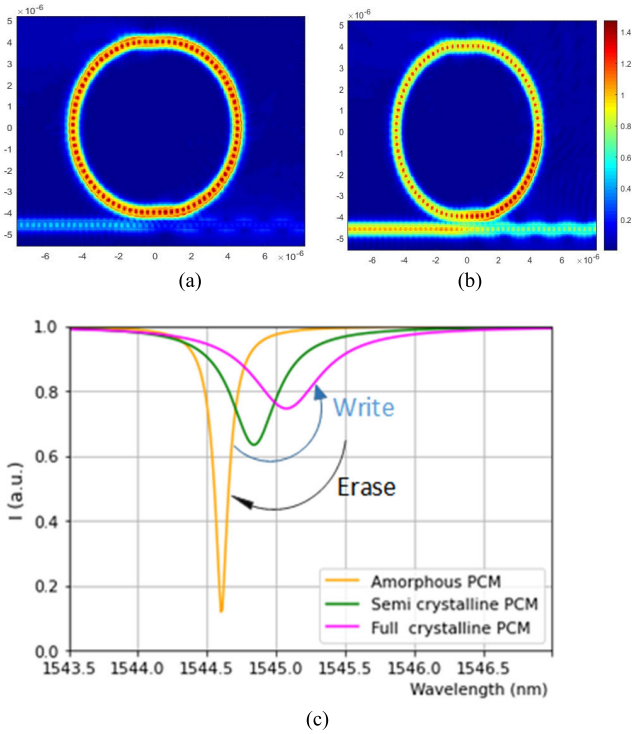

FIGURE 5. (a-b) Finite element Mode simulation of MRR with coupled PCM in (a) amorphous and (b) crystalline states. (c) The change in transmission for an individual memory cell showing Write/Erase cycling, corresponding to amorphous and crystalline states of thePCM.

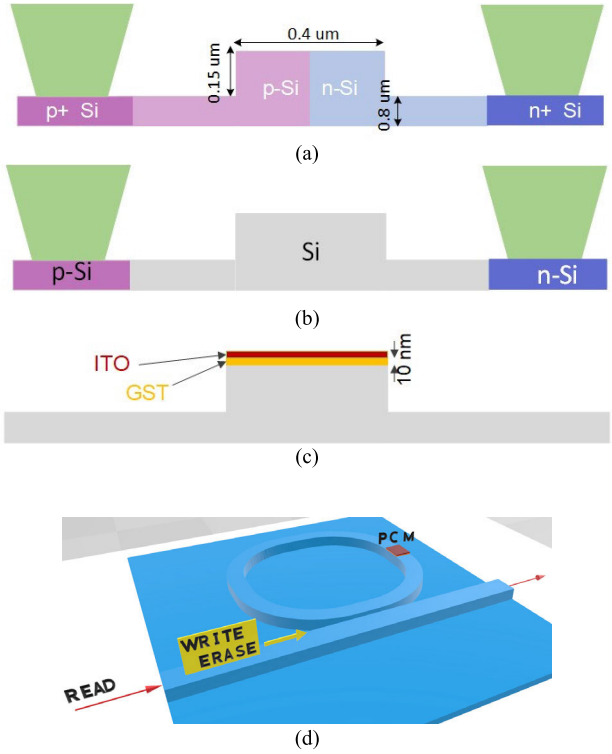

FIGURE 6. Cross section of the waveguides: (a) active MRR's waveguide at WSS section, (b) at row activator's, (c) at memory cell's. inputs, (d) Optical memory cell.

described in section II is controlled by the A and B inputs for the row selector and C and D inputs for the column selector. For example, for memory operation to occur in M23, A=0; B=1; C=1; and D=0. While the write/erase operation occurs when the appropriate pulse signals are sent to the selected MRR, the read operation occurs when there is no write/erase signal. The write/erase signals are optical signals.

A. READ OPERATION

Time domain results of the memory reading is displayed in Fig 7. Here column decoder chooses columns 00, 01,10,11 by sending voltages to active MRRs R_{00}, R_{01}, R_{10}, R_{11} at WSS section one after another. These input control signals are shown in Fig. 7a. As a result, optical signals with wavelengths corresponding to the given modulation state, probes/selects memory cells at assigned time. The results are shown in Fig. 7b where each subplot shows optical signal probing each memory, with their PCM in the crystalline state except for last subplot, to show transmission difference in '1'and '0' states of memories. The simulation is carried out at 30 Gbps speed, where reading from one cell took 33 ps.

B. MEMORY WRITE/ERASE OPERATION

To estimate the memory editing process, we conducted a simulation of the PCM (Phase Change Memory) waveguide using Comsol Multiphysics. Fig. 8a shows the cross-section of the PCM waveguide during the optical heating simulation. Here we spread heat through the upper center section of the waveguide as much of light travels through this section during coupling to PCM. By adjusting the heat rate to a certain degree, crystallization and amorphization processes were simulated in the platform, which helped to identify the required heat rate and duration for these processes.

For amorphization, it is necessary to raise the PCM temperature to the melting point (670 °C for GST) and then rapidly cool it. On the other hand, crystallization requires maintaining the PCM temperature between the crystallization temperature (160 °C for GST) [31] and the melting point for a sufficient amount of time, allowing the PCM molecules to form a crystalline structure.

In the simulation, we used a 50 mW, 20 ns heat pulse to raise the PCM temperature to the melting point (Fig. 8b), while crystallization was achieved using 11 pulses with a duration of 600 ns (Fig. 8c). Each of these pulses had a duration of 20 ns, with a 3 ns gap between them. The amplitude of the first pulse was 20 mW, and the amplitudes of the following pulses decreased due to the conversion of the PCM from the amorphous phase to the crystalline phase. This conversion led to undercoupling of the MRR, subsequently reducing the resonance depth. As a result of the decreased resonance depth, the intensity of the coupled light

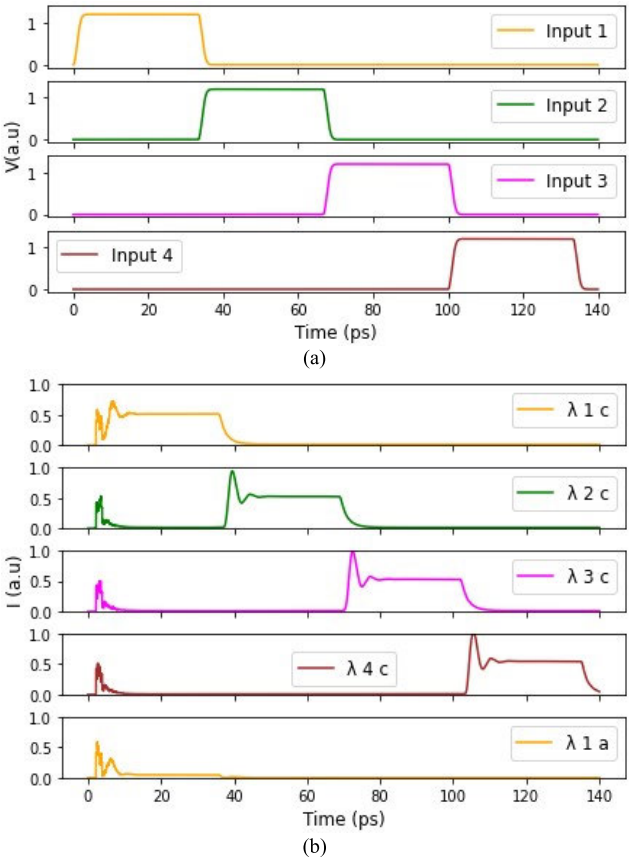

FIGURE 7. Time domain results of simulation with 4 column MRRs switch: (a) modulation voltage inputs to single MRR switch, (b) output read signals from memory cells in crytalline state respective to modulation voltage inputs.

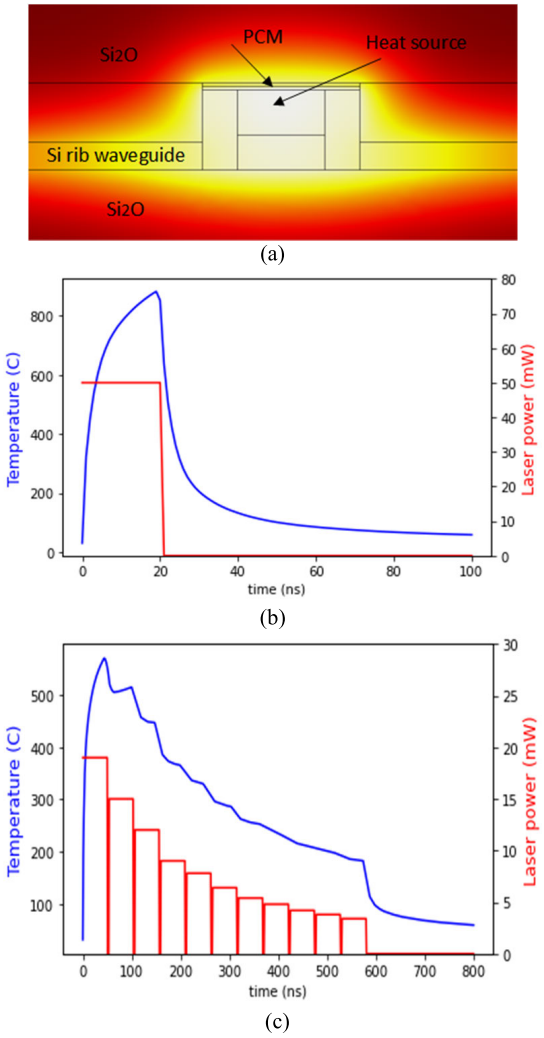

FIGURE 8. (a) PCM waveguide cross section model for Comsol simulation. (b) Amorphous and (c) crystalline heating results from Comsol Multiphysics.

into the ring cavity drops. Based on the results, the design achieves a 50 Mbps erase speed and 1.6 Mbps write speed, which corresponds to 20 ns and 600 ns erase and write time, respectively.

C. OPTICAL NONLINEARITY AND TRANSFER FUNCTION ANALYSIS

The results presented in read speed of this work study did not address the effects of intensity carried by the four wavelength signals propagating through the same waveguide. These effects are associated with third-order nonlinear optical processes, including self-phase modulation (SPM) and four-wave mixing (FWM). SPM is a nonlinear optical phenomenon that occurs when an optical pulse travels through a material with a varying refractive index induced by the Kerr effect, a third-order nonlinear effect that causes the refractive index of a material to vary with the intensity of the light passing through it [32]. This dependence on intensity is linked to the change of refractive index caused by excessive charge carriers generated by light intensity. On the other hand, FWM refers to the absorption of propagating optical signals with different wavelengths, producing a signal with a new wavelength over long length of waveguide [33]. These processes are relevant to the proposed model, which utilizes high-intensity optical signals for memory data rewriting and four wavelengths for multiplexing.

To reduce the effect of Kerr nonlinearity in electro-optic modulators, researchers in [34] and [35] emphasized the use of a p-i-n junction to sweep the free carriers generated by two-photon absorption (TPA) with voltage. Similarly, we incorporated a p-i-n modulator in the optical wavelength selecting part to reduce nonlinearity in the read process. Since 'erase' pulse carried high intensity signal, we added waveguides in direction of each column section, which can erase entire column at once. This method ensures that nonlinear effects do not hinder the 'erase' operation. We utilized Lumerical MODE and employed the nonlinear Raman and Kerr Chi3 material model to simulate our design with 4 wavelengths (Fig.9). The simulation was based on the design of 4 MRRs coupled to main waveguide posing as memory elements as in proposed design and all pass MRRs as wavelength selective switch.

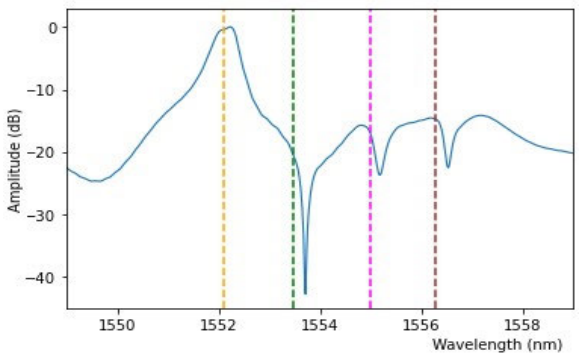

FIGURE 9. Optical spectral result of the design considering nonlinear effects.

The signals also pass through the coupling region of four MRRs, each with varying length. To demonstrate one state of memory at the output, we kept the selected MRR's PCM in the crystalline phase. With MRRs having a 4 um radius and a spectral interval of 1 nm between optical inputs, Fig. 9 depicts the simulation results. The resonance wavelengths before the nonlinear shift are represented by the dotted lines in the figure. The spectral results of the simulation reveal a significant shift in resonance, underscoring the importance of taking this effect into account.

To analyze the relationship between rise/fall time and parameters of a photonic integrated circuit (PIC), the transfer function analysis is commonly used. By obtaining the transfer function of the model and observing the step response with different parameter values, the impact of these parameters on the rise/fall time can be evaluated. For our design, we need to find the transfer function of the of the through port of the MRRs for the wavelength selecting part and the through port of the MRR for the memory cells. Additionally, the effect of connecting waveguides should be considered. The transfer functions of these individual parts can be expressed as follows [36]:

$$H_{\text{ap}}(z) = \frac{\tau - a_{rt} z^{-1}}{1 - \tau a_{rt} z^{-1}} \tag{1}$$

$$H_{\text{w}}(z) = e^{-\alpha L} z^{-\frac{nL}{cT}} \tag{2}$$

In these equations, τ represent the transmission coefficient. The term a $a_{rt} = e^{-\alpha \pi R}$ represents the round-trip attenuation factor, where α denotes the propagation loss. Although the numerator in the transfer function contains a square root, it can be modified by multiplying the waveguide length L to produce a half delay, resulting in a full delay (z^{-1}).

However, these equations only represent optical signal coupled into all pass microring resonator, thus intensity declining at exponential decay. For continuous input signals, these transfer function will be applied when step signal modulation is switched off (Fig.10a,b). As for transient response at the start of step signal due to stored light releasing at resonance shift process, it can be visualized using transfer function for

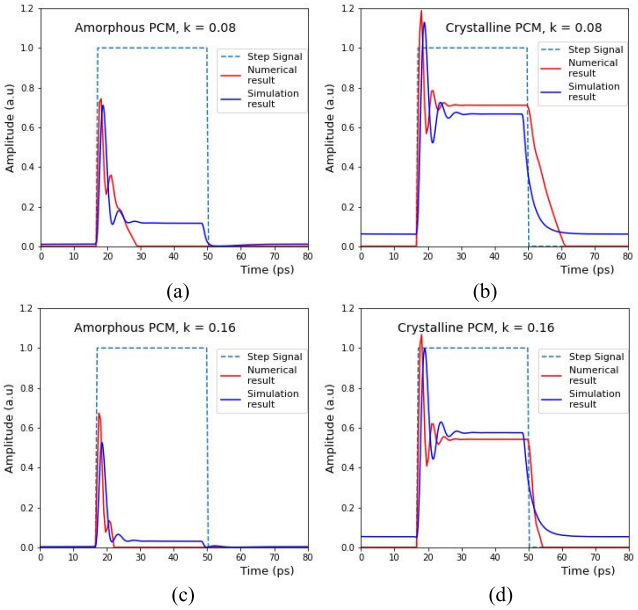

FIGURE 10. Transfer model response with 33 ps step signal. The figures include PCM readings at amprphous and crystalline phase at coupling coefficient (k) of 0.08 (a,b) and 0.16(c,d).

transient process [37]:

$$H_{tr}(z) = \frac{w_n^2}{z^2 + 2\zeta w_n z + w_n^2} \tag{3}$$

Here, w_n is natural frequency, which is the measure of how quickly the system responds, and ζ is the damping ratio. Both values range between 0 and 1 depending on the system.

The results of the model based on Equations 1-3 are presented in Fig. 10. The figure illustrates the signal output obtained from the transfer function model during a 33 ps uniform modulation, equivalent to a 30 Gbps operation. Fig. 10a displays the optical read output from the memory array in the amorphous phase of PCM, while Fig. 10b corresponds to the crystalline state. The numerical solutions derived from Equations 1-3 were compared with simulation results from Lumerical. Notably, the importance of setting the coupling coefficient to 0.08 for Fig. 10 (a) and 10 (b), and 0.16 for Fig. 10 (c) and 10 (d) is emphasized. The coupling coefficient determines how quickly light couples in and out of the MRR. A larger coupling coefficient corresponds to a faster response time but decreases the output intensity to a small extent. This is shown in the bottom figures, where they have faster decay rate and overall lower amplitude.

Upon comparing the results obtained from the numerical method and simulation, a high degree of similarity is observed, underscoring the accuracy of the transfer function model. The intensity decay in the transfer function model closely mirrors the results obtained from our proposed design in Ansys Lumerical under the same circumstances. Additionally, the model successfully captures the spikes at the onset of the modulation signal, which is attributed to light being

TABLE 3. Comparison of our work with other works.

	[17]	[24]	[25]	[27]	**This work**
Memory cells	256	16	up to 32x32	1024x1600	**16**
Number of MRRs	512	16 microcombs	Up to 2x32x32	-	**32**
Column selecting	WDM (off-chip)	WDM (on-chip)	WDM (on-chip)	on-chip	**WDM (on-chip)**
Row selecting	outside	none	on-chip	on-chip	**on-chip**
Address inputs (electrical)	none	16 (VOAs)	up to 32x32	column+ row decoder inputs	**4**
optical inputs/ outputs	2/16	4/4	up to 32/32	none	**4/4**
Memory editing	on-chip (from outputs)	-	on-chip (from inputs)	on-chip	**on-chip (from inputs)**
Access speed		13 Gbps	40 Mbps (25ns)	30 ns (33 Mbps)	**30 Gbps**
Footprint	1000 × 2400 μm^2	-	-	1.271 mm^2	**300x220 um**
Erase	50 ns (200 pJ/16)	-	25ns (180 pJ /32)	2ms /page	**20 ns (16 pJ)**
Write	150-650ns (310-890 pJ/16)	-	250ns (130 pJ /32)	8 µs /8 bit	**600 ns (32 pJ)**

trapped in the ring cavity during the resonance shift of the MRR. The PCM portion of the ring was also considered in the transfer function simulation, where the bending loss was set to the respective PCM state. This influences Equation 1, by decreasing value of a_{rt} greatly at crystalline state of PCM compared to the amorphous state, and thus resulting to the disparity in the plots.

Table 3 shows the comparison of our work with other works. Similar to EEPROM, the characteristics of optical memory arrays are presented in the table. Since EEPROM has been around for a longer time, it exhibits significant advantages, particularly in incorporating multiple memory cells. When compared with our work, the non-volatile memory arrays developed by Feldmann et al. in 2019 [17], which utilized wavelength-tuned Micro-Ring Resonators (MRRs) for 256 memory cells, fabricated their design which shows impressive results. However, it is important to note that the chip only incorporated Phase Change Memory (PCM) for active elements, and all other processes, such as addressing specific memory elements, were performed externally, while ours were performed on-chip.

In addition to their work in [17], they also built a model of an on-chip neural network design using optical memory [24]. In this design, PCM was applied on top of a segment of MRR (microcomb) to establish neural network weights. Each column comb receives a particular wavelength, and the intensity of these wavelengths was controlled by variable optical attenuators (VOAs) emitted from continuous wavelength generators (CW). Thus, the control signals of VOAs can pinpoint the memory location. However, their structure used a number of CWs and VOAs equal to the number of memory microcombs. In comparision, our model employed an equal number of active MRR modulators to memory cells, with reduced number of electrical addressers, as a result of using column-row decoders, instead of controlling optical signal to each memory cell with separate controller.

Narayan et al. [25] developed a simulation of a large-scale memory array, where columns were chosen using WDM MRRs, and rows were identified by specific active MRRs within the same row. In this configuration, it is accurate to state that a single row received a signal with the number of wavelengths equal to the number of MRRs in the row. The active MRRs connected to address inputs effectively blocked out wavelengths corresponding to the memory cells that were not pinpointed in the addressing process. However, our model utilizes an 2:4 AND decoder to send modulation voltage to WDM MRRs, and rows are selected by a 2:4 NAND decoder, maintaining a specific row in an unmodulated state. This design reduces the number of required address inputs significantly. Importantly, all components of our design are on-chip, necessitating only a constant read optical signal and two 2-input electrical address signals during the READ operation (Fig. 4a).

As for EEPROM, Xu et al. [27] demonstrated its scalability, extending to 1024 columns and 1600 rows, connected to column and row address decoders. Their work showed an access speed of 30 ns, with memory editing speed ranging from 1 to 8 μs. Although the memory capacity in our model is not as large as the work in [27], our model exhibits fast access speed.

The access (read) speed of our model was tested in Lumerical (Fig.7) and numerically verified in Matlab (Fig.10) for a 30 Gbps operation, representing a significant improvement with a fast erase time of 20ns and low ERASE/WRITE energy. Judging by the scale of components used in our model, the footprint of our design is 300×220um. In general, our work when compared with other works stands out for its fully digital address control with a minimal number of inputs, and all components are integrated on-chip.

VI. CONCLUSION

In this work, we proposed the design of a 4 × 4 bit optical memory array with memory addressing. We have successfully presented a concept model with resonances that matched our expectations and produced satisfactory results. A system address access speed of 30 Gbps which clearly differentiated memory states of '0' and '1' at outputs was obtained, with 50Mbps for erasing and 1.6Mbps for writing with accurate memory unit routing. However, challenges still exist in selecting a PCM with low refractive index change and addressing nonlinear effects. Future research should focus on addressing these issues to advance the field of optical memory arrays.

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ASSYLKHAN NURGALI received the B.Sc. degree in technical physics, physics and technology from L. N. Gumilyov Eurasian National University, Astana, Kazakhstan, in 2019, and the M.Sc. degree in electrical and computer engineering from Nazarbayev University, Astana, in 2022. Since 2021, he has been a Research Assistant with the Integrated Device Solutions and Nanophotonics (iDSN) Laboratory, School of Engineering and Digital Sciences, Nazarbayev University. His research interests include silicon photonics, optical nonvolatile memories, neural networks, and numerical modeling.

BIKASH NAKARMI (Senior Member, IEEE) received the B.E. degree in electronics and communication, information and communication engineering from Tribhuvan University, Nepal, in 2004, the M.E. degree in electronics and communication, information and communication engineering from Harbin Engineering University, Harbin, China, in 2008, and the Ph.D. degree in electronics and communication, information and communication engineering from the Korea Advanced Institute of Science and Technology, Daejeon, Republic of Korea, in 2012.

He joined the College of Electronics and Information Engineering, Nanjing University of Aeronautics and Astronautics, China, in 2016, where he is currently a Professor with the Key Laboratory of Radar Imaging and Microwave Photonics, Ministry of Education. His research has focused on developing optical blocks used in optical communication and networks using Fabry-Pérot laser diode, bio-sensors based on nano-structures, and microwave photonics. From 2012 to 2013, he was the Research and Development Manager of InLC Technology, South Korea, Postdoctoral Researcher with Nanjing University, China (2012–2014). From 2014 to 2016, he was a Research Professor with KAIST. He has authored or coauthored over 100 research papers, including 40 peer-reviewed journals, 45 papers in conference proceedings, and several invited papers and talks.

Prof. Nakarmi is a Senior Member of the Optical Society of America. He had served as a Committee Member for SPIE Photonics ASIA 2012 and IEEE ICECIT 2021 and a reviewer for several peer-reviewed journals.

CARLO MOLARDI (Senior Member, IEEE) received the master's degree in telecommunication engineering, working on numerical methods for optics and electromagnetism and the Ph.D. degree in information technologies from the University of Parma, Parma, Italy, in 2011 and 2016, respectively. He was Postdoctoral Researcher with Nazarbayev University and the Information Engineering Department, University of Parma. He is currently an Assistant Professor with the School of Engineering and Digital Sciences, Nazarbayev University, Astana, Kazakhstan. His research interests include fiber optics, fiber sensors, photonic crystal fibers design, fiber lasers for high power operations, random lasers, and numerical methods for optics and electromagnetism.

IKECHI AUGUSTINE UKAEGBU (Senior Member, IEEE) received the B.Sc. degree in electrical engineering, electromechanics, and electro-technology from the Moscow Power Engineering Institute, National Research University, Moscow, Russia, in 2004, the M.Sc. degree in electronics and microelectronics from National Research University, in 2006, and the Ph.D. degree from the Korea Advanced Institute of Science and Technology (KAIST), in 2012.

He was a "Brain Korea-21 (BK-21)" Postdoctoral Research Fellow with the Electrical Engineering Department, KAIST, from 2012 to 2013. He has been with the Electrical and Computer Engineering Department, School of Engineering and Digital Sciences, Nazarbayev University, as an Assistant Professor, since 2018, where he is currently the Founder and the Director of the Integrated Device Solutions and Nanophotonics Laboratory. His research interests include circuits and systems, digital and microwave photonics, optoelectronics, and channel modeling. He held research and development positions with the Electronics and Telecommunications Research Institute (ETRI), South Korea, from 2008 to 2009, and Lightron Fiber-Optics Inc., South Korea, in 2013. He was a Senior Engineer with the Design Technology Team, System LSI Division of Samsung Electronics Company Ltd., South Korea, from 2013 to 2016. He co-founded a venture startup company, where he was the CTO, from 2016 to 2017. He has authored or coauthored over 90 research papers, including 38 peer-reviewed journals and 55 papers in conference proceedings. He is a reviewer of several peer-reviewed journals and has served as a TPC member for several IEEE international conferences.