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RESEARCH ARTICLE

Temperature Dependent Variations of Low-Frequency Noise Sources in Cryogenic Short-Channel Bulk MOSFETs

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ABSTRACT This study investigated changes in low-frequency noise sources associated with short-channel bulk metal-oxide-semiconductor field-effect transistors (MOSFETs) by analyzing random telegraph noise (RTN) from 300 K down to 3 K. The power spectral density (PSD) of the drain current, which exhibited RTN characteristics in the frequency domain, changed with temperature. In addition, the effect of temperature on the PSD was not monotonic such that peaks were generated at specific temperatures. A comparison between p-type and n-type MOSFETs established that the former exhibited PSD values nearly an order of magnitude smaller than those of the latter. The PSD peaks observed in the temperature domain were analyzed using a theory based on the Shockley-Read-Hall model and the energy levels of the charge traps responsible for RTN were determined. Assessing the temperatures and corresponding energy levels associated with these PSD peaks showed a trend in which energy levels approached band edges as the temperature was decreased. This study assists in the development of strategies to reduce low-frequency noises generated by cryogenic qubit controllers by elucidating the impact of band-tail states on noises at 4 K.

INDEX TERMS Quantum computer, cryogenic temperature, Si spin qubit, short-channel MOSFET, random telegraph noise, band-tail state.

I. INTRODUCTION

Large-scale fault-tolerant quantum computers are potentially capable of exceptionally efficient, rapid performance and so have attracted significant attention [1], [2]. As these computers become available, they are expected to permit quantum chemical simulations with applications such as material/drug discovery, route optimization in the transportation industry and parameter optimization in quantum mechanical learning. Both silicon spin [3], [4] and superconducting [5] qubits are promising candidates for the construction of solid building blocks for these computers. Qubits make use of quantum two-level systems that are well defined below 1 K [6], [7] and so require dilution refrigerators. Even so, the development of large-scale fault-tolerant quantum computers comprising millions of qubits remains challenging, partly based on the necessary wiring. Specifically, a typical refrigerator does not provide sufficient space for this tremendous amount of wiring. Cryogenic qubit controllers, meaning classical circuits made of metal-oxide-semiconductor field-effect transistors (MOSFETs), could be a solution to this issue. Using these devices, control signals can be generated in close proximity to the qubits (e.g. at the 4-K stage of the dilution refrigerator) such that the amount of wiring required for each qubit is drastically reduced [8].

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These controllers must exhibit low-noise characteristics because charge noise, which can result from both quantum devices and cryogenic qubits controllers, can lead to coherence degradation [9]. Hence, it is vital to identify noise sources in MOSFETs operating at cryogenic temperatures when developing large-scale fault-tolerant quantum computers. The authors previously evaluated noise sources in long-channel MOSFETs during cryogenic operation [10]. The results demonstrated that noise was greater at cryogenic temperatures compared to room temperature and that the noise intensity was affected by wafer orientation. These findings suggested that noise at cryogenic temperatures is associated with charge traps at interfaces. Prior work has also shown that a number fluctuation model [11] can be used to predict noise generation at cryogenic temperatures. However, microscopic evaluations of charge traps remain difficult because our prior work focused on Flicker noise associated with large-area MOSFETs, and so only assessed charge traps on the macroscopic level. Examining these traps on the microscopic scale could assist in the development of strategies to reduce low-frequency noise. As such, in this study, we investigated the random telegraph noise (RTN) [12], [13], [14], [15] of small-area MOSFETs at cryogenic temperatures.

In the present work, the RTN values produced by short-channel bulk MOSFETs were analyzed as a means of assessing changes in noise sources with variations in temperature. In particular, the effect of temperature on power spectral density (PSD) was monitored to investigate changes in RTN in the frequency domain. This process allowed the energy levels causing RTN to be determined. Moreover, p-type and n-type MOSFETs were compared and the former were found to exhibit lower noise characteristics. This evaluation of RTN properties showed that the energy levels approached a band edge, allowing the effects of band-tail states on noises at 4 K to be predicted. The assignment of noise sources at 4 K is important because cryogenic qubit controllers are expected to work at the temperature. Compared with previously published technical digest [16], this research also generated new data related to p-type MOSFETs.

II. EXPERIMENTAL DETAILS

Short-channel bulk MOSFETs with silicon oxynitride dielectric layers were fabricated on a (100)-oriented Si wafer. Five n-type and four p-type MOSFETs were examined in this study. Each device had a gate length (L) of 90 nm while the widths (W) were in the range of 100-130 nm. Both self-aligned extension implantation and halo implantation were employed to mitigate short-channel effects in these MOSFETs. Equivalent oxide thickness was approximately 2 nm. Figure 1 presents a diagram of the structure of these devices together with I_d-V_g plots generated at various temperatures. Threshold voltages of n- and p-type MOSFETs, which is defined by constant current method ($I_d \times L/W = 10\ nA$) at 300 K, were 85 and −235 mV, respectively. These data indicate increases in the threshold voltage with decreasing temperature, attributed to increases in the bulk Fermi potential at lower temperatures [17], [18]. The distortion of the I_d-V_g plot obtained from the p-type MOSFET at 3 K is ascribed to depletion at the source and drain extension edges, as observed in our previous study [19].

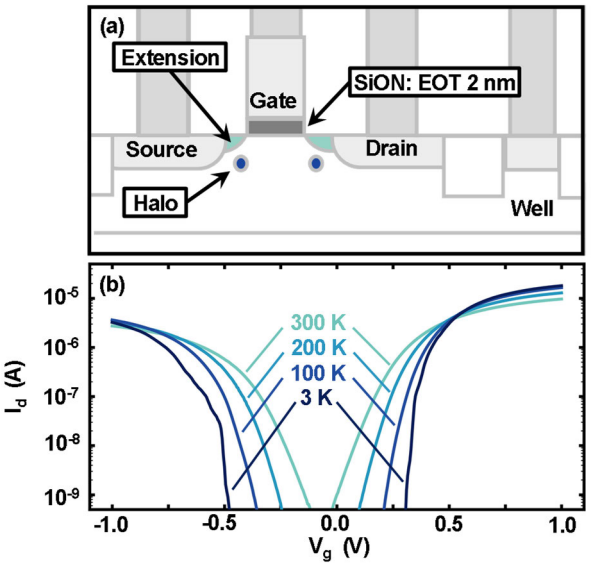

FIGURE 1. (a) The structure of the present short-channel bulk MOSFETs. Both n-type and p-type MOSFETs were fabricated on a bulk wafer. (b) I_d-V_g plots obtained at various temperatures between 3 and 300 K with V_d set at 50 mV.

After fabrication, the samples were placed in a desktop refrigerator (Optistat Dry, Oxford Instruments). The base temperature of the samples was swept from 3 to 300 K in 1 K intervals using a heater located inside the refrigerator. The source, drain, gate, and well electrodes of the samples were connected to a commercial noise analyzer (Advanced Low-Frequency Noise Analyzer, Keysight) located outside the refrigerator. The noise analyzer was utilized to measure I_d-V_g, I_d-V_d characteristics, time variation of I_d, and PSD in the frequency domain. The heater and noise analyzer were synchronized through a homemade Python script to ensure that each characteristic was automatically obtained at every temperature. Such measurements facilitated the generation of 2D plots that depicted PSD as a function of both frequency and temperature, which are presented in subsequent sections. Data were acquired 10 minutes after reaching each specific target temperature to minimize temperature overshoot.

Prior to PSD measurements, both I_d-V_g and I_d-V_d characteristics were obtained. Subsequently, the V_g necessary to produce the target I_d value while applying a specific V_d value was automatically calculated. Following this calculation, both PSD and time variation of I_d values were generated while applying the calculated V_g and target V_d values, with the source and substrate electrodes biased at 0 V. In this study, the target I_d and V_d values were set to 1 μA and 50 mV, respectively.

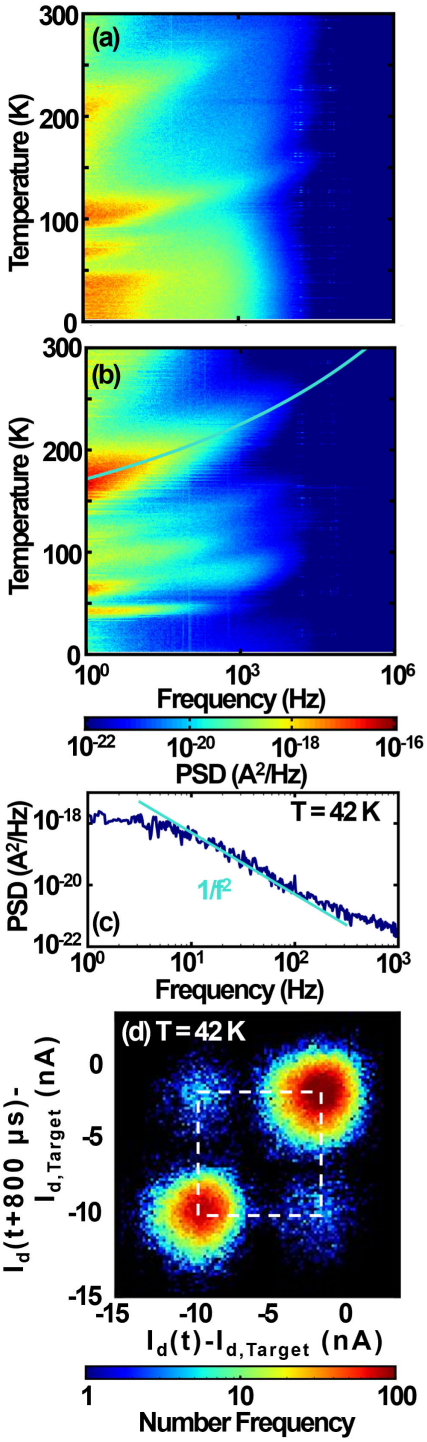

FIGURE 2. (a, b) Noise maps obtained from two different n-type MOSFETs having the same structure (L/W = 90 nm/120 nm). The blue curve in (b) traces one of the peaks, which is analyzed in Fig. 3. (c) The horizontal cross-section of (b) at 42 K. (d) A time lag plot generated from I_d data for the device shown in (b) at 42 K. The dashed square is a visual guide that demonstrates the two-level characteristic of the I_d values.

III. RESULTS AND DISCUSSIONS

A. TEMPERATURE DEPENDENCE OF PSD

The temperature-dependent PSD data obtained from two n-type MOSFETs (L/W = 90 nm/120 nm) are presented in Fig. 2. As discussed below, the high-resolution contour plots in Figs. 2(a) and (b) allow detailed characterization of noise sources in a given device and so are hereafter referred to as "noise maps." It is evident from these maps that the PSD of each short-channel MOSFET was not a monotonic function of temperature but rather exhibited peaks at some temperatures. Each peak on these noise maps represents an individual RTN. This is evident from the 42 K data extracted from Fig. 2(b) (see Fig. 2(c)), which show that the PSD exhibits a $1/f^2$ characteristic in the frequency domain. In addition, the time lag plot [20] in Fig. 2(d), obtained from raw I_d values together with the data in Fig. 2(b) at 42 K, exhibits an evident square-shaped correlation. It should be noted that this time lag plot displays number frequency as a function of I_d at arbitrary times t and $t + \Delta t$, employing a time lag, Δt, of 800 μs. The square indicated by the dashed line in this plot confirms that the raw I_d data comprised a two-level system, thus providing evidence for an individual RTN source.

Although the devices all had the same structure, the two noise maps in Figs. 2(a) and (b) acquired from different specimens are evidently different. Refer to Fig. S1 in the Supplementary Material for additional comparisons of noise maps. This result suggests that, compared with the gate area, the spatial distribution of noise sources was sparse (i.e., noise sources were distributed over a small area compared with the gate area) so that the quantity and type of noise sources varied between devices.

Each peak in each noise map was affected by both temperature and frequency and followed a curve, as demonstrated by the solid line in Fig. 2(b). This curve follows the relationship based on the Shockley-Read-Hall (SRH) model

$$\ln \frac{T^2}{f} = \frac{E_C - E_T}{k_B T} + \ln \frac{\pi}{A\alpha}, \tag{1}$$

where T and f are temperature and frequency, respectively, $E_C - E_T$ is the energy difference between the conduction band edge and the energy level of a charge trap, $k_B T$ is the thermal energy, and $A = 2k_B^2 m_E (6\pi)^{3/2} / 3h^3$ with m_E and h being the effective electron mass and Planck constant, respectively [15], [21]. For simplicity, no temperature dependence was assumed for the effective electron mass ($m_E = 3.0 \times 10^{-31}$ kg) The capture cross-section, α, is that defined in the classical SRH model.

In order to apply Eq. (1), peak temperatures at various frequencies were extracted to construct an Arrhenius plot. During this extraction process, firstly, a noise map was sliced along the ordinate to obtain a plot of PSD versus temperature at a specific frequency, such as 1 Hz. A single peak within the PSD versus temperature plot was then identified and fitted with a normal distribution function to precisely determine the peak position. This step yielded a single pair of temperature and frequency data points. The procedure was subsequently repeated for higher frequencies, allowing for the accumulation of multiple temperature and

frequency pairs necessary to create an Arrhenius plot. These steps were automated using a custom Python script.

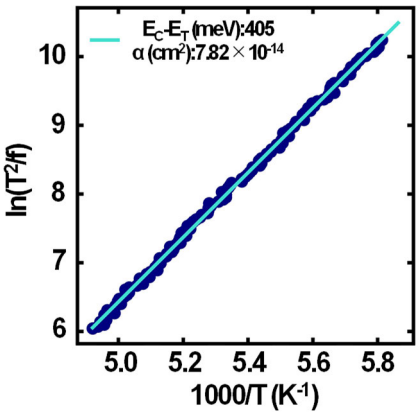

FIGURE 3. Arrhenius plot obtained from the peak indicated by the solid curve in Fig. 2(b), within the temperature range of 172 to 200 K. The solid line is the result of fitting a linear relationship to the data so as to evaluate the trap level and capture cross-section.

An example of this analysis is shown in Fig. 3, based on the peak indicated by the solid line in Fig. 2(b). The plot in this figure indicates a linear relationship confirming that these data can be described by Eq. (1). In other words, temperature dependence of RTN was well explained by the thermal activation model. Conversely, noise generation mechanisms that involve tunneling are thought to exert minimal influence on the temperature dependence of RTN because of the general characteristic of simple tunneling effect being independent of temperature. By fitting these data using this equation, $E_C - E_T = 405\ meV$ and $\alpha = 7.82\times \sim 10^{-14}\ cm^2$ were obtained. Hence, the charge traps responsible for producing the RTN indicated by the solid line in Fig. 2(b) had an energy level 405 meV below the conduction band.

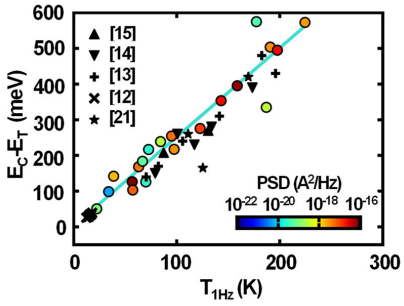

FIGURE 4. A plot of E_T and T_{1Hz} values extracted from 20 peaks in five noise maps for n-type MOSFETs (colored points), along with results from prior studies (black). The color of each point indicates the maximum PSD.

A total of 20 peaks were identified in noise maps generated from data for five n-type MOSFETs and then analyzed by the process described above. The extracted energy levels are summarized in Fig. 4. Here, T_{1Hz} is a parameter defined for each noise source and temperature at which a fitting curve on a noise map crosses the ordinate of the noise map. In other words, each noise source generates 1-Hz noise at T_{1Hz}. The frequency of 1 Hz was chosen because the value was the lowest one analyzed in this study and such low-frequency noise can lead to coherence degradation of qubits [9]. As an example, a T_{1Hz} value of 171 K was associated with the RTN indicated by the solid line in Fig. 2(b). The color of each data point in Fig. 4 indicates the maximum PSD produced by the corresponding charge trap. Note that some energy levels and T_{1Hz} values reported in prior publications [12], [13], [14], [15] are also plotted in Fig. 4 as black points. It is evident from this plot that the energy levels approached the band edge with decreases in temperature. The data extracted from prior studies also follow this trend. These prior data were obtained from a variety of devices, including conventional planar devices [12], [15] and FinFETs [14], confirming that this phenomenon is a common characteristic of MOSFETs.

The change in trap energy with temperature can be understood using two charge traps as an example. In this scenario, the traps have an energy level $E_C - E_T$ of approximately 200 meV (that is, shallow traps) or 500 meV (deep traps). In addition, the example is simplified by assuming that the capture and release of carriers take place between the conduction band and charge traps within the silicon band gap and occur at the silicon-dielectric interface.

Initially, in the vicinity of 200 K, the Fermi level at the interface is assumed to be located near the deep trap level. This assumption is based on the present experimental conditions, in which the target I_d was set to 1 μA such that each device was operating near its threshold voltage. Because of this, each deep trap did not always contain an electron and so there was a finite probability that deep traps could capture electrons from the conduction band. In this situation, the capture of a carrier by the deep trap would be followed by the release of this same carrier to the conduction band on a measurable time scale (<1 MHz). The associated transition rate was determined by the Arrhenius type relationship $k \propto \exp\left(-(E_C - E_T)/k_BT\right)$. In contrast, in the case that a carrier is captured by a shallow trap, it can be released to the conduction band or can further relax to a deep trap. Release from the shallow trap would be more rapid (>1 MHz) than that from the deep trap because of the smaller $E_C - E_T$ value, and so would be unobservable using the present equipment. Thus, as shown in Fig. 4, RTN associated with an $E_C - E_T$ value on the order of 500 meV was observed in the vicinity of 200 K while a value of 200 meV was not obtained.

Following this, as the temperature is lowered below 100 K, the Fermi level at the interface approaches the conduction band. In this situation, the deep traps are continually filled and so do not participate in carrier capture and release. Carriers captured by shallow traps can be emitted to the conduction band on a measurable time scale (<1 MHz) because the thermal energy, k_BT, is lower and the Arrhenius-type transition rate decreases. Thus, as shown in Fig. 4, RTN for which the $E_C - E_T$ value was approximately 200 meV appeared in the vicinity of 100 K whereas RTN with an $E_C - E_T$ of 500 meV did not.

This scenario explains the temperature dependent transition of energy levels that is apparent in Fig. 4. It should

be noted that K_n centers originating from dangling silicon bonds in silicon oxynitride dielectric layers will have energy levels near the center of the bandgap [22]. Furthermore, P_{b0} centers associated with dangling silicon bonds at silicon and silicon dioxide interfaces will have energy levels with centers approximately 300 meV from the conduction band [23]. Prior work demonstrated that interface traps play an important role in noise generation at cryogenic temperatures [10]. Therefore, the RTN observed at approximately 200 K and 100 K may have originated from K_n centers at dielectric layers and P_{b0} centers at interfaces, respectively.

The transition of noise sources from K_n centers to P_{b0} centers can be assessed based on a trap depth analysis. Amarasinghe et al. proposed an analytical method to evaluate trap depth, χ_T, from the effect of V_g on durations of high and low current periods in a RTN signal. The relevant equation is [24]

$$\chi_T = \left| T_{OX} \frac{k_B T}{q} \frac{d}{dV_g} \ln \frac{\tilde{\tau}_{up}}{\tilde{\tau}_{down}} \right|. \quad (2)$$

Here, χ_T is the distance from the silicon-dielectric interface, T_{OX} is the oxide thickness, q is the elemental charge. $\tilde{\tau}_{up}$ is the average time over which I_d has the higher value while $\tilde{\tau}_{down}$ is the time associated with the lower value. In the work reported herein, the RTN data acquired at 240 and 100 K were evaluated and the relationship between the $\tilde{\tau}_{up}/\tilde{\tau}_{down}$ ratio and V_g is summarized in Fig. 5. In this figure, the data obtained at 240 K exhibit a greater effect of V_g compared with the 100 K values. Hence, the charge traps responsible for the RTN observed at 240 K were deeper than those producing noise at 100 K. Assuming a T_{OX} value for the present devices of 2 nm, the χ_T values for 240 and 100 K would be 1.6 and 0.40 nm, respectively. These results support the assumption that K_n and P_{b0} centers were responsible for RTN at approximately 200 and 100 K, respectively. Note that K_n centers were evidently located within the dielectric layers [22] whereas P_{b0} centers were situated right at the interface [23].

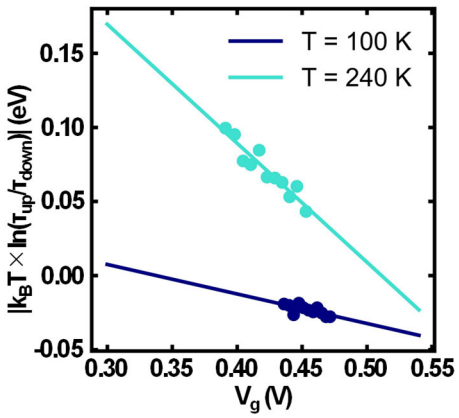

FIGURE 5. The ratio τ_{up}/τ_{down} as a function of V_g for two different RTN events at 100 and 240 K. The data points represent experimental data while the solid lines are linear fits to these data.

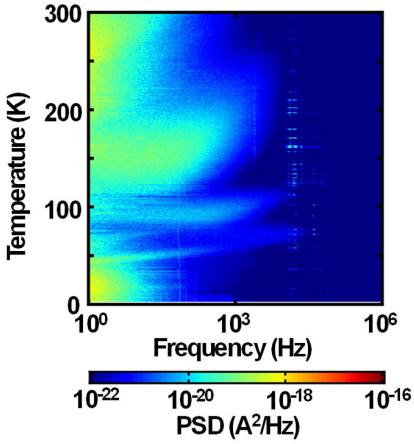

FIGURE 6. A noise map obtained from a p-type MOSFET (L/W = 90 nm/120 nm).

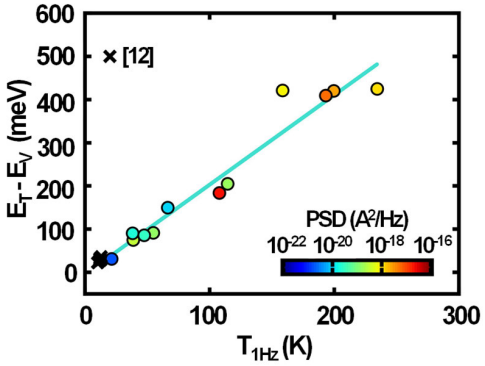

FIGURE 7. E_T as a function of T_{1Hz} based on data extracted from 12 peaks in four noise maps for p-type MOSFETs.

B. DIFFERENCES BETWEEN N-TYPE AND P-TYPE MOSFETS

The example of a noise map obtained from a p-type MOSFET is shown in Fig. 6, and the energy levels of charge traps causing RTN in the p-type MOSFETs are summarized in Fig. 7. In order to generate Fig. 7, Eq. (1) was modified so that the energy level of charge trap was related to the valence band and the relevant capture cross-section was for holes. As seen in the n-type MOSFETs, the energy levels of charge traps approached the valence band edge with decreases in temperature. However, the number of analyzable peaks was smaller than the quantity that could be obtained from the n-type MOSFETs. This difference is attributed to the less intense PSD produced by the p-type MOSFETs. The average PSD intensity in the p-type MOSFETs was $10^{-18.6}$ A^2/Hz, which was approximately one order of magnitude smaller than that in the n-type MOSFETs ($10^{-17.9}$ A^2/Hz, Fig. 4). At cryogenic temperatures, the carrier number fluctuation is the dominant mechanism of noise generation [11]. This means that the difference of PSD in the p-type and n-type MOSFETs would be originating from the difference in the amount of trap density in addition to the difference in the transconductance and the carrier mobility, although further

quantitative analysis of RTN is required for its physical understanding.

C. ENERGY LEVELS RESPONSIBLE FOR NOISE AT 4 K

The analysis of noise sources at 4 K is an important aspect of assessing potential applications for cryogenic qubit controllers. Extrapolation of the plots in Figs. 4 and 7 indicates that energy levels 12 and 3 meV from the band edges were responsible for noise at 4 K in the n-type and p-type MOSFETs, respectively. The reason for this difference between the two types of device is not clear at this time because an insufficient quantity of data was acquired, especially in the case of the p-type MOSFETs. However, it is apparent that shallow traps within several tens of meV from the band edges were most likely responsible for noise at 4 K.

Shallow traps such as these are thought to originate from band-tail states [25] generated by the stretching of silicon bonds in association with defects. If this is in fact the case, the results obtained from our prior study [10], in which long-channel MOSFETs were analyzed, can be understood. In this previous work, the PSD data did not exhibit specific peaks in the temperature domain above 100 K but rapidly increased below 100 K. In a long-channel MOSFET, various noise sources (and thus various T_{1Hz} values) are likely to exist. Therefore, various peaks were generated over the wide temperature range above 100 K, prohibiting observations of individual peaks. These noise sources also produced band-tail states that served as additional noise sources below 100 K. Hence, a single defect could function as two noise sources, one above 100 K and one below 100 K. The noise generated by a variety of defects could be convoluted below 100 K, leading to a rapid increase in the PSD.

As discussed, the noise generated in MOSFETs at cryogenic temperatures involves interfaces. As such, the assignment of noise sources at cryogenic temperatures is important as a means of reducing noise both in qubit controllers and solid-state quantum devices in which these qubits are incorporated. In fact, the majority of solid-state quantum devices, such as silicon spin or superconducting qubits, also consist of interfaces. Therefore, techniques used for future reductions in the noise values of MOSFETs at cryogenic temperatures could also be applicable to solid-state quantum devices, enabling the realization of longer-coherence qubits.

IV. CONCLUSION

The work reported herein demonstrated that noise sources in short-channel bulk MOSFETs changed with temperature. Specifically, with decreases in temperature, the noise sources transitioned to charge traps close to band edges. In particular, charge traps having energy levels several tens of meV away from band edges were responsible for the generation of noise at 4 K.

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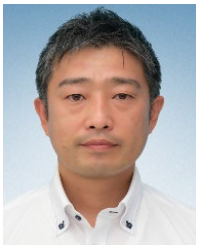

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