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RESEARCH ARTICLE

Small Signal Modeling and Performance Analysis of Conventional- and Dual-UPQC

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ABSTRACT Both the conventional and dual compensation strategies are widely adopted in a unified power quality conditioner (UPQC). However, the differences between them are lack of in-depth analysis. This article establishes the small signal models in dq-axis of conventional- and dual-UPQC (C- and D-UPQC) with consideration of the effects of the phase-locked-loop (PLL) and grid impedance, which lays the foundation for static and dynamic performance analysis. In addition, the performance of them is analyzed and compared under different conditions. It is found that: the D-UPQC has a better dynamic performance when the grid voltage or load suffers sudden variation; the harmonic rejection capabilities of the C- and D-UPQC are different; the grid impedance has an obvious influence on the load voltage quality in the C-UPQC. The findings will provide the guideline for the selection of compensation strategies in specific applications. Finally, experimental results verify the correctness of the comparative performance analysis.

INDEX TERMS Unified power quality conditioner (UPQC), compensation strategies, small signal modeling, control performance analysis.

I. INTRODUCTION

The mitigation of the power quality (PQ) issues has been always one of the focuses and becomes more and more significant due to the development of the distribution networks [1], [2]. Generally, the voltage-related PQ issues mainly include voltage sag, swell, unbalance, and harmonics, which are mainly caused by the power system faults and switching of high-power load [3]. Besides, the current-related PQ issues [4] include current unbalance, harmonics and so on, which are caused by nonlinear loads and grid connection of renewable energy system (RES). To improve the operation efficiency, the load should be prevented from suffering the voltage-related PQ issues and the power grid should be avoided suffering the current-related PQ issues.

To alleviate the PQ issues, lots of compensation devices have been developed. Based on the topologies, these compensation devices could be divided into three categories: the series compensation devices, the shunt ones, and the hybrid ones. As a representative of the series compensation devices, the dynamic voltage restorer (DVR) can mitigate all the voltage-related PQ issues [5], [6]. On the other hand, the static synchronous compensator (STATCOM) is an outstanding shunt compensation device and can suppress all the current-related PQ issues [7], [8]. Among the hybrid ones, the unified power quality conditioner (UPQC) is a promising device to mitigate all the voltage- and current-related PQ issues [9], [10], [11], [12], [13].

From the perspective of compensation strategies, the conventional and dual compensation strategies are the research focuses of the UPQC. In the conventional-UPQC (C-UPQC) [14], [15], [16], the series converter functions as a voltage source to remain the load voltage balanced and sinusoidal; while the shunt converter operates as a current source to maintain the grid current balanced, sinusoidal and in-phase with the voltage at the point of common coupling (PCC). On the contrary, in the dual-UPQC (D-UPQC) [17], [18], [19], [20], the series converter works as a current source to

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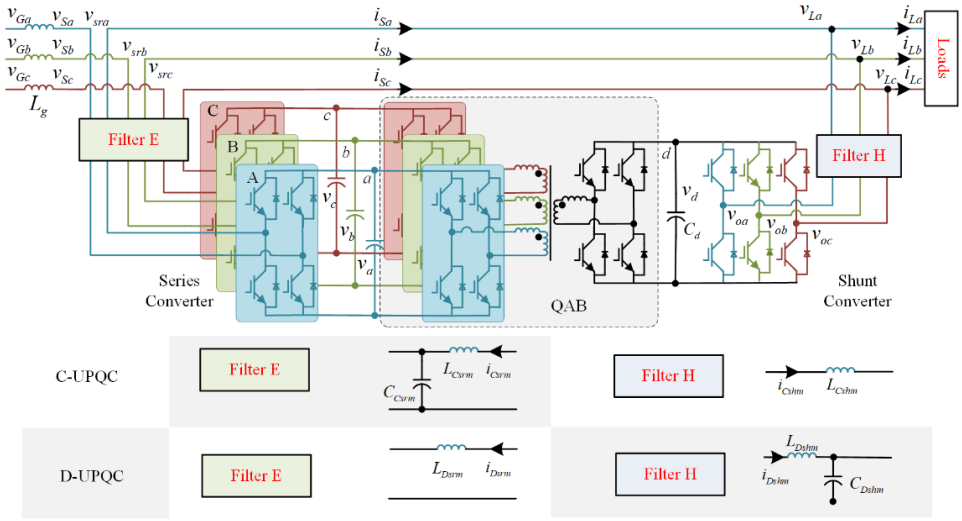

FIGURE 1. Configuration of three-phase UPQC-QAB.

control the grid current and the shunt converter operates as a voltage source to control the load voltage. Theoretically, both the C- and D-UPQC can realize the error-free tracking of the desired load voltage and grid current.

However, due to the different characteristics of the C- and D-UPQC, the topologies, models and control performance will be also different. In [21], the overall performance evaluation of the C- and D-UPQC based on proportional resonant (PR) control [22] are presented. However, many important factors are neglected in the comparative performance analysis [21]. For example, 1) all the closed-loop systems neglect the effects of the phase-locked-loop (PLL); 2) the influence of control and circuit parameters on control performance is neglected; 3) the influence of the grid impedance is also neglected.

To evaluate the performance of the C- and D-UPQC more realistically and deeply, the dq-axis small signal models based on proportional integral (PI) control are established. In synchronous rotation frame (SRF), the PLL is used to track the phase angle of the PCC voltage and helps realize the transformation from the three-phase AC signals to the DC signals in dq frame [23], [24]. Thus, the dynamics of the PLL should not be neglected because of its effect on the frequency-domain characteristic [25]. Further, based on the small signal models with consideration of the effects of the PLL and grid impedance, the static and dynamic performance of the C- and D-UPQC are discussed and compared detailly.

In summary, the main contributions of this study include:

1) This article establishes the dq-axis small signal models of the C- and D-UPQC with consideration of the effects of the PLL and grid impedance, which lays the foundation for static and dynamic performance analysis.

2) The static/dynamic performance analysis of the C- and D-UPQC is compared and evaluated. It is concluded that:

(a) The D-UPQC has a better dynamic performance when the grid voltage or load suffers sudden variation;

(b) Grid voltage harmonics have an obvious influence on load voltage quality in the C-UPQC;

(c) Load current harmonics mainly distort the gird current in the C-UPQC and load voltage in the D-UPQC;

(d) Grid impedance mainly has an influence on the load voltage quality in the C-UPQC.

The rest of contents are organized as follows. Section II and III introduce the topologies and average models of the UPQC. In Section IV, the dq-axis small signal models of the UPQC are deduced. In Section V, the comparative performance analysis of the C- and D-UPQC is presented. In Section VI, experimental results are presented and discussed. Section VII presents the conclusions.

II. TOPOLOGIES OF THREE-PHASE C- AND D-UPQC

The circuit configuration of a quadruple-active-bridge based UPQC (UPQC-QAB) [26] is presented in Fig. 1. It is mainly formed of series converters made up of three single-phase (TSP) H-bridges, a three-phase shunt converter and a QAB [27] with four DC ports. One DC port (port d) of the QAB is connected with the shunt converter, while the other three ones (port a, b and c) are connected with the series converters.

Besides, in the C-UPQC, the series converter is controlled as a voltage source, the LC filter is adopted to suppress the high-frequency voltage harmonics at series side; accordingly, the shunt converter is controlled as a current source, therefore, the L filter is used to mitigate the high frequency current harmonics at shunt side. On the contrary, in the D-UPQC, the grid current is directly controlled by controlling the series converter as a current source. Therefore, the L filter is adopted at series side; the shunt converter is controlled as a voltage source to directly control the load voltage, so the LC filter is

adopted at shunt side. These are the main differences between the topologies of the C- and D-UPQC.

III. AVERAGE MODELS OF C- AND D-UPQC

For convenience, the parameters of the LC and L filters in the C- and D-UPQC are kept the same. Namely

$$\begin{cases} L_{Csrm} = L_{Dshm} = L_V \\ C_{Csrm} = C_{Dshm} = C_V \\ L_{Cshm} = L_{Dsrm} = L_I \end{cases} \tag{1}$$

where m∈{a, b, c}. The subscripts "C" and "D" represent the variables in the C- and D-UPQC, respectively. The subscripts "*sr*" and "*sh*" are the related variables of the series and shunt converters. L_V and C_V are the filter inductance and capacitance of LC filter. L_I is the filter inductance of L filter.

Besides, considering the dynamic of the DC-link voltage is much slower than that of the grid current [25], the dynamic of the DC-link voltage is neglected in this study.

A. AVERAGE MODEL OF THREE-PHASE C-UPQC

From Fig. 1, the average model of the series converter for the C-UPQC (without line frequency transformers) is expressed as

$$\begin{cases} C_V dv_{srm}/dt = i_{Csrm} - i_{Sm} \\ L_V di_{Csrm}/dt = -v_{srm} + v_{Cim} \end{cases} \tag{2}$$

where v_{srm} is the series injected voltage, i_{Sm} is the grid current. i_{Csrm} is the inductor current of the series filter. v_{Cim} is the output voltage of series converter.

According to the Kirchhoff's law, the grid current in the C-UPQC can be written as

$$i_{Sm} = i_{Lm} - i_{Cshm} \tag{3}$$

where i_{Lm} is the load current, i_{Cshm} is the injected current.

The average model of the shunt converter is written as (4)

$$L_I di_{Cshm}/dt = v_{Com} - v_{Lm} \tag{4}$$

where v_{Lm} is the load voltage, v_{Com} is the output voltage of the shunt converter.

Besides, the relationship between the load and PCC voltage (v_{Sm}) is expressed as,

$$v_{Lm} = v_{Sm} + v_{srm} \tag{5}$$

Combing (2)-(5) and applying the *abc*/*dq* coordinate transformation, the *dq*-axis state-space representation of the C-UPQC is given by

$$\dot{\boldsymbol{x}}_C = \boldsymbol{A}\boldsymbol{x}_C + \boldsymbol{B}\boldsymbol{u}_C + \boldsymbol{W}_C \tag{6}$$

with

$$\boldsymbol{A} = \begin{bmatrix} 0 & \omega & \frac{1}{C_V} & 0 & \frac{1}{C_V} & 0 \\ -\omega & 0 & 0 & \frac{1}{C_V} & 0 & \frac{1}{C_V} \\ -\frac{1}{L_V} & 0 & 0 & \omega & 0 & 0 \\ 0 & -\frac{1}{L_V} & -\omega & 0 & 0 & 0 \\ -\frac{1}{L_I} & 0 & 0 & 0 & 0 & \omega \\ 0 & -\frac{1}{L_I} & 0 & 0 & -\omega & 0 \end{bmatrix},$$

$$\boldsymbol{B} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \frac{1}{L_V} & 0 & 0 & 0 \\ 0 & \frac{1}{L_V} & 0 & 0 \\ 0 & 0 & \frac{1}{L_I} & 0 \\ 0 & 0 & 0 & \frac{1}{L_I} \end{bmatrix},$$

$$\boldsymbol{W}_C = -\begin{bmatrix} 0 & 0 & \frac{1}{C_V} & 0 \\ 0 & 0 & 0 & \frac{1}{C_V} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \frac{1}{L_I} & 0 & 0 & 0 \\ 0 & \frac{1}{L_I} & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{Sd} \\ v_{Sq} \\ i_{Ld} \\ i_{Lq} \end{bmatrix},$$

$$\boldsymbol{x}_C = \begin{bmatrix} v_{srd} & v_{srq} & i_{Csrd} & i_{Csrq} & i_{Cshd} & i_{Csrq} \end{bmatrix}^T,$$

$$\boldsymbol{u}_C = \begin{bmatrix} v_{Cid} & v_{Ciq} & v_{Cod} & v_{Coq} \end{bmatrix}^T.$$

where the subscript "*dq*" are the *d*- and *q*-axis components of related variables. ω is the grid angular frequency.

B. AVERAGE MODEL OF THREE-PHASE D-UPQC

Based on Fig. 1, the average model of the series converter for the D-UPQC is expressed as,

$$L_I di_{Sm}/dt = v_{Dim} - v_{Lm} + v_{Sm} \tag{7}$$

where v_{Dim} is the output voltage of the series converter.

The average model of the shunt converter for the D-UPQC is expressed as,

$$\begin{cases} C_V dv_{Lm}/dt = -i_{Lm} + i_{Sm} + i_{Dshm} \\ L_V di_{Dshm}/dt = v_{Dom} - v_{Lm} \end{cases} \tag{8}$$

where i_{Dshm} is the inductor current of the shunt filter in the D-UPQC. v_{Dom} represents the output voltage of shunt converter.

Applying the Park transformation, (7)-(8) is written as

$$\dot{\boldsymbol{x}}_D = \boldsymbol{A}\boldsymbol{x}_D + \boldsymbol{B}\boldsymbol{u}_D + \boldsymbol{W}_D \tag{9}$$

with

$$\boldsymbol{W}_D = \begin{bmatrix} 0 & 0 & -\frac{1}{C_V} & 0 \\ 0 & 0 & 0 & -\frac{1}{C_V} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \frac{1}{L_I} & 0 & 0 & 0 \\ 0 & \frac{1}{L_I} & 0 & 0 \end{bmatrix} \begin{bmatrix} v_{Sd} \\ v_{Sq} \\ i_{Ld} \\ i_{Lq} \end{bmatrix},$$

$$\boldsymbol{x}_D = \begin{bmatrix} v_{Ld} & v_{Lq} & i_{Dshd} & i_{Dshq} & i_{Sd} & i_{Sq} \end{bmatrix}^T,$$

$$\boldsymbol{u}_D = \begin{bmatrix} v_{Dod} & v_{Doq} & v_{Did} & v_{Diq} \end{bmatrix}^T.$$

where matrixes $\boldsymbol{A}$ and $\boldsymbol{B}$ in (9) are the same with those in (6). Referring to (6), in the C-UPQC, if the controllers directly control the load voltage and grid current, the control quantities will contain dv_{Sm}/dt and di_{Lm}/dt. These features will affect the dynamic performance of the C-UPQC. Relatively, referring to the D-UPQC model (9), it is convenient to control the load voltage and grid current directly [21].

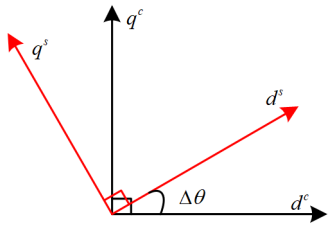

FIGURE 2. The system and control frames.

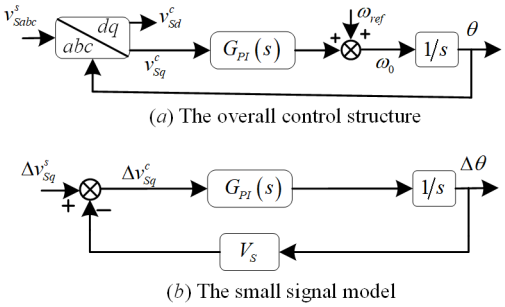

FIGURE 3. The control block diagram of the SRF-PLL.

IV. SMALL SIGNAL MODELING OF UPQC

To analyze the static and dynamic performance of the UPQC, the *dq*-axis small signal models are established in this section. To facilitate comparative analysis, both the series converter of the C-UPQC and shunt converter of the D-UPQC adopt the dual closed loop control scheme, where the PI control is used in the outer load voltage loop and the proportional (P) control is applied in the inner inductor current loop. Accordingly, both the shunt converter of the C-UPQC and series converter of the D-UPQC also utilize the dual closed loop control scheme, where both the outer DC-link voltage loop and inner grid current loop use the PI control scheme.

A. SMALL SIGNAL MODELING OF PLL

Based on the PI control schemes, both the series and shunt controllers of the UPQC need to track the phase angle of the PCC voltage to control the output voltages of the series and shunt converters. However, when the PCC voltage is disturbed, the input phase angle of the controller is affected through the PLL, and then the state variables (such as voltage, current) in the controller coordinate will be affected [25].

Fig. 2 show the UPQC system (d^sq^s) and control (d^cq^c) frames. The superscripts "s" and "c" are the variables in the system and control coordinates. The sign"Δ" represents disturbance signal. As shown, the system frame is defined by the actual PCC voltage and rotates according to the actual PCC synchronous angular speed; while the control frame is defined by the PLL, and the rotation speed is affected by the output of the PLL. In the steady-state, the PLL can realize the error-free tracking of the PCC voltage, where the system and control frames coincide; when the PCC voltage is disturbed, there will be a phase difference $\Delta\theta$ between the system and control frames. From Fig. 2, the following relationship could be obtained

$$\boldsymbol{n}^c_{dq} = \begin{bmatrix} \cos(\Delta\theta) & \sin(\Delta\theta) \\ -\sin(\Delta\theta) & \cos(\Delta\theta) \end{bmatrix} \boldsymbol{n}^s_{dq} \tag{10}$$

where n represents the related variable (voltage or current) and $\boldsymbol{n}_{dq} = [n_d\ n_q]^T$.

Fig. 3 represents the SRF-PLL structure. When the PCC voltage is slightly disturbed, the PLL output is expressed as

$$\Delta\theta = \frac{G_{PI}(s)}{s + G_{PI}(s) V_S} \Delta v^s_{Sq} \tag{11}$$

where V_s is the amplitude of the PCC voltage and $G_{PI}(s)$ is expressed as

$$G_{PI}(s) = k_{Ppll} + k_{Ipll}/s \tag{12}$$

where k_{Ppll} and k_{Ipll} are the proportional and integral gains of the PI controller. Since the controller tracks the phase angle of the PCC voltage, then the following relationship is achieved

$$\begin{bmatrix} V^s_{Sd} \\ V^s_{Sq} \end{bmatrix} = \begin{bmatrix} V_S \\ 0 \end{bmatrix} \tag{13}$$

After perturbation of (10), the following relationship is achieved

$$\Delta\boldsymbol{n}^c_{dq} = \Delta\boldsymbol{n}^s_{dq} + \begin{bmatrix} 0 & \frac{G_{PI}(s)N^s_q}{s+G_{PI}(s)V_S} \\ 0 & -\frac{G_{PI}(s)N^s_d}{s+G_{PI}(s)V_S} \end{bmatrix} \cdot \Delta\boldsymbol{v}^s_{Sdq} \tag{14}$$

where N represents the steady-state value of the variable n.

B. SMALL SIGNAL MODELING OF UPQC CIRCUIT

1) SMALL SIGNAL MODELING OF THE C-UPQC CIRCUIT

Fig. 4 shows the *dq*-axis small signal model of the C-UPQC circuit. Based on the average model (6), the dynamic of the series converter circuit in frequency domain is expressed as

$$\Delta\boldsymbol{v}^s_{Cidq} - \Delta\boldsymbol{v}^s_{srdq} = \boldsymbol{Z}_{LV}(s) \cdot \Delta\boldsymbol{i}^s_{Csrdq} \tag{15}$$

$$\Delta\boldsymbol{i}^s_{Sdq} - \Delta\boldsymbol{i}^s_{Csrdq} = \boldsymbol{Z}_{CV}(s) \cdot \Delta\boldsymbol{v}^s_{srdq} \tag{16}$$

where

$$\boldsymbol{Z}_{LV}(s) = \begin{bmatrix} sL_V & -\omega L_V \\ \omega L_V & sL_V \end{bmatrix}, \boldsymbol{Z}_{CV}(s) = \begin{bmatrix} sC_V & -\omega C_V \\ \omega C_V & sC_V \end{bmatrix}.$$

Accordingly, the dynamic of the shunt converter circuit for the C-UPQC is given by

$$\Delta\boldsymbol{v}^s_{Codq} - \Delta\boldsymbol{v}^s_{Ldq} = \boldsymbol{Z}_{LI}(s) \cdot \left(\Delta\boldsymbol{i}^s_{Ldq} - \Delta\boldsymbol{i}^s_{Sdq}\right) \tag{17}$$

where

$$\boldsymbol{Z}_{LI}(s) = \begin{bmatrix} sL_I & -\omega L_I \\ \omega L_I & sL_I \end{bmatrix}.$$

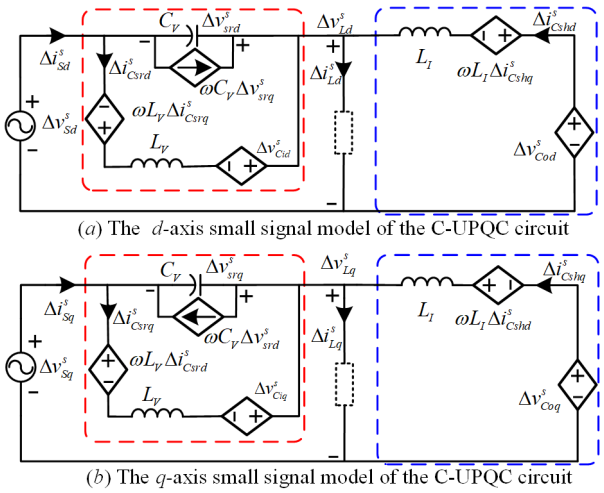

FIGURE 4. The dq-axis small signal model of the C-UPQC circuit.

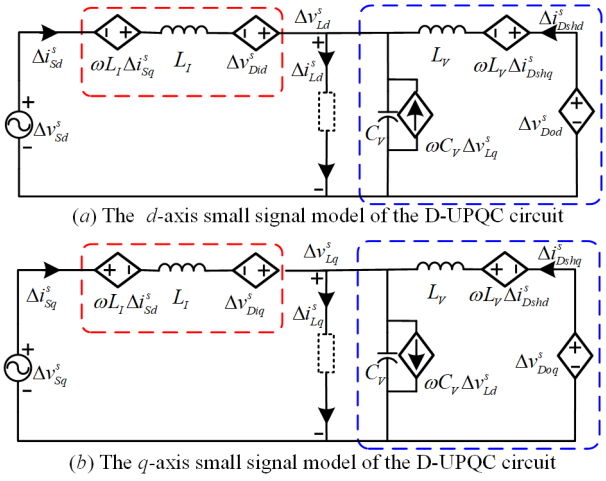

FIGURE 5. The dq-axis small signal model of the D-UPQC circuit.

2) SMALL SIGNAL MODELING OF THE D-UPQC CIRCUIT

The small signal model of the D-UPQC circuit is shown in Fig. 5. As seen, the dynamic of the series converter circuit in frequency domain can be written as

$$\Delta \boldsymbol{v}^s_{Didq} - \Delta \boldsymbol{v}^s_{srdq} = \boldsymbol{Z}_{LI}(s) \cdot \Delta \boldsymbol{i}^s_{Sdq} \tag{18}$$

The dynamic of the shunt converter circuit for the D-UPQC in frequency domain is expressed as

$$\Delta \boldsymbol{i}^s_{Sdq} + \Delta \boldsymbol{i}^s_{Dshdq} - \Delta \boldsymbol{i}^s_{Ldq} = \boldsymbol{Z}_{CV}(s) \cdot \Delta \boldsymbol{v}^s_{Ldq} \tag{19}$$

$$\Delta \boldsymbol{v}^s_{Dodq} - \Delta \boldsymbol{v}^s_{Ldq} = \boldsymbol{Z}_{LV}(s) \cdot \Delta \boldsymbol{i}^s_{Dshdq} \tag{20}$$

Besides, due to the existence of the grid impedance, the relationship between the grid and PCC voltage is expressed as

$$\Delta \boldsymbol{v}^s_{Gdq} - \Delta \boldsymbol{v}^s_{Sdq} = \boldsymbol{Z}_g(s) \cdot \Delta \boldsymbol{i}^s_{Sdq} \tag{21}$$

with

$$\boldsymbol{Z}_g(s) = \begin{bmatrix} Z_{gdd} & Z_{gdq} \\ Z_{gqd} & \boldsymbol{Z_{gqq}} \end{bmatrix} = \begin{bmatrix} sL_g & -\boldsymbol{\omega L_g} \\ \omega L_g & \boldsymbol{sL_g} \end{bmatrix},$$

where L_g is the grid inductance.

C. SMALL SIGNAL MODELING OF UPQC

1) SMALL SIGNAL MODELING OF THE C-UPQC

Fig. 6(a) shows the dual closed-loop control block diagram of the series converter for the C-UPQC. From Fig. 6(a), the output of the outer voltage loop PI controller is given by

$$\Delta \boldsymbol{i}^c_{Csrdqr} = G_{Cvv}(s) \cdot \boldsymbol{I} \cdot \left(\Delta \boldsymbol{v}^c_{Ldqr} - \Delta \boldsymbol{v}^c_{Ldq} \right) \tag{22}$$

$$G_{Cvv}(s) = k_{Cvvp} + k_{Cvvi}/s \tag{23}$$

where $G_{Cvv}(s)$ is the transfer function (TF) of the outer loop PI controller. k_{Cvvp} and k_{Cvvi} are the gains, respectively. $\boldsymbol{I}$ is the 2×2 identity matrix. In (22), the reference value $\Delta \boldsymbol{v}^c_{Ldqr}$ is given directly, the input $\Delta \boldsymbol{v}^c_{Ldq}$ is derived from (14), namely

$$\Delta \boldsymbol{v}^c_{Ldq} = \Delta \boldsymbol{v}^s_{Ldq} + \boldsymbol{F}_{CL}(s) \cdot \Delta \boldsymbol{v}^s_{Sdq} \tag{24}$$

where

$$\boldsymbol{F}_{CL}(s) = \begin{bmatrix} 0 & \frac{G_{PI}(s) V^s_{Lq}}{s + G_{PI}(s) V_S} \\ 0 & -\frac{G_{PI}(s) V^s_{Ld}}{s + G_{PI}(s) V_S} \end{bmatrix}.$$

In this study, the UPQC-P [9] scheme is used. Thus, after compensation, the load voltage should be in-phase with the PCC voltage ($Vs\ Ld = V_{S0}$ and $Vs\ Lq = 0$V).

From Fig. 6(a), the output of the inner current loop PI controller of the series converter is expressed as

$$\Delta \boldsymbol{v}^c_{Cidqr} = G_{Cvi}(s) \cdot \boldsymbol{I} \cdot \left(\Delta \boldsymbol{i}^c_{Csrdqr} - \Delta \boldsymbol{i}^c_{Csrdq} \right) \tag{25}$$

$$G_{Cvi}(s) = k_{Cvip} \tag{26}$$

where k_{Cvip} is the gain of the P controller. The inductor current reference $\Delta \boldsymbol{i}^c_{Csrdqr}$ is achieved from (22), and the input $\Delta \boldsymbol{i}^c_{Csrdq}$ is obtained by applying the transformation (14)

$$\Delta \boldsymbol{i}^c_{Csrdq} = \Delta \boldsymbol{i}^s_{Csrdq} + \boldsymbol{F}_{Cr}(s) \cdot \Delta \boldsymbol{v}^s_{Sdq} \tag{27}$$

where

$$\boldsymbol{F}_{Cr}(s) = \begin{bmatrix} 0 & \frac{G_{PI}(s) I^s_{Csrq}}{s + G_{PI}(s) V_S} \\ 0 & -\frac{G_{PI}(s) I^s_{Csrd}}{s + G_{PI}(s) V_S} \end{bmatrix}, \begin{bmatrix} I^s_{Csrd} \\ I^s_{Csrq} \end{bmatrix} = \begin{bmatrix} V_{S0} I^s_{Ld} / V_S \\ \omega C_V (V_{S0} - V_S) \end{bmatrix}.$$

Considering the effects of the PLL and control delay $G_d(s)$, the relationship between $\Delta \boldsymbol{v}^c_{Cidqr}$ and $\Delta \boldsymbol{v}^s_{Cidq}$ is expressed as

$$\Delta \boldsymbol{v}^s_{Cidqr} = \Delta \boldsymbol{v}^c_{Cidqr} - \boldsymbol{F}_{Ci}(s) \cdot \Delta \boldsymbol{v}^s_{Sdq} \tag{28}$$

$$\Delta \boldsymbol{v}^s_{Cidq} = K_{PWM} G_d(s) \cdot \boldsymbol{I} \cdot \Delta \boldsymbol{v}^s_{Cidqr} \tag{29}$$

with

$$\boldsymbol{F}_{Ci}(s) = \begin{bmatrix} 0 & \frac{G_{PI}(s) V^s_{Ciq}}{s + G_{PI}(s) V_S} \\ 0 & -\frac{G_{PI}(s) V^s_{Cid}}{s + G_{PI}(s) V_S} \end{bmatrix}, G_d(s) = \frac{\left(1 - e^{-sT_s}\right) e^{-sT_s}}{sT_s},$$

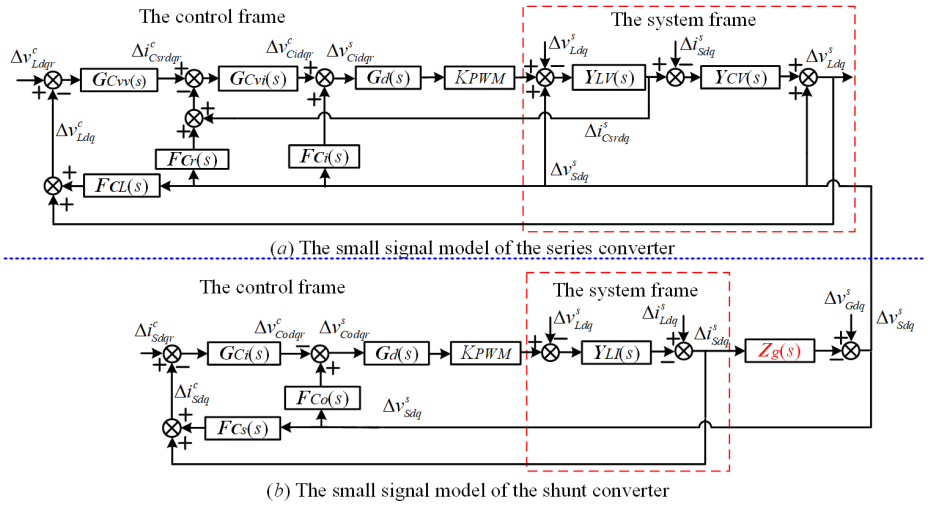

FIGURE 6. The dq-axis small signal model of the C-UPQC.

where T_s is the sampling period. K_{PWM} is the PWM gain. Combing (6) and (13), the expression of the steady-state output voltage for the series converter is

$$\begin{bmatrix} V^s_{Cid} \\ V^s_{Ciq} \end{bmatrix} = \begin{bmatrix} \left(1-\omega^2 L_V C_V\right)\left(V_{S0}-V_S\right)/K_{PWM} \\ \omega L_V V_{S0} I^s_{Ld}/K_{PWM} V_S \end{bmatrix} \tag{30}$$

Therefore, the expression of the load voltage in the C-UPQC is expressed as

$$\Delta \boldsymbol{v}^s_{Ldq} = \boldsymbol{G}_1(s)\Delta \boldsymbol{v}^s_{Sdq} + \boldsymbol{G}_2(s)\Delta \boldsymbol{i}^s_{Sdq}\,\boldsymbol{\mathcal{C}}\boldsymbol{G}_3(s)\Delta \boldsymbol{v}^c_{Ldqr} \tag{31}$$

where, as shown in the equation at the bottom of the next page.

The grid current-loop control block diagram of the shunt converter for the C-UPQC is shown in Fig. 6(*b*). The output of the grid current loop PI controller is given by

$$\Delta \boldsymbol{v}^c_{Codqr} = -G_{Ci}(s)\cdot \boldsymbol{I}\cdot\left(\Delta \boldsymbol{i}^c_{Sdqr} - \Delta \boldsymbol{i}^c_{Sdq}\right) \tag{32}$$

$$G_{Ci}(s) = k_{Cip} + k_{Cii}/s \tag{33}$$

where k_{Cip} and k_{Cii} are the gains of grid current PI controller.

In (32), the d-axis grid current reference value $\Delta \boldsymbol{ic}\ Sdr$ is given by the DC voltage loop directly and regarded as a constant value. The q-axis current reference value $\Delta \boldsymbol{ic}\ Sqr$ is given as 0A.

The input $\Delta \boldsymbol{i}^c_{Sdq}$ is derived by using the transformation (14)

$$\Delta \boldsymbol{i}^c_{Sdq} = \Delta \boldsymbol{i}^s_{Sdq} + \boldsymbol{F}_{Cs}(s)\cdot \Delta \boldsymbol{v}^s_{Sdq} \tag{34}$$

where

$$\boldsymbol{F}_{Cs}(s) = \begin{bmatrix} 0 & \frac{G_{PI}(s) I^s_{Sq}}{s+G_{PI}(s)V_S} \\ 0 & -\frac{G_{PI}(s) I^s_{Sd}}{s+G_{PI}(s)V_S} \end{bmatrix}, \begin{bmatrix} I^s_{Sd} \\ I^s_{Sq} \end{bmatrix} = \begin{bmatrix} \frac{V^s_{Ld}I^s_{Ld}+V^s_{Lq}I^s_{Lq}}{V_S} \\ 0 \end{bmatrix}.$$

From Fig. 6(*b*), the relationship between $\Delta \boldsymbol{v}^c_{Codqr}$ and $\Delta \boldsymbol{v}^s_{Codq}$ is descripted as

$$\Delta \boldsymbol{v}^s_{Codqr} = \Delta \boldsymbol{v}^c_{Codqr} - \boldsymbol{F}_{Co}(s)\cdot \Delta \boldsymbol{v}^s_{Sdq} \tag{35}$$

$$\Delta \boldsymbol{v}^s_{Codq} = K_{PWM}\cdot G_d(s)\cdot \boldsymbol{I}\cdot \Delta \boldsymbol{v}^s_{Codqr} \tag{36}$$

where

$$\begin{aligned} \boldsymbol{F}_{Co}(s) &= \begin{bmatrix} 0 & \frac{G_{PI}(s) V^s_{Coq}}{s+G_{PI}(s)V_S} \\ 0 & -\frac{G_{PI}(s) V^s_{Cod}}{s+G_{PI}(s)V_S} \end{bmatrix}, \begin{bmatrix} V^s_{Cod} \\ V^s_{Coq} \end{bmatrix} \\ &= \begin{bmatrix} \left(V_{S0}-\omega L_I I^s_{Lq}\right)/K_{PWM} \\ \omega L_I I^s_{Ld}\left(1-\frac{V_{S0}}{V_S}\right)/K_{PWM} \end{bmatrix}. \end{aligned}$$

Thus, the expression of the grid current in the C-UPQC is expressed as

$$\begin{aligned} \Delta \boldsymbol{i}^s_{Sdq} = {} & \boldsymbol{G}_4(s)\,\Delta \boldsymbol{v}^s_{Sdq} + \boldsymbol{G}_5(s)\,\Delta \boldsymbol{v}^s_{Ldq} + \boldsymbol{G}_6(s)\,\Delta \boldsymbol{i}^s_{Ldq} \\ & + \boldsymbol{G}_7(s)\,\Delta \boldsymbol{i}^c_{Sdqr} \end{aligned} \tag{37}$$

where

$$\begin{aligned} \boldsymbol{G}_4(s) &= -\frac{K_{PWM}\boldsymbol{F}_{Co}(s)\,\boldsymbol{G}_d(s) + K_{PWM}\boldsymbol{F}_{Cs}(s)\,\boldsymbol{G}_{Ci}(s)\,\boldsymbol{G}_d(s)}{\boldsymbol{Z}_{LI}(s) + K_{PWM}\boldsymbol{G}_{Ci}(s)\,\boldsymbol{G}_d(s)}, \\ \boldsymbol{G}_5(s) &= \frac{\boldsymbol{I}}{\boldsymbol{Z}_{LI}(s) + K_{PWM}\boldsymbol{G}_{Ci}(s)\,\boldsymbol{G}_d(s)}, \\ \boldsymbol{G}_6(s) &= \frac{\boldsymbol{Z}_{LI}(s)}{\boldsymbol{Z}_{LI}(s) + K_{PWM}\boldsymbol{G}_{Ci}(s)\,\boldsymbol{G}_d(s)}, \\ \boldsymbol{G}_7(s) &= \frac{\boldsymbol{G}_{Ci}(s)\,\boldsymbol{G}_d(s)}{\boldsymbol{Z}_{LI}(s) + K_{PWM}\boldsymbol{G}_{Ci}(s)\,\boldsymbol{G}_d(s)}. \end{aligned}$$

Combing (21), (31) and (37), the related TFs are written as

$$\begin{cases} \boldsymbol{G}_{LG}(s) = \dfrac{\Delta \boldsymbol{v}^s_{Ldq}}{\Delta \boldsymbol{v}^s_{Gdq}} = \left[\boldsymbol{I} - \boldsymbol{J}\boldsymbol{K}^{-1}\boldsymbol{G}_5(s)\right]^{-1} \\ \qquad \left[\boldsymbol{G}_1(s) + \boldsymbol{J}\boldsymbol{K}^{-1}\boldsymbol{G}_4(s)\right] \\ \boldsymbol{G}_{LL}(s) = \dfrac{\Delta \boldsymbol{v}^s_{Ldq}}{\Delta \boldsymbol{i}^s_{Ldq}} = \left[\boldsymbol{I} - \boldsymbol{J}\boldsymbol{K}^{-1}\boldsymbol{G}_5(s)\right]^{-1} \boldsymbol{J}\boldsymbol{K}^{-1}\boldsymbol{G}_6(s) \end{cases} \tag{38}$$

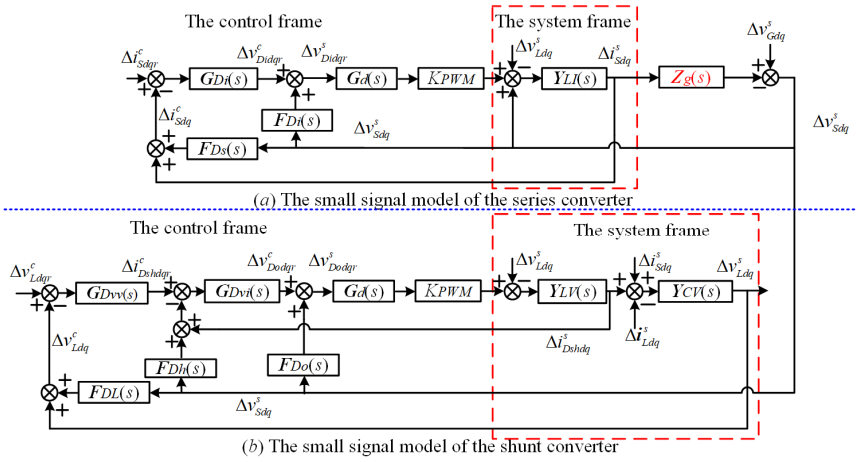

FIGURE 7. The dq-axis small signal model of the D-UPQC.

$$\begin{cases} \boldsymbol{G}_{SG}(s) = \dfrac{\Delta \boldsymbol{i}^s_{Sdq}}{\Delta \boldsymbol{v}^s_{Gdq}} = [\boldsymbol{K} - \boldsymbol{G}_5(s)\boldsymbol{J}]^{-1} \\ \qquad\qquad [\boldsymbol{G}_4(s) + \boldsymbol{G}_5(s)\boldsymbol{G}_1(s)] \\ \boldsymbol{G}_{SL}(s) = \dfrac{\Delta \boldsymbol{i}^s_{Sdq}}{\Delta \boldsymbol{i}^s_{Ldq}} = [\boldsymbol{K} - \boldsymbol{G}_5(s)\boldsymbol{J}]^{-1}\boldsymbol{G}_6(s) \end{cases} \tag{39}$$

where

$$\begin{cases} \boldsymbol{J} = \boldsymbol{G}_2(s) - \boldsymbol{G}_1(s)\boldsymbol{Z}_g(s) \\ \boldsymbol{K} = \boldsymbol{I} + \boldsymbol{G}_4(s)\boldsymbol{Z}_g(s) \end{cases}$$

2) SMALL SIGNAL MODELING OF THE D-UPQC

Fig. 7(*a*) shows the grid current-loop control block diagram of the series converter for the D-UPQC. As seen, the output of the grid current loop PI controller is

$$\Delta \boldsymbol{v}^c_{Didqr} = G_{Di}(s) \cdot \boldsymbol{I} \cdot \left(\Delta \boldsymbol{i}^c_{Sdqr} - \Delta \boldsymbol{i}^c_{Sdq}\right) \tag{40}$$

$$G_{Di}(s) = k_{Dip} + k_{Dii}/s \tag{41}$$

where k_{Dip} and k_{Dii} are the gains of the grid current PI controller.

The relationship between $\Delta \boldsymbol{v}^c_{Didqr}$ and $\Delta \boldsymbol{v}^s_{Didq}$ is expressed as

$$\Delta \boldsymbol{v}^s_{Didqr} = \Delta \boldsymbol{v}^c_{Didqr} - \boldsymbol{F}_{Di}(s) \cdot \boldsymbol{v}^s_{Sdq} \tag{42}$$

$$\Delta \boldsymbol{v}^s_{Didq} = K_{PWM} \cdot G_d(s) \cdot \boldsymbol{I} \cdot \Delta \boldsymbol{v}^s_{Didqr} \tag{43}$$

where

$$\boldsymbol{F}_{Di}(s) = \begin{bmatrix} 0 & \dfrac{G_{PI}(s)V^s_{Diq}}{s+G_{PI}(s)V_S} \\ 0 & -\dfrac{G_{PI}(s)V^s_{Did}}{s+G_{PI}(s)V_S} \end{bmatrix},$$

$$\begin{bmatrix} V^s_{Did} \\ V^s_{Diq} \end{bmatrix} = \begin{bmatrix} (V_{S0} - V_S)/K_{PWM} \\ \omega L_I V_{S0} I^s_{Ld}/K_{PWM} V_S \end{bmatrix}.$$

Thus, the expression of the grid current in the D-UPQC is expressed as

$$\Delta \boldsymbol{i}^s_{Sdq} = \boldsymbol{\varphi}_1(s)\,\Delta \boldsymbol{v}^s_{Sdq} + \boldsymbol{\varphi}_2(s)\,\Delta \boldsymbol{v}^s_{Ldq} + \boldsymbol{\varphi}_3(s)\,\Delta \boldsymbol{i}^c_{Sdqr} \tag{44}$$

where

$$\boldsymbol{\varphi}_1(s) = \frac{\boldsymbol{I} + K_{PWM}[\boldsymbol{F}_{Di}(s) - \boldsymbol{F}_{Ds}(s)\boldsymbol{G}_{Di}(s)]\boldsymbol{G}_d(s)}{\boldsymbol{Z}_{LI}(s) + K_{PWM}\boldsymbol{G}_{Di}(s)\boldsymbol{G}_d(s)},$$

$$\boldsymbol{\varphi}_2(s) = -\frac{\boldsymbol{I}}{\boldsymbol{Z}_{LI}(s) + K_{PWM}\boldsymbol{G}_{Di}(s)\boldsymbol{G}_d(s)},$$

$$\boldsymbol{\varphi}_3(s) = \frac{K_{PWM}\boldsymbol{G}_{Di}(s)\boldsymbol{G}_d(s)}{\boldsymbol{Z}_{LI}(s) + K_{PWM}\boldsymbol{G}_{Di}(s)\boldsymbol{G}_d(s)}.$$

where $\boldsymbol{F}_{Ds}(s) = F_{Cs}(s)$.

The dual closed-loop control block diagram of the shunt converter for the D-UPQC is seen in Fig. 7(*b*). From Fig. 7(*b*), the output of the outer voltage loop is

$$\Delta \boldsymbol{i}^c_{Dshdqr} = G_{Dvv}(s) \cdot \boldsymbol{I} \cdot \left(\Delta \boldsymbol{v}^c_{Ldqr} - \Delta \boldsymbol{v}^c_{Ldq}\right) \tag{45}$$

$$G_{Dvv}(s) = k_{Dvvp} + k_{Dvvi}/s \tag{46}$$

where $G_{Dvv}(s)$ is the transfer function of the outer voltage loop PI controller, k_{Dvvp} and k_{Dvvi} are the gains.

$$\boldsymbol{G}_1(s) = \boldsymbol{I} + \frac{K_{PWM}[\boldsymbol{F}_{Ci}(s) - (\boldsymbol{F}_{CL}(s)\boldsymbol{G}_{Cvv}(s) - \boldsymbol{G}_{Cvv}(s) + \boldsymbol{F}_{Cr}(s))\boldsymbol{G}_{Cvi}(s)]\boldsymbol{G}_d(s)}{\boldsymbol{I} + \boldsymbol{Z}_{CV}(s)\boldsymbol{Z}_{LV}(s) + K_{PWM}[\boldsymbol{G}_{Cvv}(s)\boldsymbol{G}_{Cvi}(s) + \boldsymbol{G}_{Cvi}(s)\boldsymbol{Z}_{CV}(s)]\boldsymbol{G}_d(s)},$$

$$\boldsymbol{G}_2(s) = -\frac{K_{PWM}\boldsymbol{G}_{Cvi}(s)\boldsymbol{G}_d(s) + \boldsymbol{Z}_{LV}(s)}{\boldsymbol{I} + \boldsymbol{Z}_{CV}(s)\boldsymbol{Z}_{LV}(s) + K_{PWM}[\boldsymbol{G}_{Cvv}(s)\boldsymbol{G}_{Cvi}(s) + \boldsymbol{G}_{Cvi}(s)\boldsymbol{Z}_{CV}(s)]\boldsymbol{G}_d(s)},$$

$$\boldsymbol{G}_3(s) = \frac{K_{PWM}\boldsymbol{G}_{Cvv}(s)\boldsymbol{G}_{Cvi}(s)\boldsymbol{G}_d(s)}{\boldsymbol{I} + \boldsymbol{Z}_{CV}(s)\boldsymbol{Z}_{LV}(s) + K_{PWM}[\boldsymbol{G}_{Cvv}(s)\boldsymbol{G}_{Cvi}(s) + \boldsymbol{G}_{Cvi}(s)\boldsymbol{Z}_{CV}(s)]\boldsymbol{G}_d(s)}.$$

TABLE 1. Main circuit parameters for the UPQC-QAB.

Symbol	Description	Value
v_{Gm}	Grid voltage (line-to-line)	380V
ω	Grid angular frequency	314rad/s
L_V	Filter inductance of the LC filter	6mH
C_V	Filter capacitance of the LC filter	80μF
L_I	Filter inductance of the L filter	4mH
v_m	Port voltage of series DC-link	400V
v_d	Port voltage of shunt DC-link	800V
C_m	Capacitance of DC port m	1e3μF
C_d	Capacitance of DC port d	4e3μF

From Fig. 7(*b*), the output of the inner current loop P controller is

$$\Delta \boldsymbol{v}^c_{Dodqr} = G_{Dvi}(s) \cdot \boldsymbol{I} \cdot \left(\Delta \boldsymbol{i}^c_{Dshdqr} - \Delta \boldsymbol{i}^c_{Dshdq}\right) \tag{47}$$

$$G_{Dvi}(s) = k_{Dvip} \tag{48}$$

where k_{Dvip} is the gain of the P controller.

Based on (14), the relationship between the variable Δi^s_{Dshdq} and Δi^c_{Dshdq} is expressed as

$$\Delta \boldsymbol{i}^c_{Dshdq} = \Delta \boldsymbol{i}^s_{Dshdq} + \boldsymbol{F}_{Dh}(s) \cdot \Delta \boldsymbol{v}^s_{Sdq} \tag{49}$$

where

$$\boldsymbol{F}_{Dh}(s) = \begin{bmatrix} 0 & \frac{G_{PI}(s) I^s_{Dshq}}{s + G_{PI}(s) V_S} \\ 0 & -\frac{G_{PI}(s) I^s_{Dshd}}{s + G_{PI}(s) V_S} \end{bmatrix},$$

$$\begin{bmatrix} I^s_{Dshd} \\ I^s_{Dshq} \end{bmatrix} = \begin{bmatrix} I^s_{Ld}\left(1 - V_{S0}/V_S\right) \\ I^s_{Lq} + \omega C_V V_{S0} \end{bmatrix}.$$

Then, the relationship between the control output and the system input for the shunt converter is descripted as

$$\Delta \boldsymbol{v}^s_{Dodqr} = \Delta \boldsymbol{v}^c_{Dodqr} - \boldsymbol{F}_{Di}(s) \cdot \Delta \boldsymbol{v}^s_{Sdq} \tag{50}$$

$$\Delta \boldsymbol{v}^s_{Dodq} = K_{PWM} \cdot G_d(s) \cdot \boldsymbol{I} \cdot \Delta \boldsymbol{v}^s_{Dodqr} \tag{51}$$

where

$$\boldsymbol{F}_{Do}(s) = \begin{bmatrix} 0 & \frac{G_{PI}(s) V^s_{Doq}}{s + G_{PI}(s) V_S} \\ 0 & -\frac{G_{PI}(s) V^s_{Dod}}{s + G_{PI}(s) V_S} \end{bmatrix},$$

$$\begin{bmatrix} V^s_{Dod} \\ V^s_{Doq} \end{bmatrix} = \begin{bmatrix} \left[V_{S0} - \omega L_V \left(I^s_{Lq} + \omega C_V V_{S0}\right)\right] / K_{PWM} \\ \omega L_V I^s_{Ld}\left(1 - V_{S0}/V_S\right)/K_{PWM} \end{bmatrix}.$$

From Fig. 7(*b*), the expression of the load voltage in the D-UPQC is expressed as

$$\Delta \boldsymbol{v}^s_{Ldq} = \boldsymbol{\varphi}_4(s)\,\Delta \boldsymbol{v}^s_{Sdq} + \boldsymbol{\varphi}_5(s)\,\Delta \boldsymbol{v}^c_{Ldqr} + \boldsymbol{\varphi}_6(s)\,\Delta \boldsymbol{i}^s_{Ldq} + \boldsymbol{\varphi}_7(s)\,\Delta \boldsymbol{i}^s_{Sdq} \tag{52}$$

with, as shown in the equation at the bottom of the next page, where $\boldsymbol{F}_{DL}(s) = F_{CL}(s)$.

TABLE 2. Control parameters for the UPQC-QAB.

Symbol	Description	Value
k_{Ppll}	Proportional gain of PLL	3
k_{Ipll}	Integral gain of PLL	1.4e3
k_{Cvvp}/k_{Dvvp}	Proportional gains of load voltage controller	1
k_{Cvvi}/k_{Dvvi}	Integral gains of load voltage controller	800
k_{Cvip}/k_{Dvip}	Proportional gains of P controller	1
k_{Cip}/k_{Dip}	Proportional gains of grid current controller	2
k_{Cii}/k_{Dii}	Integral gains of grid current controller	1e3

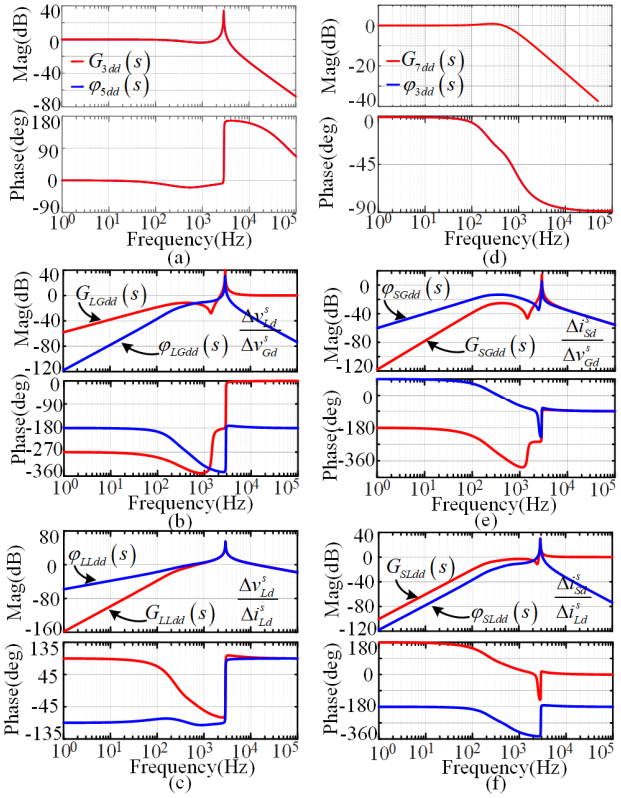

FIGURE 8. Frequency response of the TFs in the C- and D-UPQC.

Combing (21), (44) and (52), the related TFs are written as

$$\begin{cases} \boldsymbol{\varphi}_{LG}(s) = \dfrac{\Delta \boldsymbol{v}^s_{Ldq}}{\Delta \boldsymbol{v}^s_{Gdq}} = \left[\boldsymbol{I} - \boldsymbol{L}\boldsymbol{M}^{-1}\boldsymbol{\varphi}_2(s)\right]^{-1} \\ \qquad\qquad \left[\boldsymbol{\varphi}_4(s) + \boldsymbol{L}\boldsymbol{M}^{-1}\boldsymbol{\varphi}_1(s)\right] \\ \boldsymbol{\varphi}_{LL}(s) = \dfrac{\Delta \boldsymbol{v}^s_{Ldq}}{\Delta \boldsymbol{i}^s_{Ldq}} = \left[\boldsymbol{I} - \boldsymbol{L}\boldsymbol{M}^{-1}\boldsymbol{\varphi}_2(s)\right]^{-1} \cdot \boldsymbol{\varphi}_6(s) \end{cases} \tag{53}$$

$$\begin{cases} \boldsymbol{\varphi}_{SG}(s) = \dfrac{\Delta \boldsymbol{i}^s_{Sdq}}{\Delta \boldsymbol{v}^s_{Gdq}} = \left[\boldsymbol{M} - \boldsymbol{\varphi}_2(s)\,\boldsymbol{L}\right]^{-1} \\ \qquad\qquad \left[\boldsymbol{\varphi}_1(s) + \boldsymbol{\varphi}_2(s)\,\boldsymbol{\varphi}_4(s)\right] \\ \boldsymbol{\varphi}_{SL}(s) = \dfrac{\Delta \boldsymbol{i}^s_{Sdq}}{\Delta \boldsymbol{i}^s_{Ldq}} = \left[\boldsymbol{M} - \boldsymbol{\varphi}_2(s)\,\boldsymbol{L}\right]^{-1} \boldsymbol{\varphi}_2(s)\,\boldsymbol{\varphi}_6(s) \end{cases} \tag{54}$$

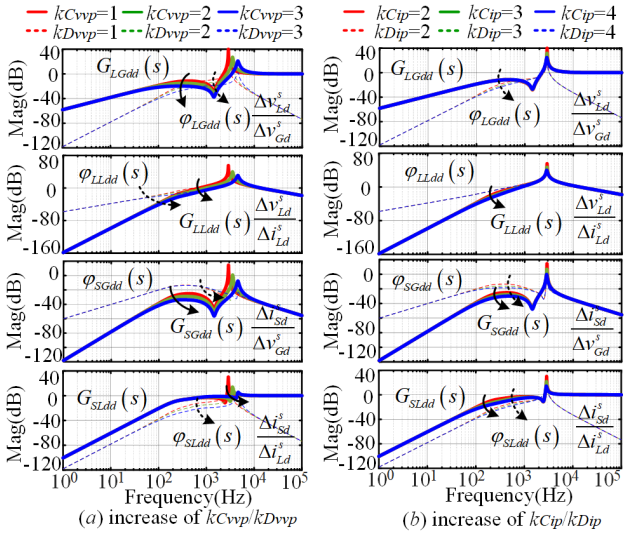

FIGURE 9. Frequency response of TFs under different control parameters.

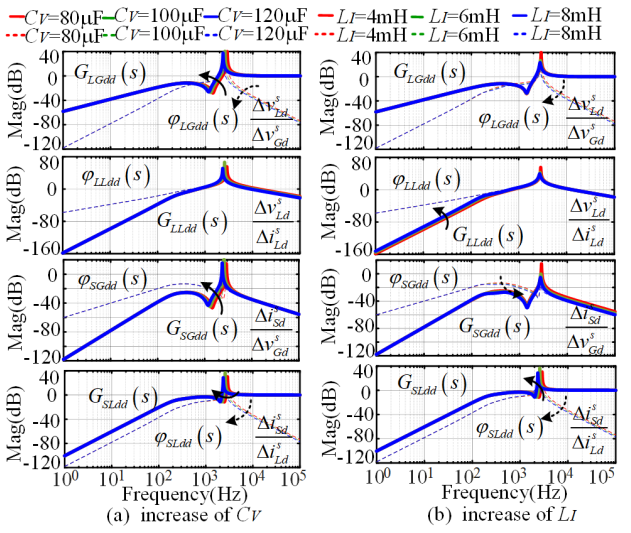

FIGURE 10. Frequency response of TFs under different circuit parameters.

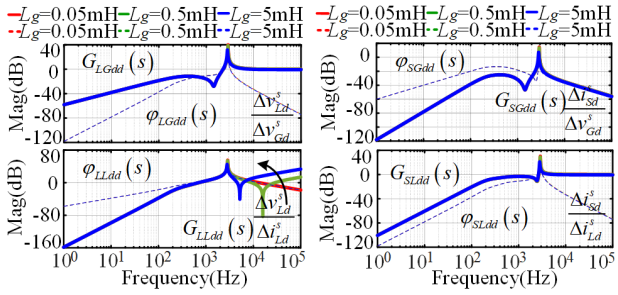

FIGURE 11. Frequency response of TFs under different grid impedance.

where

$$\begin{cases} \boldsymbol{L} = \boldsymbol{\varphi}_7(s) - \boldsymbol{\varphi}_4(s)\boldsymbol{Z}_g(s) \\ \boldsymbol{M} = \boldsymbol{I} + \boldsymbol{\varphi}_1(s)\boldsymbol{Z}_g(s) \end{cases}$$

V. CONTROL PERFORMANCE ANALYSIS OF UPQC

The *dq*-axis small signal models of the C- and D-UPQC are deduced detailly in section IV. On the basis of the models above, this section will further compare and analyze the performance of the load voltage and grid current in the C- and D-UPQC.

In addition, the control parameters of the UPQC are designed based on the system engineering design method [23]. For the load voltage controllers, both two schemes utilize the dual closed-loop PI control. Generally, the bandwidth of the inner current loop should be no more than $0.1{*}2\pi{*}f_{sw}$ (f_{sw} is the switching frequency), and the bandwidth of the outer voltage loop should be less than 1/10 of the inner current loop bandwidth. Accordingly, for the grid current controllers, both two schemes utilize the PI control. The parameter design of the grid current loop can refer to load voltage controller. The electrical and control parameters of the UPQC are shown in Table 1 and 2. The switching frequency of series, shunt and QAB converter are given as 20kHz, 20kHz and 50kHz.

A. INFLUENCE OF VOLTAGE/CURRENT HARMONICS

1) LOAD VOLTAGE TRACKING PERFORMANCE

Firstly, the load voltage tracking performance is analyzed from the topologies. Since the capacitive reactance of the LC filter is inversely proportional to the frequency, the load voltage in the C-UPQC has a poor performance in mitigating the high-frequency grid voltage harmonics. In addition, the inductive reactance of the shunt L filter is proportional to the

$$\boldsymbol{\varphi}_4(s) = \frac{[\boldsymbol{F}_{Do}(s) - (\boldsymbol{F}_{DL}(s)\boldsymbol{G}_{Dvv}(s) + \boldsymbol{F}_{Dh}(s))\boldsymbol{G}_{Dvi}(s)]K_{PWM}\boldsymbol{G}_d(s)}{\boldsymbol{I} + \boldsymbol{Z}_{CV}(s)\boldsymbol{Z}_{LV}(s) + [\boldsymbol{G}_{Dvv}(s)\boldsymbol{G}_{Dvi}(s) + \boldsymbol{G}_{Dvi}(s)\boldsymbol{Z}_{CV}(s)]K_{PWM}\boldsymbol{G}_d(s)},$$

$$\boldsymbol{\varphi}_5(s) = \frac{\boldsymbol{G}_{Dvv}(s)\boldsymbol{G}_{Dvi}(s)K_{PWM}\boldsymbol{G}_d(s)}{\boldsymbol{I}\,\boldsymbol{C}\,\boldsymbol{Z}_{CV}(s)\boldsymbol{Z}_{LV}(s) + [\boldsymbol{G}_{Dvv}(s)\boldsymbol{G}_{Dvi}(s) + \boldsymbol{G}_{Dvi}(s)\boldsymbol{Z}_{CV}(s)]K_{PWM}\boldsymbol{G}_d(s)},$$

$$\boldsymbol{\varphi}_6(s) = -\frac{\boldsymbol{G}_{Dvi}(s)K_{PWM}\boldsymbol{G}_d(s) + \boldsymbol{Z}_{LV}(s)}{\boldsymbol{I} + \boldsymbol{Z}_{CV}(s)\boldsymbol{Z}_{LV}(s) + [\boldsymbol{G}_{Dvv}(s)\boldsymbol{G}_{Dvi}(s) + \boldsymbol{G}_{Dvi}(s)\boldsymbol{Z}_{CV}(s)]K_{PWM}\boldsymbol{G}_d(s)},$$

$$\boldsymbol{\varphi}_7(s) = \frac{\boldsymbol{G}_{Dvi}(s)K_{PWM}\boldsymbol{G}_d(s) + \boldsymbol{Z}_{LV}(s)}{\boldsymbol{I} + \boldsymbol{Z}_{CV}(s)\boldsymbol{Z}_{LV}(s) + [\boldsymbol{G}_{Dvv}(s)\boldsymbol{G}_{Dvi}(s) + \boldsymbol{G}_{Dvi}(s)\boldsymbol{Z}_{CV}(s)]K_{PWM}\boldsymbol{G}_d(s)},$$

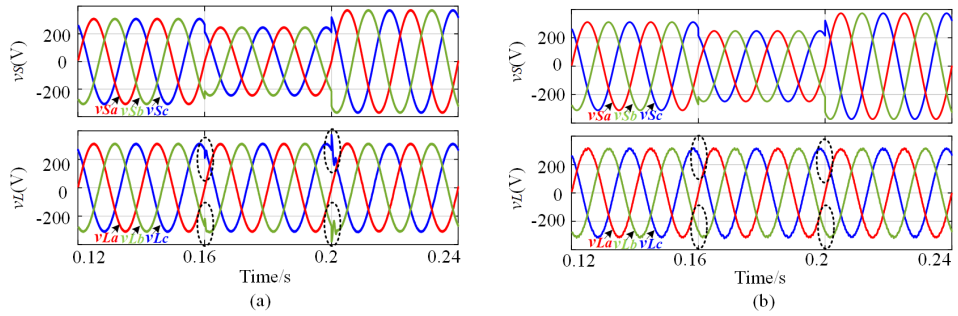

FIGURE 12. The simulation waveforms under grid voltage sag and swell: (a) C-UPQC, (b) D-UPQC.

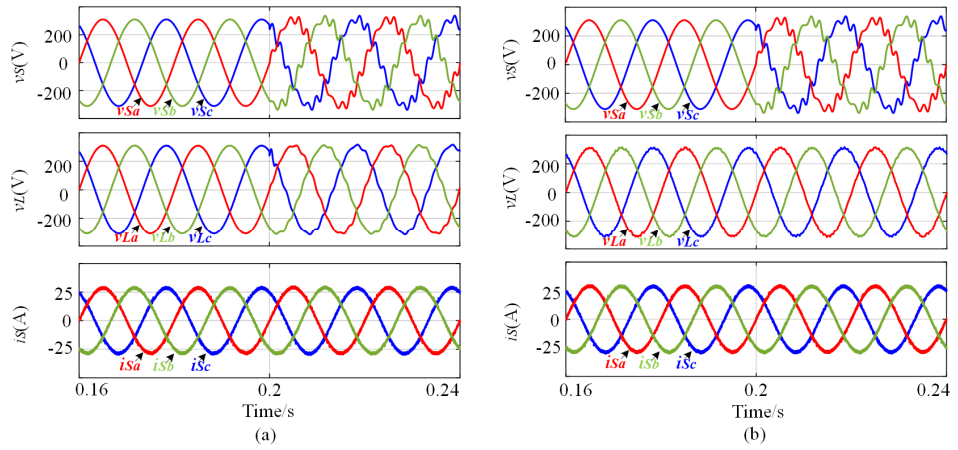

FIGURE 13. The simulation waveforms under grid voltage harmonics distortion: (a) C-UPQC, (b) D-UPQC.

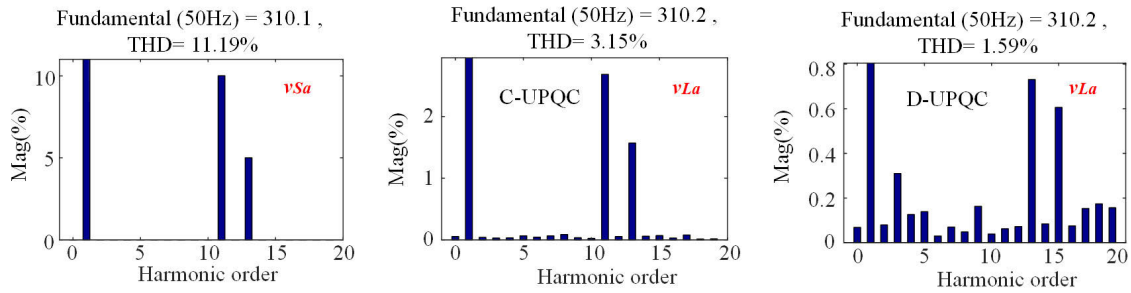

FIGURE 14. The spectrum analysis of vSa and vLa under grid voltage harmonics distortion.

frequency, thus the shunt converter in the C-UPQC tends to block the high frequency components of the load currents. It leads to the high frequency current harmonics flow into the power grid and affect the grid current and the load voltage. However, in theD-UPQC, the high-frequency load current harmonics tend to flow through the capacitor C_{Dshm} due to its smaller capacitive reactance. Thus, in the D-UPQC, the load voltage is mainly affected by the load current harmonics.

Secondly, the load voltage tracking performance is analyzed from the small signal model ((38) and (53)). For convenience, the d-axis coordinate system is taken as an example to draw the relevant TF bode diagrams (Fig. 8(a)-(c)). Fig. 8(a) shows the bode diagram of $G_{3dd}(s)$ and $\varphi_{5dd}(s)$ ($\boldsymbol{G}_3(s) = \varphi_5(s)$). As seen, in the C- and D-UPQC, the load voltages $\Delta vs\ Ld$ can realize the error-free tracking of the reference signal $\Delta vs\ Ldr$. As seen in Fig. 8(b), in most cases, the amplitude of $G_{LGdd}(s)$ is bigger than that of $\varphi_{LGdd}(s)$; especially, the amplitude of $G_{LGdd}(s)$ is equal to 0dB in high frequency range. In Fig. 8(c), the load voltage cannot suppress the influence caused by the grid current harmonics (1∼10kHz) and the amplitude of $G_{LLdd}(s)$ is smaller than that of $\varphi_{LLdd}(s)$ in low frequency range. Thus, the grid voltage

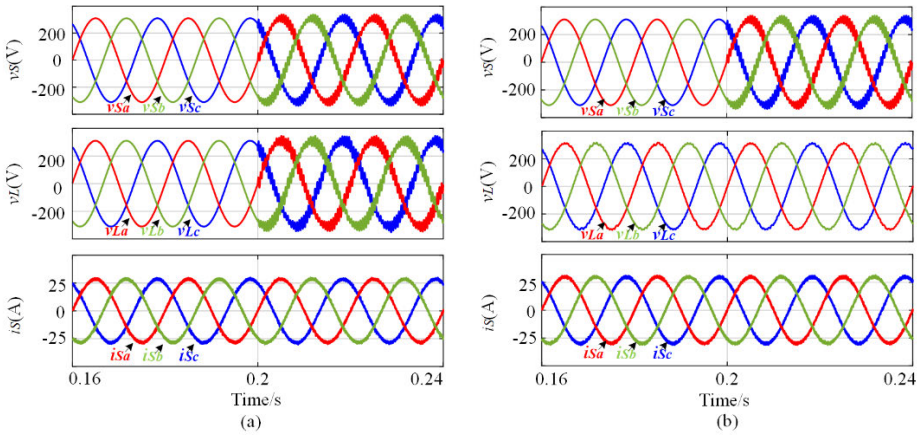

FIGURE 15. The simulation waveforms under high-frequency grid voltage harmonics distortion: (a) C-UPQC, (b) D-UPQC.

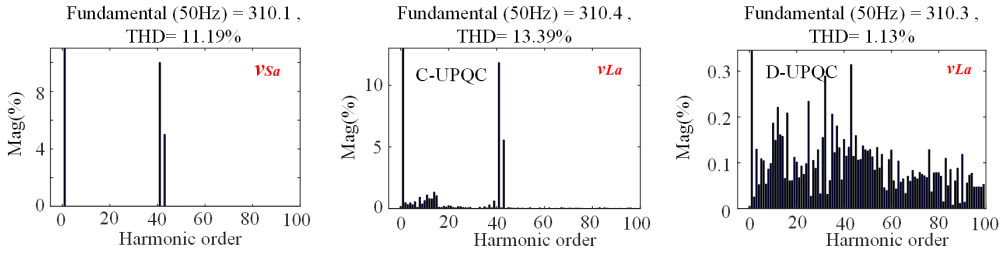

FIGURE 16. The spectrum analysis of vSa and vLa under high-frequency grid voltage harmonics distortion.

harmonics mainly distort the load voltage in the C-UPQC; the load current harmonics will distort the load voltages in two schemes.

2) GRID CURRENT TRACKING PERFORMANCE

From the topologies, the D-UPQC has a better performance in blocking the load current harmonics flowing to the power grid because the inductive reactance is higher in high frequency range. In the C-UPQC, the shunt converter blocks the high frequency load current harmonics.

Next, from the small signal models ((39) and (54)), Fig. 8(d)-(f) show the TF bode diagrams of the d-axis grid current loop in the C- and D-UPQC. In Fig. 8(d) ($G_{7dd}(s) = \varphi_{3dd}(s)$), in both two schemes, the gird current Δi^s_{Sd} can realize the error-free tracking of the reference signal Δi^s_{Sdr}. As seen in Fig. 8(e), although the amplitude of $\varphi_{SGdd}(s)$ is bigger than that of $G_{SGdd}(s)$ in low frequency range, the amplitude of $\varphi_{SGdd}(s)$ and $G_{SGdd}(s)$ is always smaller than 0dB. In Fig. 8(f), the amplitude of $G_{SLdd}(s)$ is always bigger than that of $\varphi_{SLdd}(s)$; especially in high frequency range, the amplitude of $G_{SLdd}(s)$ is equal to 0dB. Thus, the load current harmonics affect the current quality in the C-UPQC, and the influence caused by the grid voltage harmonics on the grid current is not obvious in two schemes.

TABLE 3. Load parameters in the simulations.

Load 1	Ra = 10Ω; La = 10mH Rb = 10Ω; Lb = 10mH Rc = 10Ω; Lc = 10mH
Load 2	Rectifier load: R = 10Ω; L = 10mH

B. INFLUENCE OF CONTROL AND CIRCUIT PARAMETERS

This subsection analyzes the control performance of the UPQC under different control and circuit parameters (k_{Dvvp}, k_{Cvvp}, k_{Dip}, k_{Cip}, C_V and L_I).

Fig. 9 shows the related TF bode diagrams of the C- and D-UPQC under different control parameters. As seen, with the increase of k_{Dvvp}/k_{Cvvp} and k_{Dip}/k_{Cip} (increase of the bandwidth of load voltage and grid current loop), all the amplitudes of the TFs tend to decrease. It means that increasing the bandwidth of the outer load voltage and grid current loop helps improve the load voltage and grid current quality in both two schemes.

The related TF bode diagrams under different filter parameters are seen in Fig. 10. As shown, when C_V or L_V increases, the amplitudes of the TFs in the D-UPQC tend to decrease in most cases, while these amplitudes in the C-UPQC tend to increase. It means that increasing the filter inductance and

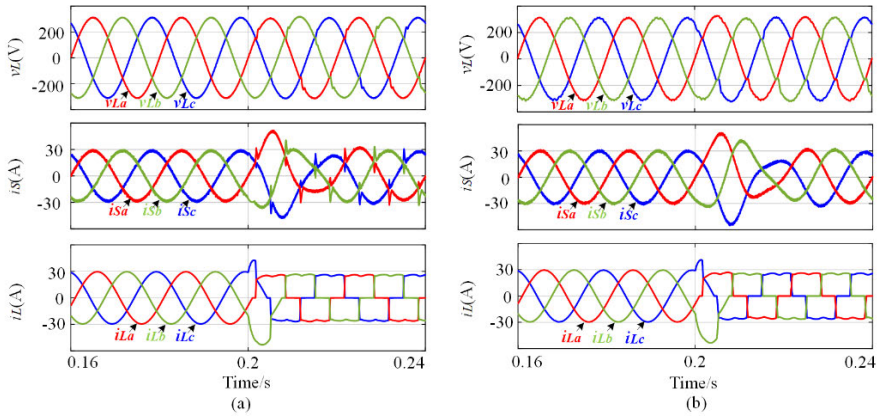

FIGURE 17. The simulation waveforms under different loads: (a) C-UPQC, (b) D-UPQC.

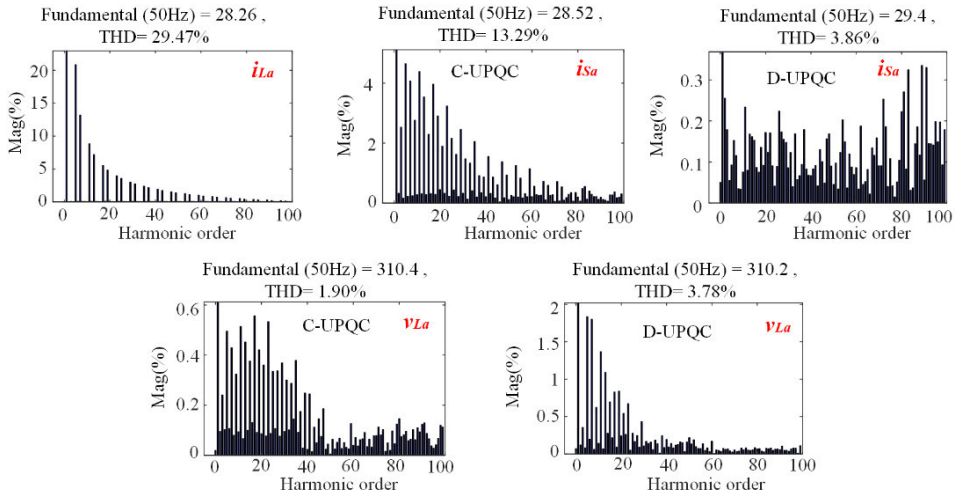

FIGURE 18. The spectrum analysis of iLa, iSa and vLa under different loads.

capacitance can improve the load voltage and grid current quality in the D-UPQC.

C. INFLUENCE OF GRID IMPEDANCE

This subsection mainly considers the control performance of the UPQC under different grid impedance.

From the UPQC circuits, the grid current controlled by the UPQC contains few harmonics, and they will flow through the grid impedance and further distort the PCC voltage quality. Since the C-UPQC cannot mitigate the high frequency PCC voltage harmonics, the load voltage quality in the C-UPQC will be poorer when L_g increases.

As seen in Fig. 11, when L_g increases, the TFs of the D-UPQC can remain unchanged. It means that the D-UPQC can still keep good load voltage and grid current quality under different grid impedance. However, in the C-UPQC, the amplitude of $G_{LLdd}(s)$ in high frequency range becomes greater and bigger than 0dB when L_g increases. Thus, the load voltage in the C-UPQC will affected heavily by the load current harmonics in weak grid. It is concluded that the grid impedance mainly affected the load voltage quality in the C-UPQC, while the performance of the D-UPQC is not affected.

VI. SIMULATION AND EXPERIMENTAL RESULTS

In this section, the correctness of the system performance analysis for the C- and D-UPQC is verified in the MATLAB/Simulink and experimental platform.

A. SIMULATION RESULTS

The circuit and control parameters in the simulations are seen in Table 1 and 2. The switching frequency of the UPQC system are the same with those in section V. And the detailed load parameters are seen in Table 3.

1) INFLUENCE OF THE GRID VOLTAGES

This case mainly illustrates the influence on the load voltage and the grid current for the C- and D-UPQC caused by the grid voltage fluctuation. The load 1 is connected, and the grid inductance is given as 0.05mH.

Fig. 12(a)-(b) show the waveforms of v_S and v_L. As seen, the grid voltage sags with a depth of 20% within [0.16, 0.20] s and swells with a depth of 20% within (0.20, 0.20] s. After compensation, the load voltage amplitudes of the C- and D-UPQC could be at the nominal values. However, the

TABLE 4. The comparative analysis results of C- and D-UPQC with different control and circuit parameters.

		Total Harmonic Distortion (THD/%)																	
		Distorted Grid Voltage and Linear Load									Sinusoidal Grid Voltage and Rectifier Load								
			k_{Dvvp}/k_{Cvvp}		k_{Dip}/k_{Cip}		C_f(μF)		L_l(mH)			k_{Dvvp}/k_{Cvvp}		k_{Dip}/k_{Cip}		C_f(μF)		L_l(mH)	
			2	3	3	4	100	120	6	8		2	3	3	4	100	120	6	8
v_{Sa}	C-UPQC	**11.3**	11.3	11.3	11.3	11.3	11.3	11.3	11.2	11.3	**1.3**	1.2	1.3	1.2	1.3	1.3	1.3	1.2	1.2
	D-UPQC	**11.3**	11.3	11.3	11.3	11.3	11.3	11.3	11.2	11.2	**1.3**	1.3	1.3	1.3	1.3	1.3	1.3	1.3	1.3
v_{La}	C-UPQC	**2.8**	**2.3**	**2.2**	2.7	2.8	**3.5**	**4.2**	5.1	5.5	**3.2**	**3.2**	**3.1**	3.1	2.9	**3.7**	**3.9**	3.3	3.7
	D-UPQC	**1.1**	**1.0**	**1.0**	1.0	0.8	**0.7**	**0.6**	0.8	0.8	**5.7**	**5.5**	**5.2**	5.7	5.7	**5.6**	**5.5**	5.7	5.7
i_{Sa}	C-UPQC	**3.5**	3.5	3.4	**3.5**	**3.4**	3.6	3.7	**3.7**	**3.8**	**9.5**	9.6	9.5	**9.3**	**9.1**	9.6	10.9	**12.3**	**14.7**
	D-UPQC	**3.8**	3.8	3.8	**3.6**	**3.6**	3.8	3.8	**2.2**	**1.7**	**3.5**	3.5	3.5	**3.3**	**3.3**	3.4	3.4	**2.1**	**1.7**
i_{La}	C-UPQC	**0.5**	0.3	0.3	0.5	1.0	0.7	0.8	1	1.1	**28.7**	29.0	29	29	28.8	29	29	28.3	28
	D-UPQC	**0.2**	0.2	0.2	0.1	0.1	0.1	0.1	0.1	0.1	**25.9**	26.8	27.4	25.9	25.9	26	26	26	25.9

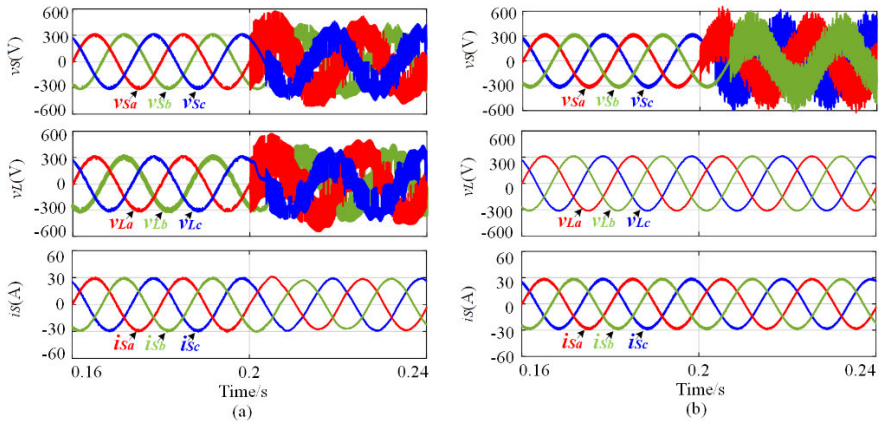

FIGURE 19. The simulation waveforms under different grid impedance: (a) C-UPQC, (b) D-UPQC

D-UPQC has a better dynamic performance when the grid voltage suffers sudden variation.

Fig. 13(a)-(b) illustrates the waveforms of v_S, v_L and i_S when the grid voltage suffers harmonic distortion. Fig. 14 is the related spectrum analysis of v_{Sa} and v_{La}. From Fig. 14, the grid voltage mainly contains 11^{th} and 13^{th} harmonic components. After compensation, the load voltage in the D-UPQC can remain sinusoidal (the total harmonic distortion (THD) is 1.59%), while the THD of the load voltage in the C-UPQC is higher (the related THD is 3.15%). Figs. 15-16 show the related waveforms and spectrum analysis when the grid voltage suffers high-frequency harmonic distortion. As shown in Fig. 16, the grid voltage mainly contains 41^{th} and 43^{th} harmonic components (the related THD is about 11.19%). After compensation, the load voltage in the D-UPQC can keep sinusoidal and the related amplitude is at nominal value (the related THD is 1.13%). However, the load voltage in the C-UPQC contains lots of harmonic components (the related THD is 13.39%). Besides, the grid currents in both two schemes can remain sinusoidal. Thus, from the above analysis, the load voltage in the D-UPQC has a stronger robustness, and the grid currents in both two schemes are robust to the grid voltage harmonic distortion.

2) INFLUENCE OF THE LOAD CURRENTS

This case study is designed to verify the performance analysis of the UPQC when the load current harmonics are considered. In addition, the grid voltage is normal and the grid inductance is given as 0.05mH. The load 2 is connected.

Figs. 17-18 shows the waveforms and spectrum analysis for the UPQC when load 1 and 2 are switched. As seen, the three-phase balanced load 1 is switched to the purely nonlinear load 2 (the THD of the load current is 29.47%). After compensation, the grid current in the C-UPQC still contains lots of harmonic components (the related THD is 29.47%), while the grid current in the D-UPQC can almost remain sinusoidal (the related THD is 3.86%). Besides, in both two schemes, the load voltage contains few harmonics.

But the THD of the load voltage in the D-UPQC (3.78%) is higher than that in the C-UPQC (1.90%). It is concluded

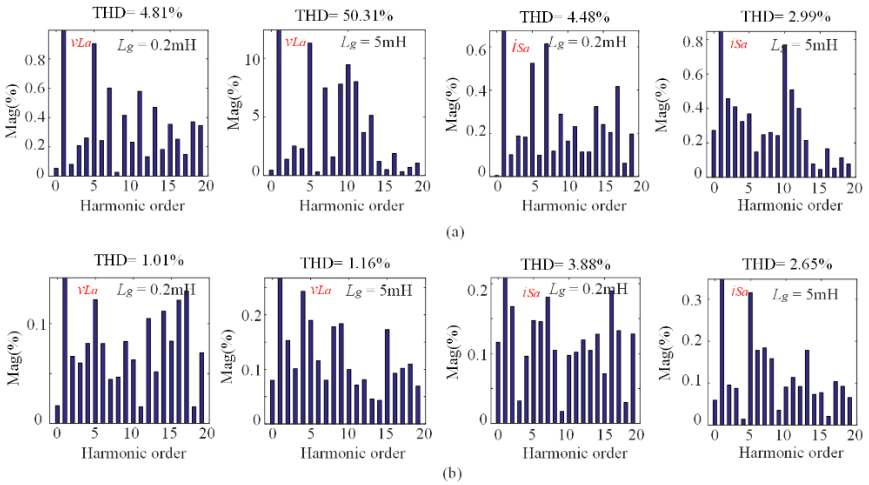

FIGURE 20. The spectrum analysis of vLa and iSa under different grid impedance: (a) C-UPQC, (b) D-UPQC

that the grid current in the D-UPQC has a better robustness and the load voltage quality in the C-UPQC is better when the load currents is distorted.

3) INFLUENCE OF CONTROL AND CIRCUIT PARAMETERS

This subsection is designed to test the performance of the UPQC under different control and circuit parameters.

Table 4 shows the comparative results of the THD for v_{Sa}, v_{La}, i_{Sa} and i_{La}. As shown, with the increase of k_{Dvvp}/k_{Cvvp}, the THD of v_{La} decreases; when C_V increases, the THD of v_{La} in D-UPQC also decreases while the THD of v_{La} in C-UPQC increases. Besides, when k_{Dip}/k_{Cip} increases, the THD of i_{Sa} in both two schemes decrease; however, with the increase of L_I, the THD of i_{Sa} in the D-UPQC decreases greatly, but the THD of i_{Sa} in the C-UPQC increases. The results in Table 4 have proven the correctness of the comparative analysis in section V.

4) INFLUENCE OF THE GRID IMPEDANCE

This case study is designed to test the performance of the UPQC under different grid impedance (L_g increases to 5mH from 0.2mH at 0.2s). And other parameters remain unchanged.

Figs. 19-20 show the waveforms and spectrum analysis for the UPQC under different gird impedance. As illustrated, when L_g increases, the PCC voltage is distorted more heavily. In the C-UPQC, the THD of the load voltage increases to 50.31% from 4.81%, while the related THD in the D-UPQC increases to 1.16% from 1.01%. And the THDs of the grid currents (always smaller than 5%) decrease in both two schemes with the increase of L_g. Therefore, the grid impedance mainly affects the load voltage quality in the C-UPQC.

B. EXPERIMENTAL RESULTS

In this section, the experimental platform is built to verify the performance analysis of the UPQC. A 2-kW prototype has been built in the laboratory, as shown in Fig. 21. The circuit parameters are seen in [26]. Besides, the QAB converter is composed of four full bridge modules and four leakage inductors, which are connected through high frequency transformer (HFT). The HFT adopts PQ 50-50 magnetic core. Chroma 61830 supplies the three-phase UPQC-QAB system.

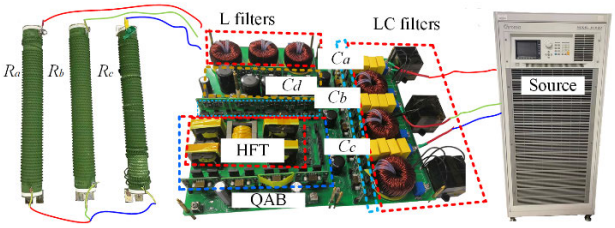

FIGURE 21. Experimental prototype

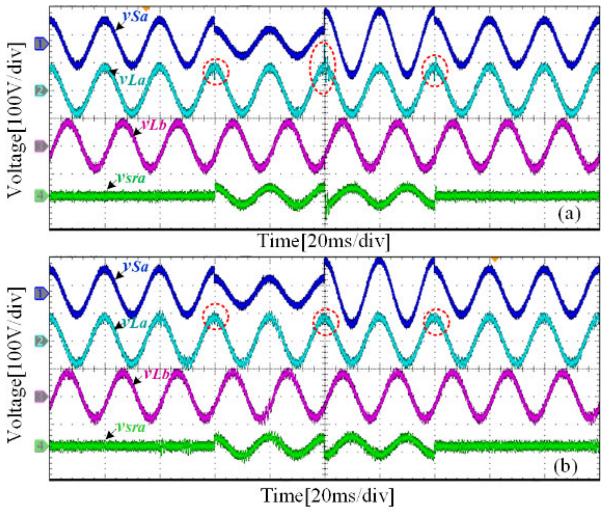

FIGURE 22. Experimental waveforms under the grid voltage sag and swell: (a) C-UPQC, (b) D-UPQC.

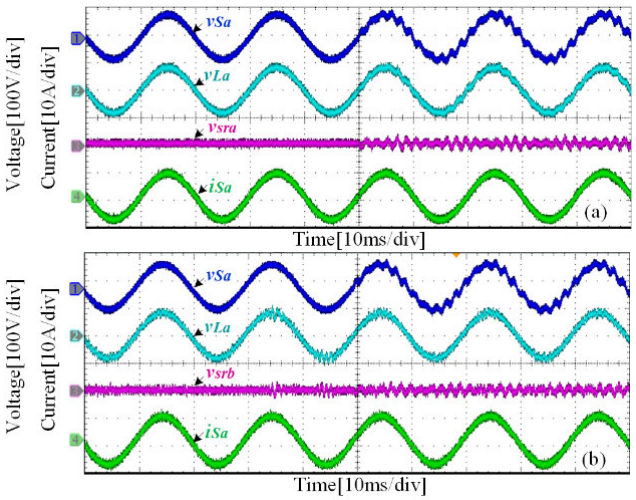

FIGURE 23. Experimental waveforms under the distorted grid voltage: (a) C-UPQC, (b) D-UPQC.

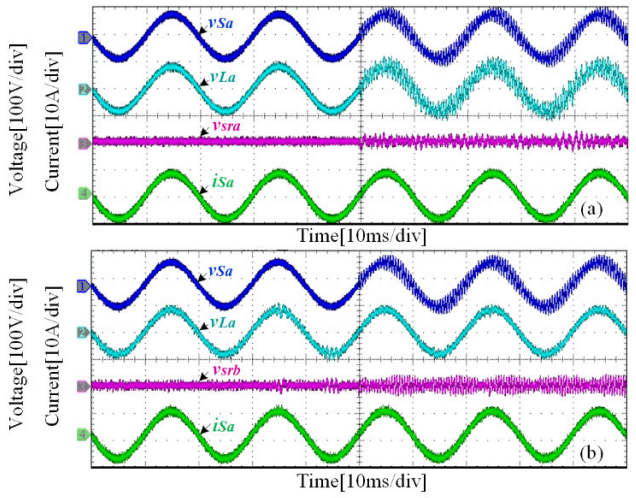

FIGURE 24. Experimental waveforms under the distorted grid voltage: (a) C-UPQC, (b) D-UPQC.

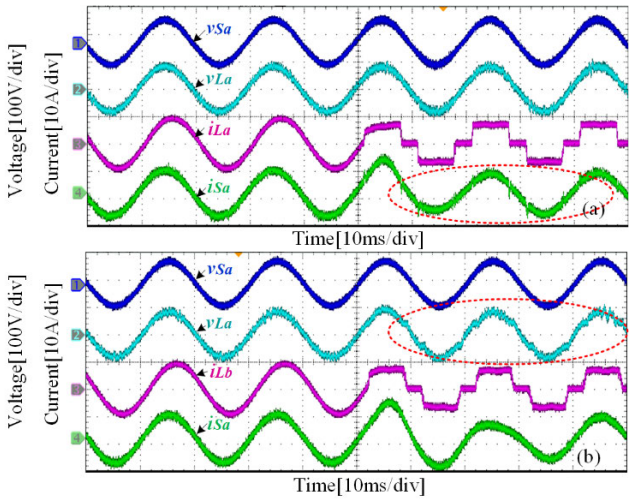

FIGURE 25. Experimental waveforms under different loads: (a) C-UPQC, (b) D-UPQC.

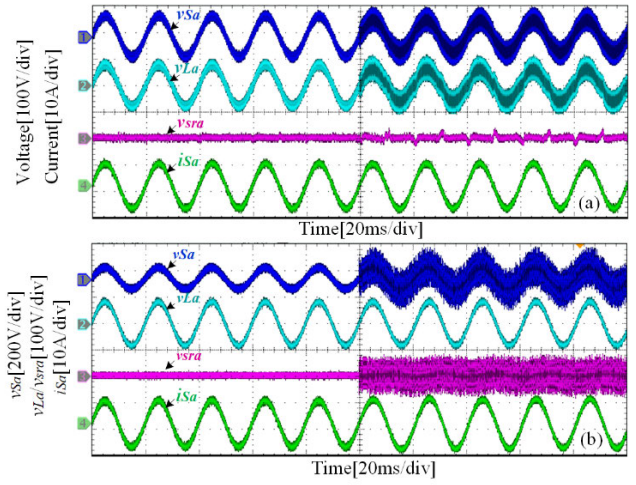

FIGURE 26. Experimental waveforms under different grid impedance: (a) C-UPQC, (b) D-UPQC.

1) INFLUENCE OF THE GRID VOLTAGES

This subsection mainly considers the grid voltage sag, swell and harmonics. The depths of the voltage sag and swell are 40%. And the load parameters are set as: $R = 8\Omega$ and $L = 12$mH.

Fig. 22 illustrates the waveforms of v_{Sa}, v_{La}, v_{Lb} and v_{sra} under the voltage sag and swell. When the PCC voltage sags or swells, the load voltage in the C- and D-UPQC remains sinusoidal and the amplitudes of v_{La} and v_{Lb} are kept constant (81.7V). However, when the PCC voltage suffers sudden sag or swell, the load voltage in the D-UPQC does not suffer the transient; in the C-UPQC, the load voltage suffers transient. Thus, the load voltage in the D-UPQC has a better dynamic performance.

Fig. 23-24 shows the waveforms of v_{Sa}, v_{La}, v_{sra} and i_{Sa} under the distorted grid voltage. As seen, when the grid voltage contains low-frequency harmonics, the load voltage in the C-UPQC is disturbed slightly; while when v_S contains high frequency harmonics, the load voltage in the C-UPQC is disturbed heavily. Besides, the load voltage in the D-UPQC can always be kept sinusoidal when the grid voltage is distorted. Thus, the load voltage quality in the D-UPQC is better under the grid voltage harmonics.

2) INFLUENCE OF THE LOAD CURRENTS

In this subsection, the nonlinear load is considered, where the rectifier load is connected ($R = 8\Omega$ and $L = 24$mH).

The waveforms of v_{Sa}, v_{La}, i_{La} and i_{Sa} for the UPQC under the nonlinear load are shown in Fig. 25. As seen, when the linear load is switched to the nonlinear load, in the C-UPQC, the load voltage is kept sinusoidal while the grid current is disturbed; in the D-UPQC, the grid current is more sinusoidal while the load voltage is disturbed. Therefore, it is concluded that load current harmonics mainly affect the grid

current in the C-UPQC and the load voltage in the D-UPQC. Besides, the grid current in the D-UPQC has a better dynamic performance under the transient of load switching.

3) INFLUENCE OF THE GRID IMPEDANCE

This subsection is designed to test the performance of the UPQC under different grid impedance ($L_g = 0.5$ and 5mH).

Fig. 26 shows the waveforms of v_{Sa}, v_{La}, v_{sra} and i_{Sa}. As seen, when L_g increases, the PCC voltages v_{Sa} in both the C- and D-UPQC are distorted more heavily, and the load voltage v_{La} in the C-UPQC are also distorted more seriously. However, the load voltage in the D-UPQC and the grid currents in both two schemes can remain sinusoidal. Thus, the grid impedance has an obvious influence on the load voltage in the C-UPQC.

VII. CONCLUSION

In this article, the *dq*-axis small signal models with consideration of the effects of PLL and grid impedance are established to analyze the performance of the C- and D-UPQC. The static and dynamic performance for the C- and D-UPQC are discussed and compared detailly, where the effect of control, circuit parameters and grid impedance are also taken into account. The main conclusions are drawn as follows:

1) The D-UPQC has a better dynamic performance when grid voltage or load suffers sudden variation;
2) Grid voltage harmonics mainly distort the load voltage in the C-UPQC;
3) Load current harmonics have a significantly influence on the grid current in the C-UPQC and load voltage in the D-UPQC;
4) Grid impedance has an obvious influence on the load voltage in the C-UPQC.

The correctness and effectiveness of the above findings are verified via the simulation and experimental results, which will provide the guideline for the selection of suitable compensation strategies in specific applications.

APPENDIX A

DESIGN OF DUAL PI CONTROL GAIN

From [23], in the dual closed-loop PI control, the bandwidth of the inner current loop α_c should be no more than $0.1^*2\pi^*f_{sw}$ (f_{sw} is the switching frequency), which means,

$$k_{pc} = \alpha_c \cdot L_V \tag{A1}$$

$$\alpha_c \le 0.2\pi f_{sw} L_V \tag{A2}$$

And the bandwidth of the outer voltage loop α_d should be less than 1/10 of α_c, which means,

$$k_{pd} = \alpha_d \cdot C_V \tag{A3}$$

$$\alpha_d \le 0.1\alpha_c \tag{A4}$$

Besides, the specific design the dual PI control gains could be achieved according to the transfer function of closed loop system.

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