IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 26 December 2023, accepted 10 January 2024, date of publication 15 January 2024, date of current version 24 April 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3354378

RESEARCH ARTICLE

Mathematical Model-Based Analysis and Mitigation of GaN Switching Oscillations

MUHAMMAD FAIZAN[1,2], KAI HAN[3], XIAOLEI WANG[1,2], AND MUHAMMAD ZAIN YOUSAF[4]

[1]Institute of Microelectronics, Chinese Academy of Sciences, Beijing 100029, China
[2]School of Microelectronics, University of Chinese Academy of Sciences, Beijing 100049, China
[3]School of Physics and Electronic Information, Weifang University, Weifang 261061, China
[4]School of Electrical and Information Engineering, Hubei University of Automotive Technology, Shiyan 442002, China

Corresponding author: Kai Han (hankai@wfu.edu.cn)

This work was supported by Shandong Provincial Natural Science Foundation under Grant ZR2022MF313.
The work of Kai Han was supported by APA.

ABSTRACT GaN high-electron-mobility transistor (HEMT) has superior features of wide band gap, high electron mobility and very high electric field strength due to its material advantages. By using the GaN HEMT, switching frequency can be enhanced up to megahertz with extremely high efficiency. Unfortunately, GaN HEMTs accomplished by undesirable switching oscillations and voltage spikes due to extremely fast switching frequencies with very high dv/dt, di/dt and parasitic parameters. In this paper, RLC equivalent circuit models are developed for turn on and turn off conditions, including all parasitic components. In addition, the relative effect of each parasitic parameter is analyzed and estimated. Moreover, simple mathematical model is developed for theoretical analysis of switching oscillation phenomenon and, for guidance of snubber or damping circuit design. To validate these simple equivalent circuit models, both circuit simulation and experimental measurements are employed.

INDEX TERMS GaN HEMT, RLC equivalent circuit model, parasitic components, snubber circuit, switching oscillations, switching loss reduction.

I. INTRODUCTION

In order to obtain greater performance power conversion, wide band gap semiconductor devices such as silicon carbide (SiC) and gallium nitride (GaN) have emerged as a possible substitute for silicon, providing very high junction working temperature, reduced specific on-resistance and fast switching-speed capabilities [1]. Among these advantages, the very fast switching performance acting a major part in lowering switching losses, cutting down on phase leg dead time and enhancing switching frequency. These are all advantageous for high-power quality, very high density, and ultra-high efficiency [2]. GaN transistors, operating as high electron mobility transistors (HEMTs), demonstrate superior characteristics compared to silicon devices. They boast a critical electric field strength of 3.3 MV/cm, a higher band gap of 3.39 eV, and greater electron mobility at 1500 cm^2/(V.s). In contrast, silicon devices exhibit values of 1.12 eV, 0.23 MV/cm, and 1400 cm^2/V.s for critical electric field strength, band gap, and electron mobility, respectively [3]. The distinctive material properties of the GaN transistor render it exceptionally well-suited for operating at higher frequencies. With $dv/dt > 100$v/ns, GaN switches faster than Si/SiC MOSFETs. Compared to the most advanced SiC MOSFET, GaN has 4× faster turn-on and ∼ 2× faster turn-off time with same $R_{DS(on)}$ value [1], [4]. With these unique attributes, GaN is able to satisfy the requirements of high temperature, very high frequency and ultra-high power for variety of industrial applications, including deep well drilling, automotive and aerospace [5], [6]. In addition, GaN-based devices can function in very low temperatures conditions, these devices are important for super conduction and quantum computing applications. GaN can effectively overcome carrier freeze-out issues due

The associate editor coordinating the review of this manuscript and approving it for publication was Wu-Shiung Feng.

to its polarization-induced doping, in contrast to other technologies, including doped silicon, which are significantly impacted by this problem [7]. GaN has already been widely adopted in fast chargers, data centers, wireless charging and electric transportation due to its physical superiority over Si and SiC for power applications [8]. Improvements in these applications might include enhancing the switching frequency to several megahertz, significantly reducing the volume or further enhancement in efficiency. Higher conversion efficiency and power density along with reduction in system weight and volume are made possible with higher switching frequency which minimize the size of passive components in power system. GaN technology is still in its infancy and far from reaching its theoretical potential, and its rate of advancement has been and will continue to be rapid [9].

However, due to high dv/dt, di/dt and circuit parasitic elements in high frequency power converters, GaN HEMT produce severe oscillations and voltage spikes during turn-off and turn-on. Not only these oscillation and spikes damage the HEMT and increasing switching losses but also they result in significant electromagnetic interference [10]. In order to avoid gate spikes go beyond from the maximum rating or threshold under Miller effect due to blending of high di/dt and dv/dt with low C_{ISS} and $V_{G(th)}$, it is necessary to reduce these oscillations and voltage spikes for safe operation [11].

Very fast switching frequency of power switches, high di/dt, dv/dt and circuit parasitic parameters are major causes of switching oscillation phenomena. An empirical analysis, how the parasitic factors affect the oscillation phenomena was reported in [12] and [13]. By varying the values of these parameters, their effect on the switching waveforms was also noticed. In [14], SiC JFET-based inverters using several kinds of diodes were observed, and provided a method to stop oscillation by slowing down JFET switching rate. In [15], it was concluded that SiC MOSFET's gate path limits its switching speed, and explained related design requirements. How to calculate the analytical formula for SiC Schottky barrier diodes, which includes the loop inductance, diode resistance and diode capacitance, is presented in [16]. In [17], a parametric research is conducted identical to empirical analysis in [12], to examine the impact of the parasitic components. All of these empirical investigations usually concur that the oscillations are caused by high di/dt and dv/dt during a SiC MOSFET's switching transient when coupling with parasitic components in circuit. This coupling effect is more significant in GaN HEMTs due to higher switching speed than SiC MOSFETs with $\mathrm{dv}/\mathrm{dt}>$ 100v/ns and $4\times$ faster turn-on and $\sim 2\times$ faster turn-off time than state of the art SiC MOSFET with equivalent $R_{DS(on)}$ [18]. Therefore, a simple analytical model for GaN HEMTs becomes more essential due to its higher potential for generation of excessive oscillations and voltage spikes that can quantitatively describe oscillation phenomena and offer theoretical guidance for suppressing the current or voltage oscillations [19], [20].

Various modeling approaches for GaN-HEMTs are available in the literature, and are classified into five categories: behavioral models, semiphysics-based models, physics-based models, numerical and mathematical models [21]. The physics-based models involve solving semiconductor physics equations in order to obtain the electrical behavior of GaN-HEMTs [22]. However, these models are not suitable for power electronics simulation because of the complex parameter extraction and long computational time. Semiphysics-based models are partly based on behavioral equations and partly on semiconductor physics [23]. The models are accurate and fast but some of their empirical parameters lack physical meaning. Numerical modeling requires detailed information regarding internal structure, device geometry, and material properties. The accuracy of numerical models is very good but complexity is very high and computation is very intensive [24]. The major advantage of behavioral models is their computational efficiency. However, when the operating conditions are changing, the accuracy of behavioral models is quite low [25]. A popular modeling approach is mathematical that is valuable for optimize device performance and explore novel designs. Mathematical models can be generalized across different devices, materials, and operating conditions. This versatility allows for broader applicability compared to some empirical models that might be more specific to certain technology nodes or manufacturing processes. In [26] and [27], existing physics based models of GaN HEMT have intricate mathematical formulations and hence computational efficiency is compromised. The Advanced Spice Model for High Electron Mobility Transistor (ASM-HEMT) is a surface potential based physical compact model for GaN HEMTs [28]. It is completely analytical and hence computationally efficient. The surface potential core is derived considering the first two energy subbands [29].

For these emerging SiC or GaN-based devices, there are a few studies has been conducted, and the majority of them are modification of Si device model with particular changes. In contrast, the behavior-level simulation modeling for Si MOSFET is mature [30]. Traditionally, phase node of dc-dc buck converters employing silicon MOSFETs has been investigated for the study of oscillation phenomena [31]. It is observed that the ringing's intensity depends on the switching speed of MOSFET, as well as stray inductances of PCB layout and MOSFET packaging [32]. The addition of L_s in the circuit reduces the spurious gate voltage and the contributions of $C_{gd}(dv/dt)$ and $L_S(di/dt)$ determine spurious triggering pulse caused by non-operating switch gate impedance according to [33]. Therefore, it can be summarized that the maximum DC voltage across the source and drain terminals, as well as the corresponding characteristics of the switching device, power loop parasitic inductances and gate loop parasitic components all of these influence the peak magnitude of voltage spikes [34]. It is also concluded that oscillations can be reduced by improving PCB layout and optimizing

gate resistance of MOSFET. In [35], a technique for reducing phase node ringing by optimizing the low-side silicon MOSFETs gate resistance is presented, and analytical formulas based on parasitic components are derived. This idea of designing simple equivalent circuits for turn-on oscillation is also satisfying and applicable to HEMTs if it is unsure whether optimizing gate resistance can effectively suppress ringing. In [36] and [37], it is stated that power MOSFETs have their own gate charge controlled to reduce overshoot and turn-off oscillations, and active gate drives to limit high di/dt and dv/dt in power switches is also presented. However, both strategies enhance the complexity of the circuit in terms of control and sensing. Alternatively in [38], RC snubber circuit is employed in buck converters to reduce ringing during the switching transient. In [39], the modeling based analysis of SiC MOSFET is performed without precise consideration of parasitic elements for turn-on and turn-off condition. However, all these researches didn't offer any analytical approach for constructing damping circuit except empirical methods based on trial and error. However, still there is lack of simple analytical models, which can quantitatively explain the oscillation phenomenon and provide the theoretical guidelines for suppressing the voltage or current oscillations.

In this paper, we have proposed two simple RLC equivalent circuit models for GaN HEMT's turn-on and turn-off switching mechanism. The research presented in our paper focuses on the 650V, 30A GaN HEMT in the TO-220 package, developed by Infineon. This device exhibits a turn-on time of less than 5 ns, which is typically 10 times faster than comparable Si MOSFETs. Furthermore, its turn-off times are 10 to 20 times less than those of comparable Si MOSFETs. These models are used to undertake an insightful analysis of the switching oscillations that provides a novel and comprehensive explanation for inherent damping of GaN HEMT by its slew times. Moreover, the analysis of RLC equivalent circuit models offers a mathematical solution that provides guidance how to reduce oscillations. Moreover, based on frequency domain analysis and developed mathematical model, a guideline for selecting the components of snubber circuits is also provided. The turn-off and turn-on equivalent circuit models are finally verified by both Cadence Spectre simulator transient simulation and experiment. In both cases, a reasonable agreement is observed. Furthermore, experimental results show that we designed a suitable and efficient RC snubber circuit based on theoretical analysis to reduce the switching oscillations without effecting GaN HEMT switching speed.

In section II, we have presented basic inductive switching circuit with all capacitive and inductive parasitic parameters of GaN HEMT. In section III, we have presented equivalent circuit model of GaN with the derivation of simple mathematical formulas and parasitic elements values for turn-off and turn-on condition. Section IV presents the analysis and discussion with derivation of condition for turn-on and turn-off oscillation damping, and design of proper RC snubber circuit for turn-off and turn-on. Section V presents the experimental verification of theoretical analysis and proposed snubber circuit. Section VI provides the conclusion of this paper.

II. BASIC INDUCTIVE SWITCHING CIRCUIT OF GAN HEMT

Fig. 1 presents the fundamental switching power-pole that has three branches: a free-wheeling GaN Schottky diode, an inductor and a GaN HEMT active switch.

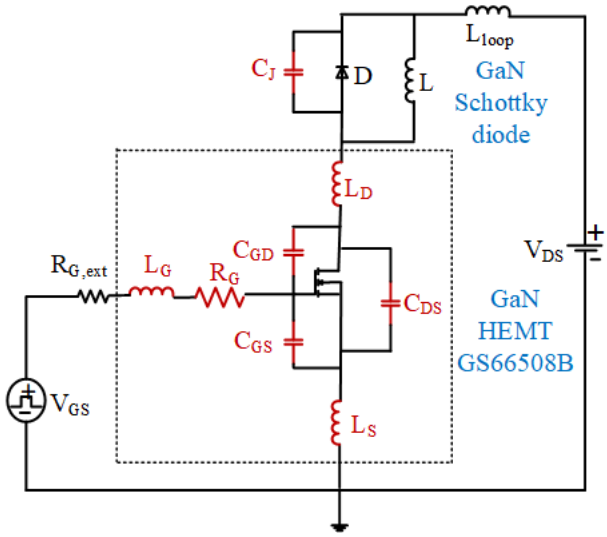

FIGURE 1. Inductive load switching circuit with all parasitic components.

Usually, the inductor 'L' is selected large enough to allow current to be considered constant during switching cycle. This steady current is followed through either by diode or by GaN HEMT, or by both. When GaN HEMT is in on-state, V_{DS} is almost 0 and the inductor current flows via GaN HEMT. GaN HEMT is fully on at this stage and diode is reverse-biased. The switch no longer carries current when GaN HEMT is turned off but the diode remains forward biased. When the switch is off, the current will flow through the inductor-diode loop and voltage V_{DS} is equivalent to dc power supply V_{DC}. The current switches between HEMT and freewheeling diode during the switching transitions. However, we must take into account the non-ideal parasitic components that really present in switching circuit as depicted in Fig. 1. The non-ideal parasitic components are indicated in blue, freewheeling diode junction capacitance C_j, drain–source capacitance C_{DS}, gate–source capacitance C_{GS}, gate–drain capacitance C_{GD}, gate inductance L_G, switching loop inductance L_{loop}, common source inductance L_S (inductance shared by gate driver loop and drain-to-source power current route), drain inductance L_D, which occurs between loading inductor and drain, having a great role in switching oscillations, and interior gate resistance R_G. The switching loop inductance (L_{loop}) represents circuit loop total parasitic inductance. Diode junction capacitance discharging and charging processes will reform the HEMT drain current. HEMT capacitances C_{GS}, C_{DS} and C_{GD} are non-linear in nature, voltage-dependent and device datasheet is used to

obtain their values. The parasitic inductances in the circuit which are mostly only a few nanohenries, are significantly smaller than the load inductor L, which is normally between tens of microhenries and several millihenries. Consequently, in this study, 'L' can be modeled without considering its parasitic resistance as a continuous current source. The HEMT internal parasitic inductances L_S, L_G, and L_D are obtained from the device package. Usually, two techniques are used for the extraction of these parasitic inductances. One method is to model and calculate packaging parasitic from device shape using finite-element analysis (FEA) simulation, such as ANSOFT Q3D Extractor [33]. In 2nd method, vector network analyzer is used in a measurement-based method for studying frequency-domain impedance [40].

There are two most general types for the packaging of GaN HEMT: TO-type and SMD-type. TO-type packages typically offer better thermal performance compared to SMD-type packages. The metal can provide better heat dissipation, which is crucial for high-power applications like switching oscillators. TO-type structures also have capacity to handle higher power due to their larger size and better thermal management. This can be beneficial in applications where high power levels are required. Furthermore, TO-type packages, being enclosed in a metal can, provide better shielding against electromagnetic interference. This can be advantageous in applications where minimizing EMI is critical, such as in sensitive electronic systems. In addition, these packages are generally more mechanically stable and robust compared to SMD-type packages. This can be important in environments with vibrations or mechanical stress. On the other hand, SMD-type packages are typically smaller and lighter than TO-type packages. If space and weight are critical factors then SMD-type structures might be preferred. SMD-type packages are often more cost-effective for mass production due to their smaller size and simplified manufacturing processes. If cost is a significant factor and the application requirements allow for it, SMD-type structures might be a more economical choice. Furthermore, SMD-type devices are designed for surface mounting directly onto the PCB (Printed Circuit Board), simplifying the assembly process [41]. TO-type packages may require additional mounting considerations. It is clear from this brief comparison, the choice between TO-type and SMD-type structures for GaN HEMT for switching oscillation mitigation depends on the specific requirements of the application, including power levels, thermal considerations, EMI sensitivity, size constraints, and cost considerations. In this paper, we have no concerned with the size, weight, cost and, mounting and assembly. Therefore, we select TO-type structure for switching oscillations mitigation.

There are two basic types of GaN models structures: Vertical GaN-on-GaN Model (like Infineon's GaN Products) and Lateral Structure (as in GaN Systems' GS66508B). Understanding the structural distinctions between these two types of GaN devices is essential for accurate analysis, especially in applications where efficiency, size, and power handling

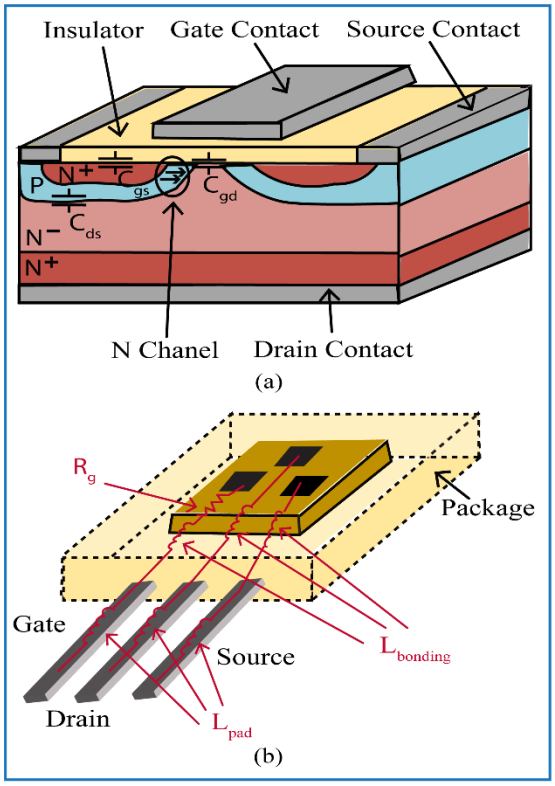

FIGURE 2. GaN HEMT simplified physical view with package (a) Parasitic Capacitances (b) Parasitic inductances and internal gate resistance.

capabilities are critical factors. Each type has its unique advantages, making them suitable for different applications in the semiconductor and electronics industries. In vertical GaN devices, the current flows vertically through the device. This design allows for higher voltage operation and better thermal performance. Vertical GaN-on-GaN models are often used in high-power applications due to their ability to handle higher currents and voltages efficiently. The structure typically has a GaN layer grown on top of another GaN substrate, which can enhance device performance. Lateral structural GaN devices, on the other hand, have a current flow that is parallel to the substrate. These devices are typically easier to manufacture and are more common in lower power applications. The GS66508B is a good example of a lateral GaN device, showcasing the efficiency and compactness typical of this design. Lateral structures are often used in applications like power supplies, adapters, and other scenarios where space and efficiency are critical.

GaN HEMTs' drain-source capacitance C_{DS}, which exists between drain and source behaves as a resonance circuit with load inductor L, is a substantial contributor to overshoot current and ringing when switch is being turn-on. Besides this, common source inductance and drain inductance also have a significant impact on the switching behavior by overshooting current during turn-on transition and slowing down the transition during turn-off. Additionally, due to same ground, common source inductance couples with gate driver circuit. With the increase in common source inductance (L_S), the

effective gate driver current and voltage are dramatically decreased and become major cause of decrease in switching rate and enhancement in switching losses. Therefore, its impact must be minimized. It can be minimized by positioning gate driver as near to GaN HEMT as feasible, and selecting suitable gate resistor value. The GaN HEMT waveform's parasitic di/dt voltage bump represents the effect of inductance on switching transition. For turn on, gate drive current can be calculated by:

$$I_G = \frac{V_{drive} - V_{GS} - V_{L_S}}{R_G} = \frac{V_{drive} - V_{GS} - L_S \frac{di_{DS}}{dt}}{R_G} \quad (1)$$

where V_{drive} is gate drive voltage, V_{Ls} is the effective voltage across L_S during device current commutation, which is equivalent to $L_S(di_{DS}/dt)$, V_{GS} is gate to source voltage of HEMT and R_G is effective gate resistance.

The high frequency loop inductance (L_{loop}), which is device commutation loop inductance, has two primary detrimental impacts on switch during turn-off: slowing of transition process and increase in voltage across source and drain. When a device is turned on, the loop inductance lowers the V_{DS} of the device that cuts down turn-on losses. The loop inductance will increase circuit losses because the overall result of two adverse impacts and one favorable effect is adverse. The drain-to-source voltage spike, which is caused by high frequency loop inductance, is another significant disadvantage, given by:

$$V_{L_{LOOP}} = L_{LOOP}\left(\frac{di_{DS}}{dt}\right) \quad (2)$$

As a conclusion, these parasitic components are major cause of undesirable resonance in switching circuit that is reflected as switching oscillations. This ringing and oscillations problem due to these parasitic components becomes much more obvious in GaN devices due to its rapid switching capability. The effect of parasitic inductances on switching ringing at different frequencies is shown in Fig. 3.

It is also worth noting that simulating accuracy of C_j and dynamic $R_{ds}(on)$ is also crucial for accurately predicting the device's behavior under dynamic conditions for predicting HEMT model. $R_{ds}(on)$ refers to the on-state resistance of a transistor, and its dynamic nature is often associated with changes in operating conditions such as frequency, temperature, and bias. In the context of HEMT models, dynamic $R_{ds}(on)$ has impacts on switching performance (turn on and off time), rise and fall time, power dissipation (especially during switching events), transconductance and output conductance. It is worth noting that the specific impact will depend on the application and the details of the HEMT model being used. In the context of oscillation mitigation analysis, dynamic Rds(on) variations affect the impedance matching and phase relationships in the circuit, potentially influencing the suppression of oscillations. It is important to consider the impact of dynamic Rds(on) for the stability of the circuit. On the other hand, junction capacitance C_j is also vital for accurately predicting the device's behavior

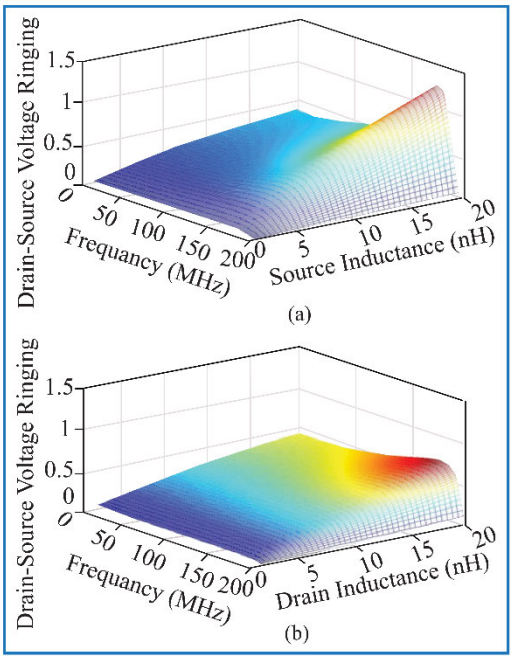

FIGURE 3. Effect of parasitic inductances on switching oscillations at different frequencies (a) Effect of common source inductance (L_S) on drain-source voltage ringing (b) effect of drain inductance (L_D) on drain-source voltage ringing.

under dynamic conditions. In the context of HEMT models, C_j has impacts on dynamic behavior of HEMTs, especially in transient conditions, and this becomes important in applications where the device experiences rapid changes in bias or signal conditions. Furthermore, Cj variations can influence the stability, resonant frequency oscillation frequency, input and output impedance of the HEMT and HEMT based circuit. The junction capacitance is also one of the factors that needs to be carefully considered.

For the inductive load switching circuit, we treated GaN HEMT as an ideal switch and all the rest parasitics are taken as external elements. The proposed RLC equivalent circuits are developed for fully turn-on and turn-off conditions. Although, Rds(on) and Cj have great impact on HEMT transition behavior and oscillation mitigation analysis but in spite of that they can be approximated to be constant when the device is fully turn–on and turn-off. In our forthcoming research, we aim to introduce an advanced GaN-HEMT model that incorporates dynamic $R_{DS(on)}$ and Cj parameters.

III. EQUIVALENT CIRCUIT MODELS OF GAN HEMT

In this section, a circuit modelling analysis is carried out to acquire understanding of the switching oscillations. The analysis is divided into turn-on and turn-off switching procedures, and based on inductive load switching circuit. It is important to notice that the proposed equivalent circuit model is based on assumption that the switch is fully on and off. Meanwhile, HEMT parasitic capacitors are nonlinear and voltage dependent. In light of this, the capacitance values employed in the computation for the turn-on procedure are

obtained when V_{DS} is almost zero while the capacitance values for turn-off procedure are recorded when V_{DS} reaches the value of dc supply voltage.

A. TRUN-ON EQUIVALENT CIRCUIT

All the parasitic components are viewed as external components and the HEMT is considered as an ideal switch. The ideal switch is switched-on during the turn-on procedure. When the switch is completely on, C_{DS} is bypassed, C_{GD} and C_{GS} are in parallel, and then these two are joined in series with R_{G1}–L_G–R_G. When freewheeling diode is reverse-biased and has voltage equal to blocking voltage then C_J is charged. Furthermore, when the switch is fully-on, turn-on-resistance $R_{DS(ON)}$ is noticeable, and cannot be ignored.

$$L'_{loop} = L_{loop} + L_D \tag{3}$$

$$C_{iss} = C_{GS} + C_{GD} \tag{4}$$

$$R'_G = R_G + R_{G,ext} \tag{5}$$

In Fig. 4(a), initial turn-on circuit is presented. In Fig. (4b), turn-on circuit is presented in more simplified form.

V(t) is step function and acts as an ideal voltage source. Due to presence of capacitors and inductors, the turn-on circuit's step response will produce oscillations and ringing which are represented as turn-on switching oscillations. The equivalent circuit is being developed with the intention of simulating V_{DS} oscillation during turn-off and turn-on. By considering the switch to be a resistor, we approximated the value of equivalent resistor voltage is V_{DS} for turn-on. In the equivalent circuit model of a GaN HEMT, under certain conditions, the capacitance and inductance elements can be approximated as resistors. This typically occurs at high frequencies where the reactive components become less significant compared to the resistive components. In high-frequency applications, the parasitic capacitances (such as gate-source capacitance, gate-drain capacitance) and parasitic inductances (such as lead inductances) can be treated as resistive elements due to their relatively higher impedance at those frequencies. This simplification helps in analyzing and designing high-frequency circuits. Therefore, in fig. 4(b), the part below Node 1 is approximated as a damping resistor. It is expected that the gate branch only provides a resistive contribution when the switch is fully on.

Thus, below the Node 1, gate branch impedance is:

$$X_G = R'_G + j\omega_{ON}.L_G + \frac{1}{j\omega_{ON}.C_{iss}} \tag{6}$$

where ω_{ON} is resonance frequency for turn-on state. When analyzing the resonance frequency of GaN HEMT for turn-on process, the gate-to-drain (Cgd) and gate-to-source (Cgs) capacitances are often ignored for simplification in certain contexts. The reasons for this simplification are related to the specific characteristics of HEMTs and the operating conditions in which they are typically used. Furthermore, the gate inductance in HEMTs is also usually quite small compared to other parasitic elements. As a result, its impact on the overall

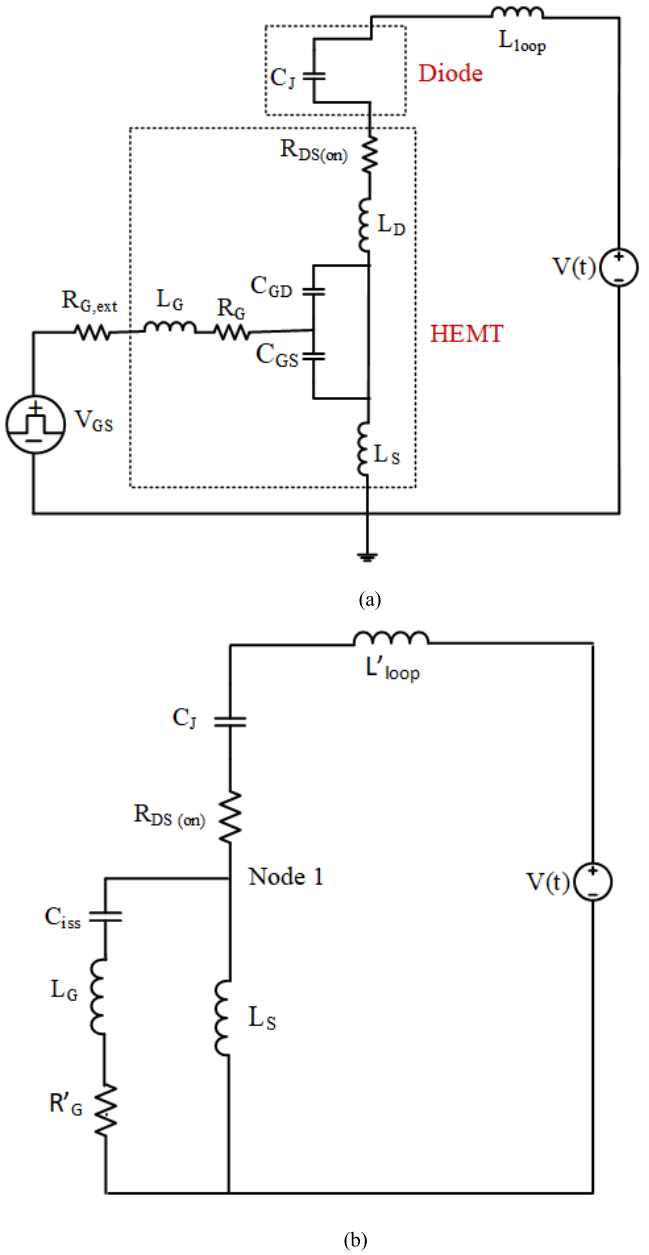

FIGURE 4. Inductive load switching turn-on circuit (a) initial turn-on circuit (b) simplified turn-on circuit.

resonance frequency is minimal, and it can be neglected in many cases for the sake of simplicity and practicality. Therefore, to facilitate circuit analysis and design, we use simplified models that capture the essential characteristics of the device without including all the parasitic elements. The simplified model helps in obtaining a more manageable and analytically tractable model for circuit simulations and design calculations. So, the resonance frequency for turn on can be estimated as:

$$\omega_{ON} \approx \frac{1}{\sqrt{\left(L'_{loop} + L_S\right) C_J}} \tag{7}$$

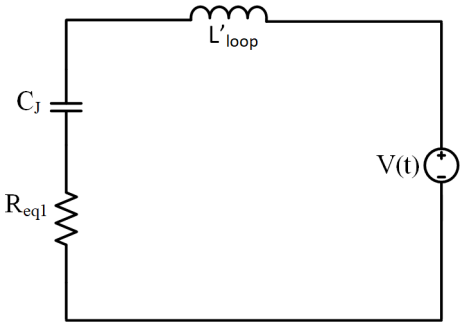

FIGURE 5. RLC equivalent circuit model for turn-on.

Consequently, the overall impedance below Node 1 is

$$X_{T1} = \frac{X_G \cdot j\omega_{ON}.L_S}{X_G + j\omega_{ON}.L_S} \tag{8}$$

The part below Node 1 is estimated as a resistor. Accordingly, the equivalent damping resistance for the turn-on process depends on the current ratio that flows through R'_G and the total current flows into the node, which can be expressed by

$$\begin{aligned} R_{eq(ON)} &= \left(R'_G \frac{|X_{T1}|}{|X_G|}\right) \cdot \frac{|X_{T1}|}{|X_G|} = R'_G \frac{|X_{T1}|^2}{|X_G|^2} \\ &= R'_G \frac{\left|\frac{X_G \cdot j\omega_{ON}.L_S}{X_G + j\omega_{ON}.L_S}\right|^2}{|X_G|^2} = R'_G \frac{|X_G \cdot j\omega_{ON}.L_S|^2}{|X_G|^2 \, |X_G + j\omega_{ON}.L_S|^2} \\ &= R'_G \left(\left|\frac{j\omega_{ON}.L_S}{X_G + j\omega.L_S}\right|\right)^2 \end{aligned}$$

By substituting the value of X_G;

$$R_{eq(ON)} = R'_G \frac{(j\omega_{ON} L_S)^2}{(R'_G)^2 + (\omega_{ON}.L_G + \omega_{ON}.L_S - \frac{1}{\omega_{ON}.C_{iss}})^2} \tag{9}$$

Then, equivalent resistance for turn-on state can be estimated as:

$$R_{eq1} = R_{eq(ON)} + R_{DS(ON)} \tag{10}$$

Finally, a simple series RLC second-order circuit is developed that simulates an inductive load switching turn-on equivalent circuit model, presented in Fig. 5. The step function v(t) varies from 0 V to V_{DC}. During the switching operation, energy will be transferred between inductor and capacitor. The energy exchange process will be accompanied by voltage or current ringing in the second-order circuit. Eventually, all of the energy will be dissipated in corresponding resistor after certain period of time and ending the oscillations. This is the whole procedure for turn-on switching oscillations.

The values of these three components (resistor, inductor and capacitor) for this second-order equivalent circuit model may be either taken from the datasheet or computed using the given equations. Using Cadence Spectre Simulator transient simulation, the developed turn-on equivalent circuit is compared with original inductive load switching circuit. Infineon GaN power HEMT GS66508B in TO-220 package and Infineon GaN Schottky diode IDW30C65D1XKSA1 are employed for simulation in order to be incompatible with experimental verification in section V, and 400 V is used as DC bus voltage.

As earlier mentioned that switching loop inductance (L_{loop}) plays a vital part in turn-on oscillation. The common value of L_{loop} for single-switch double pulse test is in range of tens to few hundreds of nanohenries (300 nH utilised in [42]). In this paper, L_{loop} is set to be 256.4 nH, and this specific value is derived from experimental measurement of turn-off oscillation frequency as discussed in section V. When the source-drain voltage is ∼0 V, the values for C_{iss}, C_{oss}, and C_{rss} are taken from the HEMT datasheet. Then, parasitic capacitances are estimated as C_{GD} = 70 pF, C_{GS} = 228 pF, and C_{DS} = 527 pF. The junction capacitance of a free-wheeling diode is C_J = 40 pF at a reverse-biased voltage of 400 V. The parasitic inductances for this GaN HEMT's TO-220 packaging are gotten from an GaN System-provided SPICE model, L_G = 2.87 nH, L_D = 1.89 nH and L_S = 0.57 nH. All these parameters are listed in Table 1.

TABLE 1. Parameters for turn-on equivalent circuit model.

Parameters	Conversion Values
C_{GS} ($V_{DS} \approx 0V$)	228 pF
C_{DS} ($V_{DS} \approx 0V$)	527 pF
C_{GD} ($V_{DS} \approx 0V$)	70 pF
C_J ($V_R \approx 400V$)	40 pF
V_{DC}	400 V
L_{loop}	256.4 nH
L_D	1.89 nH
L_G	2.87 nH
L_s	0.57 nH
R_G	1.13 Ω
$R_{G,ext}$	2 Ω
C_{ISS}	260 pF

With all the derived equations and parameters, R_{eq1} comes to be 0.2867 Ω. The RLC turn-on equivalent circuit model and the inductive load switching are compared in terms of source-drain voltage turn-on oscillations with the help of Cadence Spectre Simulator transient simulation. Table 2 shows numerical comparison and corresponding waveforms are displayed in Fig. 6. It is significant to note that comparison of differences are made with their corresponding absolute values.

In Fig. 6, the HEMT source- drain voltage turn-on oscillations for RLC equivalent circuit model and inductive load switching is compared with the help of Cadence Spectre Simulator transient simulation. The two circuits' switching transients start at same time but oscillations in equivalent circuit start sooner than inductive load switching circuit because inductive load circuit takes some time to turn on while the

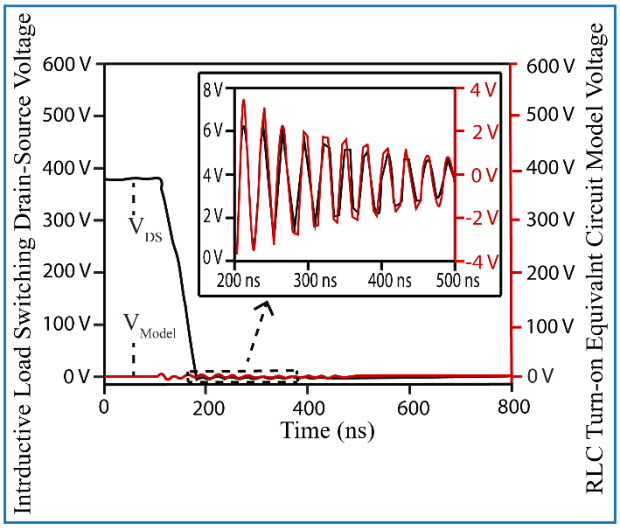

FIGURE 6. Turn-on oscillations and ringing comparison for drain source voltage (V_{DS}) between the inductive load switching Cadence Spectre Simulator transient simulation and estimation of turn-on RLC equivalent circuit model. Red and black lines curve for RLC turn-on equivalent circuit model voltage and drain source voltage (V_{DS}) of inductive load switching, respectively.

TABLE 2. Numerical comparison between RLC turn-on equivalent circuit model and inductive load switching.

Turn-on Comparison	V_{DC}	V_{Model}	Difference
Frequency	45.16 MHz	44.11 MHz	1.04 MHz
1st pulse peak to peak	6.05 V	7.48 V	1.43 V
2nd pulse peak to peak	5.24 V	6.52 V	1.28 V
3rd pulse peak to peak	5.21 V	5.80 V	0.59 V
4th pulse peak to peak	4.42 V	4.88 V	0.46 V
5th pulse peak to peak	3.82 V	4.06 V	0.24 V

oscillations begin immediately as the step voltage powers the equivalent model. The switching oscillations become more severe and their curves coincided with the turn-on equivalent model oscillations curves as we shorten the device's turn-on switching period. It can also be noticed from Fig. 6, while the amplitudes are within a 23% error range, the switching oscillations frequencies from transient simulation of Cadence Spectre Simulator for inductive load switching and oscillation of RLC turn-on equivalent circuit coincide each other with error of 3.12%. This strong agreement between these two approaches demonstrates that RLC turn-on equivalent circuit is simple but reasonably efficient and accurate oscillations modelling tool.

B. TRUN-OFF EQUIVALENT CIRCUIT

The turn-off equivalent circuit model is also developed, same as turn-on switching. The switch is switched off during the turn-off procedure. In this case, C_{DS} is charged after switch is fully turn-off. The junction capacitance C_J of free-wheeling diode is bypassed and diode is forward biassed. For simplicity, as in turn-on case

$$L'_{loop} = L_{loop} + L_D \tag{11}$$

$$R'_G = R_G + R_{G,ext} \tag{12}$$

In Fig. 7(a), initial turn-off circuit is presented. The following formulas may be used to convert the delta connection to a star connection, as illustrated in Fig. 7(b), in order to create a circuit design that is comparable to the turn-on circuit

$$X_{C_G} = \frac{X_{C_{GS}}.X_{C_{GD}}}{X_{C_{GS}} + X_{C_{GD}} + X_{C_{DS}}} \tag{13}$$

$$X_{C_D} = \frac{X_{C_{DS}}.X_{C_{GD}}}{X_{C_{GS}} + X_{C_{GD}} + X_{C_{DS}}} \tag{14}$$

$$X_{C_S} = \frac{X_{C_{DS}}.X_{C_{GS}}}{X_{C_{GS}} + X_{C_{GD}} + X_{C_{DS}}} \tag{15}$$

where X_{C_i}=$(1/\omega_{OFF} C_i)$, i = DS, GD, G, GS, S, D. And ω_{OFF} is resonance frequency for turn-off. In the context of GaN HEMTs, the gate capacitance (C_G) is often ignored when discussing the resonance frequency. Because the gate capacitance in GaN HEMTs is typically much smaller compared to the capacitances associated with other parts of the device, such as the parasitic capacitance between the source and drain. The primary capacitances that affect the resonance frequency are the parasitic capacitances associated with the source, drain, and other interconnections. These parasitic capacitances are usually much larger than the gate capacitance. The contribution of gate capacitance to the resonance frequency is often considered negligible in comparison to other capacitances. Therefore, for simplification and practical reasons, the gate capacitance can be ignored when analyzing the resonance frequency of HEMTs in certain contexts. Furthermore, the gate inductance (L_G) in HEMTs is also usually quite small compared to other parasitic elements. As a result, its impact on the overall resonance frequency is minimal, and it can be neglected in many cases for the sake of simplicity and practicality. So, the resonance frequency for turn on can be estimated as:

$$\omega_{OFF} \approx \frac{1}{\sqrt{\left(L'_{loop} + L_S\right)(C_{GD} + C_{DS})}} \tag{16}$$

Now simplified turn-off circuits are attained which are identical to turn on circuit, therefore, the similar simplification rules can be utilized. Below Node 2, the gate branch impedance is

$$X_G = R'_G + j\omega_{OFF} L_G + \frac{1}{j\omega_{OFF} C_G} \tag{17}$$

The source branch impedance is

$$X_S = j\omega_{OFF}.L_S + \frac{1}{j\omega_{OFF}.C_S} \tag{18}$$

As a result, total impedance below Node 2 is

$$X_{T2} = \frac{X_G.X_S}{X_G + X_S} \tag{19}$$

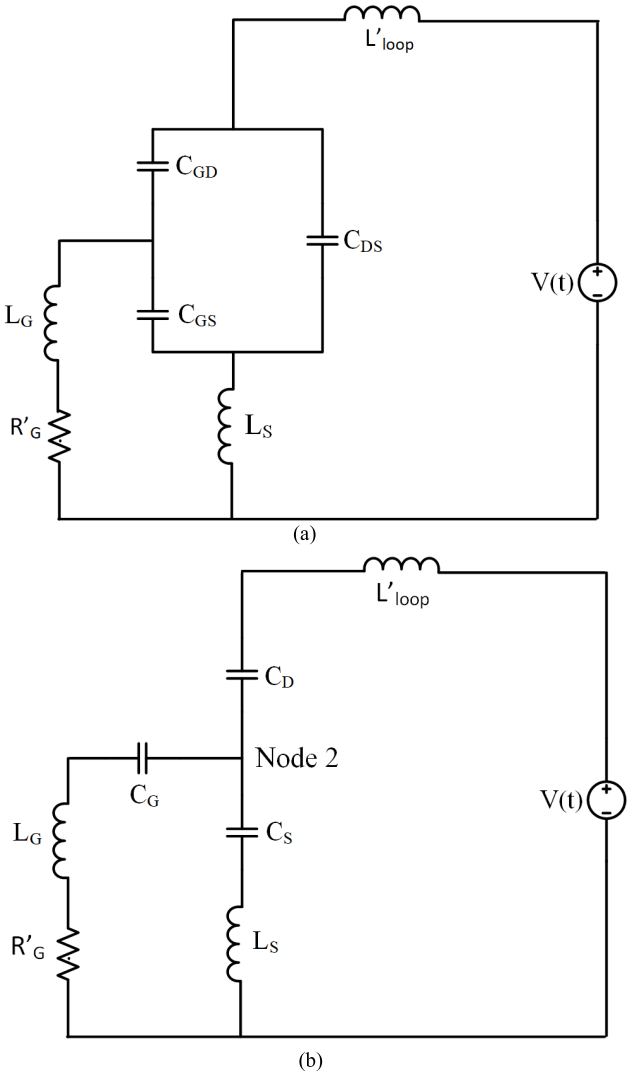

FIGURE 7. Inductive load switching turn-off circuit (a) initial turn-off circuit (b) simplified turn-off circuits.

The ratio of current flowing via R_G to total current flowing into node determines equivalent damping resistance for turn-off procedure.

$$R_{eq2} = \left(R'_G \frac{|X_{T2}|}{|X_G|}\right).\frac{|X_{T2}|}{|X_G|} = R'_G \frac{|X_{T2}|^2}{|X_G|^2}$$

$$= R'_G \frac{\left|\frac{X_G.X_S}{X_G+X_S}\right|^2}{|X_G|^2} = R'_G \frac{|X_G.X_S|^2}{|X_G|^2\,|X_G+X_S|^2}$$

$$R_{eq2} = R'_G \left(\left|\frac{X_S}{X_G+X_S}\right|\right)^2$$

By substituting the values of $X_G and X_S$;

$$= R'_G \frac{\left|j\omega_{OFF}.L_S + \frac{1}{j\omega_{OFF}.C_S}\right|^2}{\left|R'_G + j\omega_{OFF}L_G + \frac{1}{j\omega_{OFF}C_G} + j\omega_{OFF}.L_S + \frac{1}{j\omega_{OFF}.C_S}\right|^2}$$

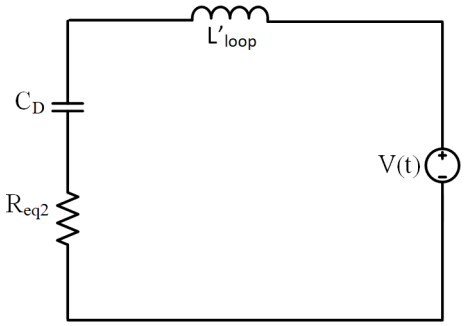

FIGURE 8. RLC equivalent circuit model for turn on.

$$R_{eq2} = R'_G \frac{\left(\omega_{OFF}.L_S - \frac{1}{\omega_{OFF}.C_S}\right)^2}{(R'_G)^2 + \left(\omega_{OFF}.L_G + \omega_{OFF}.L_S - \frac{1}{\omega_{OFF}.C_G} - \frac{1}{\omega_{OFF}.C_S}\right)^2} \quad (20)$$

TABLE 3. Parameters for Turn-oFF equivalent circuit model.

Parameters	Conversion Values
C_{GS} $(V_{DS} \approx 400V)$	228 pF
C_{DS} $(V_{DS} \approx 400V)$	527 pF
C_{GD} $(V_{DS} \approx 400V)$	70 pF
C_J $(V_R \approx 400V)$	40 pF
V_{DC}	400 V
L_{loop}	256.4 nH
L_D	1.62 nH
L_G	3.12 nH
L_s	0.89 nH
R_G	1.13 Ω
$R_{G,ext}$	2 Ω
C_{ISS}	260 pF

Accordingly, inductive load switching turn-off equivalent circuit model is presented in Fig. 8. Similarly to the turn-on equivalent model, a simple second-order equivalent circuit model for turn-off is also developed. A step voltage v(t) switches from V_{DC} to 0 V to turn off the HEMT. The energy transfer between the inductor and the capacitor will continue until it dissipates through equivalent resistor. C_{iss}, C_{oss}, and C_{rss} values are attained from datasheet when V_{DS} is ∼400 V. From these values, the parasitic capacitances are estimated as, $C_{GD} = 2$ pF, $C_{GS} = 258$ pF and $C_{DS} = 63$ pF. The parasitic inductances for turn-off switching condition are different from turn on with $L_G = 3.12$ nH, $L_D = 1.62$ nH, and $L_S = 0.89$ nH [43]. The maximum DC voltage across the source and drain terminals, the power loop parasitic inductances, the gate loop parasitic components and the equivalent switching device characteristics are the parameters that contribute to the peak magnitude of voltage spikes. Therefore, the parasitic inductances values should be taken separately for turn on and turn off conditions. With all the derived equations and parameters, turn-off equivalent resistance is estimated to be $R_{eq2} = 0.1463$ Ω. All these parameters are listed in Table 3.

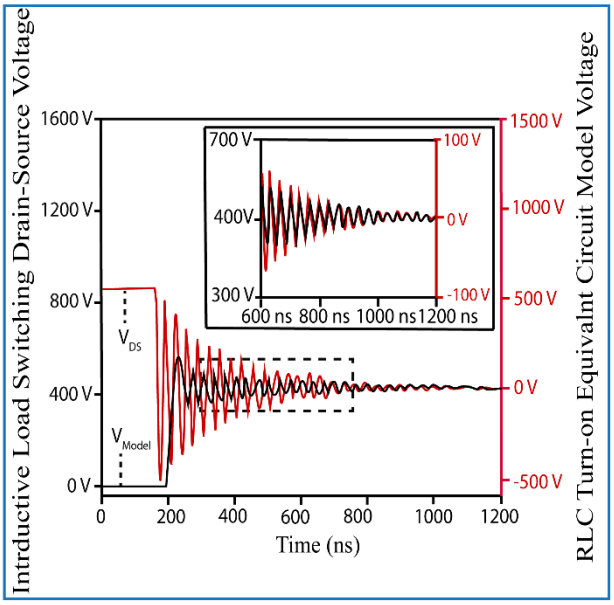

FIGURE 9. Turn-off oscillations and ringing comparison for drain source voltage (V_{DS}) between the inductive load switching Cadence Spectre Simulator transient simulation and estimation of turn-off RLC equivalent circuit model. Red line curve for RLC equivalent circuit model voltage while black line curve for inductive load switching drain-source voltage (V_{DS}).

TABLE 4. Numerical comparison between RLC turn-oFF equivalent circuit Model and inductive load switching.

Turn-on Comparison	V_{DC}	V_{Model}	Difference
Frequency	49.13 MHz	48.45 MHz	0.68 MHz
1st pulse peak to peak	176.66 V	589.76 V	213.10 V
3rd pulse peak to peak	146.78 V	388.66 V	241.88 V
9th pulse peak to peak	114.45 V	261.34 V	146.89 V
15th pulse peak to peak	48.79 V	79.67 V	30.78 V
21st pulse peak to peak	37.17 V	41.73 V	4.56 V

The RLC turn-off equivalent circuit model and inductive load switching Cadence Spectre Simulator transient simulation are also compared in terms of drain-source voltage turn-off oscillations. The resultant waveforms are presented in Fig. 9, and Table 4 gives numerical comparison. It's worth mentioning that comparison of differences are made with their corresponding absolute values.

In Fig. 9, the right vertical axis is for source-drain voltage oscillation from turn-off RLC equivalent circuit model, while the left vertical axis is for Cadence Spectre Simulator transient simulation. In the same manner as in turn-on, both circuits' switching transients start at simultaneously. It is clear from turn-off comparable model waveforms that the oscillation and ringing start immediately after step function is powered off. The oscillation can be dampened during the time that the HEMT is taking to switch off, the process known as intrinsic damping from slew time. It follows that if components in the inductive switching circuit switch faster then turn-off switching oscillations will likewise be severer and similar to the equivalent model oscillations curves. It is noted that there is good agreement between the frequency estimates using the simple RLC model and the simulation using the Cadence Spectre Simulator, with an inaccuracy of 0.78 percent. However, the oscillations amplitudes from these two methodologies show a significant disparity at first but will better match as it progresses. The approximations which are used to simplify the equivalent circuit model may be the cause of initial discrepancies. Another potential reason for the discrepancy is utilization of nominal values of parasitic capacitance from GaN HEMT datasheet, even though there may be some variance from device to device. More significantly, during the initial period, the turn-off oscillation becomes more severe because variations in the voltage-dependent parasitic capacitances is considerable in that duration. But in designed equivalent circuit model, these parasitic capacitances have been considered constant. It can be observed that these two curves match significantly better when ringing or oscillation is not considerable since the capacitances remain virtually constant when voltage variation is not significant.

IV. ANALYSIS AND DISCUSSION

As we earlier mentioned that the dv/dt has been increased from 3 V/ns for silicon IGBTs to 50 V/ns and 100V/ns for SiC MOSFETs and GaN HEMT respectively; therefore, the oscillations can be even more pronounced for GaN devices [1], [4]. It is generally believed that the oscillation phenomenon is triggered by the high di/dt and dv/dt during switching transients coupled with the external parasitic elements. It is worth pointing out that the RC snubber is not the only way of suppressing switching oscillation. In general, the switching oscillation damping techniques are divided into three categories: circuit modification (adding RC snubber circuit or ferrite bead), reduction of di/dt (reducing gate driver switching speed) and novel gate driver design (adding an external gate resistor). Adding external elements modifies the circuit, and the oscillation can be damped with the circuit modification. RC snubber has its own drawbacks, such as additional power losses but offer more effective damping solution than the gate driver slow down or extra gate resistor approach [44].

Our insightful analysis of the switching oscillations provides a new intuitive explanation about the non-mitigated oscillations. According to our analysis, the slew times of the GaN HEMT provides intrinsic damping due to which initial non-mitigated oscillation are not large as much as expected. But we also provide a complete and versatile guidance for the selection of optimal snubber components for the mitigation of these oscillation and validation of the RLC model. The design guidelines are summarized based on the circuit modeling analysis by considering the concept of higher-order circuit. Moreover, this approach can be employed in more complicated applications and as a design guideline for switching circuits because it is easier to adapt for various HEMT structures and fabrication processes with some modifications.

Modeling analysis of GaN HEMT for switching oscillations under low currents involves several complexities. Modeling under low level currents required a good small signal model due to non-linear nature of GaN devices. Small-signal modeling involves linearizing the device characteristics around a bias point, but capturing the behavior under low currents can be challenging. Parasitic elements, such as capacitances and inductances, and gate lag and trapping phenomena has more significant impact on the performance of GaN HEMTs at low currents. Therefore, the accurate modeling of these parameters also becomes more crucial for understanding the switching behavior and optimizing circuit performance. Furthermore, for accurate modeling, temperature effects becomes more crucial under low current conditions where self-heating becomes more pronounced. In addition, material dispersion and interaction between the device and its surroundings are also become more important for predicting the switching behavior under low currents across a wide frequency range. Moreover, noise considerations and, gate and drain current dynamics are also have a pronounced impact on the overall performance of the device. Therefore, for the simplicity of proposed model, we perform the analysis up to 4A.

A. TURN-ON OSCILLATION DAMPING

In figure 3, resistor, capacitor and inductor are connected in series with step voltage in second-order turn-on equivalent circuit model. The second-order circuit differential equation is attained by using Kirchhoff's voltage law (KVL),

$$\frac{d^2i(t)}{dt^2} + 2\alpha\frac{di(t)}{dt} + \omega_0 i(t) = 0 \tag{21}$$

where ω_0 is resonance frequency while α is called attenuation or neper frequency, which indicates how quickly the transient response will vanish. These two frequencies for turn-on equivalent circuit model are given as:

$$\alpha = \frac{R_{eq1}}{2L'_{loop}} \tag{22}$$

$$\omega_0 = \frac{1}{\sqrt{L'_{loop}C_J}} \tag{23}$$

The ratio of α and ω_0 is known as damping factor (ζ). Additionally, value of damping factor determines the kind of transient that the circuit will experience. These are: overdamped ($\zeta > 1$), critically damped ($\zeta = 1$) and underdamped ($\zeta < 1$).

$$\zeta = \frac{\alpha}{\omega_0} = \frac{R_{eq1}}{2}\sqrt{\frac{C_J}{L'_{loop}}} \tag{24}$$

When $\alpha > \omega_0$ i.e $\zeta > 1$, $\alpha = \omega_0$ i.e $\zeta = 1$ and $\alpha < \omega_0$ i.e $\zeta < 1$, the roots are real (overdamped), equal (critical damped) and complex (underdamped) respectively.

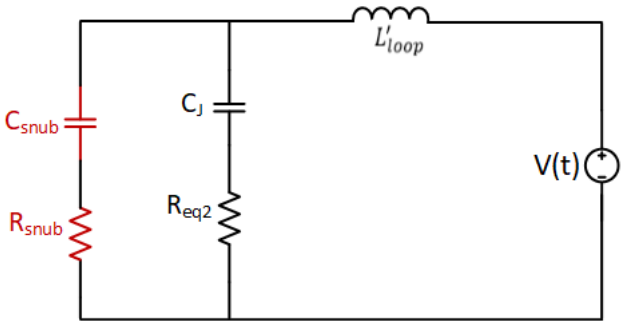

FIGURE 10. Turn-on RLC equivalent circuit with RC snubber.

The turn-on RLC equivalent circuit model's characteristic equation is written as:

$$s^2 + \frac{R_{eq1}}{L'_{loop}}s + \frac{1}{L'_{loop}C_J} = 0 \tag{25}$$

There are three cases for the characteristic equation's roots which are: 1) for underdamped condition, characteristic equation discriminant, $\Delta < 0$ (equivalently $\zeta < 1$), $v_t(t) = e^{-\alpha t}(A_1 \cos\omega_d t + A_2 \sin\omega_d t)$; 2) For critically damped condition, $\Delta = 0$ (equivalently $\zeta = 1$), $v_t(t) = e^{-\alpha t}(A_1 t + A_2)$; and 3) for overdamped condition $\Delta > 0$ (equivalently $\zeta > 1$),), $v_t(t) = A_1 e^{s_1 t} + A_2 e^{s_2 t}$, where $v_t(t)$ is the second-order circuit transient response. The starting current and voltage levels in circuit for transient as well as predicted value to which they will settle after an indefinite period of time serve as the boundary conditions that define the coefficients A_1 and A_2. The characteristic equation for the underdamped case has complex conjugate roots that causes the inverse Laplace transform to insert sinusoidal terms—exactly the oscillations—into system. The switching circuit is underdamped practically speaking.

According to above description, if we are able to shift the circuit from an underdamped condition to overdamped or critically damped condition, we can suppress oscillations. When just second-order circuit is involved, circuit operation region can be shifted from under damped to critical damped condition, simply, by increasing equivalent resistance Req1 that is attained by increasing gate resistance. However, resulting in undesirable increment in switching times due to which a very huge increment in switching losses.

In this article, we transformed second order circuit into a higher order circuit by adding RC snubber circuit. Basically, this is the purpose of addition of RC snubber circuit. The equivalent model that has been presented in Fig. 10 is a third-order circuit, as a result of the addition of snubber.

By choosing the appropriate values for C_{snub} and R_{snub}, the equivalent circuit with an RC snubber were converted from an underdamped condition to overdamped or critically damped. Equivalent circuit characteristic equation with snubber (3rd order circuit) are determined using initial condition and basic frequency domain analysis. By putting the discriminant is equal to zero for this cubic function, multiple roots are

attained from this function and all of which are real. After omitting the sinusoidal terms, the frequency domain characteristic equation's inverse Laplace transform only contains the exponential terms. Accordingly, the switching oscillations are also eliminated. Hence, the damping approach is: 1) select any one component, R_{snub} or C_{snub} as the initial element; 2) To determine relationship between R_{snub} or C_{snub} by putting discriminant, $\Delta = 0$; and 3) correspondingly other component value are estimated.

Cadence Spectre Simulator simulation is used to verify the idea. Starting with a constant value of C_s and resistance values ranging from 1 Ω to 20 Ω, the effects of each component were examined to determine the best resistance and capacitance values. In Fig. 11(a), waveforms show the impact of variation of resistance value on damping. Reduced initial overshoot maximum could result in a shorter overall duration of the resonant oscillations. In next step, capacitance C_s was varying from 1 nF to 10 nF while keeping the resistance value constant. This had an impact on the first overshoot's maximum value and also altered the resonant frequency, resonant frequency decreases as capacitance value increases, as shown in the waveforms of Fig. 11(b).

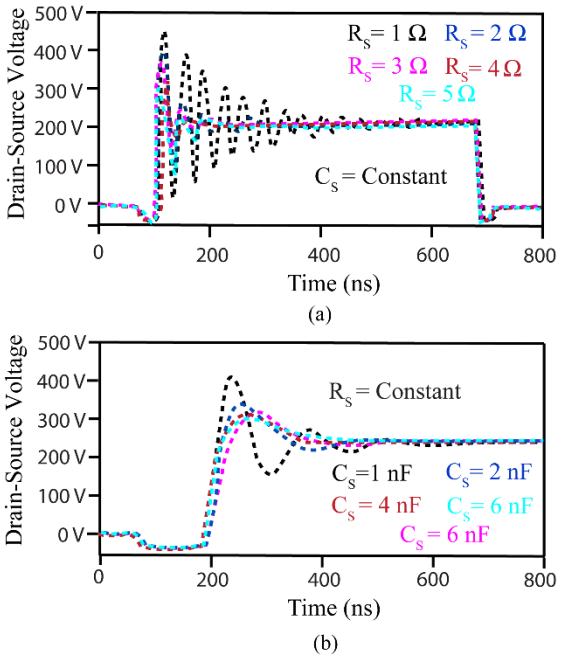

FIGURE 11. Drain-source voltage (V_{DS}) waveforms of GaN HEMT for various snubber values: a) varying Rs, while Cs = constant = 1 nF and b) varying Cs, while Rs = constant = 10Ω.

By using the relation $\Delta = 0$, the snubber resistor value is estimated, R_{snub}= 17.326Ω or R_{snub}= 10.99Ω. Either of the two snubber resistor values can be employed, as the cubic function possesses real roots for each of these values. R_{snub}= 10.99Ω is chosen for simulation, and corresponding waveforms are presented in Fig. 12.

It is depicted from waveforms of Fig. 12, the first voltage overshoot is significantly reduced with snubber circuit, and

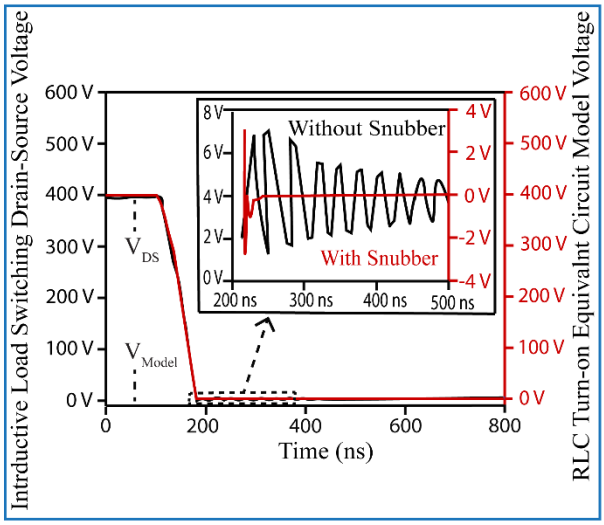

FIGURE 12. Cadence Spectre Simulator transient simulation GaN HEMT turn-off drain source voltage (V_{DS}) oscillations with and without RC snubber. Red line curve for RLC equivalent circuit model voltage and black line curve for inductive load switching drain-source voltage (V_{DS}).

the damping of the resonant oscillations and the number of oscillations are also improved. According to the simulation findings, the proposed snubber circuit have eliminated oscillations by reducing peak voltage overshoot upto 22.80% (from 468.75 V to 453.13 V) and the overall number of oscillations. This proves efficacy of the proposed approach. This theoretical analysis also provides us ability to control the damping system.

B. TURN-OFF OSCILLATION DAMPING

Similar to the turn-on equivalent circuit model, the turn-off equivalent circuit model is also a series second-order circuit. As a result, characteristic equations for turn-on and turn-off equivalent circuit models are same. The turn-off equivalent circuit with RC snubber is shown in Fig. 13.

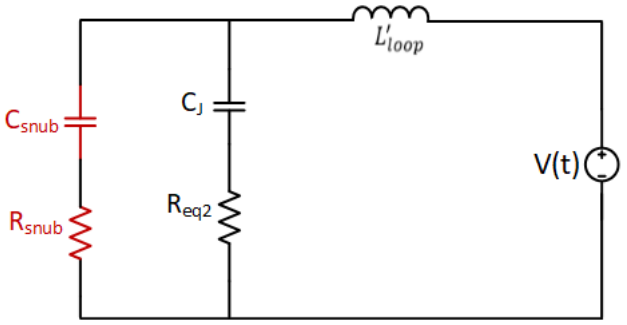

FIGURE 13. Turn-off RLC equivalent circuit with RC snubber.

Turn-off equivalent model also becomes a third-order circuit by including the snubber. Therefore, similar principles are utilized for turn-off oscillation damping as for turn-on. The initial element is selected as capacitor with value 2.2 nF and then value of snubber resistor achieved R_{snub} = 20.644Ω

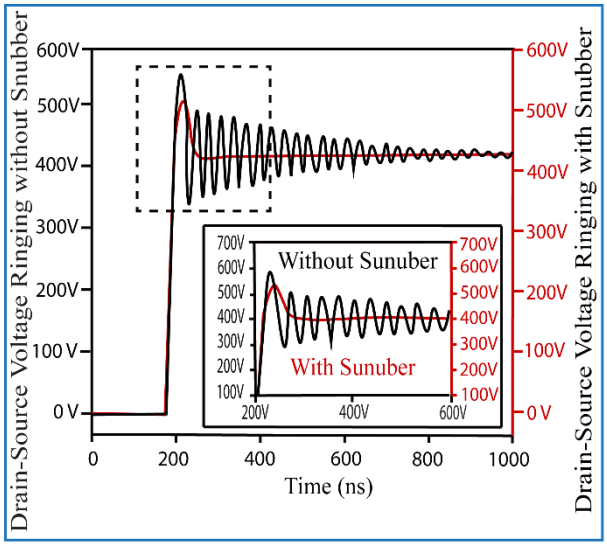

FIGURE 14. Cadence Spectre Simulator transient simulation GaN HEMT turn-off drain source voltage (V_{DS}) oscillations with and without RC snubber. Red line curve for RLC equivalent circuit model voltage and black line curve for inductive load switching drain-source voltage (V_{DS}).

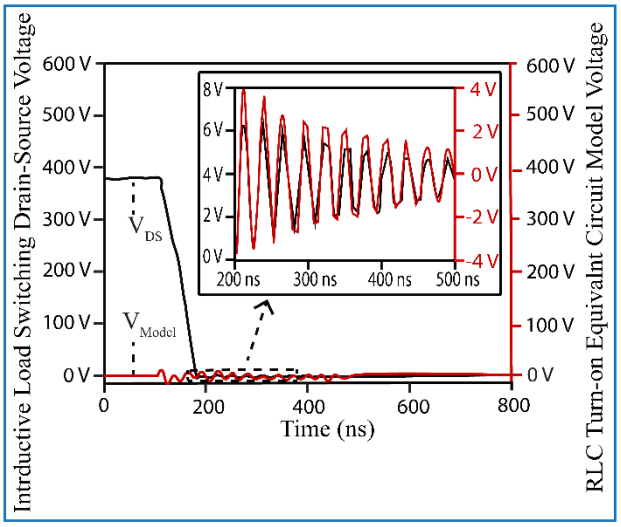

FIGURE 15. Turn-on oscillations and ringing comparison for drain source voltage (V_{DS}) between the inductive load switching and turn-on RLC equivalent circuit model. Red and black lines curve for RLC turn-on equivalent circuit model voltage and drain source voltage (V_{DS}) of inductive load switching, respectively.

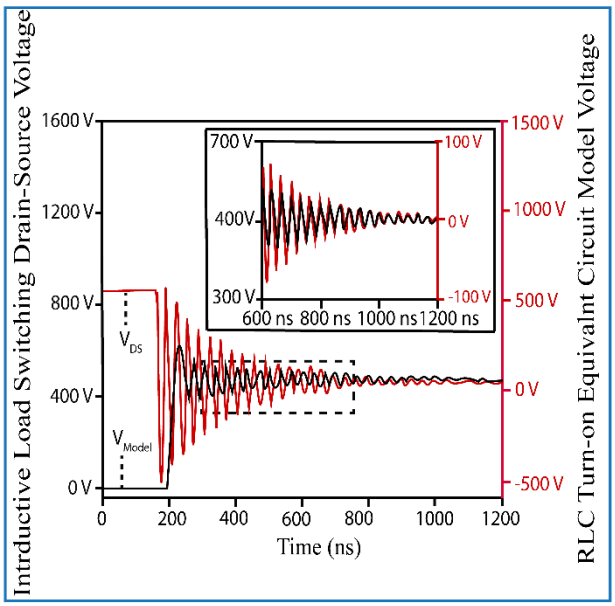

FIGURE 16. Turn-off oscillations and ringing comparison for drain source voltage (V_{DS}) between the inductive load switching and turn-off RLC equivalent circuit model. Red line curve for RLC equivalent circuit model voltage while black line curve for inductive load switching drain-source voltage (V_{DS}).

or $R_{snub} = 11.204\Omega$. $R_{snub} = 11.204\Omega$ is utilized in simulation and the resulting waveforms are presented in Fig. 14.

The predicted equivalent capacitance in turn-off equivalent circuit model is greater than turn-on case because turn-off oscillation is commonly noticeable and severe. According to the simulation findings, the proposed snubber circuit have eliminated oscillations by reducing peak voltage overshoot up to 29.57 % and the overall number of oscillations.

V. EXPERIMENTAL VERIFICATION

In this section, experimental verification is conducted to validate theoretical analysis. This is accomplished by using an inductive load switching test with test fixture setup from infenon. Infineon GaN power HEMT GS66508B in TO-220 package and Infineon GaN Schottky diode IDW30C65D1XKSA1 are utilized in the double pulse test experiment. 400 V is taken as the dc bus voltage. For snubber circuit, the capacitor of 2.2 nF is chosen as the starting component. In the simulation, two different snubber resistor values are used for turn-off and turn-on, as demonstrated in section VI. The turn-off and turn-on phases of switching operation are actually monitored during same switching cycle. It is important to take into account that the values obtained from computation are critical values and the corresponding oscillations are also in critically damped condition at a particular point. Both turn-off and turn-on ringing could potentially be converted to an over-damped condition by choosing the appropriate value of snubber components. In experiment, R_{snub} is selected 11.024 Ω for turn-off, and over-damped condition for turn-on oscillation is also achieved for this value. Figs. 15 represents the waveforms comparison for the RLC turn-on equivalent circuit model and inductive load switching in terms of source-drain voltage turn on oscillations on the basis of experimental verification.

Figs. 16 represents the waveforms comparison for the RLC turn-off equivalent circuit model and inductive load switching in terms of source-drain voltage turn on oscillations on the basis of experimental verification Figs. 17 and 18 represent the waveform for turn-on and turn-off for the inductive load switching without and with RC snubber, respectively. In Fig. 17(a), waveforms for inductive load switching for turn-on without snubber are presented. The RC snubber is

employed to dampen the oscillation and waveforms are presented in Fig. 17(b). Because the oscillations are relatively very small in the beginning, therefore, the turn-on damping effect is not immediately obvious but that is consistent with transient simulation results from Cadence Spectre Simulator.

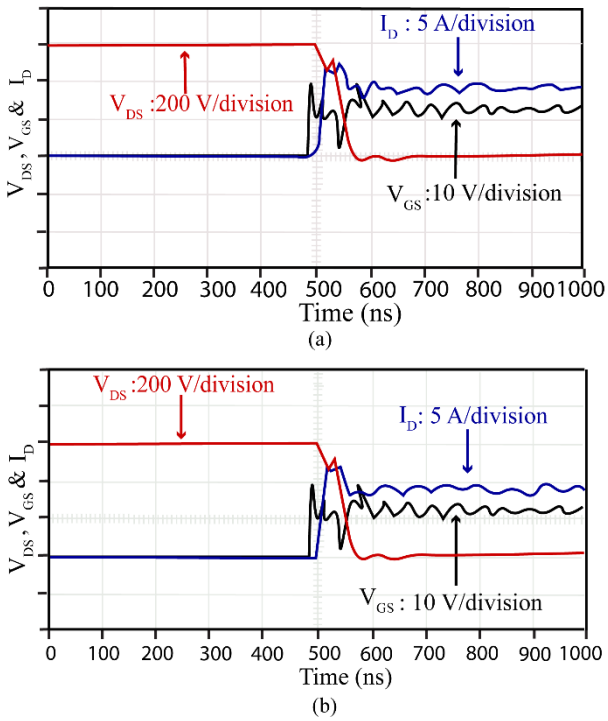

FIGURE 17. Measured turn-on inductive load switching waveforms, blue line: gate-source voltage (V_{GS}), green line: drain current (I_D) and red line: drain-source voltage (V_{DS}) (a) without snubber (b) with snubeer.

However, the waveform of drain current shows that the current oscillations becomes more moderate with the addition of snubber. Similarly in Fig. 18(a), turn-off inductive load switching is presented. Fig. 18(b) illustrates the switching waveforms that exhibit the impact of the RC snubber. In table 5, turn-off source-drain voltage ringing and oscillation damping effect is shown. The results of the experiment demonstrate that the snubber circuit's dampening effect can eliminate the oscillations with 26.47% decrement in overshoot voltage peak and number of oscillations. The drain current and source-drain voltage waveforms are extremely smooth and the neper frequency is also reduced when the snubber circuit is included.

Fig. 18(a) shows turn-off oscillation frequency of 49.13 MHz. From this oscillation frequency value, the loop inductance L_{loop}, which is utilized for the computation in section IV, may be calculated as 256.4 nH using turn-off resonance frequency equation (12).

Fig. 19 presents the source-drain voltage waveforms for design with different loop inductances and show its effect on voltage overshoot.

Fig. 19's waveforms reveal that, with the four time reduction in loop inductance, the overshoot voltage also reduce four

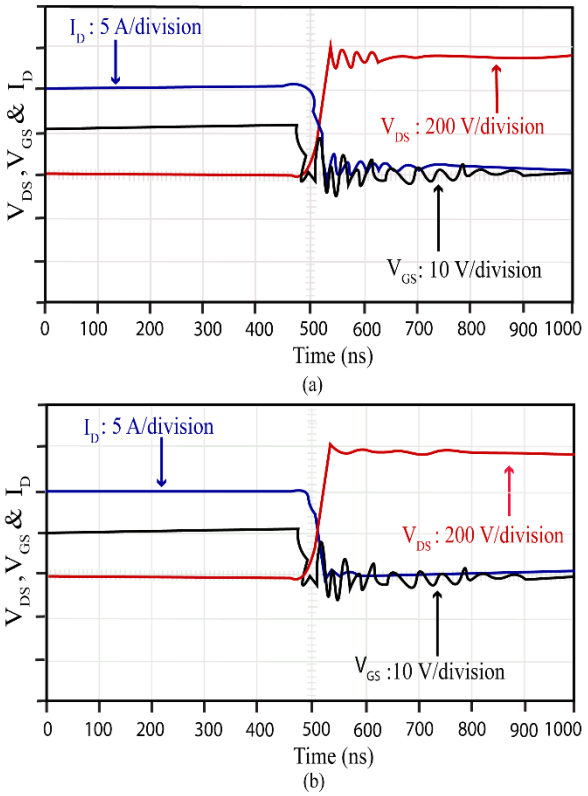

FIGURE 18. Measured turn-off inductive load switching waveforms blue line: gate-source voltage (V_{GS}), green line: drain current (I_D) and red line: drain-source voltage (V_{DS}) (a) without snubber (b) with snuber.

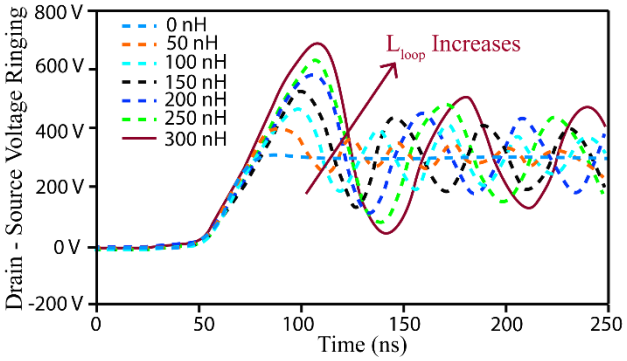

FIGURE 19. Effect of different loop inductances on switching oscillations.

times. Consequently, if advance packing of GaN eliminates or reduced this critical inductance then oscillations can be significantly reduced.

Fig. 20 presents the variations in source-drain voltage (V_{DS}) oscillations with varying loop inductances at different frequencies.

Fig. 20 indicates that loop inductance is less effected by change in frequency as compared to common source inductance because it is inductance of whole circuit not only the switching components. Consequently, the overshot voltage and switching oscillations are less effected with variation in loop inductance due to change in frequency. Table 5 gives the

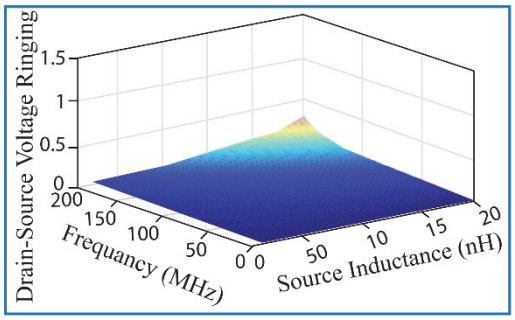

FIGURE 20. Effect of loop inductance on switching oscillations at different frequencies.

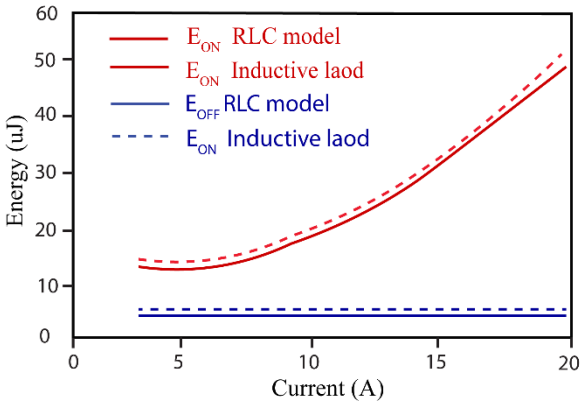

FIGURE 21. Switching energy comparison for two approaches with experimental and simulation results.

TABLE 5. Numerical comparison between RLC turn-on equivalent circuit model and inductive load switching.

Turn-on Comparison	V_{DC}	V_{Model}	Difference
Frequency	46.16 MHz	43.71 MHz	2.44 MHz
1st pulse peak to peak	6.34 V	7.68 V	1.34 V
2nd pulse peak to peak	5.44 V	6.72 V	1.28 V
3rd pulse peak to peak	5.31 V	5.91 V	0.60 V
4th pulse peak to peak	5.12 V	4.68 V	0.44 V
5th pulse peak to peak	4.82 V	4.08 V	0.74 V

numerical comparison between RLC turn-on circuit model and inductive load switching on the basis of experimental results.

Table 6 gives the numerical comparison between turn-off equivalent circuit model and inductive load switching on the basis of experimental results.

The switching energy also strongly depends upon the switching oscillation and spike. The switching energy can be defined and computed using the switching waveforms. The energies consumed on the switch during turn-off and turn-on transitions of switch are referred to as the turn-off energy (E_{OFF}) and turn-on energy (E_{ON}), respectively. The computation of E_{ON} and E_{OFF} based on the suggested RLC model waveforms for V_{DS} and I_{DS} in Figs. 17 and 18. Fig. 21

TABLE 6. Numerical comparison between RLC turn-oFF equivalent circuit model and inductive load switching.

Turn-on Comparison	V_{DC}	V_{Model}	Difference
Frequency	49.23 MHz	48.58 MHz	0.65 MHz
1st pulse peak to peak	176.66 V	389.76 V	213.10 V
3rd pulse peak to peak	156.78 V	347.64 V	190.86 V
9th pulse peak to peak	124.45 V	281.44 V	156.79 V
15th pulse peak to peak	38.74 V	69.67 V	30.98 V
21st pulse peak to peak	33.27 V	41.73 V	8.46 V

shows that the resulting waveforms of proposed RLC model match well with inductive load switching waveform. The turn-on energy is consistently higher than turn-off energy, which is result of excessive current oscillations and spikes.

Additionally, comparison of experimental and theoretical results is provided as evidence for the proposed RLC model. With a suitable agreement of 7.68%, the turn-off switching oscillation frequency in inductive load switching test is 49.13 MHz and it is comparable with 48.45 MHz which is gotten from RLC equivalent circuit model by using Cadence Spectre Simulator transient simulation. Since the effect of parasitic loop resistance was not taken into account in our simulation, there is a greater disparity between the oscillation amplitudes and the neper frequency between the RLC modeling simulation and experiment due to this exclusion of loop resistance. Another, more significant factor is that the values of parasitic capacitances in the RLC circuit model is taken as constant throughout switching process while the voltage-dependent parasitic capacitances change along with the oscillations. The double pulse test experiment demonstrates the effectiveness of the advised simple RLC equivalent circuit models in choosing the best snubber elements values as well as the validity of RLC models. This approach can be employed in more complicated applications and as a design guideline for switching circuits.

VI. CONCLUSION

GaN HEMTs provides a huge opportunity for high density and very high frequency power electronics designs. However, this potential is severely constrained by the switching oscillation phenomena related to the ultrafast switching properties of GaN HEMTs. Still, deficiencies exist in terms of comprehensive and simple analytical models that can quantitatively illustrate oscillation phenomena and offer theoretical guidance for suppressing of current or voltage oscillations. In this paper, we proposed two simple RLC equivalent circuit models for turn-off and turn-on of GaN HEMT respectively. The theoretical analysis of switching oscillation phenomenon and design guidelines for damping or snubber circuit are also presented using simple mathematical approach. A strong agreement is achived between the switching oscillation frequencies from transient simulation of Cadence Spectre Simulator for inductive load switching and oscillation of RLC turn-on equivalent circuit with an error of only 3.12%. These

simple equivalent circuit models are verified using both simulation and experimental techniques. In summary, an insightful analysis of the switching oscillation is performed at turn-on and turn-of, which presents a new and intuitive explanation that the slew times of the GaN HEMT provides intrinsic damping. A complete and versatile guidance for the selection of optimal snubber components as well as the validation of RLC model is provided. Moreover, this approach can be employed in more complicated applications and as a design guideline for switching circuits because it is easier to adapt for various HEMT structures and fabrication processes with some modifications.

APPENDIX

The double pulse test for a Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) is a method used to evaluate the switching performance and dynamic characteristics of the transistor. Specifications of double pulse test applied in our research for experimental verification are: device under test (DUT) GaN power HEMT GS66508B in To-220 package, text fixture setup from Infineon, Infineon GaN Schottky diode IDW30C65D1XKSA1, starting value of $C_{snub} = 2.2$ uF and $R_{snub} = 11.024\ \Omega$. The key components are: Pulse generator, load inductor, DC supply, gate driver, oscilloscope, current and voltage probes, Device under test (DUT) board, GaN power HEMT, GaN Schottky diode, C_{snub}, R_{snub}, resistor, capacitor and inductor. The major steps applied for double pulse test are: (1) Inductive load switching turn-on and turn-off (2) RLC Model circuit turn-on and turn-off (3) RLC model circuit turn-on and turn-off for the selection of snubber components (4) RLC model circuit turn-on and turn-off with snubber (5) Observe the effect of different loop inductances.

ACKNOWLEDGMENT

The authors are grateful to the Institute of Microelectronics, Chinese Academy of Sciences, Beijing, China, and the School of Physics and Electronic Information, Weifang University, Weifang, China, for conducting this research.

REFERENCES

[1] K. H. Teo, Y. Zhang, N. Chowdhury, S. Rakheja, R. Ma, Q. Xie, E. Yagyu, K. Yamanaka, K. Li, and T. Palacios, "Emerging GaN technologies for power, RF, digital, and quantum computing applications: Recent advances and prospects," *J. Appl. Phys.*, vol. 130, no. 16, Oct. 2021.

[2] M. Faizan, X. Wang, and M. Z. Yousaf, "Design and comparative analysis of an ultra-highly efficient, compact half-bridge LLC resonant GaN converter for low-power applications," *Electronics*, vol. 12, no. 13, p. 2850, Jun. 2023.

[3] A. Lidow, M. De Rooij, J. Strydom, D. Reusch, and J. Glaser, *GaN Transistors for Efficient Power Conversion*. Hoboken, NJ, USA: Wiley, 2019.

[4] C.-C. Lai, T.-J. Liang, W.-J. Tseng, K.-H. Chen, and S.-Q. Chen, "Design and implementation of 1 MHz DC–DC LLC resonant converter with GaN enhancement mode HEMT," in *Proc. IEEE 7th Southern Power Electron. Conf. (SPEC)*, Dec. 2022, pp. 1–6.

[5] Y. Ma, M. Xiao, Z. Du, H. Wang, and Y. Zhang, "Tri-gate GaN junction HEMTs: Physics and performance space," *IEEE Trans. Electron Devices*, vol. 68, no. 10, pp. 4854–4861, Oct. 2021.

[6] J. A. del Alamo and E. S. Lee, "Stability and reliability of lateral GaN power field-effect transistors," *IEEE Trans. Electron Devices*, vol. 66, no. 11, pp. 4578–4590, Nov. 2019.

[7] Y. Zhang, A. Zubair, Z. Liu, M. Xiao, J. Perozek, Y. Ma, and T. Palacios, "GaN FinFETs and trigate devices for power and RF applications: Review and perspective," *Semiconductor Sci. Technol.*, vol. 36, no. 5, May 2021, Art. no. 054001.

[8] A. Hassan, M. Ali, A. Trigui, Y. Savaria, and M. Sawan, "A GaN-based wireless monitoring system for high-temperature applications," *Sensors*, vol. 19, no. 8, p. 1785, Apr. 2019.

[9] Y. Zhang, A. Dadgar, and T. Palacios, "Gallium nitride vertical power devices on foreign substrates: A review and outlook," *J. Phys. D, Appl. Phys.*, vol. 51, no. 27, Jul. 2018, Art. no. 273001.

[10] N. Keshmiri, D. Wang, B. Agrawal, R. Hou, and A. Emadi, "Current status and future trends of GaN HEMTs in electrified transportation," *IEEE Access*, vol. 8, pp. 70553–70571, 2020.

[11] R. A. Khadar, C. Liu, R. Soleimanzadeh, and E. Matioli, "Fully vertical GaN-on-Si power MOSFETs," *IEEE Electron Device Lett.*, vol. 40, no. 3, pp. 443–446, Mar. 2019.

[12] Z. Chen, "Characterization and modeling of high-switching-speed behavior of SiC active devices," Virginia Tech, Rep., 2009.

[13] Z. Chen, D. Boroyevich, and R. Burgos, "Experimental parametric study of the parasitic inductance influence on MOSFET switching characteristics," in *Proc. Int. Power Electron. Conf.*, Jun. 2010, pp. 164–169.

[14] M. Adamowicz, S. Giziewski, J. Pietryka, and Z. Krzeminski, "Performance comparison of SiC Schottky diodes and silicon ultra fast recovery diodes," in *Proc. 7th Int. Conf.-Workshop Compat. Power Electron. (CPE)*, Jun. 2011, pp. 144–149.

[15] P. Anthony, N. McNeill, and D. Holliday, "High-speed resonant gate driver with controlled peak gate voltage for silicon carbide MOSFETs," *IEEE Trans. Ind. Appl.*, vol. 50, no. 1, pp. 573–583, Jan. 2014.

[16] O. Alatise, N.-A. Parker-Allotey, D. Hamilton, and P. Mawby, "The impact of parasitic inductance on the performance of silicon–carbide Schottky barrier diodes," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3826–3833, Aug. 2012.

[17] J. Wang, H. S. Chung, and R. T. Li, "Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 573–590, Jan. 2013.

[18] J. P. Kozak, R. Zhang, Q. Song, J. Liu, W. Saito, and Y. Zhang, "True breakdown voltage and overvoltage margin of GaN power HEMTs in hard switching," *IEEE Electron Device Lett.*, vol. 42, no. 4, pp. 505–508, Apr. 2021.

[19] R. Zhang, J. P. Kozak, Q. Song, M. Xiao, J. Liu, and Y. Zhang, "Dynamic breakdown voltage of GaN power HEMTs," in *IEDM Tech. Dig.*, Dec. 2020, pp. 23.3.1–23.3.4.

[20] A. Jarndal, "On modeling of substrate loading in GaN HEMT using grey wolf algorithm," *J. Comput. Electron.*, vol. 19, no. 2, pp. 576–590, Jun. 2020.

[21] H. A. Mantooth, K. Peng, E. Santi, and J. L. Hudgins, "Modeling of wide bandgap power semiconductor devices—Part I," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 423–433, Feb. 2015.

[22] E. Santi, K. Peng, H. A. Mantooth, and J. L. Hudgins, "Modeling of wide-bandgap power semiconductor devices—Part II," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 434–442, Feb. 2015.

[23] H. Li, X. Zhao, W. Su, K. Sun, X. You, and T. Q. Zheng, "Nonsegmented PSpice circuit model of GaN HEMT with simulation convergence consideration," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8992–9000, Nov. 2017.

[24] K. Shah and K. Shenai, "Simple and accurate circuit simulation model for gallium nitride power transistors," *IEEE Trans. Electron Devices*, vol. 59, no. 10, pp. 2735–2741, Oct. 2012.

[25] J. Waldron and T. P. Chow, "Physics-based analytical model for high-voltage bidirectional GaN transistors using lateral GaN power HEMT," in *Proc. 25th Int. Symp. Power Semiconductor Devices IC's (ISPSD)*, May 2013, pp. 213–216.

[26] M. Li and Y. Wang, "2-D analytical model for current–voltage characteristics and transconductance of AlGaN/GaN MODFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 1, pp. 261–267, Jan. 2008.

[27] X. Cheng, M. Li, and Y. Wang, "Physics-based compact model for AlGaN/GaN MODFETs with close-formed I–V and C–V characteristics," *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 2881–2887, Dec. 2009.

[28] S. Khandelwal, C. Yadav, S. Agnihotri, Y. S. Chauhan, A. Curutchet, T. Zimmer, J.-C. De Jaeger, N. Defrance, and T. A. Fjeldly, "Robust surface-potential-based compact model for GaN HEMT IC design," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3216–3222, Oct. 2013.

[29] S. Khandelwal, Y. S. Chauhan, and T. A. Fjeldly, "Analytical modeling of surface-potential and intrinsic charges in AlGaN/GaN HEMT devices," *IEEE Trans. Electron Devices*, vol. 59, no. 10, pp. 2856–2860, Oct. 2012.
[30] T. Liu, Y. Zhou, Y. Feng, T. T. Y. Wong, and Z. J. Shen, "Experimental and modeling comparison of different damping techniques to suppress switching oscillations of SiC MOSFETs," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Portland, OR, USA, Sep. 2018, pp. 7024–7031.
[31] G. Zulauf, S. Park, W. Liang, K. N. Surakitbovorn, and J. Rivas-Davila, "COSS losses in 600 V GaN power semiconductors in soft-switched, high- and very-high-frequency power converters," *IEEE Trans. Power Electron.*, vol. 33, no. 12, pp. 10748–10763, Dec. 2018.
[32] M. Faizan, J. Bi, M. Liu, L. Wang, V. Stempitsky, and M. Z. Yousaf, "Long life power factor corrected LED driver with capacitive energy mechanism for street light applications," *Sustainability*, vol. 15, no. 5, p. 3991, Feb. 2023.
[33] T. Liu, R. Ning, T. T. Y. Wong, and Z. J. Shen, "Modeling and analysis of SiC MOSFET switching oscillations," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 747–756, Sep. 2016, doi: 10.1109/JESTPE.2016.2587358.
[34] Z. Tong, J. Roig-Guitart, T. Neyer, J. D. Plummer, and J. M. Rivas-Davila, "Origins of soft-switching coss losses in SiC power MOSFETs and diodes for resonant converter applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 4, pp. 4082–4095, Aug. 2021.
[35] B. Sun, R. Burgos, X. Zhang, and D. Boroyevich, "Active dv/dt control of 600 V GaN transistors," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2016, pp. 1–8.
[36] W. Zhang, F. Wang, D. J. Costinett, L. M. Tolbert, and B. J. Blalock, "Investigation of gallium nitride devices in high-frequency LLC resonant converters," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 571–583, Jan. 2017.
[37] X. Zhang, Z. Shen, N. Haryani, D. Boroyevich, and R. Burgos, "Ultra-low inductance vertical phase leg design with EMI noise propagation control for enhancement mode GaN transistors," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2016, pp. 1561–1568.
[38] J. E. Makaran, "Gate charge control for MOSFET turn-off in PWM motor drives through empirical means," *IEEE Trans. Power Electron.*, vol. 25, no. 5, pp. 1339–1350, May 2010.
[39] M. Xu, X. Yang, and J. Li, "C-RC snubber optimization design for improving switching characteristics of SiC MOSFET," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 12005–12016, Oct. 2022.
[40] Z. Chen, R. Burgos, D. Boroyevich, F. Wang, and S. Leslie, "Modeling and simulation of 2 kV 50 a SiC MOSFET/JBS power modules," in *Proc. IEEE Electric Ship Technol. Symp.*, Apr. 2009, pp. 1–10.
[41] N. Hari, S. Ramasamy, M. Ahsan, J. Haider, and E. M. G. Rodrigues, "An RF approach to modelling gallium nitride power devices using parasitic extraction," *Electronics*, vol. 9, no. 12, p. 2007, Nov. 2020.
[42] L. Zhang, S. Guo, X. Li, Y. Lei, W. Yu, and A. Q. Huang, "Integrated SiC MOSFET module with ultra low parasitic inductance for noise free ultra high speed switching," in *Proc. IEEE 3rd Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Nov. 2015, pp. 224–229.
[43] A. Lemmon, M. Mazzola, J. Gafford, and C. Parker, "Stability considerations for silicon carbide field-effect transistors," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4453–4459, Oct. 2013.
[44] Z. Liu, X. Huang, F. C. Lee, and Q. Li, "Package parasitic inductance extraction and simulation model development for the high-voltage cascode GaN HEMT," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1977–1985, Apr. 2014.

MUHAMMAD FAIZAN was born in Pākpattan, Punjab, Pakistan, in 1992. He received the B.Sc. degree in electrical engineering from the University of Engineering and Technology, Lahore, Pakistan, in 2015, and the M.S. degree in electrical engineering from the University of Gujrat, Gujrat, Pakistan, in 2020. He is currently pursuing the Ph.D. degree in microelectronics and solid state electronics engineering with the Key Laboratory of Microelectronics Devices and Integrated Technology, Institute of Microelectronics, Chinese Academy of Sciences, UCAS, Beijing, China. His current research interests include devices and circuits to implement power electronics and analogue systems using CMOS technology, silicon and wide bandgap power device modeling, design and applications, power electronics, and power semiconductor devices and ICs.

KAI HAN received the Ph.D. degree in electronic engineering from the University of Chinese Academy of Sciences, Beijing, China, in 2013. He joined Weifang University, in 2013. He was a Professor, in 2022. His research interest includes semiconductor materials and devices.

XIAOLEI WANG was born in Xingtai, China, in 1985. He received the B.S. degree in physics from Northwestern Polytechnical University, Xi'an, in 2008, and the Ph.D. degree in microelectronics and solid state electronics from the Institute of Microelectronics, Chinese Academy of Sciences, Beijing, in 2013. Since 2013, he has been with the Institute of Microelectronics, Chinese Academy of Sciences. He is the author of more than 107 articles. His research interest includes hafnium oxide-based ferroelectric FET.

MUHAMMAD ZAIN YOUSAF received the B.Eng. degree in electronics and electrical engineering from Swansea University, U.K., in 2014, the M.Sc. degree in electrical engineering from The University of Lahore, Pakistan, and the Ph.D. degree from the College of Electrical Engineering, Guangxi University, Guangxi, China, in June 2022. Since July 2022, he has been a Lecturer with the School of Electrical and Information Engineering, Hubei University of Automotive Technology, Shiyan, Hubei, China. His research interests include power system optimization and control and protection of multiterminal dc transmission systems.