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RESEARCH ARTICLE

Cryogenic Body Bias Effect in DRAM Peripheral and Buried-Channel-Array Transistor for Quantum Computing Applications

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ABSTRACT This study investigated a novel forward body bias (FBB) analysis to optimize the threshold voltage (V_{th}) at cryogenic temperatures in the latest dynamic random-access memory (DRAM). Electrical measurements were conducted to analyze the cryogenic body bias effect in terms of performance, reliability, and short-channel effect in two types of transistors: DRAM peripheral low V_{th} transistors (Peri LVT) and buried-channel-array transistors (BCAT). At 77 K, the V_{th} shift (ΔV_{th}) in BCAT was larger than that in Peri LVT due to the difference in channel doping concentration. It was observed that only BCAT experienced a decrease in saturation drain current ($I_{d,sat}$) at cryogenic temperature because of the large ΔV_{th}. To compensate for the ΔV_{th}, FBB was applied to transistors. As a result, FBB effectively controlled the V_{th} and improved carrier mobility. Furthermore, this study demonstrated that FBB reduced hot-carrier degradation (HCD) at cryogenic temperature and improved short-channel effect, such as drain-induced barrier lowering (DIBL). These findings offer valuable solutions for optimizing cryogenic memory operation in quantum computing applications.

INDEX TERMS Buried-channel-array transistor (BCAT), cryogenic, drain-induced barrier lowering (DIBL), forward body bias, hot-carrier degradation, threshold voltage.

I. INTRODUCTION

Quantum computers are considered as a next-generation technology to overcome the data processing limitations of conventional binary systems [1]. However, thermal noise-sensitive quantum computing requires cryogenic temperatures for a stable operation [2]. Dynamic random-access memory (DRAM) is a primary candidate for cryogenic memory in quantum computing due to its high speed and technological maturity [3]. At cryogenic temperatures, DRAM performance has many benefits, such as increased carrier mobility and reduced subthreshold swing [4]. However, an increased threshold voltage (V_{th}) at cryogenic temperatures is undesirable in the circuit design for a multi-V_{th} scheme [5]. Therefore, various studies on V_{th} tuning have been conducted at cryogenic temperatures [6], [7], [8], [9], [10], [11]. Particularly, in our previous study [11], we revealed that a forward body bias (FBB) technique could effectively modulate V_{th} because an FBB reduced V_{th} and improved the drive current.

However, this previous study exclusively focused on peripheral n-type transistors with a conventional planar bulk structure. In order to apply an FBB technique to modern DRAM devices at cryogenic temperatures, it is necessary to

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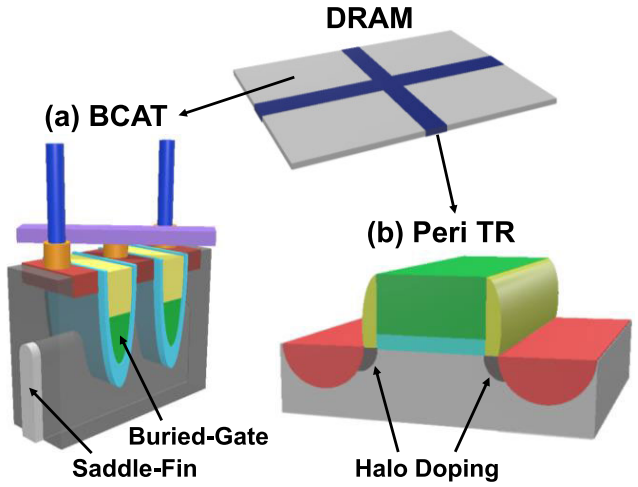

FIGURE 1. (a) Schematic of DRAM cell transistor with buried-gate and saddle-fin structure. (b) Schematic of DRAM peripheral transistor with halo doping.

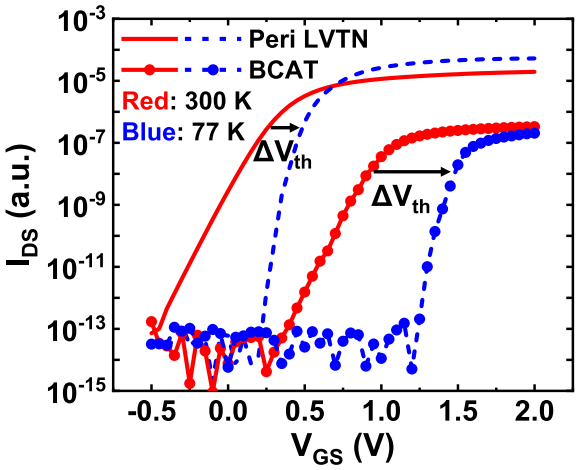

FIGURE 2. I_{DS}-V_{GS} curves of Peri LVTN and BCAT at different temperatures at V_{DS} = 50 mV. (Peri LVTN L_g = 1.7 μm). The actual off-current may be lower than the value indicated on I_{DS}-V_{GS} curves due to the measurement setting limit.

investigate the FBB effect on peripheral p-type transistors and cell transistors with a buried-channel-array transistor (BCAT).

Therefore, this study evaluates cryogenic FBB effects on BCAT and peripheral n-type and p-type transistors at different channel lengths. Furthermore, we propose the highly distinct advantages of FBB operation at cryogenic temperature in terms of device performance, reliability, and the short-channel effect.

II. DEVICE STRUCTURE AND METHODS

As shown in Fig. 1(a), a device of sub-30 nm BCAT is a state-of-the-art DRAM cell transistor with a buried-gate structure to minimize gate-induced drain leakage (GIDL). Additionally, BCAT incorporates a saddle-fin structure, similar to that of FinFET, for enhanced electrostatic control [12], [13].

Fig. 1(b) shows a schematic of a DRAM peripheral transistor with a conventional planar bulk structure, polysilicon/silicon oxy-nitride (poly/SiON) gate stacks, and halo doping near the source/drain regions. This study examined two types of peripheral transistors: peripheral n-type low V_{th} transistors (Peri LVTN) and peripheral p-type low V_{th} transistors (Peri LVTP).

Current-voltage (I-V) measurements were conducted using a Keithley 4200A-SCS parameter analyzer in conjunction with a vacuum chamber probe station. V_{th} was extracted by a constant current method from the drain current (I_{DS})-gate voltage (V_{GS}) curve [14].

III. THE NECESSITY OF FORWARD BODY BIAS

Fig. 2 shows the I_{DS}-V_{GS} curves of the DRAM Peri LVTN and BCAT at 300 K and 77 K, respectively. As shown in this figure, DRAM provides a multi-V_{th} scheme depending on the purpose of the device. At 300 K, Peri LVTN gains a high drive current using a low V_{th} even though the off-current is high because Peri LVTN is manufactured for high-performance operation. In contrast, BCAT maintains a low off-current using a high V_{th} to prevent the loss of data stored in the storage capacitor [15]. At 77 K, V_{th} increases in both types of transistors. However, the V_{th} shift (ΔV_{th}) in BCAT is larger than that in Peri LVTN because the ΔV_{th} is larger in lightly doped channel transistors. The equation for ΔV_{th} is as follows:

$$\Delta V_{th} = \Delta V_{fb} + \Delta 2\Psi_B + \Delta \frac{\sqrt{2\varepsilon_{si} q N_a (2\Psi_B)}}{C_{ox}} \quad (1)$$

$$\Delta \Psi_B = \Delta (E_i - E_f), \quad (2)$$

where V_{fb} is the flat band voltage, Ψ_B is the potential difference between the intrinsic Fermi level (E_i) and Fermi level (E_f) of silicon, and ε_{si}, q, N_a, and C_{ox} are the permittivity of silicon, electron charge, acceptor doping concentration, and oxide capacitance, respectively. It is worth noting that, the $\Delta\Psi_B$ parameter in (2) requires careful consideration. As the channel becomes less doped, there is a larger variation in (E_i - E_f) as the temperature decreases; therefore, the $\Delta 2\Psi_B$ parameter in (1) increases [4], [16]. Consequently, an increased $\Delta 2\Psi_B$ leads to a larger ΔV_{th}. In modern cryogenic memory devices, a large ΔV_{th} inevitably occurs because advanced transistors use lightly doped or undoped channels to enhance mobility and reduce random dopant fluctuations.

As shown in Fig. 3, V_{th} increases as the gate length (L_g) scales down in Peri LVTN with halo doping because halo doping in a short-channel increases the effective surface doping concentration, resulting in a higher V_{th} [17]. V_{th}, already elevated at 300 K, further increases at 77 K. Consequently, it becomes challenging for a short-channel Peri LVTN with halo doping to function as a low V_{th} transistor at cryogenic temperatures.

The results of Fig. 2 and Fig. 3 demonstrate the necessity of V_{th} optimization at cryogenic temperatures for the lightly doped channel BCAT and short-channel peripheral

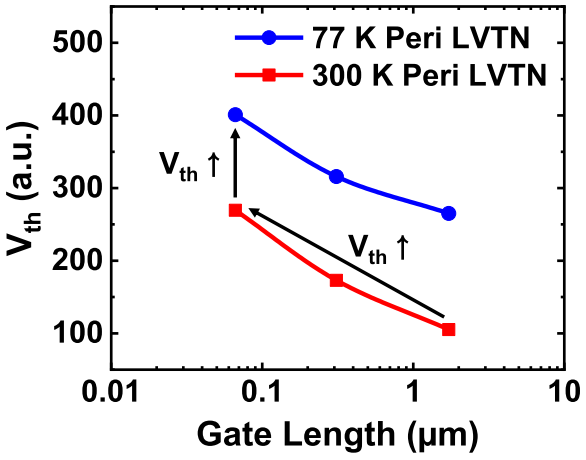

FIGURE 3. V_{th} as a function of the gate length in Peri LVTN with halo doping at different temperatures. V_{th} is extracted from I_{DS}-V_{GS} curves at V_{DS} = 50 mV. (L_g = 1.7 μm, 0.3 μm, and 66 nm, respectively, in same gate widths).

low V_{th} transistors (Peri LVTs) with halo doping. In this study, we have demonstrated that an FBB reduces V_{th} at cryogenic temperatures and has significant advantages in terms of device operation. These findings are further discussed in the following sections.

IV. RESULTS AND DISCUSSION

A. V_{th} MODULATION

As shown in Fig. 4(a), the V_{th} of the short-channel Peri LVTN increased as the temperature decreased from 300 to 77 K (red-to-blue curve). When an FBB of 0.8 V was applied (blue-to-black curve), V_{th} was adjusted to the same level as it was 300 K, and the maximum transconductance ($g_{m.max}$) increased by 5.2%. Therefore, a constant V_{th} was maintained independent of the temperature, ensuring the proper function of a low V_{th} transistor. The increased $g_{m.max}$ also offered the advantage of improved mobility, enabling faster operations at cryogenic temperatures.

Similarly, as shown in Fig. 4(b), ΔV_{th} of the short-channel Peri LVTP was effectively compensated by an FBB of 0.8 V (blue-to-black curve), and $g_{m.max}$ increased by 4.3%.

As shown in Fig. 4(c), the V_{th} of the BCAT increased significantly as the temperature decreased from 300 to 77 K (red-to-blue curve). In Fig. 5, it is evident that the ΔV_{th} of the BCAT was 4.79 times greater than that of Peri LVTN due to the influence of the lightly doped channel. For BCAT, the saturation drain current ($I_{d.sat}$) decreased at 77 K compared to 300 K because the overdrive voltage ($V_{OV} = V_{GS} - V_{th}$) decreased at 77 K (refer to Fig. 5(a)). In contrast, as shown in Fig. 5(b), $I_{d.sat}$ of the Peri LVTN increased at 77 K compared to 300 K, as the effect of increased carrier mobility outweighed the effect of decreased overdrive voltage.

An FBB of 0.7 V was applied in BCAT (blue-to-black curve in Fig. 4(c)) to modulate the increased V_{th}, and consequently, V_{th} decreased again and $g_{m.max}$ increased by 39.3%. Consequently, as shown in Fig. 5(a), $I_{d.sat}$ of the BCAT with

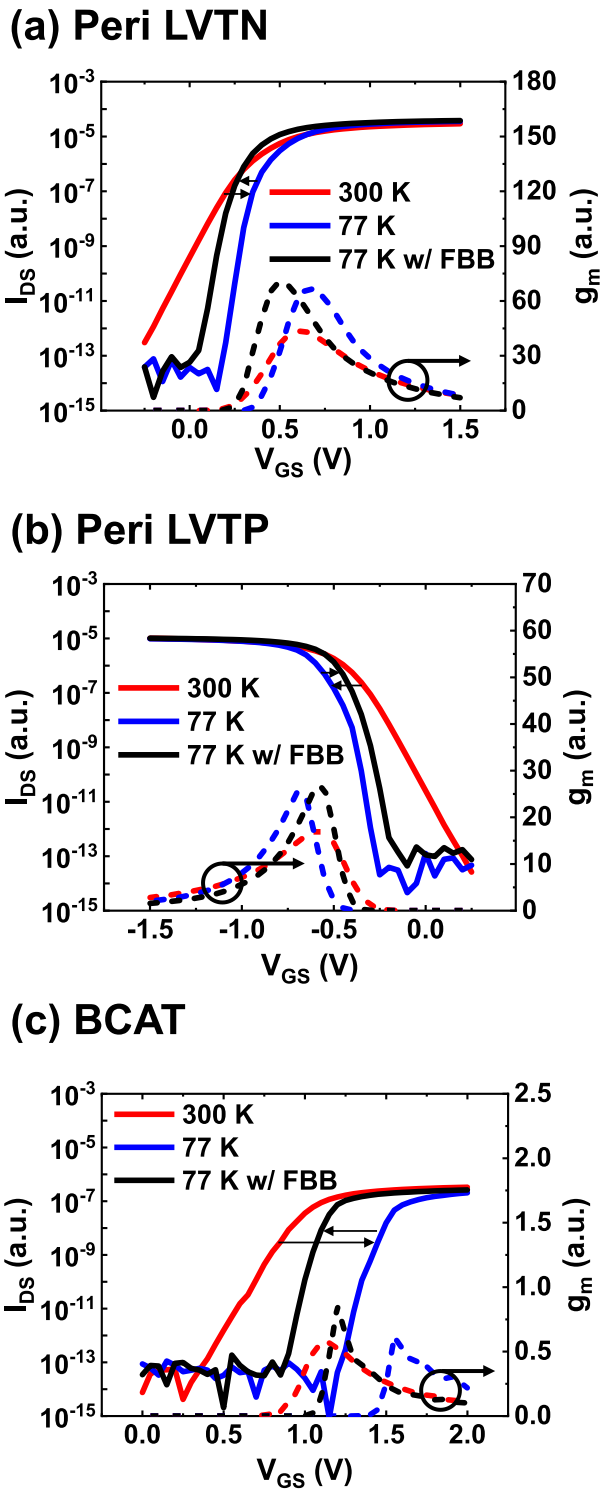

FIGURE 4. I_{DS}-V_{GS} curves at V_{DS} = |50 mV| at different temperatures and body bias in (a) short-channel Peri LVTN with halo doping, (b) short-channel Peri LVTP with halo doping, and (c) lightly doped channel BCAT. Dashed lines are transconductance (g_m) curves. FBB in Peri TR is 0.8 V and FBB in BCAT is 0.7 V. (Peri LVTN L_g = 66 nm, Peri LVTP L_g = 69 nm). The actual off-current may be lower than the value indicated on I_{DS}-V_{GS} curves due to the measurement setting limit.

FBB at 77 K (77 K w/FBB) was adjusted to the same level as it was 300 K. However, it should be noted that there was a limitation in reaching the same level of V_{th} at 300 K

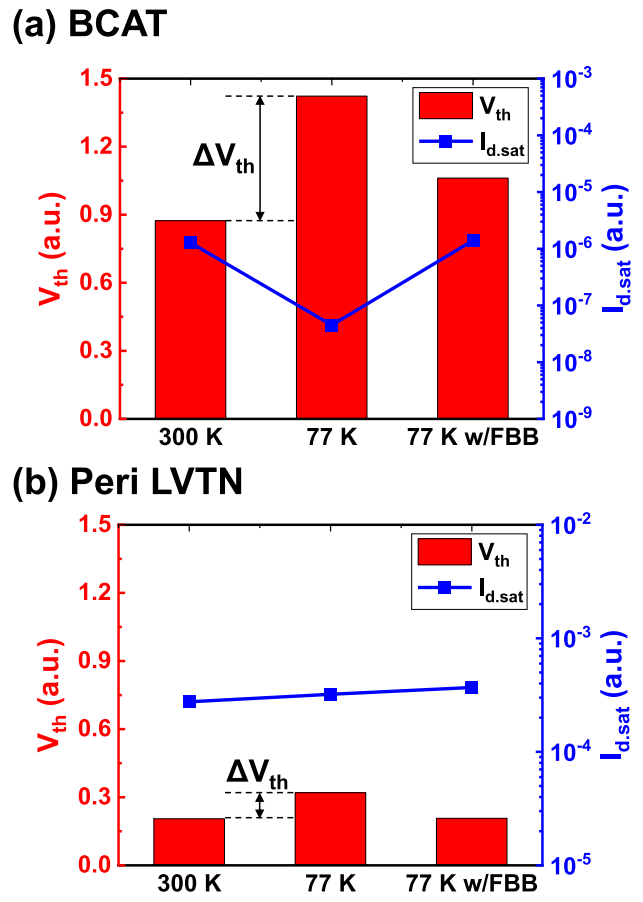

FIGURE 5. V_{th} and $I_{d.sat}$ at different temperatures and body bias in (a) BCAT and (b) Peri LVTN. I_{dsat} is a drain current at $V_{GS} = V_{DS} = 1.5$ V.V_{th} is extracted from I_{DS}-V_{GS} curves at $V_{DS} = 1.5$ V. (Peri LVTN $L_g = 66$ nm.)

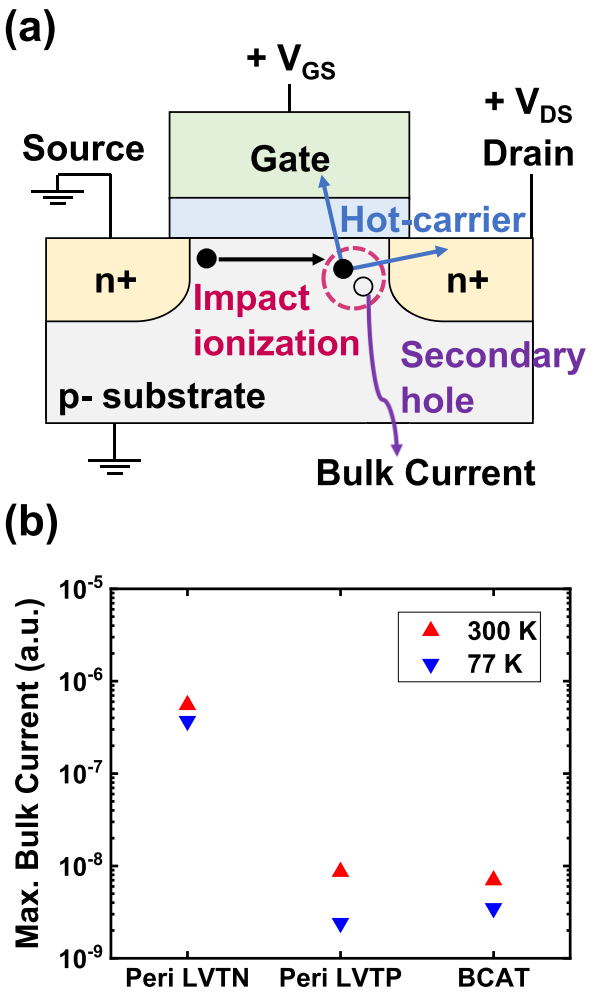

FIGURE 6. (a) Schematic of impact ionization in the nMOSFET structure. (b) Maximum bulk current at different temperatures in Peri LVTN, Peri LVTP, and BCAT. Maximum bulk current is extracted from the bulk current vs. V_{GS} curve at the bias condition of $V_{GS} = 0$ to $|2.2$ V$|$ sweep, $V_{DS} = |2.2$ V$|$ in Peri TR, and $V_{DS} = 2.5$ V in BCAT. (Peri LVTN $L_g = 66$ nm, Peri LVTP $L_g = 69$ nm.)

because applying a high FBB exceeding 0.7 V induced a forward-biased p-n junction diffusion current. Therefore, the upper limit of FBB should be considered when optimizing the circuit design for cryogenic memory. In this study, when FBB of 0.7 V was applied in BCAT and FBB of 0.8 V was applied in Peri LVTs, the off-currents of the source, bulk, and gate maintained almost the same level as without FBB (data now shown). These results confirm that optimal FBB enhances DRAM performance at cryogenic temperatures without leakage current issues.

B. HOT-CARRIER DEGRADATION

As shown in Fig. 6(a), hot carriers generated by impact ionization move into the gate or drain side by a positive voltage. In contrast, secondary holes move into the bulk side, contributing to the bulk current. Since the number of electron-hole pairs generated by impact ionization is the same, the hot-carrier effect can be inferred from the bulk current.

Fig. 6(b) shows the maximum bulk current at different temperatures in Peri LVTN, Peri LVTP, and BCAT. At 77 K, the maximum bulk current was lower than that at 300 K in all cases, indicating that the hot-carrier effect decreased at cryogenic temperatures because a low temperature reduced the carrier energy distribution influenced by electron-electron scattering [18].

To evaluate the cryogenic body bias effect in terms of reliability, we conducted hot-carrier degradation (HCD) stress tests, applying both FBB and reverse body bias (RBB) as depicted in Fig. 7. Stress conditions involved $V_{GS} = V_{DS} = 2.2$ V for Peri LVTN, $V_{GS} = V_{DS} = -4$ V for Peri LVTP, and $V_{GS} = V_{DS} = 3.5$ V for BCAT, which were suitable for observing HCD in our devices.

Fig. 7(a) and Fig. 7(b) show the $I_{d.sat}$ and ΔV_{th} in Peri LVTN after the HCD stress tests. In the RBB case, $I_{d.sat}$ decreased by 47.2%, and ΔV_{th} increased significantly compared to the initial value, which could potentially lead to severe degradation in the device. In contrast, in the FBB case, $I_{d.sat}$ decreased by only 4.3%, and ΔV_{th} increased slightly (13.8% of the RBB case) because FBB reduced the electric field near the drain side [19].

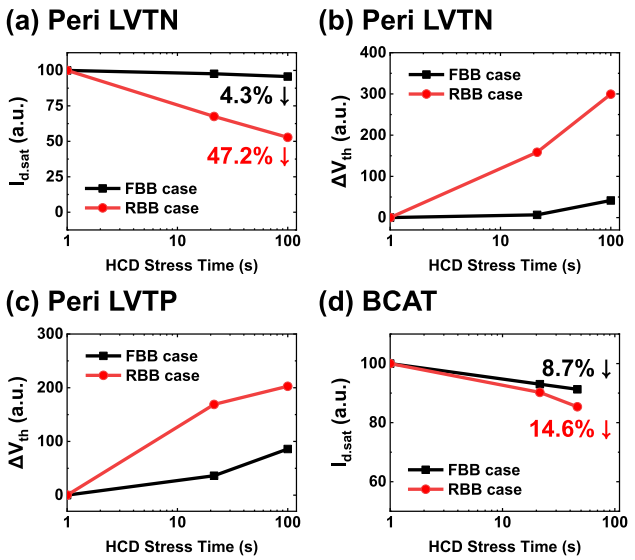

FIGURE 7. $I_{d.sat}$ and ΔV_{th} as a function of HCD stress time at 77 K: (a), (b) Peri LVTN, (c) Peri LVTP, and (d) BCAT. Here, FBB = 0.5 V and RBB = - 0.5 V for n-type, and p-type is opposite. In case of Peri TR, I_{dsat} is a drain current at $V_{GS} = V_{DS} = |1.5\ V|$, and stress time is 100 s. In case of BCAT, I_{dsat} is a drain current at $V_{GS} = V_{DS} = 2$ V, and stress time is 50 s. V_{th} is extracted from I_{DS}-V_{GS} curves at $V_{DS} = |50\ mV|$. (Peri LVTN L_g = 66 nm, Peri LVTP L_g = 69 nm.)

Fig. 7(c) and Fig. 7(d) show the ΔV_{th} in Peri LVTP and $I_{d.sat}$ in BCAT after the HCD stress tests, respectively. As shown in Fig. 7(c), the ΔV_{th} in Peri LVTP in the RBB case was 2.4 times larger than that in the FBB case. In Fig. 7(d), the $I_{d.sat}$ in BCAT for the RBB case decreased by 14.6%, whereas the $I_{d.sat}$ for the FBB case decreased by 8.7%. Consequently, the FBB case demonstrated improved HCD results compared to the RBB case in Peri LVTN, Peri LVTP, and BCAT. These results confrm that FBB enhances DRAM reliability at cryogenic temperatures.

C. DRAIN-INDUCED BARRIER LOWERING

Drain-induced barrier lowering (DIBL) is one of the key parameters that can identify the short-channel effect [20], [21]. The equation for DIBL value in this study is as follows:

$$DIBL = \frac{V_{th(V_{DS}=0.05\ V)} - V_{th(V_{DS}=V_{DD})}}{V_{DD} - 0.05\ V} \quad (3)$$

Fig. 8(a) shows the DIBL values at various channel lengths of the Peri LVTN as a function of temperature. The gate lengths of the long-, mid-, and short-channel were 1.7 μm, 0.3 μm, and 66 nm, respectively. In the case of long- and mid-channel, the DIBL was lower at 77 K compared to 300 K because the effective channel length increased due to the influence of surface potential at cryogenic temperatures [22]. Additionally, the carrier became difficult to overcome the channel energy barrier between the source and drain due to the reduced thermionic emission at cryogenic temperatures [23].

However, an unusual DIBL inversion phenomenon occurred in the short-channel, where the DIBL was higher

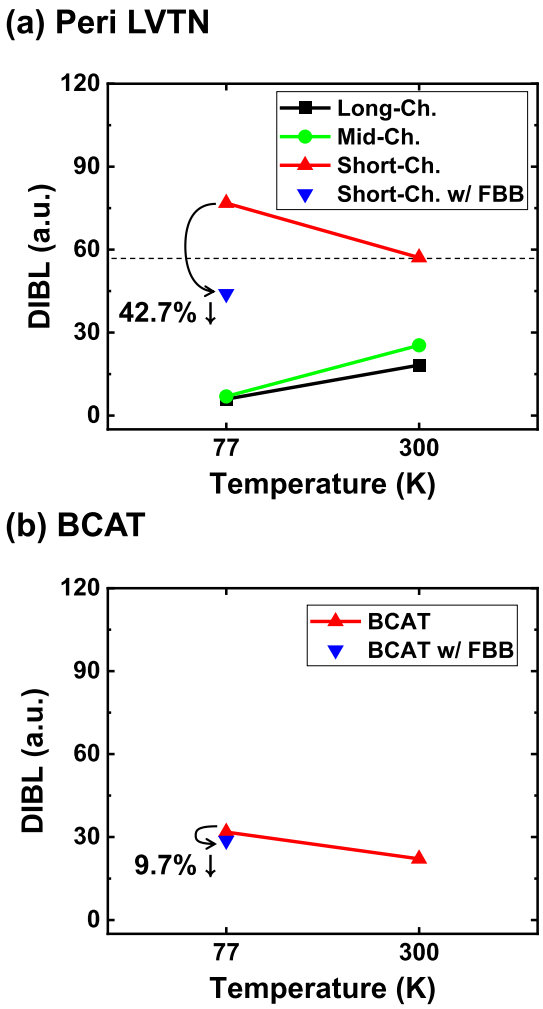

FIGURE 8. (a) DIBL as a function of temperature in Peri LVTN at different channel lengths and body bias. (b) DIBL as a function of temperature in BCAT at different body bias. (BCAT V_{DD} = 1.5 V. Peri LVTN V_{DD} = 1.05 V. Peri LVTN L_g = 1.7 μm, 0.3 μm, and 66 nm, respectively, in same gate widths.)

at 77 K compared to 300 K. The reason for this phenomenon was that the widened p-n junction depletion width (bulk-to-source, bulk-to-drain) at cryogenic temperatures reduced the effective channel length [24], [25]. To overcome this phenomenon, FBB of 0.8 V was applied to the short-channel Peri LVTN at 77 K (red-to-blue in Fig. 8(a)). Consequently, the DIBL decreased by 42.7%, even lower than the DIBL value at 300 K. This effect resulted from the narrowing of the p-n junction depletion width when FBB was applied, thereby increasing the effective channel length. This mechanism could also be applied to BCAT.

Fig. 8(b) shows the DIBL value in BCAT as a function of temperature. The DIBL was higher at 77 K compared to 300 K due to the widened p-n junction depletion width (bulk-to-source, bulk-to-drain) at cryogenic temperatures. Subsequently, an FBB of 0.7 V was applied to BCAT at 77 K. As a result, the DIBL decreased by 9.7% due to the shortened p-n junction depletion width. Based on these results,

this study provides a novel solution to overcome DIBL degradation in short-channel devices and BCAT at cryogenic temperatures for the first time.

V. CONCLUSION

The cryogenic body bias effect was comprehensively analyzed using DRAM Peri LVTN, Peri LVTP, and BCAT. The experimental results confirm that FBB is highly effective in controlling V_{th} at cryogenic temperatures. These findings provide a valuable solution for cryogenic memory circuit design. Furthermore, FBB enhances carrier mobility and improves reliability by reducing HCD. Therefore, cryogenic memory can operate faster and more reliably. Finally, FBB can mitigate DIBL degradation in short-channel Peri LVTN and BCAT at cryogenic temperatures. The FBB applications demonstrated in this study will serve as a guide for optimizing V_{th} at cryogenic temperatures and provide insights into device operation for quantum computing.

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