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RESEARCH ARTICLE

Performance Comparison of Nanosheet FET, CombFET, and TreeFET: Device and Circuit Perspective

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ABSTRACT In this article, the comparison of nanosheet (NS) FET, CombFET, and TreeFETs at advanced technology nodes is performed. Initially, the DC metrics like I_{ON}, I_{ON}/I_{OFF} and I_D-V_{DS} are dominated by TreeFET compared to Comb and NSFET. The TreeFET exhibits higher I_{ON} and ensures high-performance (HP) applications at advanced nodes. However, the NSFET continues as a better performer towards low power (LP) applications. The TreeFET dominates the performance and switching performance for temperature variation. At lower temperatures, the NS, Comb, and TreeFETs have a marginal impact on I_{OFF}. The analog performance is dominated by TreeFET due to higher I_{ON}. The NSFET exhibits lower Cgd and Cgs due to the absence of interbridges (IB) between channels. The RF performance is also dominated by Comb and TreeFETs due to the presence of IBs. Further, TreeFET based CMOS inverter outperforms in terms of switching current (I_{SC}) compared to the NSFET and CombFET counterparts. The 27-stage ring oscillator (RO) performance of TreeFET dominates Comb and NSFET with 11.56 GHz ensuring driving radio frequency applications. Thus, the paper will give deep insights into the performance of emerging FETs at both device as well as circuit levels.

INDEX TERMS CombFET, TreeFET, NSFET, temperature, CMOS inverter, ring oscillator.

I. INTRODUCTION

Downsizing the Fin-FET device for smaller technology nodes necessitates using slimmer and taller fins. However, this change results in the decline and instability of the driving current [1], [2]. Enhancing the driving capacity of such thin fin-based standard cells [SS] also becomes extremely challenging. As technology advances beyond the 5 nm nodes, stacked nanosheet (NS) gate-all-around (GAA) FETs are anticipated to take over from FinFETs [3], [4]. This shift is due to their superior gate control, elevated current density per device footprint, and the ability to adjust sheet width, which facilitates adaptable circuit design [5], [6]. Having a flexible and expanded channel width provides the confidence to achieve a substantial ON current through the vertical arrangement of slender conducting channels. This is a departure from traditional devices that only allow a single fin. Nonetheless, the vertical stacking of nanosheets introduces heightened secondary effects that impede the overall circuit performance [7]. Hence, in the pursuit of enhancing device current, a range of channel configurations have been proposed, including U-shaped [8], H-shaped [9], Tree-shaped [10], and Comb-shaped [11] channels.

Notably, the CombFET and TreeFET have gained prominence due to their feasibility in adhering to the existing

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fabrication process. Moreover, these emerging innovative FET fabrication methods are compatible with the established FinFET manufacturing process [11]. In the context of TreeFET, the channel structure is created by combining stacked nanosheets with fin-like interbridges (IBs). Achieving this geometry involves selectively etching sacrificial layers between channel layers during the release process of NS channels, resulting in the formation of vertical interbridge (IB) channels resembling fins amidst the NSs [10]. On the other hand, the channel formation in CombFET involves selective epitaxy on side walls. This approach has the potential to substantially increase the effective width per footprint (W_{eff}/FP) [11].

Additionally, the incorporation of IBs can lead to a remarkable up to 76% enhancement in ON-current for stacked NSs without requiring an expansion of the device footprint [10], [12]. The presence of fin edges further prevents the deformation of sheets once the channel is released, contributing to the mitigation of various issues related to stacked NSFETs and effectively boosting ON current. However, it is important to note that a comprehensive investigation encompassing DC, analog/RF, and circuit aspects is still warranted to thoroughly assess the overall performance metrics. In order to seamlessly integrate these novel devices into integrated circuit fabrication, a comprehensive analysis of both device-level and circuit-level performance is crucial. Therefore, this paper presents a comprehensive analysis of the performance of emerging devices such as NSFETs, CombFETs, and TreeFETs. The initial focus lies in delineating the behavior of these devices through transfer characteristics (I_D-V_{GS}) and output characteristics (I_D-V_{DS}). While there have been recent studies investigating the performance of NSFETs, TreeFETs, and CombFETs [13], [14], [15], it is noteworthy that none of these studies have reported a comprehensive performance comparison encompassing both device-level and circuit-level aspects. The article is divided into five parts: The state of the art is given in Section I. Section II deals with NSFET, CombFET, and TreeFET structure, geometry, and physics incorporated for simulations. Section III discusses electrical performance as well as analog/RF performance.

Section IV explores the circuit level analysis and performance comparison. Finally, section V gives the conclusion of the paper.

II. DEVICE STRUCTURE AND SIMULATION METHODOLOGY

Figures 1(a), (b), and (c) illustrate the three-dimensional representations of NSFET, CombFET, and TreeFETs, respectively. According to IRDS predictions for sub-5-nanometer technology nodes, a gate length (L_G) of 16 nm and a spacer length of 8 nm are adopted [10], [16]. The width of the NSFET (NSW) is set at 10 nm, and for both CombFET and TreeFET, a consistent interbridge width (W_{IB}) of 5 nm is maintained. Additionally, the interbridge (IB) height (H_{IB}) is standardized at 30 nm for both CombFET and TreeFET configurations. A fixed OFF current (I_{OFF}) of 252 pA is maintained for NSFET, CombFET, and TreeFETs for fair comparison [10].

TABLE 1. Device parameters.

Device Parameter	NSFET	CombFET	TreeFET
Gate length (L_G)	16 nm	16 nm	16 nm
Nanosheet width (N_W)	15 nm	10 nm	15 nm
Nanosheet thickness (N_T)	5 nm	5 nm	5 nm
Width of Interbridge (W_{IB})	-	5 nm	5 nm
Height of Interbridge (H_{IB})	-	30 nm	30 nm
EOT	0.78 nm	0.78 nm	0.78 nm
Effective width (Weff)	80 nm	120 nm	140 nm
Spacer dielectric	Nitride	Nitride	Nitride
Length of spacer	8 nm	8 nm	8 nm
Source/drain doping	1×10^{20} cm^{-3}	1×10^{20} cm^{-3}	1×10^{20} cm^{-3}
Channel doping	1×10^{15} cm^{-3}	1×10^{15} cm^{-3}	1×10^{15} cm^{-3}
Gate work function	4.346 eV	4.367 eV	4.3765 eV

The source/drain doping concentration of 1×10^{20} cm^{-3} and channel doping of 1×10^{15} cm^{-3} are considered for NSFET, CombFET, and TreeFETs respectively. The metal gate height of 60 nm is considered. Also, to avoid gate oxide tunneling current the gate stack with a combination of SiO_2 of 0.5 nm and HfO_2 of 1.5 nm is considered. All the structures are built on silicon on insulator (SOI), called buried oxide (BOX) substrate, which consists of SiO_2 of 50 nm, placed below the channel to avoid substrate leakages.

Further, the effective width (W_{eff}) is calculated for each device as shown in Fig. 2. The performance investigation of NSFET, CombFET, and TreeFET is carried out by using Cogenda Visual TCAD [17]. Along with Poisson and carrier continuity equations, a self-consistently solved drift-diffusion transport model is incorporated. The effects of quantum confinement were taken into account by using the density-gradient model. The doping-dependent bandgap variations were modeled using the Slotboom bandgap narrowing model.

The low-field ballistic model was included to consider quasi-ballistic effects as the carriers flow in narrow channels. The mobility degradation effects are taken into account by incorporating Lombardi mobility, inversion, and accumulation layer mobility models due to phonon and Coloumb scatterings at the Si-SiO_2 interface. Moreover, the generation and recombination conditions of carriers are also activated in the continuity equation by the Shockley-Read-Hall recombination model. Fig. 3 depicts the comparison of I_D-V_{GS} characteristics of simulated and experimental data. The good match of simulation with experimental results shows that the physical models are able to capture the device's behavior in a real-time environment. Thus, the well calibrated physics used throughout the simulations. Further, the devices' dimensions are listed in Table 1.

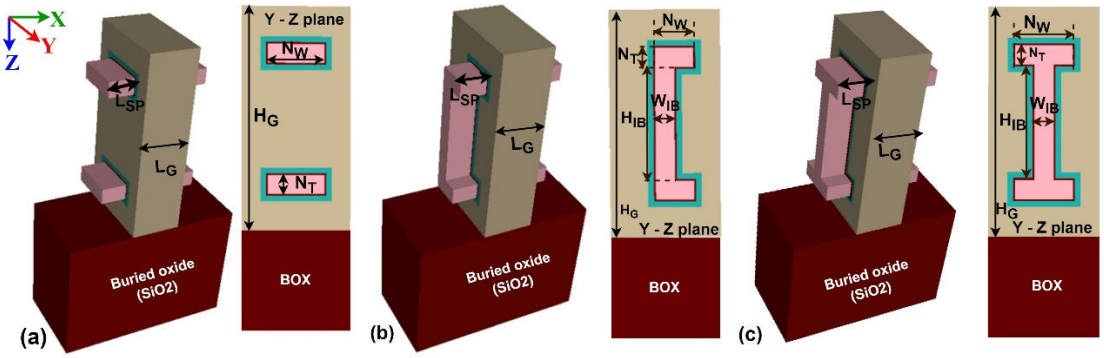

FIGURE 1. 3-D view and cross-sectional views of (a) NSFET, (b) CombFET and (c) TreeFET devices.

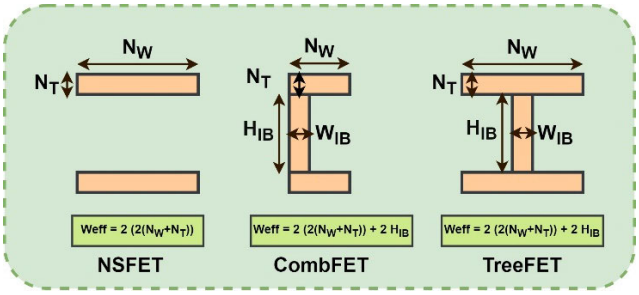

FIGURE 2. Effective width calculation of NSFET, CombFET and TreeFET.

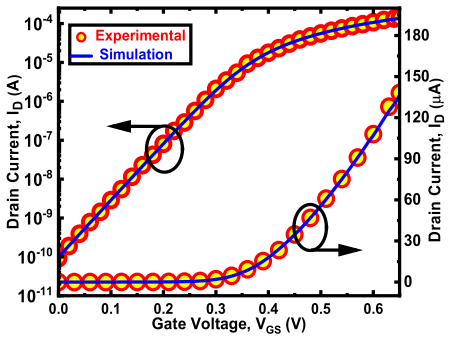

FIGURE 3. Calibration of TCAD simulation models with the experimental results of stacked GAA NS-FET [14], [15].

III. RESULTS AND DISCUSSION

Figure 4(a)-(c) depicts the I_D-V_{GS} characteristics of NSFET, CombFET, and TreeFET at both V_{DS} = 0.7 V and 0.04 V respectively. The transfer and output characteristics are taken at fixed I_{OFF} (V_{DS} = 0.7 V and V_{GS} = 0 V) of 252 pA to have a better comparison by adjusting the gate work function. Fig. 3 (d)-(f) depicts output characteristics from V_{GS} of 0.3 V to 0.7 V with a step of 0.1 V respectively. The I_D-V_{DS} characteristics show better saturation currents with CombFET and TreeFET compared to NSFET and ensure good analog and mixed domain applications. Fig 5(a) depicts the I_{ON} (V_{DS} = 0.7 V and V_{GS} = 0.7 V) for NSFET, CombFET, and TreeFET. The I_{ON} of 60 μA with NSFET, 85 μA with CombFET, and 102 μA with TreeFET is obtained as shown in Fig. 5(a). Compared to NSFET, the CombFET has 42.3% rise in I_{ON} and compared to combFET, the TreeFET has 9.28% rise in I_{ON}. The TreeFET exhibits higher I_{ON} compared to CombFET and NSFET, which is feasible for high performance (HP) applications. The tunneling area is linearly related to the effective width of the channel [18], due to which, the TreeFET exhibits the highest I_{ON}. The I_{ON}/I_{OFF} ratio of NSFET, CombFET, and TreeFET is demonstrated in Fig 5(b).

An increment of 43.5% and 10% in I_{ON}/I_{OFF} ratio is obtained from NSFET to CombFET and CombFET to TreeFET, respectively. The highest I_{ON}/I_{OFF} ensures TreeFET towards high speed logic applications. Fig 5(c) and (d) depict the drain induced barrier lowering (DIBL) and subthreshold swing (SS) performance of NSFET, CombFET, and TreeFET respectively. DIBL and SS are short channel performance metrics and lower values of both are preferred for optimum performance. The TreeFET and ComFET exhibits marginal increment in SS and DIBL compared to NSFET. Due to the trade-off between increased channel area and gate controllaility, higher values of SS are observed for CombFET and TreeFET device.In addition, the effect of sub-fin leakage is evidenced by quantum confinement and leads to the degradation of subthreshold features. This may be also attributed to the fact that the gate controllability in IB is from two sides only. Although the presence of IB increases I_{ON}, it also deteriorates subthreshold performance. The tradeoff exists between gate control capability and total tunneling area. Thus, a relevant study on IB dimensions towards performance is needed which will be presented in upcoming sections.

A. IMPACT OF INTERBRIDGE (IB) SCALING AND GATE LENGTH (L_G)

To investigate the impact of IB on novel Comb and TreeFET performance, various designs are simulated. Fig. 6 depicts the height and width of IB for Comb and TreeFETs by keeping other parameters constant. Fig 6(a) shows the width of IB (W_{IB}) on device performance. The TreeFET exhibits higher I_{ON} compared to CombFET for H_{IB} of 10 nm to 30 nm.

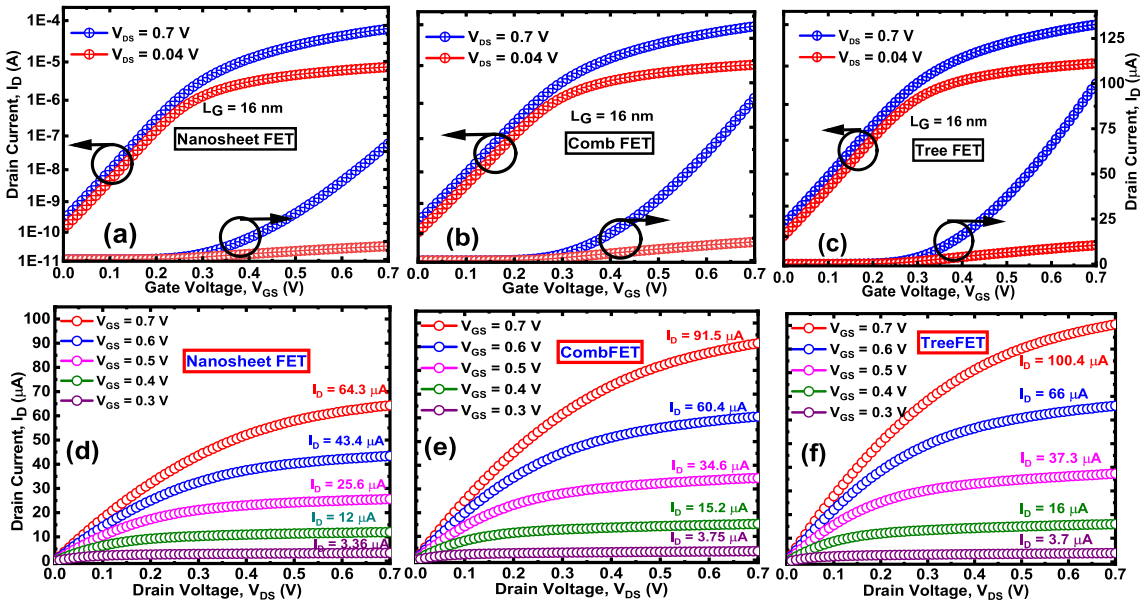

FIGURE 4. The I_D-V_{GS} (a,b and c), and I_D-V_{DS} (d,e and f) characteristics of NSFET, CombFET and TreeFET respectively.

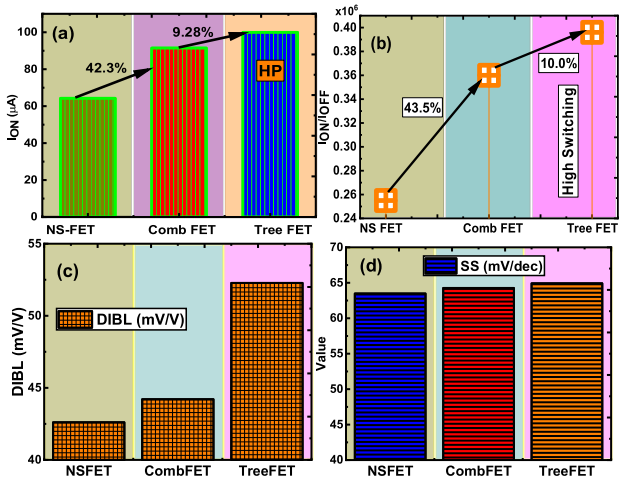

FIGURE 5. (a) I_{ON}, (b) I_{ON}/I_{OFF} (c) DIBL, and (d) SS of NSFET, CombFET, and TreeFET.

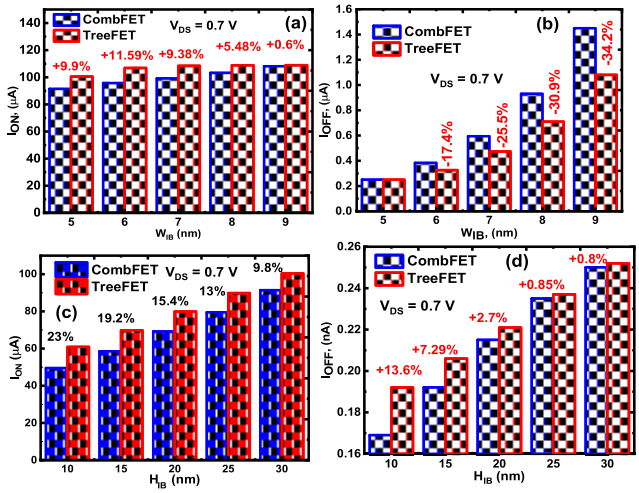

FIGURE 6. (a) I_{ON} and (b) I_{OFF} with variation in W_{IB}, and (c) I_{ON} and (d) I_{OFF} with variation in H_{IB} for TreeFET and CombFET.

This is attributed to the fact that TreeFET can offer a higher effective width for the channel compared to CombFET. The increment of 11.59% is noticed at H_{IB} of 6 nm. However, an increase in W_{IB} has less impact on I_{ON} with TreeFET i.e., only 0.6% rise at W_{IB} of 9 nm. Fig. 6(b) shows the effect of I_{OFF} on W_{IB}. The I_{OFF} is low for TreeFET compared to CombFET with the rise in W_{IB}. The increment of I_{OFF} for CombFET at higher W_{IB} rises by 34.2% compared to TreeFET. Fig. 6(c) depicts the I_{ON} with various H_{IB} for Comb and TreeFETs. The percentage of increment is higher at lower H_{IB} compared to higher. Fig. 6(d) depicts the I_{OFF} with various H_{IB}. The I_{OFF} is lower for CombFET compared to TreeFET. At lower H_{IB} the percentage of variation is high compared to higher H_{IB}. Further, the contour plots of the electric field and potential are shown in Fig. 7(a) and (b), respectively. Higher values of the electric field are noticed for TreeFET owing to more charge density [18]. In Fig. 8(a) the impact of scaling on the performance of NSFET, ComFET, and TreeFET is demonstrated. Fig. 8(a) depicts the I_{ON} variation with L_G scaling. The I_{ON} increases largely from NSFET to Comb and TreeFET due to larger W_{eff}/FP. The switching (I_{ON}/I_{OFF}) performance of three FETs is shown in Fig. 8(b). The I_{ON}/I_{OFF} performance is more for TreeFET compared to Comb and NSFET for all L_G. The V_{th} effect with scaling at $V_{DS} = V_{GS} = 0.7$ V is depicted in Fig. 8(d). The Tree and CombFET has more advantage towards V_{th} and ensure fundamental scaling compared to NSFET. The SS performance is better with NSFET compared to Comb and,

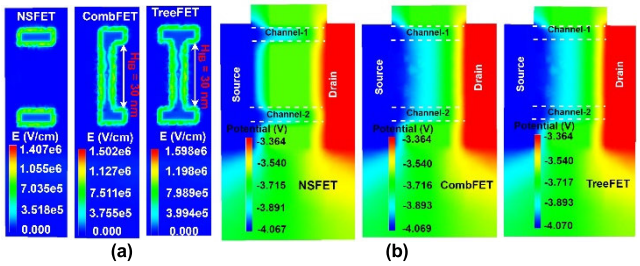

FIGURE 7. Contour plots for (a) electric field in Y-Z (b) potential in X-Z plane for NSFET and TreeFET with different H_{IB}.

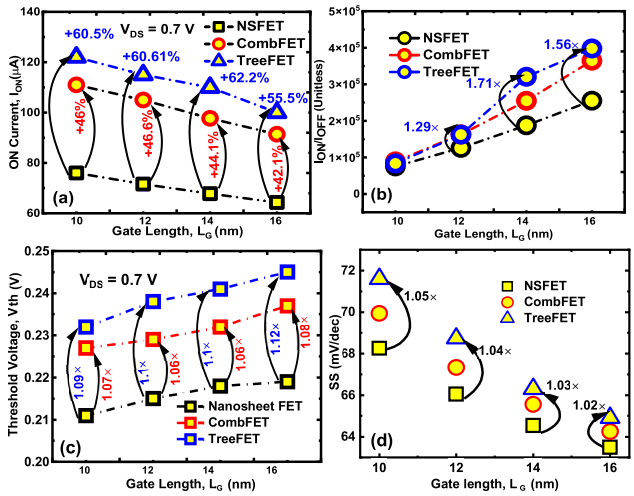

FIGURE 8. (a) I_{ON}, (b) I_{ON}/I_{OFF}, (c) V_{th} and (d) SS of NSFET, CombFET and TreeFET.

TreeFETs due to the tradeoff between gate controllability and channel area, i.e., the gate starts losing its control with increased width [18] (Fig 8(d)), thus ensuring low power applications.

B. IMPACT OF TEMPERATURE ON ELECTRICAL PERFORMANCE

In this sub-section, to observe the thermal stability, the temperature is varied and its impact on device performance is analyzed. The temperature is varied from 300 K to 420 K for NSFET, CombFET, and TreeFETs respectively. Fig 9(a) shows the impact of temperature I_{ON}. The I_{ON} decreases with a rise in temperature due to various phenomena like phonon and lattice scatterings [19]. A higher effective width tends to offer a higher current of the device due to a wider area for carriers to flow [20]. Compared to the NSFET and CombFET, the TreeFET exhibits larger I_{ON} due to its more effective width. The impact of temperature on NSFET, CombFET and TreeFET is marginal on I_{OFF} (300 K to 360 K). However, at higher temperatures, there is a significant impact on device performance. The TreeFET exhibits higher I_{OFF} due to more corners than CombFET and NSFET as shown in Fig. 9(b). Fig 9(c) exhibits the I_{ON}/I_{OFF} ratio of NSFET, CombFET and TreeFETs respectively. Although the NSFET exhibits better I_{OFF}, larger I_{ON} with Comb and TreeFET

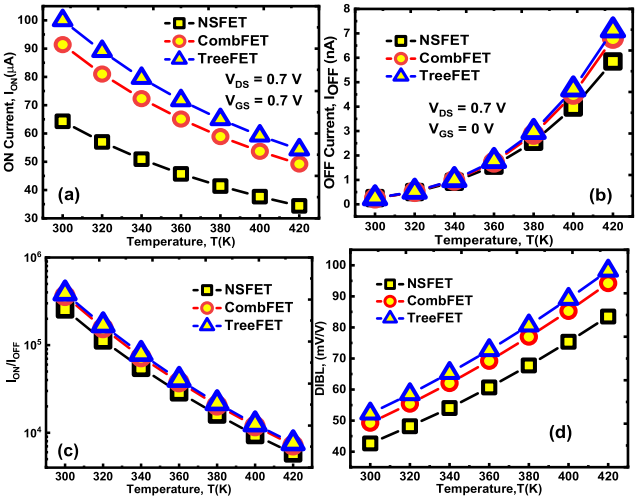

FIGURE 9. (a) I_{ON} (b) I_{OFF} (c) I_{ON}/I_{OFF} (d) DIBL of NSFET, CombFET and TreeFET.

dominates the I_{ON}/I_{OFF} ratio. However, a decrease in I_{ON} and increase in I_{OFF} with the rise in temperature leads to marginal impact on device I_{ON}/I_{OFF} ratio at higher temperatures. Figure 9(d) shows the DIBL performance of NSFET, CombFET, and TreeFET respectively. The DIBL increases with an increase in temperature. The NSFET exhibits better DIBL performance compared to CombFET and TreeFET.

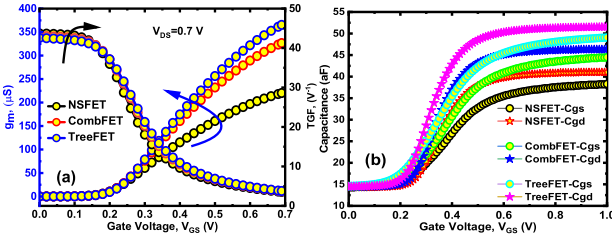

FIGURE 10. (a) Transconductance (g_m) and TGF (b) C_{gs} and C_{gd} of NSFET, CombFET and TreeFET.

C. ANALOG AND RF PERFORMANCE

In this sub-section, the analog/RF performance is demonstrated for NSFET, CombFET, and TreeFET. Fig. 10 shows the analog/RF performance of NSFET, Comb, and TreeFET at $V_{DS} = 0.7$ V respectively. From Fig 10(a) it is noticed that compared to NSFET, the Comb and TreeFET exhibit higher g_m. At high V_{GS}, the g_m value increases linearly. However, with higher V_{GS}, the g_m value peaks and continues to fall. A maximum g_m of 350 μS with TreeFET ensures higher cutoff frequency (f_T) and gain. Fig 10(b) depicts the variation of transconductance generation factor (TGF) for three FETs at a V_{DS} of 0.7 V. Devices with higher TGF can offer higher speed of operation [20]. The NSFET exhibits higher TGF at low V_{GS} compared to other FETs. However, at higher V_{GS} the TreeFET marginally dominates in TGF.

TABLE 2. Performance comparison of various device metrics.

Parameter	NSFET	CombFET	TreeFET
I_{ON} (μA)	64.3	91.5	100
DIBL (mV/V)	42.61	44.21	52.28
SS (mV/dec)	63.49	64.266	64.92
g_m (mS)	0.22	0.33	0.36
f_T (THz)	0.454	0.590	0.594
τ_P (ps)	0.84	0.675	0.674 nm

The total capacitance ($C_{gg} = C_{gs} + C_{gd}$) is the combination of gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) and is shown in Fig. 10(b) as a function of V_{GS}. This is driven by an increase in source originating charge in the channel region that causes the C_{gs} component to grow linearly. It is discovered that at low V_{GS}, C_{gd} declines and at high V_{GS} levels, it appears to be practically constant. This arises because the change in V_{GS} has less impact on the charge over the channel region for a given V_{DS}. The TreeFET has high C_{gs} and C_{gd} compared to CombFET due to the existence of more corners or intersections. However, the NSFET exhibits lower gate capacitance due to its structural advantage. The parasitic capacitance directly proportionally increases with the effective conduction area for TreeFET and CombFETs. Fig 11(a) shows the transconductance frequency product (TFP) and gain frequency product (GFP) of the NSFET, CombFET and TreeFET respectively. The TFP is a trade-off between bandwidth and power which signifies high speed applications. The TFP is higher for CombFET at mid V_{GS} and TreeFET exhibits a marginal rise at high V_{GS}. The CombFET exhibits higher TFP at $V_{GS} = 0.45$ V, however at higher V_{GS} the TreeFET exhibits a marginal increment in TFP. Higher TFP indicates better linearity of the device. Fig. 11(b) depicts the cut-off frequency (f_T) of NSFET, CombFET, and TreeFET at $V_{DS} = 0.7$ V respectively. The f_T increases with Comb and TreeFET compared to NSFET due to larger g_m. An increment of 1.3× compared to NSFET is noticed which ensures a promising device for RF applications at nano-regime.

High f_T values demonstrate that the performance of Comb and TreeFET is not constrained by external fringing parasitic capacitances. Fig. 11(c) shows the intrinsic delay (τ) of NSFET, CombFET, and TreeFET at $V_{DS} = 0.7$ V respectively. The τ is lower for Comb and TreeFET compared to NSFET due to lower Cgg. Lower τ ensures better digital switching applications. The gain bandwidth product (GBW), which is shown in Fig. 11(d) is an FOM that exhibits a trade-off between g_m and C_{gd}. Higher g_m benefits the circuit performance and higher C_{gd} increasescircuit delays. Although C_{gd} dominates in TreeFET and CombFETs, due to predominant g_m, both FETs outperform GBW compared to NSFET. Further, Table 2 gives various crucial performance metrics in tabular format.

IV. CIRCUIT LEVEL ANALYSIS OF NSFET, COMBFET AND TREEFET

In this section, the circuit performance comparison of NSFET, CombFET, and TreeFET is analyzed using the Cadence tool [21]. Initially, I_D-V_{GS}, and C-V characteristics are obtained from 3D TCAD.

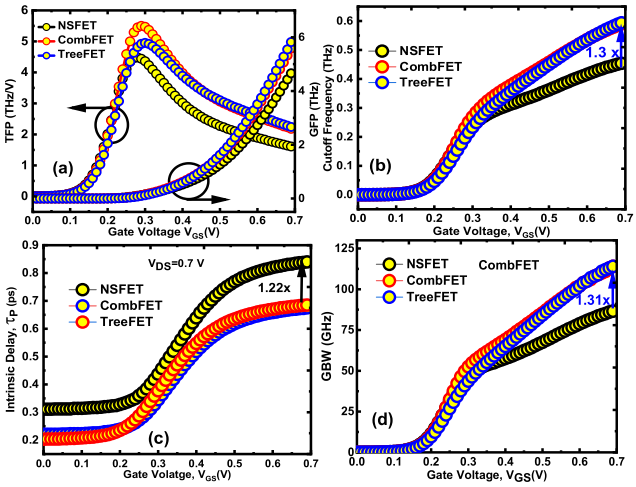

FIGURE 11. (a) TFP and GFP, (b) f_T, (c) T_P, and (d) GBW of NSFET, CombFET and TreeFET.

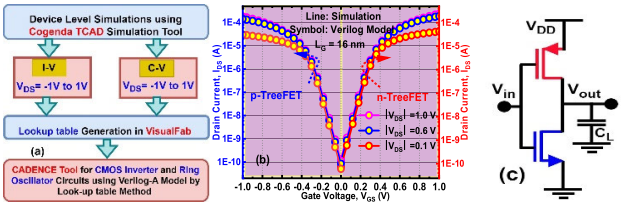

FIGURE 12. (a) Flowchart of the device to circuit with TCAD and CADENCE simulator, (b) Calibration of look-up-table based models with TCAD data for transfer characteristics at different V_{DS} for TreeFET (c) schematic of CMOS inverter.

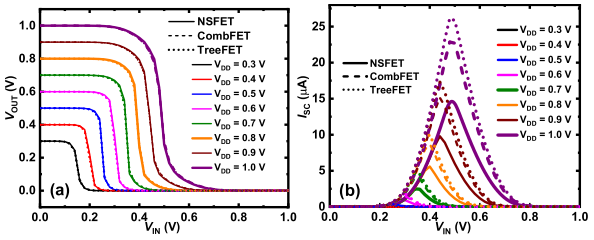

FIGURE 13. (a) Voltage transfer characteristics (VTC) (b) Switching characteristics of NSFET, Comb, and TreeFET with various V_{DD}.

A lookup-table based Verilog-A code is used to create symbols and those symbols are used in the Cadence platform for circuit simulation. The overall flow from TCAD to circuit level analysis is depicted in Fig. 12(a). The I_D-V_{GS} characteristics of TreeFET, which are obtained from the Cadence platform by Verilog-A interface is verified against the TCAD simulator at V_{DS} of 1 V, 0.3 V, and 0.1 V respectively as depicted in Fig 12(b). Fig 12(c) depicts the complementary metal oxide semiconductor (CMOS) inverter with input voltage (V_{IN}), output voltage (V_{OUT}), supply voltage (V_{DD}), output load capacitance (C_L), and ground (GND). The voltage transfer characteristics (VTC) of

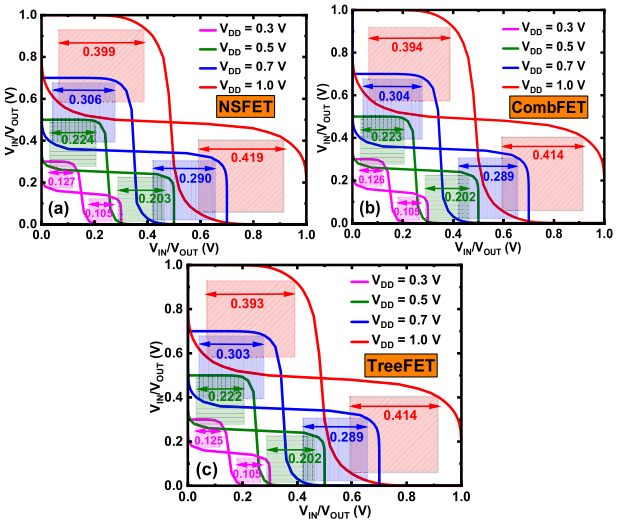

FIGURE 14. Noise margins (NMs) of (a) NSFET (b) CombFET and (c) TreeFET for various V_{DD}.

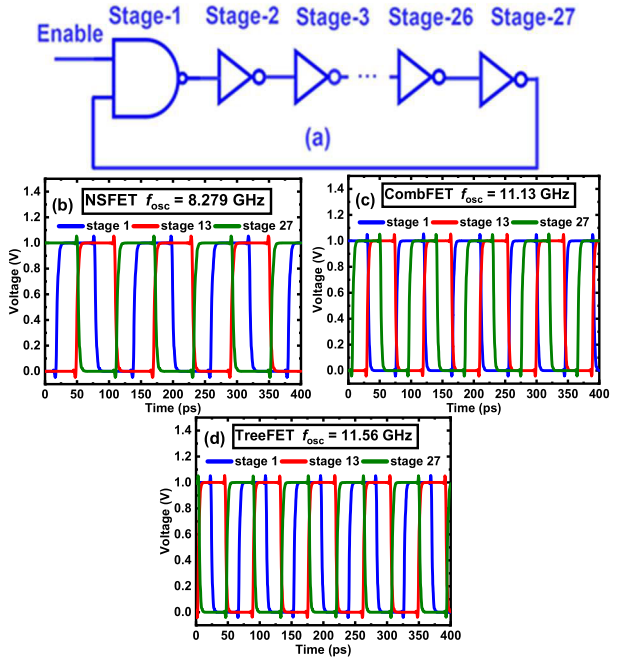

FIGURE 15. (a) 27-stage ring oscillator (RO), frequecny of oscillation (f_{OSC}) for (b) NSFET (c) CombFET (d) TreeFET respectively.

CMOS inverter with various V_{DD} for NSFET, CombFET, and TreeFET are shown in Fig 13(a). In addition, the switching current characteristics (I_{SC}) of CMOS inverter with various V_{DD} are depicted in Fig 13(b). The Tree and CombFET exhibits larger I_{SC} compared to NSFET due to higher I_{ON}. The butterfly curves of CMOS inverter based NSFET, Comb, and TreeFETs for various V_{DD} are shown in Fig 14. The signal noise margin (SNM) will be determined by the largest square fit in the butterfly curve. Higher NMs are exhibited by the NSFET followed by Comb and TreeFETs due to better short channel performance. At $V_{DD} = 1$ V, the NSFET, CombFET and TreeFET exhibit NM_L of 0.399 V, 0.394 V and 0.393 V whereas, the NM_H of 0.419 V, 0.414, and 0.414 respectively. Reduced V_{DD} decreases the NM levels for all three FETs. The 27-stage ring oscillator (RO) circuit performance is studied with NSFET, Comb and TreeFET at V_{DD} of 1 V and depicted in Fig.15. The NSFET, CombFET and TreeFET exhibit f_{OSC} of 8.279 GHz, 11.13 GHz and 11.56 GHz, respectively. The TreeFET exhibits the highest f_{OSC} compared to other FETs due to a higher drive current.

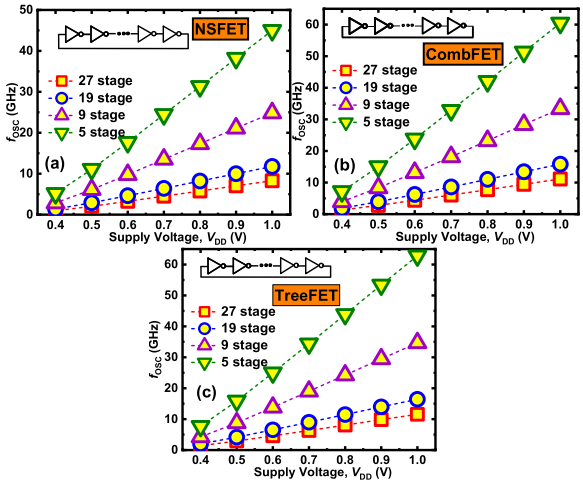

FIGURE 16. (a) Frequency of oscillation (f_{OSC}) of (a) NSFET (b) CombFET (c) TreeFET for various values of the number of stages (N) and V_{DD}.

Figure 16 depicts the ring oscillator (RO) [22] f_{OSC} performance of NSFET, CombFET, and TreeFET at various V_{DD} with 5 stages, 9 stages, 19 stages, and 27 stages. The f_{OSC} is increased with an increase in V_{DD} due to higher I_{ON}. Compared to NSFET and CombFET, the TreeFET exhibits higher f_{OSC} for all supply voltages. At lower V_{DD} the variation is marginal and at higher V_{DD} there is a significant variation in f_{OSC}. From the above analysis, it is observed that the TreeFET followed by CombFET exhibits better f_{OSC} which is suitable for driving high-speed circuit applications.

V. CONCLUSION

This article investigates the performance characteristics of NS, Comb, and TreeFET devices within advanced technology nodes. Introducing an additional interbridge (IB) between two channels leads to enhanced performance when compared to the performance of NSFETs. The outcome analysis underscores the potential of emerging FET designs like TreeFET and CombFET to facilitate essential scaling while improving DC, analog, and RF metrics. Furthermore, the proposed emerging FET architectures also exert notable influence on circuit performance. The study's temperature analysis across all FETs serves to establish their robustness over a wide temperature range.

Moreover, the subthreshold performance of CombFET and TreeFET exhibits a slight decline compared to the NS FET, although this can be fine-tuned by adjusting the width of the interbridge (IB). The incorporation of IBs significantly

impacts the switching current of CMOS inverters, with CombFET and TreeFET taking the lead. Demonstrating enhanced speed, the 5-stage ring oscillator featuring TreeFET achieves a notably higher operating frequency in comparison to CombFET and NSFET configurations. Thus, these emerging FETs can be employed in applications such as Neuromorphic computing, High frequency applications for optimum performance. Moreover, the modeling of these FETs can be considered a promising area for incorporating them in VLSI architecturesels.

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