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RESEARCH ARTICLE

An Adaptive Series-Dynamic-Resistor-Based Protection Scheme for Brushless Doubly-Fed Induction Generator Under Asymmetrical Fault Conditions

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ABSTRACT Low-voltage ride-through (LVRT) is one of the most important criteria for integrating wind energy into the power grid. Based on grid connection codes, wind generators must remain connected during fault conditions. However, this requires a careful protection scheme design for addressing the successful ride through of the brushless doubly fed induction generator (BDFIG) during severe voltage dips. This paper proposes a comprehensive solution for enhancing the BDFIG ride through during asymmetrical faults. Furthermore, since the proposed solution is dependent on the type and severity of voltage dips, an updated harmonic resilient scheme is developed to detect the dip level and type of faults. Performance of the proposed protection scheme is investigated for further improvement of the brushless DFIG LVRT capability based on series dynamic resistor (SDR) circuit design in order to limit post-fault oscillations. With the proposed solution, the BDFIG can satisfy ride through requirements for severe voltage dip scenarios. The proposed framework which includes a voltage detection method, appropriate SDR value determination procedure, and SDR control circuit was implemented and validated with a coupled circuit model in MATLAB/Simulink for a BDFIG prototype.

INDEX TERMS Brushless doubly fed induction generator, low voltage ride-through, series dynamic resistor, grid code, voltage dip detection.

I. INTRODUCTION

Offshore wind energy is considered as an environmentally friendly alternative for energy production due to less installation constraints and higher energy harvesting efficiency. Although doubly fed induction generator (DFIG) is the most common technology among the existing generators for wind energy applications [1], assessment of wind turbines for large scale offshore applications implies that generator reliability in onshore applications is not enough for offshore use [2]. Besides, according to IEEE 1547 standard [3], the generation facilities need to stay connected during the voltage dips (i.e., low voltage ride through (LVRT)) which poses another operating complexity to DFIGs [4]. Hence, the wind turbine design approach should be adjusted to tackle these issues. In this sense, the Brushless DFIG is particularly an attractive choice for offshore wind turbines since it has no brushed contact to the rotor, eliminating a common source of failures [5]. It is suggested in [6] that higher leakage inductance of BDFIG provides an effective limitation in control winding (CW)

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current amplitude which is beneficial in LVRT capability of the machine requiring further analysis for different prototype designs and parameters [7].

Thanks to the similar ride through behavior, DFIG ride through designs [8], [9] can be utilized for BDFIG LVRT with some modifications [10]. For example, performance of BDFIG was examined during severe symmetrical voltage dips without any extra hardware using a crowbarless control strategy [7], [11]. However, such methods not only increase the complexity of power electronic (PE) converter control, but also only offer adequate response under moderate voltage sags for symmetrical faults [12]. Thus, addressing a successful LVRT of BDFIGs during asymmetrical faults is an open problem. Besides, sensitivity analysis shows that the worst-case scenario for fault ride through (FRT) assessment of BDFIG is phase to phase voltage dip [13]. This is because the negative sequence of electromotive force (EMF) plays an important role in equivalent model of the machine, whereas such presumption will lead to unacceptable LVRT performance [12]. Therefore, modifying controller is not a well generalized solution for BDFIG LVRT under asymmetrical voltage dips. As a result, researchers should still rely on optimized innovative solutions based on hardware based protective circuits.

A. SUMMARY OF MAJOR CONTRIBUTIONS

In this paper, our proposed approach offers an effective solution to enhance the BDFIG ride-through capability during asymmetrical faults. This enhancement is achieved through the design of an adaptive multi-step SDR circuit where appropriate resistance values are determined to reduce post-fault oscillations and provide enhanced controllability over the machine's operation. The proposed framework also meets the reactive power injection and machine controllability requirements specified in the updated grid code requirements. Additionally, it effectively limits the peak values of the control winding, power electronic converter inrush current, and the BDFIG's transient response during the occurrence and clearance of asymmetrical voltage dips which occurs due to zero and negative sequence components. The main contributions of this paper are summarized as follows:

- We introduce an adaptive SDR protection circuit which is designed analytically based on the BDFIG's equivalent circuit model. By leveraging a multi-step SDR circuit and the distinctive design of the BDFIG with higher leakage inductance, our approach accurately controls converter current and mitigates post-fault oscillations. Besides, this scheme requires no coordination with additional protection circuits or alterations in the machine control.
- A modified voltage dip detection scheme is integrated into the proposed protection scheme to identify the type and severity of the voltage dip with a fast response time for effective generator ride-through. Specifically, the proposed modifications are applied to the existing Goertzel method to detect voltage dips in less than half a cycle by leveraging both phase voltage magnitudes (e.g., R or S or T) and angle value. The modified procedure is robust against power quality issues in the grid, proving to be an important asset for the ride-through enhancement scheme.
- Efficient activation and deactivation procedures are proposed for the multi-step SDR protection circuit. These procedures were inspired by the fact that the different fault scenarios require different resistance values in the SDR circuit. The proposed adaptive procedure adjusts the resistance values to the type and severity of the faults. Simulation results corroborate the effectiveness of the proposed solution by ensuring acceptable LVRT across all voltage dip scenarios and effectively limiting post-fault oscillations while enhancing machine controllability.

B. RELATED WORKS

Existing studies [7], [11], [15], [16], [17], [18], [19] have investigated the ride through capability of BDFIGs during symmetrical faults. However, asymmetrical ride through poses a more important and challenging problem, attributed to the zero and negative sequence components of EMF. There are a few works in the literature which have focused on the asymmetrical fault ride through capability of BDFIG [12], [13], [20]. However, these studies lack a viable solution for limiting the CW inrush current and controlling machine's transient response [12]. Additionally, they fail to ensure a successful ride through for severe voltage dips where the CW current peak exceeds its permissible limit for high pre-fault speed [13], [17]. An effective method for determining the appropriate crowbar resistance value is proposed in [13] to enhance the ride through capability of the BDFIG during asymmetrical voltage dip scenarios. However, while the control circuit is bypassed upon crowbar activation [8], this approach might not align with stringent grid codes, as it requires reactive power injection [3]. Overall, developing a reliable protection scheme considering the associated constraints (e.g., transient currents) to meet the grid code requirements for the asymmetrical ride-through capability of BDFIGs remains unexplored in the existing literature [12], [13], [21].

The SDR-based protection implemented for DFIG LVRT in [22], [23], and [24] aims to maintain the machine's controllability during different fault conditions. However, a primary challenge with the SDR circuits is the occurrence of transients in machine behavior upon fault clearance [25]. Therefore, modifications to the machine's controller are needed [26]. Some studies have proposed combining the SDR protection circuit with either crowbar protection [27] or DC chopper [28] to address this issue in the asymmetrical fault ride-through of DFIGs. Nevertheless, these solutions may reduce the system reliability due to their topology and potentially increase the operational cost. The utilization of an SDR circuit to enhance symmetrical BDFIG LVRT is discussed in [21]. However, it lacks the capability to limit post-fault transients in the

machine during severe asymmetrical voltage dips. Hence, it is of paramount importance to design an efficient protection scheme to limit the CW current and post-fault oscillations during asymmetrical faults.

Moreover, it is important to identify the type and severity of the voltage dip for effective generator ride-through before activating and adjusting the LVRT protection system. Incorporating a voltage dip detection method into the machine's LVRT capability is essential. Existing literature lacks an efficient voltage dip detection method that aligns with LVRT schemes. While digital signal processing methods have been extensively explored for signal analysis across various applications, the Goertzel algorithm stands out for its simplicity and speed in evaluating signal characteristics with minimal computations, making it promising for power system applications [28], [29]. However, the Goertzel's voltage dip detection scheme [14] fails to respond quickly enough for LVRT conditions. As the current in the control winding and converter may exceed the maximum tolerable threshold immediately after a voltage dip, failing to quickly detect the voltage dips can lead to serious safety issues. Moreover, previous studies [30] solely monitor voltage sag magnitude which in turn can reduce the detection accuracy of the detection algorithm. Hence, there is an urgent need to design a ride-through scheme that synchronizes the protection circuit with a suitable voltage detection algorithm while detecting the voltage dips in a timely manner.

In section II, a dynamic model for LVRT is provided, section III introduces an improved ride through scheme. Finally, in section IV the proposed methodology, including voltage detection method, appropriate SDR value determination and control of SDR circuit was implemented and validated by simulation in MATLAB with experimentally verified coupled circuit model of the BDFIG prototype.

II. ANALYSIS OF THE BDFIG LVRT CAPABILITY

A. ASYMMETRICAL LVRT MODEL OF BRUSHLESS DFIG

BDFIG consists of two stator windings cross-coupled through a special rotor structure. The power-winding is directly connected to the grid and the control-winding is connected to the PE converter [31]. The machine side converter (MSC) is connected to the CW, controlling the CW current and the grid side converter (GSC) controls the oscillations of dc-link voltage. Higher cross coupling and magnetizing inductances may be in favor of BDFIM designers. However, it is obvious that higher magnetizing inductances and lower rotor leakage inductances may lead to higher CW currents, which may damage the power electronics converter [6].

The asymmetrical LVRT capability of the Brushless DFIG can be analyzed from generalized symmetrical component theory [32]. All asymmetrical voltages can be decomposed into three symmetrical voltages. Each component causes a corresponding power winding (PW) flux. The PW flux cannot change immediately, according to the principle of constant flux linkage. The zero-sequence component of PW flux called as frozen or neutral flux is presented for any asymmetrical faults in [12]. Based on (1) and (2), three PW fluxes induce three EMFs in the CW is calculated by:

$$E_2 = E_{2,p} + E_{2,z} + E_{2,z} \tag{1}$$

where:

$$E_{2,p} = \frac{M_{1r}\,M_{2r}}{L_1\,L_r - M_{1r}^2}\left[\frac{R_1\,L_r}{L_1\,L_r - M_{1r}^2} - j\,(N_r\,\omega_r - \omega_1)\right]\left(v_{1p}/\omega_1\right)$$

$$E_{2,n} = \frac{M_{1r}\,M_{2r}}{L_1\,L_r - M_{1r}^2}\left[\frac{R_1\,L_r}{L_1\,L_r - M_{1r}^2} - j\,(N_r\,\omega_r + \omega_1)\right]\left(v_{1n}/-\omega_1\right)$$

$$E_{2,z} = \frac{M_{1r}\,M_{2r}}{L_1\,L_r - M_{1r}^2}\left[\frac{R_1\,L_r}{L_1\,L_r - M_{1r}^2} - j\,(N_r\,\omega_r)\right]\overrightarrow{\lambda}_{1,z}(t_0^+)e^{j\,N_r\,\omega_r\,t}\,e^{-\sigma t} \tag{2}$$

where p, n, z are subscripts related to positive, negative and zero sequences, and 1,2 are superscripts representing PW, CW reference frames, respectively. Also, M_{1r}, M_{2r} are mutual inductance between rotor and PW, CW, respectively. In [33] two axis model of the Brushless DFIG was acquired. As shown in [12], by neglecting the PW resistance machine dynamics during voltage dips in the stationary p_2 pole pairs reference frame can be expressed by (3). Note that the term $R_1L_r/(L_1L_r - M_{1r}^2)$ is negligible in comparison with $N_r w_r$ based on the machine's parameter values [19]. Therefore, the BDFIG equivalent circuit is achieved as presented in Figure 1.

As shown in Figure 1, transient resistance of the CW and their time constants are different in the three sequences. Where N and p represent the number of nested loops and pole pairs of BDFIG, respectively. Also, σ is damping coefficient of PW flux.

$$\begin{aligned} v_2 &= \left(v_{2,p}\right) + \left(v_{2,N}\right) + \left(v_{2,z}\right) \\ &= \begin{pmatrix} R_2 i_2 + j(\omega_1 - N_r\omega_r)L_2' i_2 + L_2'\left(di_2/dt\right) \\ -\dfrac{j(\omega_1 - N_r\omega_r)}{j\omega_1 + \left(R_1L_r/L_1L_r - M_{1r}^2\right)}\dfrac{M_{1r}M_{2r}}{L_1L_r - M_{1r}^2}v_{1p} \\ j(\omega_1 - N_r\omega_r)\dfrac{M_{1r}M_{2r}}{L_1L_r - M_{1r}^2}R_1\dfrac{M_{1r}M_{2r}}{L_1L_r - M_{1r}^2}i_2 \\ + \dfrac{}{j\omega_1 + \left(R_1L_r/L_1L_r - M_{1r}^2\right)} \end{pmatrix} \\ &\quad + \begin{pmatrix} R_2 i_2 + j(-\omega_1 - N_r\omega_r)L_2' i_2 \\ -\left(j(-\omega_1 - N_r\omega_r)/-\omega_1\right) \\ \left(M_{1r}M_{2r}/L_1L_r - M_{1r}^2\right)v_{1,n} \\ + \left(j(\omega_1 + N_r\omega_r)/\omega_1\right)\left(M_{1r}M_{2r}/L_1L_r - M_{1r}^2\right)^2 R_1 \end{pmatrix} \\ &\quad + \begin{pmatrix} \left[R_2 + R_1\left(\dfrac{M_{1r}\,M_{2r}}{L_1\,L_r - M_{1r}^2}\right)^2\right] i_2 + L_2'\left(di_2/dt\right) \\ + \left(\dfrac{R_1\,L_r}{L_1\,L_r - M_{1r}^2} - j\,N_r\,\omega_r\right) \\ \dfrac{v_{1-0} - v_{1,p}(t_0^+) + v_{1,n}(t_0^+)}{\omega_1}\,e^{j(N_r\,\omega_r)t}\,e^{-\sigma t} \end{pmatrix} \\ L_2' &= L_2 - \left(L_1 M_{2r}^2 \Big/ L_1L_r - M_{1r}^2\right) \end{aligned} \tag{3}$$

Therefore, negative components have the largest time constant. As described in [13], the CW currents can be stated by equation (4):

$$I_2 = k_1 e^{-(R_2'/L_2')t} + k_2 e^{j(N_r\,\omega_r - \omega_1)t} + k_3 e^{j(N_r\,\omega_r + \omega_1)t} + k_4 e^{j(N_r\,\omega_r)t} e^{-\sigma t} \quad (4)$$

Note that the CW current plays an important role in design procedure of the protection circuit as it prevents any damage to the PE converter during disconnection of generator from the grid by effectively limiting large currents and high transient values due to voltage dips.

III. THE BDFIG LVRT CAPABILITY ENHANCEMENT

A. THE EFFICIENT ADAPTIVE RIDE-THROUGH SCHEME

The SDR is activated upon fault detection by monitoring CW current. The SDR activation occurs when the default threshold value of CW current is violated. In the case of sever asymmetrical faults with high negative and zero sequence components, higher values of SDR are required; however, such large SDRs can lead to high transients, PW overvoltage, and higher conducting losses. In such cases, variable multi step SDRs was previously presented for the DFIG, which contains multiple series resistors with isolated IGBT switches [24]. The steps are not extracted simultaneously but deactivated in a pre-determined time interval to reduce transients.

Furthermore, it was shown in [34] that for symmetrical faults, SDR placement in series with the generator terminal, as shown in Figure 2, not only limits the converter current, but also provides satisfactory reactive power for the grid code. In this Figure R_{s1}, R_{s2} and R_{s3} are resistance values of SDR steps.

Figure 3 shows the proposed protection scheme for successful LVRT operation of BDFIG. Note that as the maximum instantaneous value of CW current occurs right after voltage dips, the SDR must be activated as quick as possible. In this sense, a fast voltage dip detection method (i.e., less than half a cycle) is needed for controlling the machine in FRT mode.

In the initial stage, measurements of terminal voltage and converter current are collected. Upon detecting a voltage dip, the protection circuit triggers the activation procedure of the SDR circuit when the converter current exceeds 1.8 pu. Considering that the magnitude of CW current correlates with the type of voltage dips, the suitable resistance value for the protection circuit is derived from a pre-study analysis including various types of voltage dips, specifically for a maximum rotor speed of 650 rpm. To avoid post-fault transients during protection circuit deactivation, SDR values need to be selected carefully to strike a balance between machines transients occurring at the time of fault and during fault clearance. Upon recognizing fault clearance, the multi-step SDR goes through the deactivation procedure outlined in Figure 4. This procedural approach helps to determine and incorporate appropriate SDR values into the protection circuit to mitigate the post-fault transients effectively. Consequently, this

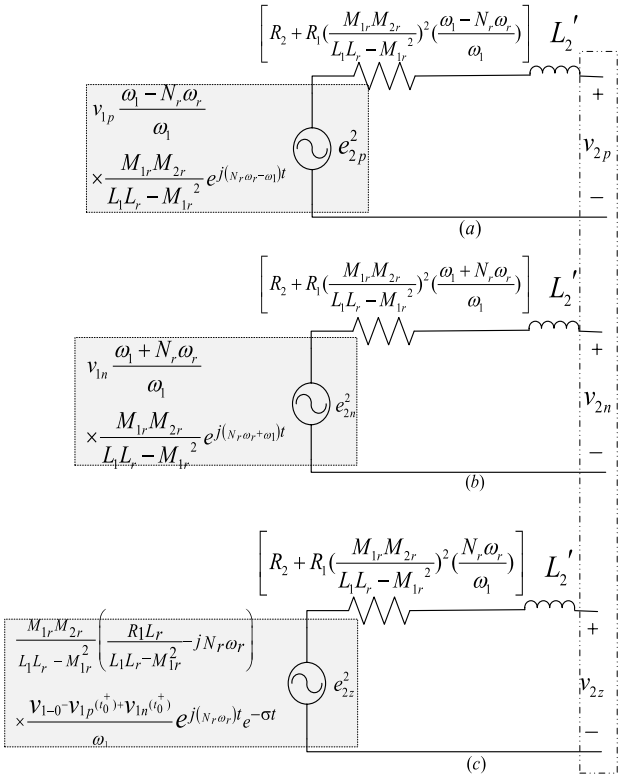

FIGURE 1. F Dynamic model of Brushless DFIG for positive (a), negative (b) and zero (c) sequence components [12].

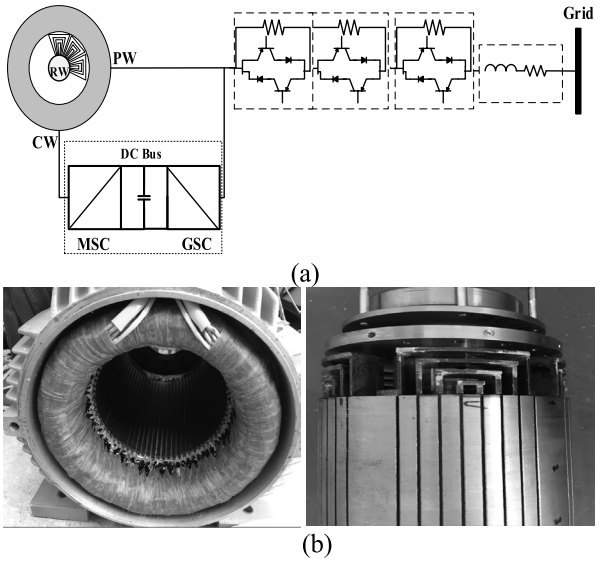

FIGURE 2. (a). BDFIG system with the proposed variable SDR, (b). A D-180 prototype.

method ensures BDFIG's low voltage ride-through capability, even under the most severe scenarios of voltage dips and at maximum rotor speed.

Figure 4 shows the activation and deactivation procedures of the SDR circuit. It is shown that a suitable SDR value is selected and inserted to the circuit depending on the type and severity of voltage dips. Correspondingly, 200*ms* after fault

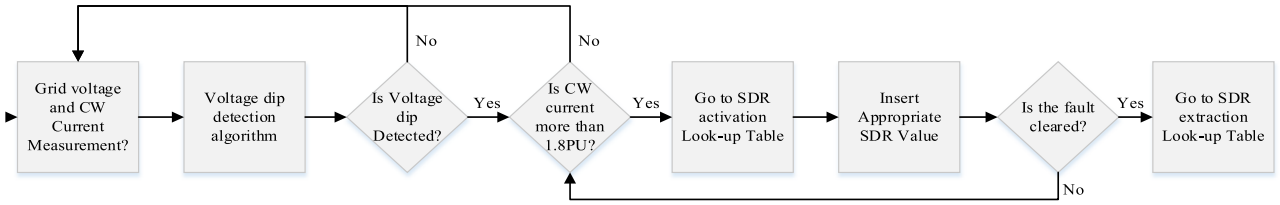

FIGURE 3. Proposed framework for successful LVRT operation of BDFIG.

clearance, the connected SDR steps should be deactivated according to the resistance values. This requires developing a fast voltage dip detection algorithm.

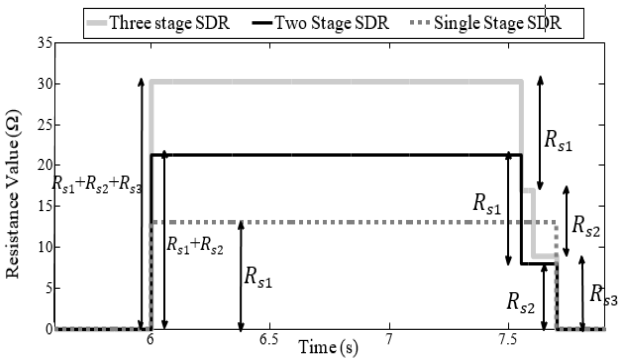

FIGURE 4. Control procedure for activation and deactivation of SDR.

B. VOLTAGE DETECTION METHOD

In this paper, we modify the Goertzel's voltage dip detection scheme by leveraging Z-transform [14]. The original expression between output and input is defined in Z-transform as follows:

$$y_k(z) = X(z)\frac{1 - e^{-j\frac{2\pi k}{M}}z^{-1}}{1 - 2\cos\left(\frac{2\pi k}{M}\right)z^{-1} + z^{-2}} \tag{5}$$

In this equation, $y_k(z)$ is the output of kth sample in z transform. X(z) is the input (discrete data) and M is the number of samples in a period of signal. In order to implement the method in Z-transform, a middle stage is defined as Q as follows:

$$Q_m = x(m) + 2\cos\left(\frac{2\pi k}{M}\right)Q_{m-1} - Q_{m-2} \tag{6}$$

Based on (5) and (6), a simpler calculation of output y_k can be obtained as

$$y_k(m) = Q_m - Q_{m-1}e^{-j\frac{2\pi}{M}k} \tag{7}$$

Note that (7) requires complete cycle data while the voltage dip for the fault ride through application should be detected in half a cycle. Therefore, the equations above should be modified to detect voltage dip in less than half a cycle. In this sense, by taking advantage of the symmetric property in a sinusoidal wave, a complete sinusoidal wave with a half cycle can be built by leveraging

$$M = 2n \tag{8}$$

Note that n is the number of samples in a half cycle. By replacing (8) in (5), modified Goertzel is derived as

$$y_k(z) = X(z)\frac{(1 - e^{-j\frac{2\pi k}{2n}}z^{-1})}{1 - 2\cos(\frac{2\pi}{2n}k)z^{-1} + z^{-2}} \tag{9}$$

Figure 5 shows the Z-Transform Block diagram of modified Goertzel method. It is shown that the feedback-loop is repeated n times while the final step to calculate the output is done once at the end of the iterations for each output. Therefore, this approach does not need extensive complex calculations. To detect the severity and type of voltage dips, the phase shift and amplitude of output (y_k) must be determined. For symmetrical voltage dips, phase shift for all three phases remains constant during voltage dips. However, Ph-Ph voltage dips have phase shift during voltage dips. Therefore, phase of output (y_k) together with its amplitude is used for detection of the voltage dip.

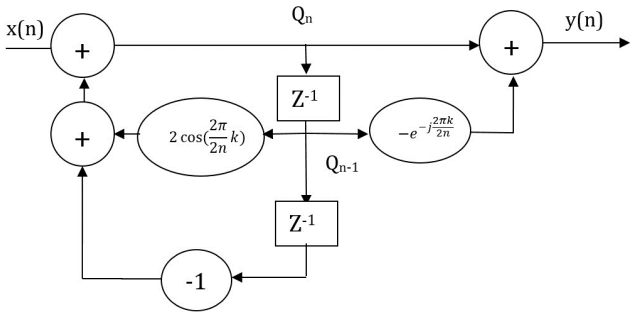

FIGURE 5. Z- Transform block diagram of modified Goertzel method.

C. SDR VALUES FOR LVRT CONDITION

Combining feed-forward control with SDR circuit can provide an acceptable solution for symmetrical low voltage ride through of BDFIG [19]. However, such methods cannot fulfill grid code requirements due to high transient current amplitudes and power oscillations during severe asymmetrical faults [34]. Therefore, an appropriate scheme should be utilized to determine the SDR value to ensure the safe and reliable operation of the system during asymmetrical faults.

The SDR consists of three-phase resistors with bipolar IGBT switches, which are inactive during normal conditions. Since voltage dip detection is an inseparable part of LVRT

solution, a fast and harmonic resilient method is leveraged to detect voltage dip characteristics and obtain the appropriate protection circuit. Such resistors are connected in series with the generator windings upon voltage dip detection to limit the CW transient by introducing high impedance into the circuit. Moreover, it can be realized from dynamic model of the BDFIG that the higher SDR values lead to the lower amplitude of the CW current and the faster damping.

In contrast, leveraging high values of SDR may result in high transient values in the deactivation procedure. Therefore, there exists a trade off in determining suitable values for SDR. Based on equation (4), the CW current can be described as a summation of four components. However, due to fast damping of the first term, it can be neglected [13]. Thus, if the latter three terms have simultaneous peaks, the maximum amplitude of CW current is achieved. Note that CW current is the main constraint for determining the SDR values. Specifically, the minimum SDR values must maintain the CW current less than the maximum instantaneous current tolerable by the converter, which is determined by (10).

$$\left\{ \begin{array}{c} \dfrac{\max\left\{E_{2,p}\right\}}{\sqrt{\left(R'_{2,p}+R_{SDR}\right)^2+\left(L'_2\right)^2\left(\omega_1-N_r\,\omega_r\right)^2}} \\ +\dfrac{\max\left\{E_{2,n}\right\}}{\sqrt{\left(R'_{2,n}+R_{SDR}\right)^2+\left(L'_2\right)^2\left(\omega_1+N_r\,\omega_r\right)^2}} \\ +\dfrac{\max\left\{\left\{E_{2,z}\right\}\right\}}{\sqrt{\left(R'_{2,z}+R_{SDR}\right)^2+\left(L'_2\right)^2\left(N_r\,\omega_r\right)^2}} \end{array} \right\} \leq i_{2\max}, \tag{10}$$

where R'_2, L'_2 are transient resistance and inductance of CW, respectively. It should be noted that maximum EMF values and CW transient resistance depend on the rotor speed of the generator, and fault's type and severity [12].

As per the converter manufacturer's specifications, the peak current of CW should never surpass the maximum permissible value of the switches current. During transient analysis, the power electronic converter's current must remain below a threshold for 200ms [6]. In the proposed scheme, this post-fault oscillation time (i.e., 200ms) is subdivided into 4 quarters (i.e., 50ms each). Consequently, four different values for the resistance of the protection circuit are deactivated sequentially within these 50ms intervals. For one phase to ground and moderate Ph-Ph-G faults, R_{S1} is used which is determined using (10) for Ph-G voltage dips. Similarly, for severe Ph-Ph-G and moderate Ph-Ph voltage dips, $R_{s1} + R_{s2}$ is used in the circuit 10 ms after fault appearance. These two resistors are active 50 ms after fault clearance in which the larger resistance (R_{s1}) is removed and 100 ms later, R_{s2} is removed to avoid high transient oscillations, as well as limiting CW current. Finaly, three stage resistors with unequal step sizes is inserted after severe Ph-Ph voltage dips occurrence. Accordingly, the resistors are removed within 200 ms from the highest to the lowest value. The choice of selecting one, two or three step SDR, and the corresponding resistance values is determined by calculating maximum instantaneous value of the CW current.

IV. RESULTS AND DISCUSSION

A. SIMULATION SETUP

Coupled circuit model was experimentally developed in [35] and verified as a powerful tool for studying dynamic behavior of the BDFIG [11], [19]. We consider the proposed model in [20] as an acceptable benchmark for assessment of the Brushless DFIG dynamic performance and verifying analytical studies for asymmetrical voltage dips. The specification of the BDFIG prototype is given in Table 1. To ensure the functionality of the proposed protection framework, it is necessary to assess ride through capability for different fault scenarios. The 1.5s fault is simulated on the terminal of power winding at $t = 6s$. The input torque was $50 - Nm$ and power factor is equal to 0.8.

TABLE 1. BDFIG prototype specification [12].

Parameter	Value	Parameter	Value
frame size	D 180	L_1	0.3498 H
p_1	2	L_2	0.3637 H
p_2	4	L_r	0.044521 mH
N_r	6	M_{1r}	0.0031 H
PW rated voltage	240 V	M_{2r}	0.0022 H
CW rated voltage	240 V	R_1	2.3 Ω
PW rated current	8 A	R_2	4 Ω
CW rated current	8 A	J	0.53 kgm^2
f_1	50 Hz	B	0.036 Nms

B. VOLTAGE DIP DETECTION

Figure 6 shows the response of our proposed voltage dip detection scheme. Specifically, a 95% Ph-Ph voltage dip occurring at $t = 6s$ for a 1.5s period is simulated to evaluate the performance of the proposed scheme for LVRT condition. The adaptive SDR circuit inserts different steps of resistances based on the severity of voltage dip. Furthermore, the phase shift between three phases must also determine types of different voltage dips. Figure 6.a and Figure 6.b show the amplitude and phase angle of three phase's voltages, respectively. The voltage dip severity and phase angle can be detected in less than half a cycle.

Harmonics originate from nonlinear sources such as PV inverters and nonlinear loads like rectifiers. While harmonic frequencies are not limited to certain orders, previous studies indicate the occurrence of some specific harmonic orders within power systems [36]. Notably, the 5th and 7th harmonics significantly contribute to the overall harmonic contents generated by inverters. These particular harmonic orders have been also highlighted as significant contributors in the power quality analysis report [37]. Therefore, it is important to investigate the effect of these harmonics on the performance

of the proposed scheme. Moreover, the performance of the detection method in presence of 25% of the 5th harmonic (250 Hz) and 25% of 7th harmonic is shown in Figure 6.c and Figure 6.d, respectively.

The results indicate effectiveness of the proposed voltage dip detection method for a severe (95% depth in terminal voltage) Ph-Ph voltage dip for a 1.5s period in presence of harmonics. Note that small fluctuations in the output are cleared shortly. Therefore, unlike the available methods such as *dq* and peak methods [38] which do not work properly under unbalanced voltage dips in presence of harmonics, our proposed detection scheme is resilient to these issues.

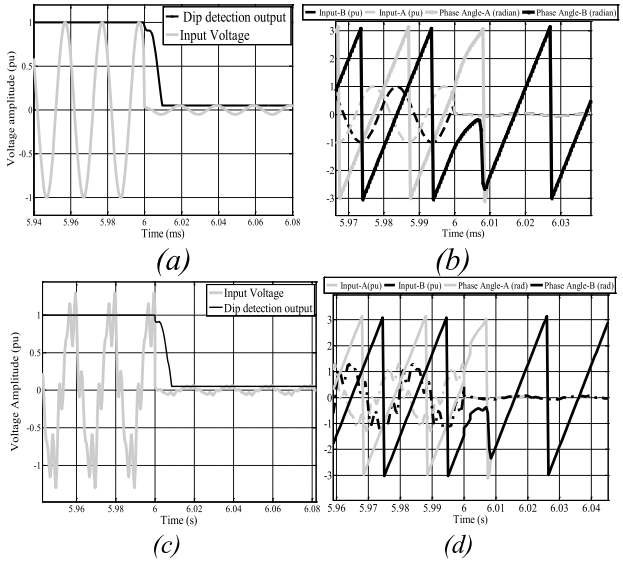

FIGURE 6. Results for the response of proposed dip detection algorithm (a) Amplitude detection, (b). Phase angle detection in normal condition and (c) Amplitude detection, (d). Phase angle detection in presence of 25% of the 5th harmonic (250 Hz) and 25% of 7th harmonic.

C. ANALYSIS OF SDR CIRCUIT FOR ASYMMETRICAL LOW VOLTAGE RIDE-THROUGH

The protective circuit of SDR includes a set of series resistances which are controlled by parallel switches. Therefore, depending on the voltage dip type and severity, their effective resistance may be controlled. Moreover, to limit transients during and after voltage dips for any pre-fault speed, the proposed adaptive scheme is leveraged for a voltage dip at maximum rotor speed of 650 rpm. This protects converter switches in the case of any LVRT scenario.

The determination of SDR values for activation and deactivation procedures requires comprehensive pre-studies involving various voltage dip scenarios. The idea of SDR control procedure comes from the fact that various voltage dips require considerably different values of resistance. The SDR value should be sufficiently high to limit the CW and converter current during the fault, yet low enough to effectively minimize fault clearance time in the post-fault period. The most critical scenario for the LVRT problem occurs during Ph-Ph voltage dip, where the highest SDR values are required. However, empirical data reveals the most common grid fault type is Ph-G voltage dip, requiring the lowest SDR value. Therefore, an adaptive LVRT solution that leverages different resistance values could enhance system efficiency by limiting CW transient currents. Hence, using (3) and (10), the required SDR values for Ph-G, Ph-Ph-G, and 100% Ph-Ph voltage dips for maximum pre-fault speed are obtained as 13.52Ω, 21.66Ω and 30.68 Ω, respectively. Therefore, resistance values for steps of the proposed SDR are 13.5 Ω, 8.2 Ω and 9.1 Ω for R_{s1}, R_{s2} and R_{s3}, respectively. The calculated values of the required SDR for various voltage dips are shown in Table 2.

Note that it is not necessary to implement high SDR values for Ph-G faults or moderate Ph-Ph voltage dips. Performance of the proposed scheme in limiting CW maximum current is shown in Figure 7. It is argued that by inserting a well-designed SDR in less than half a cycle for any pre-fault rotor speed (up to 650 rpm) and for any voltage dip level, the CW current remains below its limit. The SDR remained connected for 200*ms* after voltage recovery to avoid high current transients. Furthermore, Table 2 shows that for Ph-G and moderate Ph-Ph-G voltage dips (up to 80 %), a one-step SDR with small resistance value satisfies LVRT requirements.

TABLE 2. Required SDR value for various types and levels of voltage DIPS (Ω).

P (%)	Ph-G		Ph-Ph-G		Ph-Ph	
50	-	-	-	-	6.3	R_{s2}
60	-	-	-	-	11.2	R_{s1}
70	-	-	-	-	14.3	R_{s1}+R_{s2}
80	-	-	12.6	R_{s1}	20.4	R_{s1}+R_{s2}
90	-	-	16.3	R_{s1}+R_{s2}	25.7	R_{s1}+R_{s2}+R_{s3}
100	13.5	R_{s1}	21.7	R_{s1}+R_{s2}	30.6	R_{s1}+R_{s2}+R_{s3}

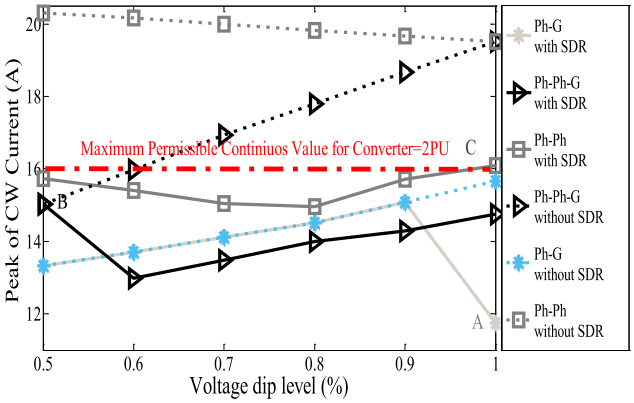

FIGURE 7. CW Current limiting with employing adaptive SDR.

Figure 8 shows the differences of implementing appropriate and overdesigned (Fixed) SDR values for a 95% Ph-G voltage dip occurring at $t = 6s$ for a 1500*ms* period. The CW current peak (Figure 8.a) and the transient oscillation of reactive (Figure 8.b) and real power (Figure 8.c) after

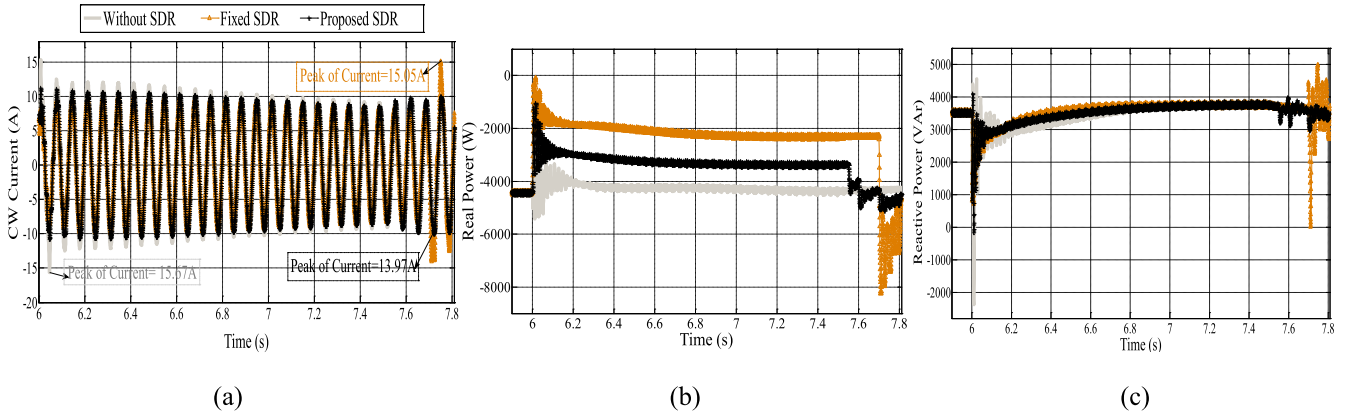

FIGURE 8. Application of adaptive SDR in comparison with conventional method for Ph-G voltage dips. (a) CW current, (b) Real power, (c), Reactive power.

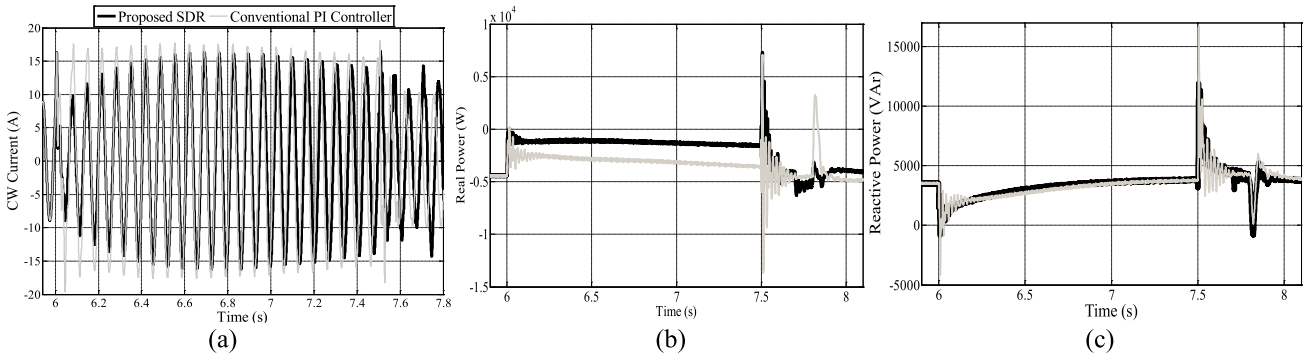

FIGURE 9. LVRT assessment during a severe Ph-Ph voltage dips. (a) CW current, (b) Real power, (c), Reactive power.

fault clearance can be effectively reduced by our proposed protection scheme. Using adaptive SDR with lower values for resistances can offset the negative effects of active power losses (Figure 8.c). Meanwhile, the converter current and supporting real and reactive power are satisfying the grid code requirements. Moreover, the post-fault transients can be effectively damped by implementing adaptive SDR instead of using a conventional SDR.

D. LVRT ENHANCEMENT DURING ASYMMETRICAL VOLTAGE DIPS

Since the highest values of peak transient happen in the case of Ph-Ph fault, improvements of the BDFIG LVRT capability for this situation ensures desired operation for all other type of faults. Based on the equivalent circuit model of the BDFIG (Figure 1), since negative and zero sequence components have a key role in Ph-Ph dip transients, using SDRs in series with the power winding can change the equivalent transient resistance of the generator which in turn limits overshoots of the transient behavior. Besides, since the resistance value of power winding is multiplied by the rotor speed, the proposed protection scheme can guarantee a successful ride through capability for higher pre-fault speeds.

In order to assess the enhancement of the proposed protection framework during LVRT condition for asymmetrical faults, a 95% Ph-Ph voltage dip as a severe fault condition is occurred at t = 6ms and the protective circuit is activated within 10 *ms*, which is needed for the voltage dip detection. The results are shown in Figure 9 for 650 *rpm* pre-fault shaft speed. Results indicate that the proposed strategy can successfully limit the current of control winding to 2 *pu*. as shown in (Figure 9.a) even for the worst-case scenario. The results also indicate a faster increase in damping of the CW current and reduced reactive and real power oscillations compared to conventional methods (Figure 9.b). Although the variation in reactive power is similar to the case of using PI controller, its amplitude is significantly limited after fault occurrence and clearance (Figure 9.c).

The multi-step SDR design ensures proportional activation of SDR resistors during asymmetrical voltage dips by effectively limiting CW and converter current. Similarly, sequential deactivation of the SDR values after clearance of the fault mitigates post-fault oscillations in the BDFIG. This approach successfully limits peak values of control winding inrush current and stabilizes BDFIG transient behavior during both voltage dip occurrence and clearance by suppressing the transients caused by zero and negative sequence components of the BDFIG EMF. The variations in the injected reactive power after voltage dip clearance underscore the advantages of the proposed SDR scheme. Leveraging the proposed rapid and harmonically resistant voltage dip detection method, the appropriate SDR values are calculated which in turn effectively limits the transient oscillations. Hence, the proposed framework significantly enhances BDFIG LVRT

under asymmetrical voltage dip conditions. The proposed scheme shows promising performance in limiting transient currents and reinforcing oscillation damping particularly in the common Ph-G grid fault scenarios where a large SDR value is not required. It should be noted that these results were obtained without modifications to the converter controllers during voltage dips. In other words, dynamic behavior of the SDR can be improved even further.

While leveraging SDR-based protection circuits offers significant advantages, it often lacks direct control over the DC link voltage [26]. To address this limitation, recent studies such as those in [25] and [27] suggest a coordinated protection strategy between the SDR and DC-link brake chopper, which in turn enhances the dynamic response of wind turbines. Note that such a method contributes to the improvement of voltage response at the point of common coupling of wind turbines, an area worth considering for the future works.

V. CONCLUSION

In this paper, we proposed a comprehensive protection framework by leveraging a fast voltage dip detection scheme and the ride through capability of BDFIG. Note that Ph-Ph (Ph-Ph-G) faults result in high transient currents which in turn cause BDFIG to fail satisfying ride through requirements without incorporating the hardware-based protection schemes. In this sense, dynamic behavior of the BDFIG was investigated during asymmetrical fault conditions. Moreover, a fast and harmonic resistant scheme was suggested for voltage dip detection and its performance was verified for different fault scenarios. It was shown that the proposed scheme can be used for detecting all kinds of voltage dips in presence of harmonics. Besides, since the SDR circuit is in series with power winding of the BDFIG, reactive power injection can be controlled which is a necessary requirement for the recent strict grid codes. It was also shown that determination of SDR values needs a tradeoff between post-fault CW current and transient values in the protection circuit deactivation procedure. This paper strikes the balance by introducing adaptive SDR activation and deactivation mechanisms. Specifically, using adaptive SDR with lower value for resistances can effectively damp post fault transients and reduce active power losses unlike the conventional SDR. The outcomes of this work can be used as an efficient and simplified ride through solution for BDFIG LVRT condition, especially where severe grid code requirements are required.

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