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RESEARCH ARTICLE

Low Loss Hybrid-Plane PCB Structure for Improving Signal Quality in High-Speed Signal Transmission

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ABSTRACT Due to the inherent loss characteristics of transmission lines today, the challenges in signal transmission are increasing. Typically, the most widely used printed circuit boards (PCBs) in transmission lines employ FR-4 as the insulation material due to its advantages in electrical insulation and cost-effectiveness. Nevertheless, PCBs that rely solely on FR-4 for the entire insulation layer are unsuitable for high-speed circuits due to significant dielectric losses. Efforts have been made to reduce losses by researching hybrid-stackup PCBs that stack low loss dielectric materials vertically. However, due to the high cost of these low loss dielectric materials, they have mainly been applied in high-end and high-speed applications. Therefore, in this paper, we propose a hybrid-plane PCB structure that uses low loss dielectric materials only in the planes adjacent to high-speed signal traces, minimizing the use of expensive low loss dielectric materials while achieving similar enhancements in signal quality compared to previously researched hybrid-stackup each PCB was modeled using Ansys Q2D Extractor, and S-parameters and eye diagrams were extracted for each to compare their electrical characteristics and signal quality. The simulation results confirm that the proposed hybrid-plane PCB structure in this paper has been found to exhibit improved electrical characteristics compared to PCBs constructed solely with an FR-4 insulation layer. Furthermore, various low loss dielectric thicknesses were compared to interpret the optimal thickness of the low loss dielectric for the hybrid-plane PCB, based on the signal integrity assurance rate.

INDEX TERMS High-speed, low loss dielectric material, PCB, signal integrity (SI), signal loss.

I. INTRODUCTION

The size of systems is today continuously shrinking, and the traces and components on PCBs are getting smaller and smaller. At the same time, with the rapid advancement of the electronics industry, high-speed circuit design has become a critical technology [1]. However, as the density and signal frequencies continue to increase, issues related to signal integrity (SI) and power integrity (PI) have also become more prominent due to high-speed circuit design. Therefore, achieving higher data rates and transmission bandwidths in systems has become a crucial challenge [2]. System design now requires higher bandwidth, high-speed capabilities, high performance, and a greater number of components.

With the advancement of high-speed circuit design, the characteristics of transmission lines, such as PCBs have become increasingly important. As data rates have risen into the GHz and higher frequency ranges, there has been an increase in power and signal losses during signal transmission. Additionally, as the bandwidth has increased, the bit error rate has also increased [3], [4]. Similarly, SI has been severely affected in the GHz and higher frequency ranges. This is due to the occurrence of reflection waves at impedance mismatch points such as device connection pins, via holes, and connection points where the wavelength of the electrical signal is much shorter than the length of PCB traces. These reflections are a major cause of SI degradation and

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waveform distortion. Impedance matching of transmission lines is one of the key characteristics of transmission lines and is a critical factor influencing SI. In practical PCB design, impedance control of transmission lines is primarily achieved through stack distribution and adjusting trace widths and spacing [5], [6].

Another factor contributing to losses in transmission lines due to the influence of high-speed circuit design is DC/AC losses. One primary cause of DC losses is the heat generated by resistance when DC current flows through the transmission line. The resistance losses increase proportionally with the intensity of the current. AC losses, on the other hand, are primarily caused by the skin effect and dielectric losses [7], [8]. First, the skin effect refers to the phenomenon where high-frequency AC currents penetrate only a limited depth from the surface of a conductor. The ''skin depth'' varies depending on the characteristics of the conductive material, frequency, resistivity, and more. When the skin effect occurs, current becomes concentrated near the surface of the conductor, leading to increased resistive losses in the surface area [9], [10]. Considering the second cause, dielectric losses, frequency is a critical factor. Dielectrics exhibit a high frequency dependence, resulting in significant transmission losses in relatively high-frequency ranges compared to low-frequency ones. According to Jonscher's 'universal dielectric response law,' the frequency dependence of dielectric losses follows an empirical law over dozens of frequencies, ranging from low frequencies to $\omega/2\pi \sim 10^9$ Hz. The formula indicated in (1) represents the power law region that expands with frequency ω, where the exponent n is fixed.

$$x''E(\omega) \propto \omega^{n-1}, \quad with\ 0 < n < 1 \tag{1}$$

Materials mentioned in (1) include inorganic ceramics, polymers, glass, inorganic crystalline and amorphous materials, with some being insulators or semiconductors. Additionally, organic and biological systems are also encompassed. Generally, the dielectric constant of dielectric materials can vary with frequency, and as the frequency increases, dielectric losses also increase. Furthermore, the dielectric constant of dielectric materials can also impact losses. Since the transmission speed of electrical signals in circuits is inversely proportional to the dielectric constant, it is essential to reduce the dielectric constant of dielectric materials to decrease transmission losses [11], [12], [13], [14]. In this paper, we focus on losses in AC, which is one of the key causes of losses due to high-speed signals, and specifically, we concentrate on the issue of dielectric losses.

The remaining sections of this paper are structured as follows: Chapter 2 reviews previous studies that attempted to reduce signal distortion and minimize the use of expensive low loss dielectric materials. In Chapter 3, we model the cross sections of each PCB using the Ansys Q2D Extractor. It covers the settings for extracting S-parameters and eye diagrams to compare the electrical properties and signal quality assurance rate. Chapter 4 compares and analyzes the extracted S-parameters and eye diagrams based on the results. Chapter 5 introduces the manufacturing process of the hybrid-plane PCB proposed in this paper, providing a brief comparison with the commercially available hybrid-stackup PCB. It explores the economic benefits attained by reducing the usage of expensive low loss dielectric materials. Finally, in Chapter 6, conclusions are drawn regarding this study, examining the positive effects and prospects of the proposed structure contributing to the electronics industry.

II. PRIOR STUDY

FR-4 is the fundamental material for PCB in the industry and is widely utilized due to its advantages, such as its ideal insulating properties and cost effectiveness. However, as the importance of high-speed and high-bandwidth signal transmission continues to grow, the high dielectric constant and loss coefficient of FR-4 have emerged as critical drawbacks. With increasing data rates, significant dielectric losses have become a concern. Research into low loss PCB dielectric materials with lower dielectric constants and loss coefficients is needed to enhance the SI performance of high-speed signals.

While using low loss dielectric materials effectively reduces losses compared to traditional models, these materials are often more expensive than the widely used FR-4. Consequently, it can be challenging to fabricate the entire insulating layer using low loss dielectric materials. To mitigate this issue, research has been conducted on vertical hybrid-stackup PCBs, where low loss materials are used in specific layers adjacent to high-speed signal layers rather than throughout the entire insulating layer [15], [16], [17], [18]. However, hybrid-stackup PCBs require additional processes for bonding vertical composite dielectric layers and typically involve a significant quantity of low loss materials for layer formation. As a drawback, they are generally applied only to high-end and high-speed application products.

Therefore, in order to effectively save expensive low loss dielectric materials and provide electrical properties similar to those of hybrid-stackup PCBs (reduced frequency loss due to high-speed operation circuits), this paper proposes the structure of a hybrid-plane PCB, which is formed in a horizontal structure only on the plane adjacent to the high-speed signal traces rather than on the entire layer.

III. PROPOSED METHOD

In this chapter, we introduce the PCB structure to be analyzed and aim to extract S-parameters and eye diagrams to compare the electrical characteristics concerning structural variations. Fig. 1 illustrates cross-sections of the models using Ansys Q2D Extractor to facilitate a comparison between the conventional PCB using only FR-4, the previously researched vertical hybrid-stackup PCB, and the horizontal hybrid-plane PCB proposed in this paper. In each model, a differential signaling structure renowned for its robust resistance to noise, commonly employed in high-speed lines, was applied. About this, the most suitable termination method chosen was to set the termination resistance of the differential lines to

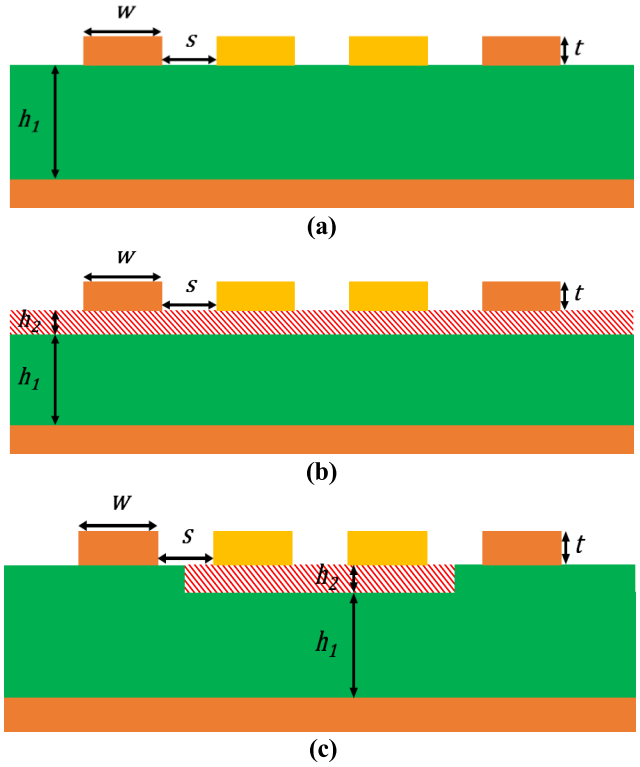

FIGURE 1. The hatched square represents the dielectric made of PTFE. Commonly, "t" has a value of 35 μm, and "s" is set at 100 μm; (a) Cross section of the conventional PCB structure where the entire insulating layer is made of FR-4, (b) Cross section of the hybrid-stackup PCB with a vertical structure, and (c) Cross section of the hybrid-plane PCB with a horizontal structure.

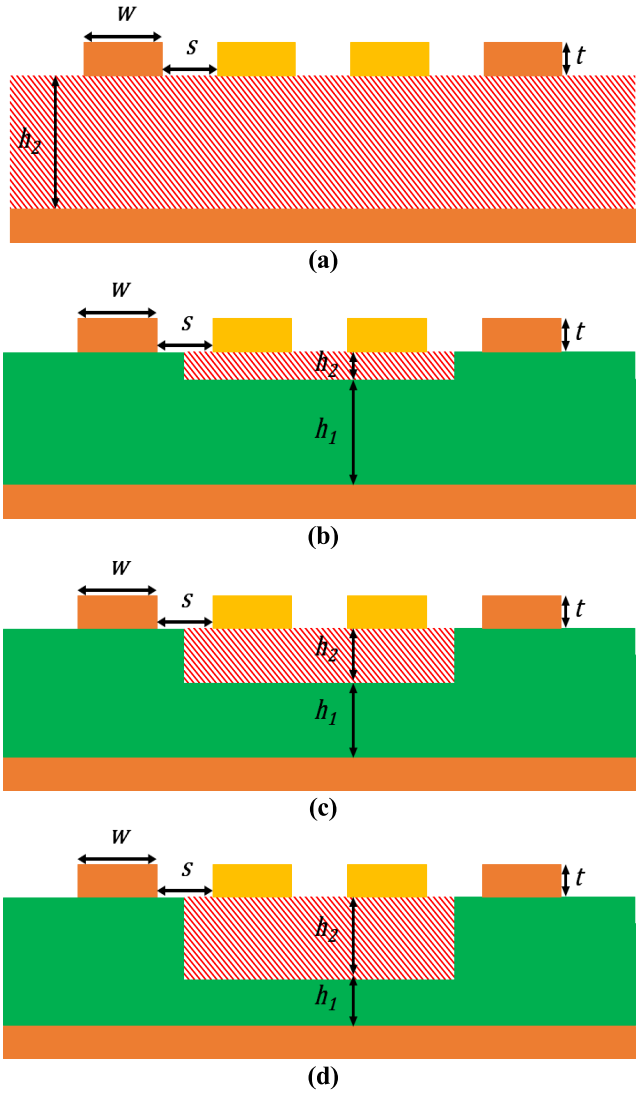

FIGURE 2. Cross sections of hybrid-plane PCBs with different thicknesses of PTFE. Common values of "t" are 35 μm and "s" is 100 μm; (a) Cross section of a PCB with an all-PTFE insulating layer, (b) Cross section with 30 μm of PTFE, (c) Cross section with 60 μm of PTFE, and (d) Cross section with 90 μm of PTFE.

100Ω [19]. This decision was made considering increased compatibility and standardization within the industry, aiming to mitigate signal reflections, waveform distortion, and noise through impedance matching efforts.

$$Dk_{layered} = \frac{1}{\sum_{n=1}^{all\_layers} \frac{h_n}{h_t Dk_n}} \tag{2}$$

The low loss dielectric material used in this study is polytetrafluoroethylene (PTFE), with a permittivity of 2.02 and a loss tangent of 0.00022. For FR-4, the permittivity is set at 4.4, with a loss tangent of 0.02. Furthermore, the direct calculation of the dielectric constant was performed for a composite dielectric consisting of two different dielectric materials placed between the ground plane and trace. When employing a dielectric material in a complex configuration within a single layer, it modifies the dielectric constant, thereby impacting the trace—a pivotal factor in impedance matching. As a result, the dielectric constant of such a composite dielectric can be determined using the provided formula (2) [20]. In equation (2), "Dk" represents the dielectric constant of the stack, while "h_t" denotes the overall height of the dielectric stack.

In fig. 1 and fig. 2, "t" represents the thickness of the trace, "h_1" is the thickness of the FR-4 layer, "h_2" is the thickness of the low loss dielectric material, "w" denotes the width of the trace, and "s" represents the spacing between traces. The models are simple structures created using Ansys Q2D extractor, and they are designed with impedance matching in mind for increased compatibility and standardization. These structures feature differential lines, which are resilient against signal reflections, waveform distortion, and noise. To effectively compare signal distortion in the PCB under different frequency conditions, we represented an extremely high-speed, long-length channel structure. Therefore, all models share a common channel length of 1000 mm and set the T_X frequency to 10 GHz.

In fig. 1(a), "h_1" is 140 μm, "w" is 125 μm, and dielectric constant ε_r is 4.4. In fig. 1(b) and (c), "h1" is 110 μm, "h_2" is 30 μm, "w" is 150 μm, and for the composite dielectric, ε_r is 3.51. The structure proposed in this paper, (c), is designed to be applied partially to high-speed

signal transmission lines by arranging it on a plane to effectively reduce the use of costly low loss dielectric materials. To model this, it maintains the same length, trace width, trace thickness, and spacing as the conventional hybrid-stackup PCB structure, but instead of using low loss dielectric material throughout the entire layer, it is applied near the spacing between the GND and the high-speed signal traces.

In fig. 2, electrical characteristics were extracted for different thicknesses of the low loss dielectric material, namely 30, 60, and 90 μm, to assess signal quality. For each thickness, cross-sections of the PCB and a cross section of a structure where the entire insulating layer is made of PTFE (used as a reference for comparing signal quality assurance) were added to fig. 2.

In fig. 2, (a) "h_2" is 140 μm, "w" is 210 μm, and ε_r is 2.02. In fig. 2 (b), "h_1" is 110 μm, "h_2" is 30 μm, "w" is 150 μm, and for the composite dielectric, ε_r is 3.51. In fig. 2 (c), "h_1" is 80 μm, "h_2" is 60 μm, "w" is 170 μm, and for the composite dielectric, ε_r is 2.92. In fig. 2 (d), "h_1" is 50 μm, "h_2" is 90 μm, "w" is 190 μm, and for the composite dielectric, ε_r is 2.50. Additionally, in fig. 3, circuit models were presented to extract eye diagrams, enabling the analysis of the electrical characteristics of the models shown in fig. 1 and 2. The voltage range for the eye source is set from -3V to 3V, and the rise time and fall time are both configured as 500 ps. The termination resistance was set to 100Ω.

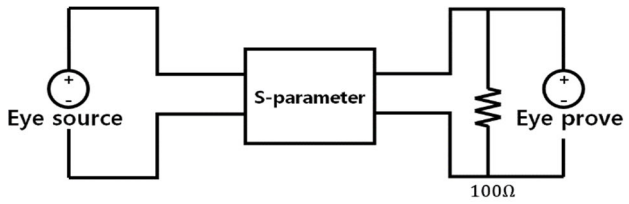

FIGURE 3. Circuit model for eye diagram extraction.

IV. RESULT & DISCUSSION

To assess the insertion loss (IL) of the differential line, S-parameters were extracted. The S-parameters were obtained through a frequency sweep, analyzing the range from 20 MHz to 40 GHz with points of 2000. Additionally, to evaluate the quality of high-speed signals, the eye height, eye width, eye jitter (RMS) and eye opening factor (ratio of eye height to eye amplitude) of the eye diagram were analyzed. In fig. 4, the S-parameter results for the models from fig. 1 are compared, and fig. 5 illustrates the eye diagram results for these models. As mentioned in the preceding chapters, a channel structure with high frequencies and extended lengths was utilized to vividly demonstrate signal distortion and loss. As a result, the eye diagram prominently displayed instances of jitter and noise.

Fig. 6, 7, and 8 present graphs comparing the eye height, eye width, and eye opening factor for each structure. Upon examining the results of the eye diagram, the hybrid-plane

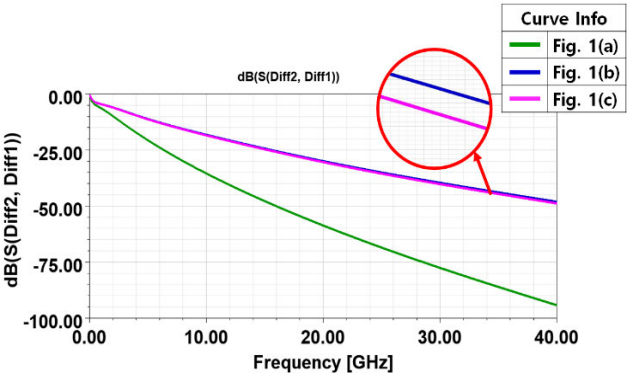

FIGURE 4. S-parameter; (a) PCB with the entire insulating layer made of FR-4, (b) Hybrid-stackup PCB with a vertical structure, and (c) Hybrid-plane PCB with a horizontal structure.

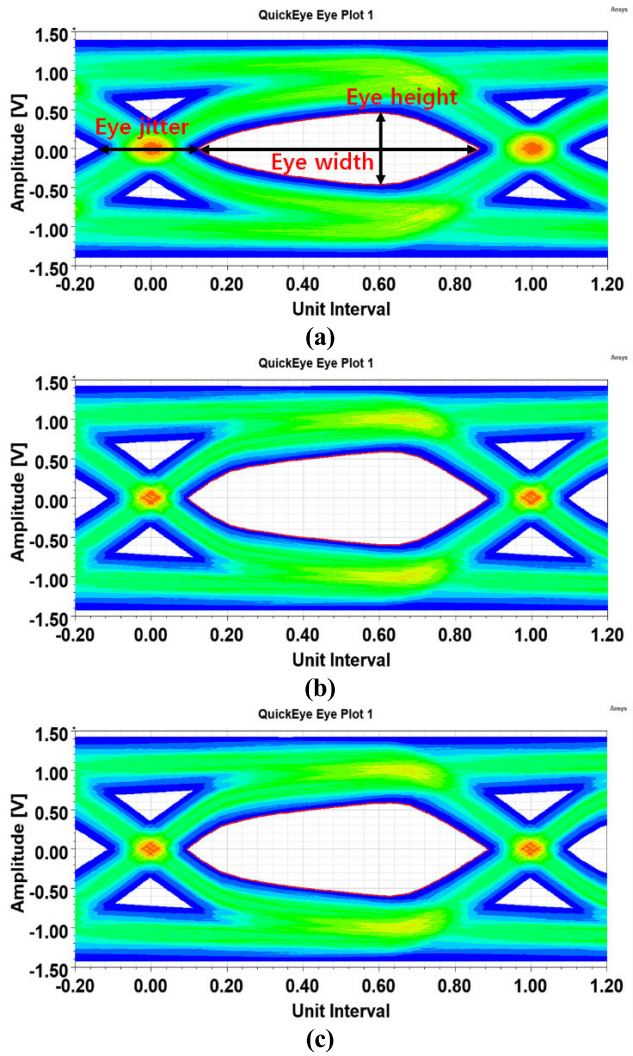

FIGURE 5. Eye diagrams for assessing signal quality; (a) PCB with the entire insulating layer made of FR-4, (b) Hybrid-stackup PCB with a vertical structure, and (c) Hybrid-plane PCB with a horizontal structure.

PCB structure proposed in this paper exhibits an increase of approximately 49.2% from 0.53 V to 0.80 V in eye height,

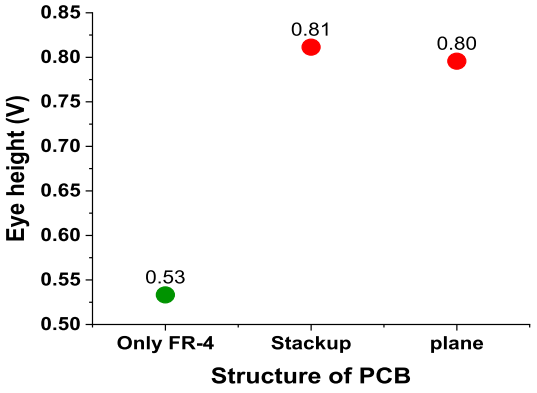

FIGURE 6. Eye height for each PCB structure.

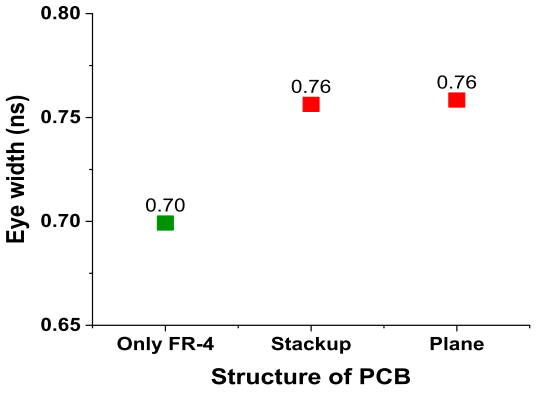

FIGURE 7. Eye width for each PCB structure.

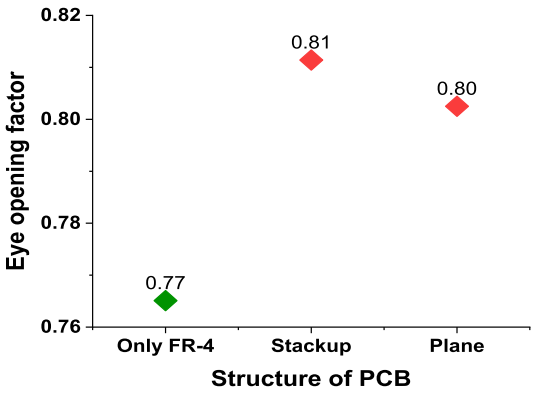

FIGURE 8. Eye opening factor for each PCB structure.

an increase of approximately 8.5% from 0.70 ns to 0.76 ns in eye width, and an increase of approximately 5% from 0.77 to 0.80 in the eye opening factor compared to the PCB utilizing the entire insulation layer composed solely of FR-4.

Fig. 9 illustrates the jitter (RMS) for each structure, showing that using low loss dielectric materials, as shown in hybrid-stackup PCB and hybrid-plane PCB, reduces jitter by approximately 19.6%, from 0.05 (ns) to 0.04 (ns) compared to PCBs using the entire insulating layer with only FR-4. Referring to fig. 4, which represents the S-parameters, and fig. 6, 7, 8, and 9, which depict the eye diagrams,

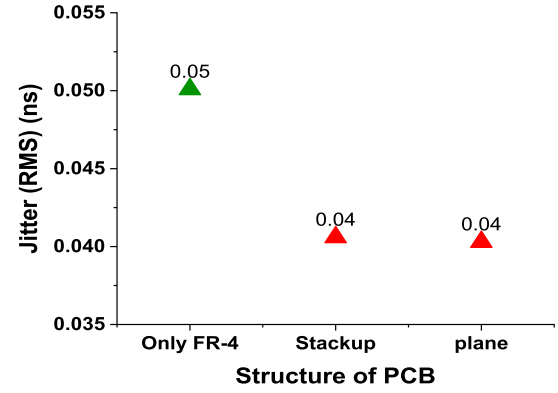

FIGURE 9. Jitter (RMS) for each PCB structure.

the proposed hybrid-plane PCB demonstrates superior electrical characteristics compared to PCBs composed entirely of FR-4 as the insulating layer. Furthermore, the hybrid-plane PCB exhibited marginal differences in electrical characteristics such as eye height, eye width, eye opening factor, and jitter when compared to the hybrid-stackup PCB.

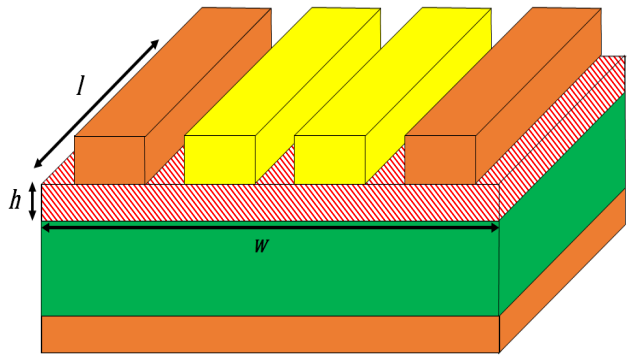

FIGURE 10. The three-dimensional structure of a hybrid-stackup PCB with a PTFE thickness of 30 μm.

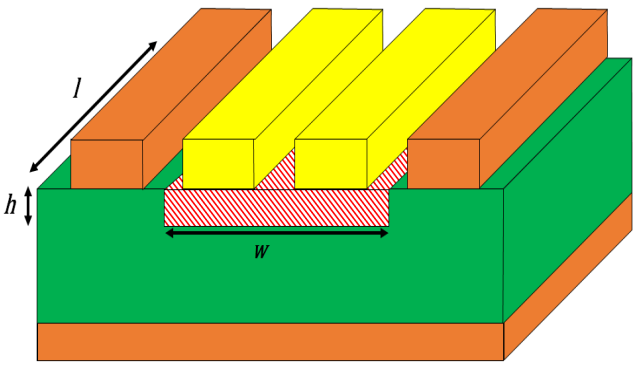

FIGURE 11. The three-dimensional structure of a hybrid-plane PCB with a PTFE thickness of 30 μm.

Fig. 10 and 11 represent the three-dimensional structures of the hybrid-stackup PCB and the hybrid-plane PCB, respectively, with all parameters identical except for the width of

the low loss dielectric material. The PTFE thickness for each PCB was set to 30 μm, the same value used in the simulations comparing the electrical characteristics of the hybrid-stackup PCB and the hybrid-plane PCB. In fig. 10, the entire layer adjacent to the high-speed signal traces is composed of PTFE, with h at 30 μm, w at 1500 μm, and a channel length l of 1000 mm. Therefore, the volume of PTFE used in the hybrid-stackup PCB structure can be expressed as 45 mm^3. In fig. 11, only the plane adjacent to the high-speed signal traces is made of PTFE, with h at 30 μm, w at 500 μm, and a channel length l of 1000 mm. Therefore, the volume of PTFE used in the hybrid-plane PCB structure is 15 mm^3. Fig. 10 and 11 demonstrate that the hybrid-plane PCB utilizes approximately 1/3 of the PTFE compared to the hybrid-stackup PCB. Therefore, when comparing the volume of the low loss dielectric material used in the simulations and the electrical characteristics of each PCB structure, the hybrid-plane PCB demonstrates a significantly lesser amount of low loss dielectric material used, yet shows a similar signal quality improvement effect to the hybrid-stackup PCB.

In fig. 12, S-parameters were depicted to interpret the insertion loss and signal quality based on the thickness of the low loss material layers in the proposed hybrid-plane PCB, fig. 13 and 14 illustrate the trends of eye height, eye width, jitter (RMS), and eye opening factor based on the results of the eye diagram. Similar to fig. 4, the S-parameters in fig. 12 were analyzed over a range from 20 MHz to 40 GHz with 2000 points. Based on the simulation results of S-parameters and eye diagrams, it can be observed that as the low loss material layer thickness increases (30 μm $<$ 60 μm $<$ 90 μm), there is a tendency for the eye height, eye width, and eye opening factor to increase, while jitter decreases, indicating superior electrical characteristics.

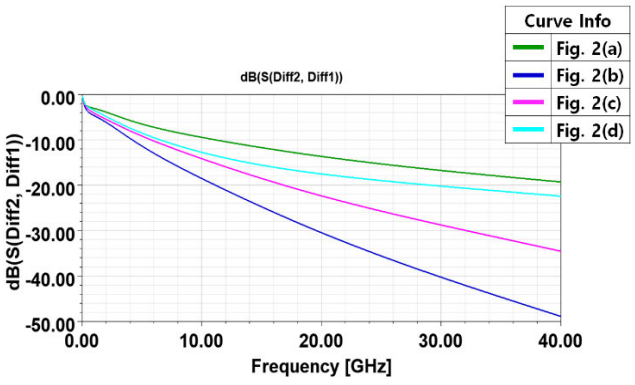

FIGURE 12. S-parameter as a function of the thickness of the low loss dielectric layer in the hybrid-plane PCB; (a) PCB with the entire insulating layer made of PTFE, (b) Hybrid-plane PCB with a PTFE thickness of 30 μm, (c) Hybrid-plane PCB with a PTFE thickness of 60 μm, and (d) Hybrid-plane PCB with a PTFE thickness of 90 μm.

In fig. 15, the signal integrity retention rates are presented based on the eye opening factor to comprehensively evaluate the signal quality according to the thickness of low loss dielectric material. Assuming the eye opening factor of the

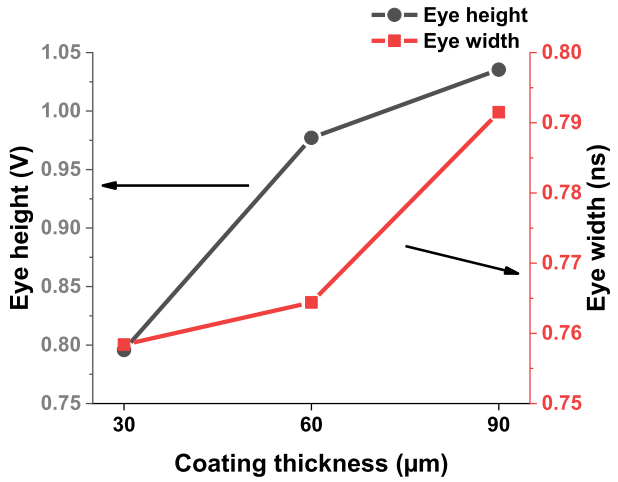

FIGURE 13. Eye height and eye width for each PCB structure.

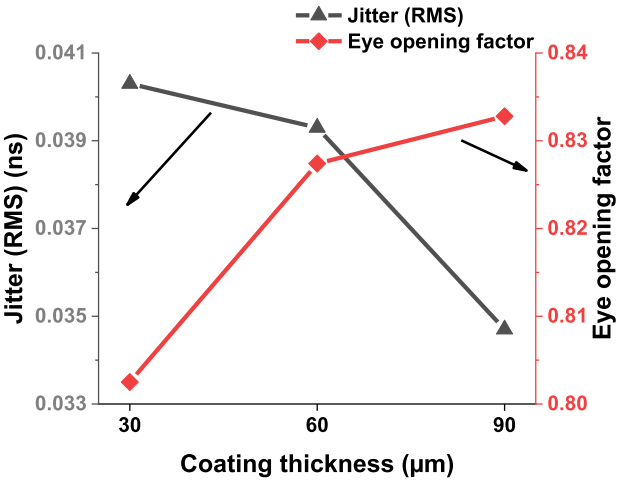

FIGURE 14. Jitter (RMS) and eye opening factor for each PCB structure.

entire insulating layer on the PCB made of PTFE is set to 100%, the signal quality retention rates for low loss dielectric layer thicknesses of 30, 60, and 90 μm are 95.5%, 98.5%, and 99.2%, respectively. Therefore, to demonstrate an improvement effect of signal quality by over 99% compared to the signal quality of the PCB with the entire insulating layer made of PTFE, it is necessary for the thickness of the low loss dielectric layer to be approximately 80 μm or more.

V. MANUFACTURING PROCESS & ECONOMICS

In the preceding Chapter 4, an investigation was conducted comparing the eye height, eye width, eye opening factor, and jitter (RMS) extracted from eye diagrams based on various thicknesses of low loss dielectric material layers. This aimed to discern trends in electrical characteristics concerning thickness and propose an optimal thickness. Additionally, it involved comparing the volumes of low loss dielectric material used in PCB fabrication. This chapter shifts focus towards providing a concise introduction to the manufacturing process of the proposed hybrid-plane PCB in this paper. The aim is

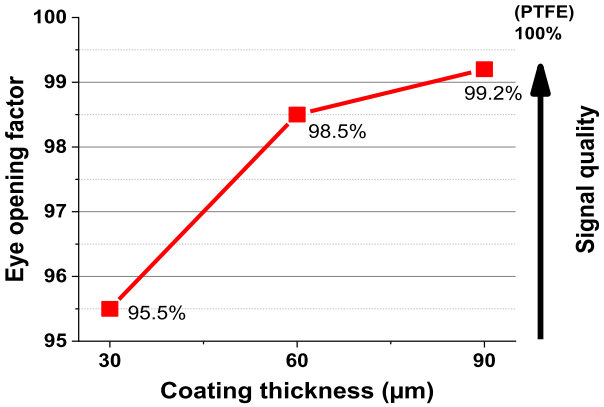

FIGURE 15. Signal quality improvement ratio (eye opening factor) depending on the thickness of the low loss dielectric layer in the hybrid-plane PCB.

to identify the ideal area for the low loss dielectric material layer through simulation-based verification, with a focus on cost reduction.

Low loss dielectric material layers have been studied to mitigate dielectric losses at higher data speeds and an expanded range of signal transmission frequencies as the electronics industry progresses. However, the drawback lies in the high cost and manufacturing complexity of materials like PTFE. Consequently, the application of PCB products utilizing low loss dielectrics differs from typical PCBs that use cost-effective FR4 as the dielectric material. Despite cost overheads, products employing low loss dielectrics are primarily limited to high-end products where signal transmission quality is paramount.

The method proposed in this study aims to minimize dielectric losses in high-end products where high-speed signal transmission is critical, while maintaining signal quality. It seeks to propose a cost-effective approach by utilizing a reduced quantity of low loss dielectric material compared to conventional products. Conventional products using low loss dielectrics typically apply these materials, such as PTFE or synthetic substances with a high content of low loss dielectric material, to the top or bottom layers where high-speed signal lines are wired. For the remaining wiring layers, FR4 is commonly used. The hybrid-plane PCB structure proposed in this research separates wiring areas for high-speed signals and general signals on the same layer. It employs low loss dielectric material in sections adjacent to high-speed signal wiring.

The proposed hybrid-plane PCB, aiming to partially utilize low loss dielectric material, may incur additional process costs by grinding FR-4 in the area designated for high-speed signal line wiring and subsequently bonding PTFE. However, commercially available products employing typical low loss dielectrics also incur additional process costs by bonding PTFE as the dielectric material on the top or bottom layer. Conversely, in the case of the proposed hybrid-plane PCB, during the design phase illustrated in fig. 16, the PCB segregates the general signal trace area and the

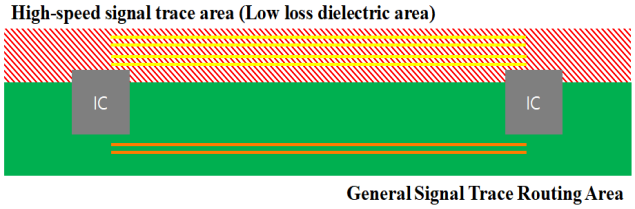

FIGURE 16. Differentiation between high-speed signal and general signal trace areas.

high-speed signal trace area. By significantly reducing the usage of low loss dielectric material, it can achieve higher cost-effectiveness.

Fig. 17 depicts a more realistic structure illustrating the manufacturing process of the hybrid-plane PCB, ensuring consideration for practical implementation compared to the previously discussed PCB model. Within this illustration, "l" represents the channel length, "h" denotes the thickness of the low loss dielectric material, "w_1" stands for the width of the PCB, and "w_2" signifies the width of the low loss dielectric material layer. This depiction segregates the left side to represent the general signal trace area employing FR-4 as the layer, while the right side showcases the high-speed signal trace area utilizing PTFE, a low loss dielectric material, to minimize dielectric losses. Subsequent stages involve a similar process, where S-parameters for insertion loss and eye diagrams are extracted, continuing the methodology used previously. This approach aims to conduct a comparative analysis between the electrical characteristics and eye diagrams of the hybrid-plane PCB and the commercially available hybrid-stackup PCB structure. The objective is to evaluate the performance and the extent of signal quality enhancement achieved by implementing the hybrid-plane PCB in contrast to the existing hybrid-stackup PCB structure.

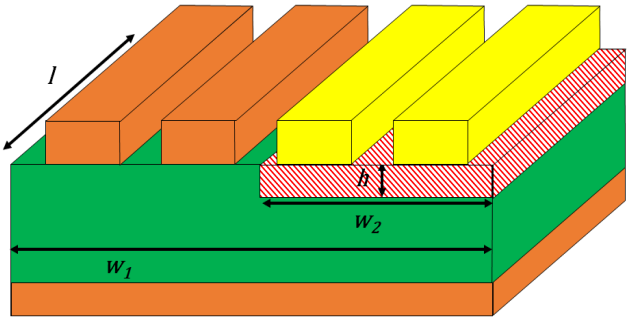

FIGURE 17. A PCB structure designed considering high-speed signal line design and manufacturing process. The parameters are set as follows: "l" is 1000 mm, "h" is 30 μm, "w_1" is 1500 μm, and "w_2" is 500 μm.

In fig. 18, cross-sections of the hybrid-plane PCB in suitable forms for the manufacturing process are depicted. In (b), "w_2" is set at 500 μm, representing 30% of the total PCB width, while in (c), "w_2" is set at 750 μm, representing 50% of the total PCB width. These proportions were arbitrarily

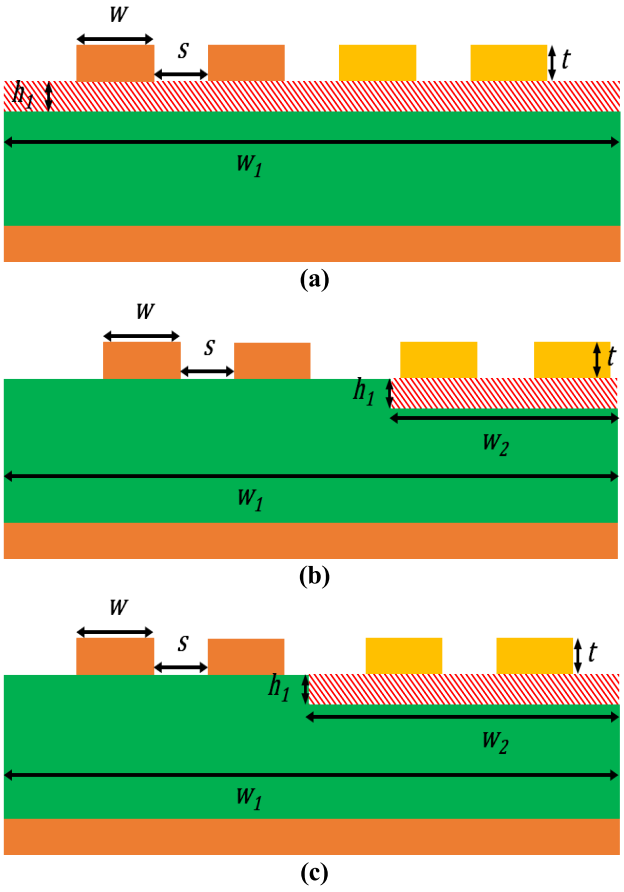

FIGURE 18. A cross-sectional view of PCB structures considering the manufacturing process. Commonly, "t" is 35 μm, "s" is 100 μm, "h_1" is 30 μm, and "w_1" is 1500 μm; (a) cross-section of a hybrid-stackup PCB, (b) cross-section of a PCB where the low loss dielectric material layer comprises 30% of the total width, (c) cross-section of a PCB where the low loss dielectric material layer comprises 50% of the total width.

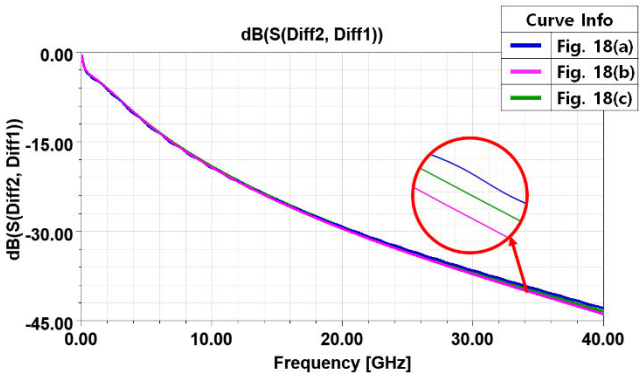

FIGURE 19. S-parameter depending on the width of the low loss dielectric material layer.

TABLE 1. Interpretation of signal quality in the eye diagram.

	(a)	(b)	(c)
Eye height (V)	1.0937	0.8581	0.9360
Eye width (ns)	0.7884	0.7627	0.7640
Eye opening factor	0.8444	0.8109	0.8227
Eye jitter (RMS) (ns)	0.0353	0.0395	0.0393

chosen to examine the tendencies in electrical characteristics and signal quality based on the width of the low loss dielectric material layer. The values may vary to better suit the process and signal line design, serving as a means to understand the trends associated with the width of the low loss dielectric material layer.

In fig. 19, a comparison was made among the S-parameters corresponding to varying widths of the low loss dielectric material layer. These S-parameters are indicative of the insertion loss in the signal line. Similar to earlier experiments, there is a marginal enhancement in the electrical characteristics concerning insertion loss as the usage of the low loss dielectric material layer increases progressively from (b) to (c) and (a). However, overall, all three models exhibit a similar trend, demonstrating consistent patterns in terms of insertion loss characteristics.

Table 1 lists the eye height, eye width, eye opening factor, and eye jitter (RMS) of the eye diagram presented in fig. 20, aimed at interpreting the signal quality. The S-parameters exhibited a similar trend, showcasing an overall enhancement in signal quality capabilities as we progress from (b) to (c) and (a). However, it's noteworthy that these variations showed remarkably close tendencies. In reference to the opening factor of the hybrid-stackup PCB model denoted as (a), the model with a 30% width of the low loss dielectric material layer represented in (b) showed a level of 96%, whereas the model with a 50% width of the low loss dielectric material layer in (c) demonstrated a level of 97.4%. Hence, in a design considering the manufacturing process, the hybrid-plane PCB confirms its ability to possess similar electrical characteristics and signal quality enhancement capabilities comparable to the hybrid-stackup PCB. Additionally, referring to the simulation verification comparing the volumes of the hybrid-stackup PCB and the hybrid-plane PCB (each with a PTFE thickness of 30 μm) as described in Chapter 4, the structure proposed in this paper achieves a 98.8% eye opening factor improvement compared to commercially available PCBs. This suggests a similar enhancement in signal quality while utilizing significantly less expensive low loss dielectric material, approximately one-third the amount used in standard PCBs. (This result is based on the low loss dielectric material's width being one-third of the total PCB width. By adjusting the width or height appropriately to suit process feasibility or application requirements, the amount of low loss dielectric material used in PCB fabrication can be further reduced while comparing electrical characteristics and signal quality enhancement.)

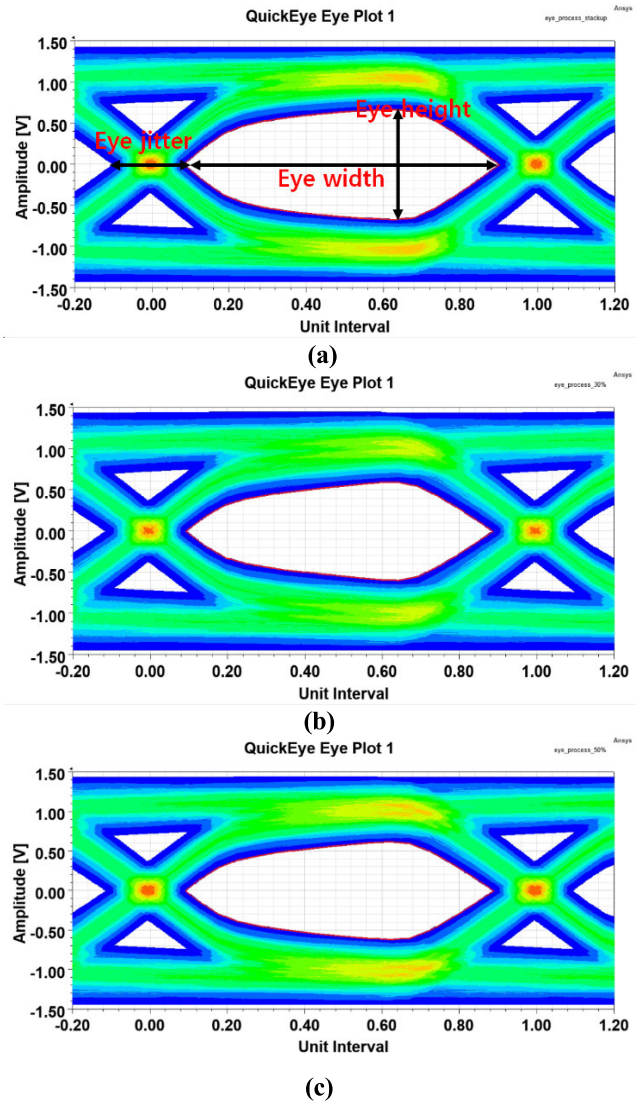

FIGURE 20. Eye diagrams for signal quality evaluation; (a) Hybrid-stackup PCB, (b) PCB with low loss dielectric material layer accounting for 30% of the total width, (c) PCB with low loss dielectric material layer accounting for 50% of the total width.

VI. CONCLUSION

In this paper, we propose a hybrid-plane PCB structure that can reduce the frequency loss of high-speed operation circuits while saving costs of expensive low loss dielectric materials by using low loss dielectrics only on the planes adjacent to high-speed signal traces. Through on-site simulations, we extracted S-parameters and eye diagrams to analyze the insertion loss and signal quality of the proposed structure. Simulation results confirm that the hybrid-plane PCB structure proposed in this paper shows approximately 49.2% increase in eye height, about 8.5% increase in eye width, approximately 5% increase in eye opening factor, and a decrease in jitter (RMS) by approximately 19.6% compared to PCBs constructed solely with an FR-4 insulation layer, indicating an improvement in electrical characteristics. Through simulations comparing the amount of low loss dielectric material used, it was possible to achieve approximately a 1/3 reduction in material compared to the original hybrid-stackup PCB (with a PTFE thickness of 30 μm). Moreover, the extent of improvement in electrical characteristics, based on the eye opening factor, was observed to be approximately 99% of the electrical characteristics of the hybrid-stackup PCB. Furthermore, in order to ensure signal quality, an analysis of the eye opening factor was conducted for different thicknesses to determine the optimal PTFE thickness in a hybrid-plane PCB. Through simulations, it was observed that a minimum low loss dielectric material thickness of 80 μm is required to guarantee signal quality of over 99% compared to using PTFE for the entire insulating layer in the PCB. From a manufacturing perspective, considering the potential difficulty in applying low loss dielectric material selectively only to the layers adjacent to high-speed signal routing in complex signal layout designs, this paper proposes a practical structure that simplifies the design by segregating the general signal trace area and the high-speed signal trace area in PCB design. Rather than executing a complex manufacturing process to create patterns for the low loss dielectric material layer, the proposed structure involves grinding FR-4 in the high-speed signal trace area and bonding PTFE in its place. While this may lead to additional process costs akin to commercially applied hybrid PCBs, the proposed hybrid-plane PCB offers the advantage of utilizing a reduced quantity of low loss dielectric material. From a performance perspective, when comparing the hybrid-plane PCB structure that uses 30% and 50% of the total PCB width for the low loss dielectric material against the hybrid-stackup PCB, enhancements of 96% and 97.4% in signal quality, respectively, were observed. The electrical characteristics were found to be similar to those of the conventional structure.

Through simulation-based verification, this paper demonstrates that the hybrid-plane PCB significantly reduces the use of expensive low loss dielectric material compared to the previously employed hybrid-stackup PCB. Notably, it achieves similar electrical characteristics and signal quality improvements, effectively minimizing frequency loss. The application of the hybrid-plane PCB could reduce production costs for high-end and high-speed applications employing hybrid PCBs. Furthermore, it is anticipated that subsequent research aimed at improving the manufacturing process will expand the application of low loss hybrid PCBs to various fields within the electronics industry.

REFERENCES

[1] J. Liu, M. Zhang, and G. Hu, "Analysis of power supply and signal integrity of high speed PCB board," in *Proc. IEEE 8th Joint Int. Inf. Technol. Artif. Intell. Conf. (ITAIC)*, Chongqing, China, May 2019, pp. 412–416.

[2] Q. Wu, Y. Li, J. Liu, and Y. Jiao, "High speed muti-board signal integrity simulation and implementation," in *Proc. IEEE Int. Conf. Artif. Intell. Comput. Appl. (ICAICA)*, Dalian, China, Mar. 2019, pp. 444–447.

[3] T. Swirbel, A. Naujoks, and M. Watkins, "Electrical design and simulation of high density printed circuit boards," *IEEE Trans. Adv. Packag.*, vol. 22, no. 3, pp. 416–423, Aug. 1999.

[4] M. M. Mechaik, "Signal attenuation in transmission lines," in *Proc. IEEE 2nd Int. Symp. Quality Electron. Design*, San Jose, CA, USA, Mar. 2001, pp. 191–196.
[5] H. Inoue, M. Yasunaga, K. Kanazawa, and N. Aibe, "Signal integrity evaluation of segmental transmission line under real-world application," in *Proc. IEEE Electr. Design Adv. Packag. Syst. Symp. (EDAPS)*, Dec. 2013, pp. 108–111.
[6] H. Shimada, S. Akita, M. Ihiguro, M. Yasunaga, and I. Yoshihara, "Signal-integrity improvement based on the segmental-transmission-line," in *Proc. IEEE 20th Conf. Electr. Perform. Electron. Packag. Syst.*, San Jose, CA, USA, Oct. 2011, pp. 251–254.
[7] N. Idir, Y. Weens, and J.-J. Franchaud, "Skin effect and dielectric loss models of power cables," *IEEE Trans. Dielectr. Electr. Insul.*, vol. 16, no. 1, pp. 147–154, Feb. 2009.
[8] Y. Weens, N. Idir, R. Bausiere, and J. J. Franchaud, "Modeling and simulation of unshielded and shielded energy cables in frequency and time domains," *IEEE Trans. Magn.*, vol. 42, no. 7, pp. 1876–1882, Jul. 2006.
[9] H. A. Wheeler, "Formulas for the skin effect," *Proc. IRE*, vol. 30, no. 9, pp. 412–424, Sep. 1942.
[10] P. Waldow and I. Wolff, "The skin-effect at high frequencies," *IEEE Trans. Microw. Theory Techn.*, vol. MTT-33, no. 10, pp. 1076–1082, Oct. 1985.
[11] K. L. Ngai and C. T. White, "Frequency dependence of dielectric loss in condensed matter," *Phys. Rev. B, Condens. Matter*, vol. 20, no. 6, pp. 2475–2486, Sep. 1979.
[12] A. K. Jonscher, "Physical basis of dielectric loss," *Nature*, vol. 253, no. 5494, pp. 717–719, Feb. 1975.
[13] I. Nishimura, S. Fujitomi, Y. Yamashita, N. Kawashima, and N. Miyaki, "Development of new dielectric material to reduce transmission loss," in *Proc. IEEE 70th Electron. Compon. Technol. Conf. (ECTC)*, Orlando, FL, USA, Jun. 2020, pp. 641–646.
[14] A. K. Jonscher, "The 'universal' dielectric response," *Nature*, vol. 267, pp. 673–679, Jun. 1977.
[15] T. Su, J. Hsu, C. Ye, X. Ye, and A. Grigoras, "Signaling enabler in high-speed system design by using hybrid stackup printed circuit board," in *Proc. 8th Int. Microsyst. Packag. Assem. Circuits Technol. Conf. (IMPACT)*, Taipei, Taiwan, Oct. 2013, pp. 85–88.
[16] C. Méndez Ruiz, C. Ye, X. Ye, E. Lopez, M. Yin, J. Hsu, and T. Su, "Improve signal integrity performance by using hybrid PCB stackup," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, Denver, CO, USA, Aug. 2013, pp. 317–321.
[17] J.-I. Chen, S. He, and E. Zhang, "Characterization of low loss materials for high frequency PCB application," in *Proc. Int. Microsyst. Packag. Assem. Circuits Technol.*, Taipei, Taiwan, 2007, pp. 373–376.
[18] J. Zhang, A. C. Scogna, J. Fan, B. Archambeault, J. L. Drewniak, and A. Orlandi, "A hybrid stack-up of printed circuit board for high-speed networking systems," in *Proc. IEEE Int. Symp. Electromagn. Compat.*, Pittsburgh, PA, USA, Aug. 2012, pp. 554–559.
[19] K. Shenqing, H. Le, W. Fei, and Z. Mingmin, "Coplanar waveguide structure of the differential connector impedance control," in *Proc. 8th Int. Symp. Antennas, Propag. EM Theory*, 2008, pp. 1056–1059.
[20] B. C. Wadell, *Transmission Line Design Handbook*. Norwood, MA, USA: Artech House, 1991, pp. 413–419.

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