IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 18 December 2023, accepted 29 December 2023, date of publication 8 January 2024, date of current version 22 January 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3351184

RESEARCH ARTICLE

Overvoltage Protection of Series-Connected 10kV SiC MOSFETs Following Switch Failures in MV 3L-NPC Converter for Safe Fault Isolation and Shutdown

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ABSTRACT This paper presents a design methodology for overvoltage protection across 10kV SiC MOSFETs during turn-off after switch failure in a MV SST Power Conditioning System (PCS) enabled by a cascaded Three-Phase (3P) Three-level (3L) Neutral Point Clamped (NPC) Active Front-End Converter (AFEC) and Dual Active Bridge (DAB) using series-connected 10kV SiC MOSFETs and 10kV SiC JBS diodes. The methodology uses an active voltage clamp at the gate terminal and desat detection technique to identify abrupt open and turn-on switch failures across series-connected 10kV SiC MOSFETs. The analytical model estimates over-current time and turn-off voltage transition by considering bus bar inductance, device base plate capacitance and common mode (CM) choke tied between the heat sink and midpoint of the DC link capacitor. The transition model is used to evaluate the turn-off timing for series-connected MOSFETs, snubber resistors, snubber capacitors, and gate resistors to avoid MOSFET overvoltage during converter shutdown, without affecting the voltage balancing and efficiency during normal operation. The MOSFET turn-off transition during the shutdown has been verified in the Saber RD simulation using the validated Saber RD MAST model of 10kV SiC MOSFETs and 10kV SiC JBS diodes at 13.8kV AC/24kV DC level. The fault isolation and MV SST PCS shutdown have been verified in a real-time environment using HIL setup with Xilinx FPGAs and RTDS, at 13.8kV AC/24kV DC link under PCS operating conditions. The normal operation of 3L-NPC pole hardware with modified snubber resistors, snubber capacitors, and gate resistors is verified by experiments conducted at 7kV DC, 10A load current.

INDEX TERMS AsMPCS, fault, JBS, MOSFET, NPC, protection, RTDS, Saber, SiC, shutdown.

NOMENCLATURE

M_{11},M_{12}	Series-connected Top MOSFETs
M_{41},M_{42}	Series-connected Bottom MOSFETs
M_{31},M_{32}	Series-connected Top Mid-MOSFETs.
M_{41},M_{42}	Series-connected Bottom Mid-MOSFETs.
M_{ij}	Notation for MOSFETs in 3L-NPC pole, where $i = 1-4, j = 1-2$.
D_{ij}	Notation for clamping diodes in 3L-NPC pole, where $i = 1-4, j = 1-2$
m_{ij}	Modulation index of MOSFET M_{ij}
$C_{bs,Mij}$	Base plate capacitance of M_{ij}
$C_{bs,Dij}$	Base plate capacitance of D_{ij}.
$C_{s,Mij}$	Snubber capacitor across M_{ij}.
$C_{s,Dij}$	Snubber capacitor across D_{ij}.

The associate editor coordinating the review of this manuscript and approving it for publication was Francesco G. Della Corte.

$R_{s,Mij}$	Snubber resistor across M_{ij}.
$R_{s,Dij}$	Snubber resistor across D_{ij}.
$R_{goff,ij}$	Turn-off gate resistance for M_{ij}.
$t_{d,ij}$	Turn-off time delay between the series-connected 10kV SiC MOSFETs M_{i1} & M_{i2}.
p	Refers to p^{th} iteration. For initial value,p=0.
$R_{goff,ij}(p)$	Turn-off gate resistance for M_{ij}, in p_{th} iteration.
$C_{s,Mij}(p)$	Snubber capacitor across M_{ij}, in p_{th} iteration.
$C_{s,Dij}(p)$	Snubber capacitor across D_{ij}, in p_{th} iteration.
$R_{s,Mij}(p)$	Snubber resistor across M_{ij}, in p_{th} iteration.
$R_{s,Dij}(p)$	Snubber resistor across D_{ij}, in p_{th} iteration.
$t_{d,ij}(p)$	Turn-off time delay between the series-connected 10kV SiC MOSFETs M_{i1} & M_{i2}, in p_{th} iteration.
t_{AC}	Turn-off timing for AC circuit breaker.
t_{DC1}, t_{DC2}	Turn-off timing for DC circuit breaker.
L_{ch}	Common mode choke.
$L_{b,Mij}$	Parasitic bus bar inductance in path of M_{ij}.
$L_{b,Dij}$	Parasitic bus bar inductance in path of D_{ij}.
L_{mod}	Module package inductance.
L_p, L_s	Primary and Secondary inductance at AC terminal of DAB.
C_{oss}	Output Capacitance for M_{ij}.
t_k	Time interval with k discrete points, k=1-300.
$i_{s,Mij(t_k)}$	Snubber current through $R_{s,Mij}$ at time t_k.
$i_{s,Dij(t_k)}$	Snubber current through $R_{s,Dij}$ at time t_k.
$v_{ds,Mij(t_k)}$	Turn-off voltage across M_{ij} at t_k.
$v_{ds,Dij(t_k)}$	Turn-off voltage across D_{ij} at t_k.
$i_{bs,Mij(t_k)}$	Current through $C_{s,Mij}$ at t_k.
$i_{bs,Dij(t_k)}$	Current through $C_{s,Dij}$ at t_k.
$C_{s,D}$,$C_{s,M}$	Snubber capacitor across M_{ij} and D_{ij} for open heat sink, $i_{Cbs,Mij}(t_k)$=$i_{Cbs,Dij}(t_k)$=0.
$i_{ds,Mij(t_k)}$	Device drain current during switch failure.
V_{hs}	Heat sink voltage.
t_{bl}	Blanking time.
t_{sf}	Soft Turn-off time period.
t_r	Transition time to device blocking voltage during shutdown.
V_{DC}	DC link voltage.
I_z	Current injected at gate terminal during active voltage clamping.
$R_{on,ij}$	On state resistance across M_{ij}
$V_{on,Dij}$	On-state voltage drop across D_{ij}
$V_{lb,Mij}$	Voltage across parasitic $L_{b,Mij}$
$V_{lb,Dij}$	Voltage across parasitic $L_{b,Dij}$
t_d	Dead time
t_c	Delay between desat detection to shutdown signal generation.
t_{ov}	Over current time.
t_{CB}	Circuit Breaker response time.
t_{dt}	Maximum time gap in fault detection.

I. INTRODUCTION

The advancement of renewable energy technology has resulted in a growing demand for Medium Voltage (MV) Solid State Transformer (SST) Power Conditioning Systems (PCS), to control the flow of bidirectional power transfer and maintain a standard operating grid voltage and frequency for interconnection of Micro-grid to the grid and Micro-grid to Micro-grid [1]. The emergence of high-voltage SiC MOSFETs (10kV-15kV) and IGBTs has opened new opportunities for the development of MV SST PCS at 13.8kV AC/24kV DC interface, operating at 10-20kHz frequency [2]. The three-phase (3P) three-level (3L) neutral point clamped converter (NPC) has the potential to implement MV SST PCS, using cascaded Active Front End Converter (AFEC) and Dual Active Bridge (DAB), as shown in Fig. 1(a) [2].

The operation of the MV SST PCS at 24kV DC requires a soft start-up scheme to build up DC link voltage without high inrush currents [3], [4]. Sachin have demonstrated the regulation of DC link voltage and grid current during soft start-up operation for cascaded Medium Voltage (MV) AFEC and DAB [5]. The fault-tolerant controller (FTC) with soft start-up schemes has been developed for Modular Multilevel Converters (MMC) and MV Cascaded H-Bridge converters [6], [7], [8]. Existing literature has shown fault detection and shutdown schemes for 480V AC grid-interfaced converters [9], [10], [11], [12], [13], [14]. Sachin have demonstrated the shutdown of cascaded 3P-3L MV AFEC and DAB due to overvoltage detection [15]. However, the shutdown is not safe for mitigating the effect of open switch and turn-on switch failures in power converters. Predictive modeling control methods have been used for the diagnosis of open and turn-on switch failures in the 3-L NPC inverter, using the sparse matrix representation and the support vector machine approach [16], [17], [18], [19], [20]. The diagnosis implements fault-tolerant operation by identifying space vectors, that can operate the converter safely. Switch failures at 24kV DC result in an inrush current that can saturate the filter and transformer, therefore the affected 3L-NPC pole must be turned off safely and isolated from MV SST PCS during the shutdown [7]. Moreover, designing a shutdown scheme for MV SST PCS requires assessment of switch failures in DAB, where DAB operates using 3L square wave [21].

The ResNet and Wavelet Packet- RBF Neural Network have been utilized for the open switch failure diagnosis in 3-phase DAB [18], [22]. However, the diagnosis mechanism is complex due to the extraction of wavelet packet energy using artificial intelligence. A simple fault diagnosis strategy was proposed, to detect the DC component of transformer current [24]. However, this strategy could not diagnose the failed transistor. Hitherto, Rastogi et al. have identified the failed transistor for the two-level (2L) 3P DAB by evaluating the pattern of DC bias voltage [25]. The 3L-NPC converter generates a similar DC bias voltage for open switch failure across mid-MOSFETs, which makes it difficult to identify

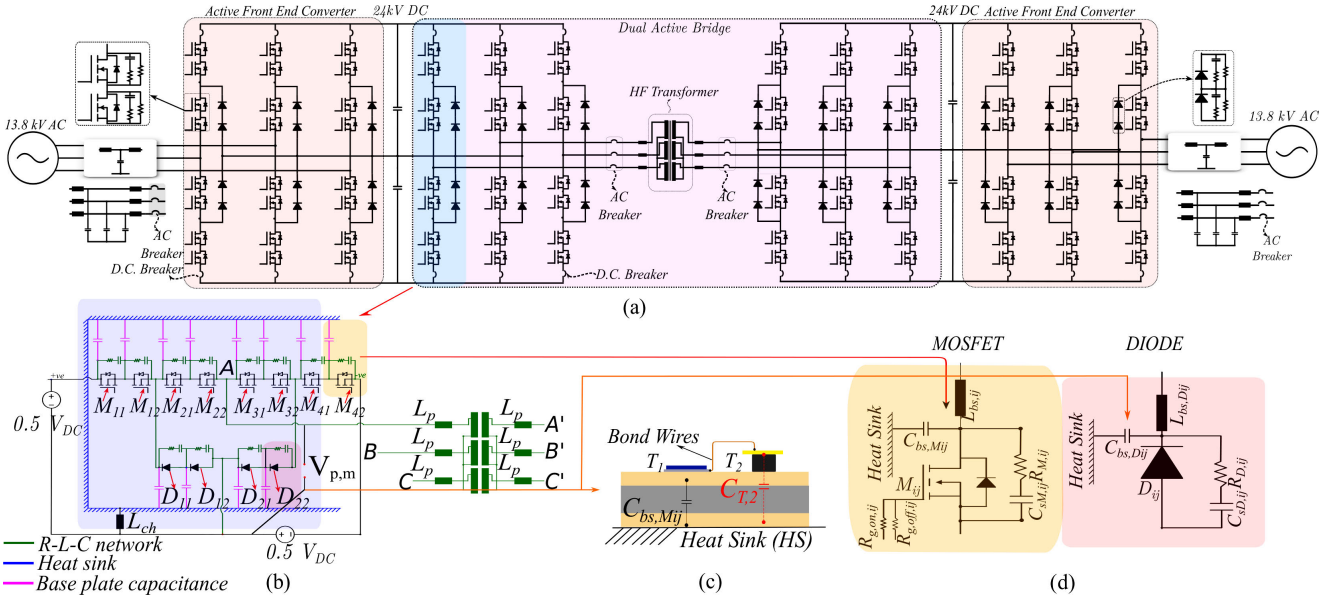


FIGURE 1. (a) Asynchronous Micro-grid power conditioning system with DC current interrupters and AC semiconductor switch across T_1 and T_2 i'n each pole [2].(b) The electrical structure of 3L NPC pole with base plate capacitance attached to the heat sink (c) The capacitance between the die and base plate of XHV-9 module (d) Schematic of the MOSFETs and Diodes with $C_{bs,Mij}$ and $L_{b,Mij}$. $C_{bs,Mij}$ = 0.2nF and Max($L_{b,Mij}$,$L_{b,Dij}$) = 230nH, Min($L_{b,Mij}$, $L_{b,Dij}$) = 120nH.

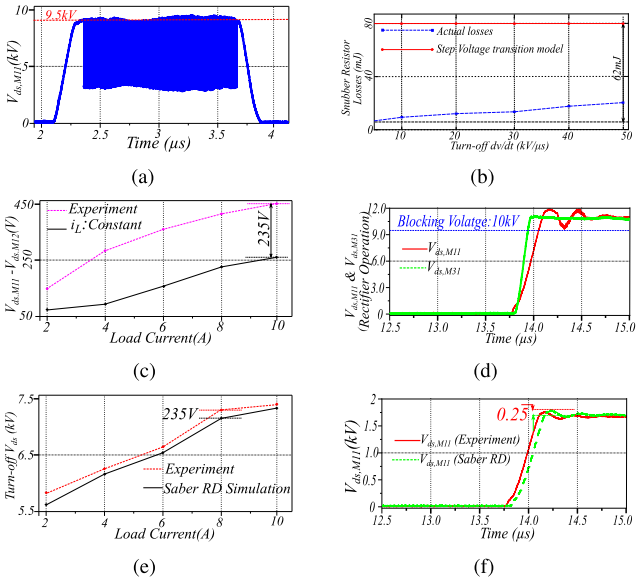


FIGURE 2. (a) Oscillation across $V_{ds,M11}$ due to current injection in gate terminal during the overvoltage clamping (b) Comparison between experimental data of snubber loss with the data obtained using step voltage transition. (c) Comparison of the experimental turn-off voltage mismatch in 3L-NPC pole with the circuit model considering constant current at load output (Deviation:235V,55% (max)) (d) Turn-off $V_{ds,M11}$ during conduction through MOSFET body diode after shutdown (e) Comparison of experimental $V_{ds,M11}$ with the Saber RD simulation results (Deviation:0.5%). (f) Experimental waveform of $V_{ds,M11}$ with Saber RD simulation at 6.6kV DC bus voltage for 10A load current (Deviation:0.4%).

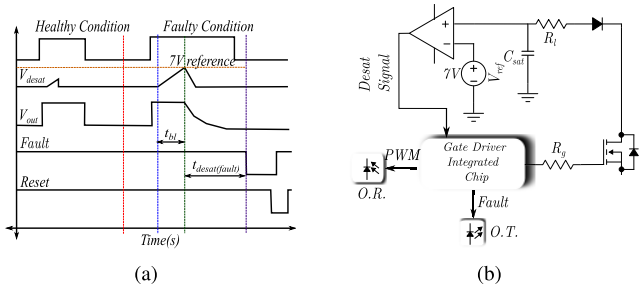
the failed MOSFET [24], [25], [26]. Therefore, the mid-point voltage has been utilized as a diagnosis criterion to identify the location of a switch failure in the triple-phase shift converter [27], [28], [29]. However, the process is slow and takes 20-25 switching cycles, whereas open switch failure across mid-MOSFETs M_{21}-M_{32} in 3L-NPC pole at 24kV DC causes avalanche breakdown in a single switching cycle, if it is not mitigated [30].

Unlike 480V AC applications, MV power converters such as PCS consist of 3L-NPC poles enabled by series-connected 10kV SiC MOSFETs and 10kV SiC JBS diodes, as shown in Fig. 1(b). The balancing resistor (R_B) is used to implement the static voltage balancing across series-connected SiC MOSFETs [31]. The dynamic voltage balancing (DVB) across series-connected 10kV SiC MOSFETs and 10kV SiC JBS diodes is implemented using R-C snubber [31], [32]. Existing literature has shown the desat detection and protection scheme to shut down the MV Solid State Transformer (SST), enabled by a 3L-NPC converter using 15kV SiC IGBTs [33]. It can detect open switch and short circuit failures within 10μs, which is faster than DC bias and mid-point voltage diagnosis [34]. However, the turn-on switch failure across a single SiC MOSFET in a series-connection cannot be detected instantly using the desat detection [35]. The turn-on failure across M_{11} causes overvoltage during turn-off across series-connected M_{12} [35]. The active clamp at the gate terminal turns-on M_{12}, thus creating a dead short circuit, which is identified by desat detection [35]. The active clamp has been demonstrated for clamping turn-off voltage after short circuit failure in series-connected 10kV SiC MOSFETs [36]. However, it results in oscillation across $V_{ds,Mij}$ due to repetitive charge and discharge of input capacitance (C_{iss}), as shown in Fig.2(a). Hence, the turn-off timing of series-connected SiC MOSFETs should be precise to avoid oscillation due to overvoltage clamping.

TABLE 1. Description of previous literature in the design of switch failure detection and protection scheme for power converters.

Literature	PWM Type	Protection Type Open switch failure	$C_{bs,Mij}$, L_{ch},$L_{b,Dij}$ $L_{b,Mij}$	$L_p + L_s$ & $C_{s,Mij}$ Oscillation	Back up failure Protection	Types of: Open Switch failure	Types of: Turn on Switch failure	Modification of 3L-NPC parameters:- Turn-on switch failure	Finite dv/dt Modeling (AFEC)
[16]	Space Vector	Model Predictive	×	×	×	×	×	×	×
[22]- [23]	Space Vector	Decoupled Sequence	×	×	×	×	×	×	×
[18] [22]- [23]	Space Vector	Wavelet & ResNET	×	×	×	×	×	×	×
[20]	Space	1-D CNN Network	×	×	×	×	×	×	×
[7], [35]	Sine Triangle	Desat detection Active Clamp	×	×	✓	×	✓	×	×
[15]	Sine Triangle & Square wave	Closed-loop Control	×	×	×	×	×	×	×
This paper	Sine Triangle & Square wave PWM	Desat detection, Active Clamp, $t_{d,ij}$	✓	✓	✓	✓	✓	✓	×

[II] The Column shows the type of PWM method on which different switch failures were analyzed for the literature article referenced in Column.II.
[III] Column III depicts open switch failure detection and protection strategy used by the literature mentioned in the column.I.
[IV] The sinusoidal oscillation qnd voltage overshoot created due to parameters C_{bs}, $L_{b,Mij}$ is considered as a criteria to compare existing literature.
[V] The sinusoidal oscillation in drain voltage $V_{ds,Mij}$ of Dual Active Bridge (DAB) due to power transfer inductance (L_p + L_s) and MOSFET snubber capacitance ($C_{s,Mij}$) as well as Diode snubber capacitance ($C_{s,Dij}$).
[VI] The detection of negative sequence components of AC and AFEC and DAB terminal is used as a backup for fault protection and detection when the desat detection system fails.
[VII] The open switch failure refers to sudden turn-off across: 1. Single MOSFETs M_{11} -M_{12}, 2. Series-connected MOSFETs M_{11}-M_{12},M_{21}-M_{22},M_{31}-M_{32} and M_{41}-M_{42} 3. Four SiC MOSFETs : M_{11}-M_{12},M_{21}-M_{22},M_{31}-M_{32} and M_{41}-M_{42}.
[VIII] The Turn-on switch failure refers to sudden short circuit across : 1. Single MOSFETs M_{11} -M_{12}, 2. Series-connected MOSFETs M_{11}-M_{12},M_{21}-M_{22},M_{31}-M_{32} and M_{41}-M_{42} 3. Four SiC MOSFETs : M_{11}-M_{12},M_{21}-M_{22},M_{31}-M_{32} and M_{41}-M_{42}.
[IX] Column IX compares the research work done by existing literature on mitigation of turn-on switch failure in power converters by adjusting the design parameters:1. Gate resistors ($R_{gs,Mij}$), 2. Snubber capacitors ($C_{s,Mij}$) 3. Snubber resistors ($R_{s,Mij}$).
[X] Finite dv/dt model is used for analyzing switching transition across series-connected SiC MOSFETs and JBS diodes in Active Front End Converter (AFEC), when certain MOSFET fails open or short (open and turn-on switch failure).



(a) (b)

FIGURE 3. (a) Timing diagrams for desat detection using V_{desat}, fault signal generation and system reset (b) Schematic of desat protection system, showing comparator of reference voltage generation.

The $t_{d,ij}$ adjustment has been used for minimizing overvoltage across series-connected SiC MOSFETs in 3L-NPC inverter with isolated heat sink, under normal operating condition [21], [37]. Fig. 1(b) shows the layout of twelve $C_{bs,Mij}$ in a 3L-NPC pole, which leads to higher turn-off voltage mismatch due to uneven $C_{bs,Mij}$ charging during switch failure, compared to normal operation. The $C_{bs,Mij}$ exists due to capacitance through the DBC substrate in the XHV-9 module, as illustrated in Fig. 1(c). The $C_{bs,Mij}$ and L_{ch} oscillate during t_d (dead time), resulting in V_{hs} overshoot, which further increases the voltage imbalance across series-connected MOSFETs. The effect of $C_{bs,Mij}$ on active voltage balancing has been studied for two-level converter [38]. It considers the step-turn-off voltage transition, which is suitable for high $\frac{dv}{dt}$ switching [39]. Fig. 1(d) shows R-C snubber across M_{ij} and D_{ij}, which reduces $\frac{dv}{dt}$ to 20kV/μs. The snubber loss estimated using the step voltage transition deviates from experimental data by 80% in Fig. 2(b). The finite $\frac{dv}{dt}$ transition has been used to analyze $V_{ds,Mij}$ across series-connected devices in the 3L-NPC inverter, by modeling load output as constant current. However, the model is suitable for inverters with $L_{fl} \gg$ 3mH for $t_d = 2.5\mu$s. Fig. 2(c) shows that experimental $V_{ds,M11}$-$V_{ds,M12}$ for 3P-3L DAB differs from the theoretical model if the load is approximated as a constant current source. Therefore, the equivalent circuit model of DAB load output should consider oscillation between L_p, L_s and $C_{s,Mij}$ during t_d.

The fault current through M_{ij} during the short circuit is unequal due to dissimilar $L_{b,Mij}$ and conduction through $C_{bs,Mij}$. Therefore, MOSFETs in the fault path have soft turn-off non-simultaneously, which results in device overvoltage during shutdown [36]. The converter shutdown is followed by the commutation of load current through the MOSFET body diode, which leads to overvoltage across M_{11} and M_{31}, as shown in Fig. 2(c). The $t_{d,ij}$ cannot mitigate overvoltage during soft turn-off and post-shutdown of the 3L-NPC pole. Therefore, passive R-C snubbers and $R_{goff,Mij}$ are adjusted to limit $V_{ds,Mij}$ during turn-off. The switching loss, DC offset voltage, and $V_{ds,Mij}$ mismatch during normal operation should be within specified limits using the modified value of R-C snubber and $R_{goff,Mij}$.

A fault detection scheme is required as a backup during circumstances, when desat detection scheme fails to operate. DC bias monitoring at load output responds slowly for failure detection and therefore is not suitable as a backup for failure detection [40].

This paper develops overvoltage protection for series-connected 10kV SiC MOSFETs to allow safe fault isolation of the affected 3L-NPC pole followed by shutdown of MV SST PCS during open and turn-on switch failures. Table 1 lists the comparison between the proposed methodology and existing literature. This research focuses on the analysis of open switch failures and the 3L-NPC shutdown scheme in the context of two distinct pulse width modulation (PWM) strategies addressed in column II of Table.1: sine triangle PWM for Active Front End Converter (AFEC) application and square wave PWM for 3-level 3-phase Dual Active Bridge (DAB) operation. In contrast to prior research, our approach integrates Active Voltage Clamping and introduces time delay adjustments across series-connected 10kV SiC MOSFETs to mitigate overvoltage following open switch failures, listed in column III.

In Column IV, we juxtapose our research with existing literature, highlighting sinusoidal oscillations among base plate capacitance (C_{bs}), CM choke (L_{ch}), and bus bar inductance ($L_{b,ij}$). Our paper further presents a model for the sinusoidal $V_{V_{ds,Mij}}$ arising from the interaction between power transfer inductance ($L_p + L_s$) and snubber capacitance for MOSFETs ($C_{s,Mij}$) and diodes ($C_{s,Dij}$) during the dead time period in the Dual Active Bridge, as listed in column V. This model accurately predicts voltage transitions during open and turn-on switch failures.

Column VI lists our approach to the utilization of the negative sequence component of AC port current at AFEC and DAB terminal, as a backup detection and protection when the desaturation detection and protection system fails.

In Columns VII and VIII, we compare our work with existing literature regarding open switch and turn-on switch failures. While prior research typically analyzes switch failures across single MOSFET/IGBT in 3L-NPC poles, our paper delves into open switch failures across single SiC MOSFETs (M_{11}-M_{12}), two series-connected SiC MOSFETs (M_{11}-M_{12}, M_{21}-M_{22}, M_{31}-M_{32}, and M_{41}-M_{42}), and four SiC MOSFETs (M_{11}-M_{22}, M_{21}-M_{32}, M_{31}-M_{42}). Since, the desaturation detection disables the PWM signal to the MOSFET gate terminal, our paper proposes a design algorithm for adjusting the passive components of series-connected 10kV SiC MOSFETs, specifically $R_{goff,Mij}$, $C_{s,Mij}$, and $R_{s,Mij}$,to mitigate overvoltage clamping during MOSFET turn-off after failure detection, as listed in column IX. Column X lists the transition model developed by this paper for turn-off $V_{ds,Mij}$ during switch failure in Active Front End Converter (AFEC) by considering a finite dv/dt during switching transition across complimentary MOSFETs.

The analysis of $V_{ds,Mij}$ transition is complex due to the involvement of multiple types of switch failure in AFEC and DAB, as well as circuit elements such as $C_{bs,Mij}$, $L_{b,Mij}$, L_p and L_{ch}. Therefore, Section.II discusses a simplified approach for analytical modeling to estimate the turn-off voltage transition after switch failures, using an iterative procedure to evaluate the effect of $C_{bs,Mij}$, $L_{b,Mij}$, and L_{ch} for 3L-NPC AFEC and DAB pole. Section.III discusses the evaluation of $t_{d,ij}$ and modification of 3L-NPC design parameters, such as $R_{g,offij}$,$R_{s,Mij}$ and $C_{s,Mij}$ to reduce turn-off voltage mismatch across series-connected MOSFETs during turn-off after switch failures. Section IV discusses the simulation and experimental results to verify the proposed overvoltage protection scheme. Fig. 2(e) shows that the Saber RD simulation of $V_{ds,M11}$ using MAST model of 10kV SiC MOSFETs and 10kV SiC JBS diodes is accurate up to 99.64% with respect to experimental results at different loads. Hence, $V_{ds,Mij}$ transition is verified using the Saber RD simulation, as confirmed by its correlation with experimental waveforms, depicted in Fig. 2(f) [41], [42], [43]. The shutdown mechanism of MV SST PCS has been verified by simulation in HIL environment [44], [45], [46]. The switching loss and turn-off voltage mismatch with modified design parameters in the 3L-NPC setup have been experimentally verified on 3L-NPC hardware at 7kV DC bus, 10A load current.

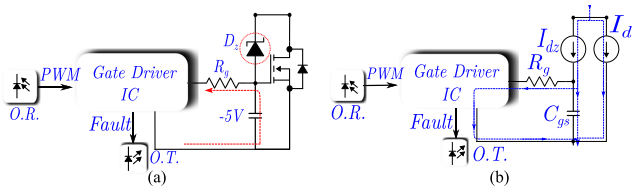


FIGURE 4. (a) Schematic of active voltage clamp circuit during normal operation (b) Operation of active voltage clamp during overvoltage detection (c) Single switch failures, Double switch failures and four switch failures (M_{11}-M_{22}, M_{21}-M_{22}, M_{31}-M_{42}) in 3L-NPC pole with series-connected devices.

II. FAULT ANALYSIS OF SERIES CONNECTED 10KV SIC MOSFET SWITCHES

The short circuit withstand time of Gen-3 10kV SiC MOSFET is 8.1μs at 6kV DC bus [36]. Fig. 3(a) shows the desat detection mechanism for the gate driver represented in Fig. 3(b). The desat detection system senses the over-current failure across MOSFETs. When the PWM signal is high and the voltage at the desat detection terminal is within the specified limit of 7V, the PWM signal is not affected. However, as shown in Fig. 3(a), when the voltage at desat detection terminal goes beyond 7V, the IC detects the failure and initiates a fault signal. The fault signal takes time $t_f = 2\mu$s to be detected. After fault detection, the signal is received by the control board, which initiates a turn-off signal across all the MOSFETs to shut down the converter pole. The turn-off signal across all MOSFETs is initiated with a certain time delay $t_{d,ij}$, in order to reduce the turn-off voltage mismatch across series-connected 10kV SiC MOSFETs so that they do not go in overvoltage.

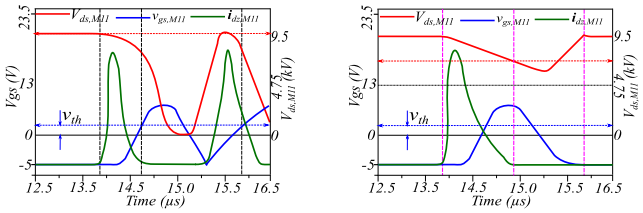


FIGURE 5. Saber RD simulation results for device drain voltage ($V_{ds,Mij}$), gate voltage ($v_{gs,Mij}$) and clamping diode current ($i_{dz,Mij}$) under condition,(a) The $v_{gs,Mij}$ discharges prior to $C_{s,Mij}$ discharge (b) The $v_{gs,Mij}$ discharges after $V_{ds,Mij}$ turn-on voltage value.

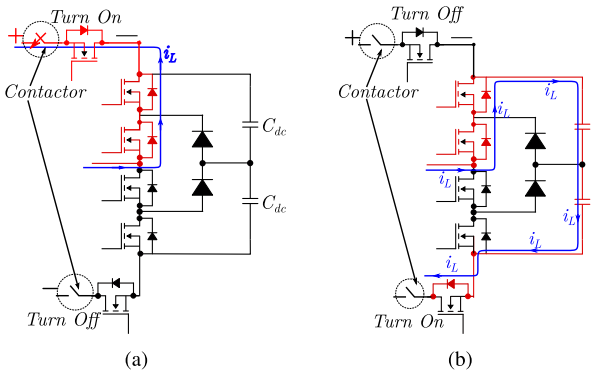


FIGURE 6. Operation of the circuit breaker situated at terminal T_1 & T_2 (a) Under normal condition (b) During fault isolation operation.

The TVS diode, positioned between the drain terminal of the MOSFET and the gate terminal of the diode, serves as a voltage clamp, activated when the drain-source voltage ($V_{ds,Mij}$) surpasses the breakdown limit of the TVS diode. In Fig.4(a), the overvoltage protection system for a series of connected 10kV SiC MOSFETs is depicted, when $V_{ds,Mij}$ is below the TVS diode breakdown limit. The equivalent circuit of the active voltage clamp is illustrated in Fig.4(b), engaging when the device's drain voltage exceeds the TVS diode breakdown limit. The TVS diode behaves as current source, controlled by drain voltage. During overvoltage clamping, a current is introduced into the gate terminal, causing a shift in gate voltage beyond the 4V threshold limit. This activation turns on the conduction channel of the MOSFET. The initiation of the MOSFET channel results in the discharge of $C_{s,Mij}$. Concurrently, $v_{gs,Mij}$ undergoes discharge, leading to two distinct dynamics in the $V_{ds,Mij}$ waveform:

(a): Fig.5(a) portrays $V_{ds,Mij}$ and $v_{gs,Mij}$ when the gate-source voltage discharges below the 4V threshold limit before snubber capacitor discharge. This scenario causes the MOSFET to turn off before reaching the on-state voltage.

(b): Fig.5(b) illustrates $V_{ds,Mij}$ and $v_{gs,Mij}$ when the snubber capacitor ($C_{s,Mij}$) discharges before $v_{gs,Mij}$ attains the 4V threshold limit. Consequently, the MOSFET remains turned on until $v_{gs,Mij}$ discharges below 4V.

The location of DC interrupter and AC switch for the 3L-NPC pole is shown in Fig. 1 [7]. The AC switch comprises

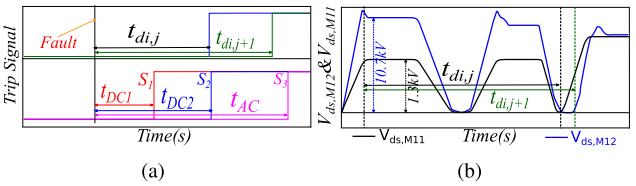


FIGURE 7. (a) Turn-off timing delay ($t_{d,ij}$,$t_{d,ij+1}$) represented with the drain-source voltage waveform (b) Waveform depicting the detection of the fault signal during the and turn-on switch failure.

two 15 kV SiC MOSFETs and anti-parallel SiC JBS diodes for current regulation, with two 10kV series-connected 15kV SiC MOSFETs serving as a backup to prevent bidirectional current flow in case of primary relay failure [35]. Upstream, a CEF-type fuse rated at 6A and 17.5 kV provides secondary protection [35]. Furthermore, within the PCS, a Metal Oxide Varistor (MOV) safeguards against overvoltage [47], [48]. The DC current interrupter located at terminal T_1 and T_2 utilizes a SiC MOSFET and a mechanical contractor to isolate the affected pole from the 24kV DC link [35]. Fig. 6(a) shows the normal operation of the DC current interrupter [35].

Fig. 7(a) illustrates the 3L-NPC pole isolation signal S_1, S_2 and S_3 with delay of t_{AC}, t_{DC1} and t_{DC2} [35]. $t_{d,ij}$ is maintained between the detection of failure and turn-off PWM signals for operating MOSFETs M_{ij}. Fig.7(b) shows turn-off $V_{ds,M11}$ and $V_{ds,M12}$ after applying $t_{d,ij}$ and $t_{d,ij+1}$. The signals are not sent immediately after failure detection, due to inherent propagation and processing delay in fault signal. Therefore, the $t_{d,ij}$ is delayed till $V_{ds,M11}$ clamps twice during failure. The switch with fast voltage transition is delayed to reduce the turn-off voltage mismatch. The signal S_1 and S_2 turns off the DC current interrupter, thus directing i_L through DC link capacitors, shown in Fig. 6(b) [35]. The DC link capacitor features a balancing resistance of 5MΩ, discharging the 24kV voltage within ($5 \times R \times C_{dc}$) = 750s, following the operation of the DC current interrupters.

A. OPEN SWITCH FAILURE IN 3L-NPC POLE

Fig. 8(a) shows $V_{ds,M31}$ and $V_{ds,M21}$ during open switch failure across M_{21} & M_{31}. Fig. 8(b) shows that open switch failure across either M_{31} and M_{32} leads to 24kV DC bus applied across them at the instant when M_{41} and M_{42} are on during normal operation. Similarly, a 24kV DC bus is applied during open switch failure across either of M_{21} and M_{22}, if M_{11} and M_{12} are on at the instant, as illustrated in Fig. 8(c). The open switch failure across either the top or bottom MOSFET leads to $V_{ds,Mij}$=12kV, which is above 10kV. Fig. 9 shows different switch failures in the 3L-NPC pole analyzed in this paper, which result from abrupt turn-off or turn-on of the switch, erroneous desat detection, or mechanical damage such as breaking of the optical fiber.

Fig. 10 shows the open switch failure detection across M_{12} and its subsequent turn-off across M_{11} immediately. The failure is detected after t_d+t_{bl} when the PWM signal is high, as shown in Fig. 11(a). However, the turn-on switch

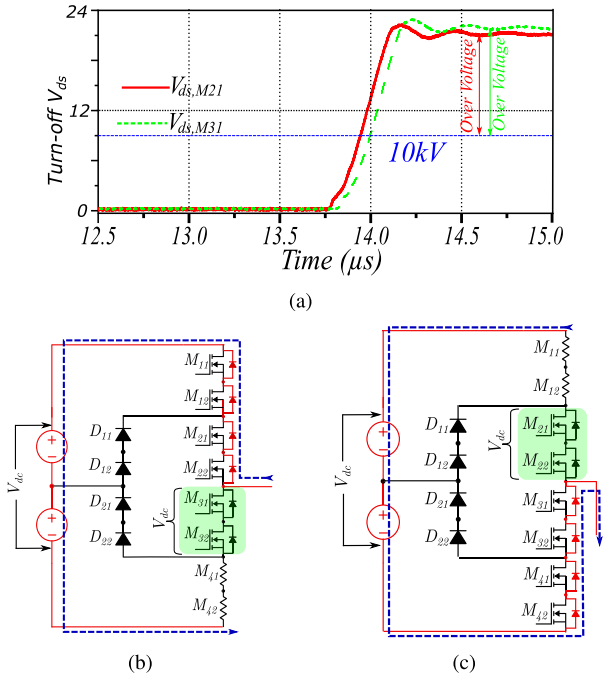


FIGURE 8. (a) $V_{ds,M21}$ and $V_{ds,M31}$ during single open switch failure across M_{21} & M_{31}, 24kV DC bus applied failed mid MOSFETs when (b) Switch M_{31} or M_{31} have and (c) Switch M_{21} or M_{22} have open switch failure.

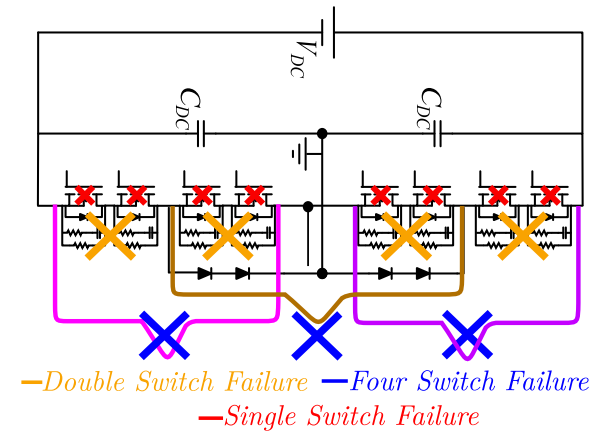


FIGURE 9. Single switch failures, Double switch failures and four switch failures (M_{11}-M_{22}, M_{21}-M_{22}, M_{31}-M_{42}) in 3L-NPC pole with series-connected devices.

failure is detected after complimentary MOSFET M_{31} turns on, as shown in Fig.11(b). The internal design of the gate driver for the safe operation of MV SST PCS requires t_{bl} = 0.5μs, t_d = 1.5μs and t_c = 1.5μs [2]. The fault signal from M_{11} detects the over-current failure and initiates a shutdown signal. Fig. 12(a) shows the sine triangle PWM scheme for AFEC, for which the maximum failure detection time (t_{dt}) is listed in Table 2. Fig. 12(b) shows the square wave PWM scheme for DAB, with t_{dt} listed in Table 2. Table 2 lists the minimum t_{ov} and peak driving voltage during open switch failures in the 3L-NPC pole used for AFEC and DAB operation.

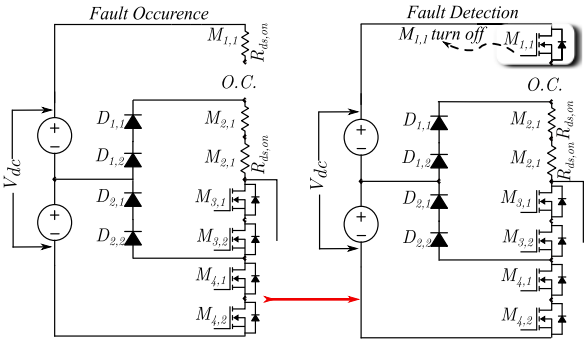


FIGURE 10. Open switch failure detection across M_{11} using desat detection method and its subsequent turn-off.

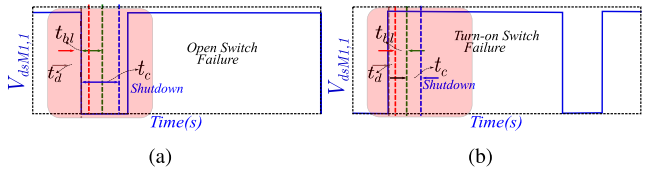


FIGURE 11. (a) Turn-off timing for the respective switches, DC and AC circuit breaker during 3L-NPC pole fault isolation (b) Waveform depicting the detection of the fault signal during the open switch failure.

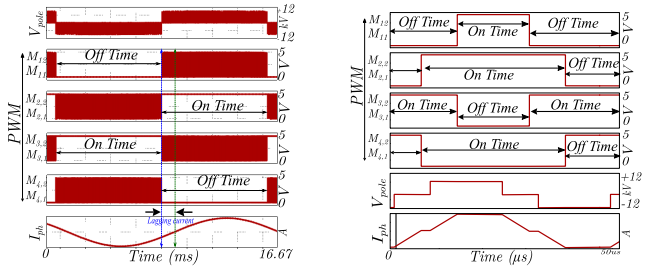


FIGURE 12. (a) PWM structure of the three-Level AFEC with gate driver signals for four switches (b) PWM structure of the three-level DAB with gate driver signals for four switches.

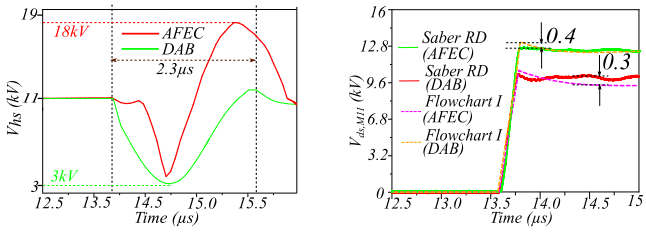


FIGURE 13. (a) Heat sink voltage during failure across switch M_{11} in 3L NPC pole for sine triangle and square wave operation.(b) Turn-off waveform of $V_{ds,M11}$ after single switch open circuit failure across M_{11} in AFEC and DAB, compared with the waveform obtained by Flowchart I (maximum deviation:0.6%).

The $t_{d,ij}$ for mid-MOSFETs should be higher than top or bottom MOSFETs, to avoid the overvoltage across mid-MOSFETs, during the 3L-NPC fault isolation and shutdown.

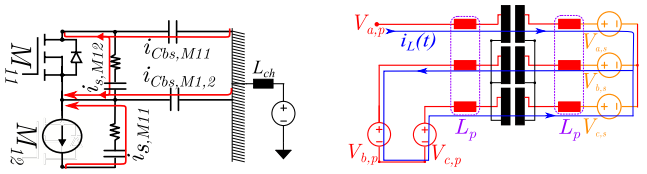


FIGURE 14. (a) $i_{s,Mij}$ conduction through the functioning M_{ij} and failed M_{ij} during open switch fault (b) Equivalent circuit of pole output for DAB during $V_{ds,Mij}$ transition.

TABLE 2. Minimum over-current detection time for open switch failure in AFEC and DAB.

	Active Front End Converter			Dual Active Bridge		
Failure Type	t_{ov}	t_{dt}	Peak Driving	t_{ov}	t_{dt}	Peak Driving
Single Switch	40.67ms	8.34ms	23.9 kV	2.34ms	25µs	12 kV
Double Switch	18.67ms	8.34ms	25.8 kV	2.34ms	25µs	12 kV
Four Switch	22ms	0.1ms	23.9 kV	1.17ms	25µs	24 kV

Fig. 13(a) shows that V_{hs} oscillates between 18kV to 3kV during open switch failure across M_{11}, which further increases voltage imbalance across series-connected MOSFETs. Fig.14(a) illustrates the equivalent circuit model for the functioning switch (M_{11}) and failed switch (M_{12}). Fig. 14(b) shows the equivalent circuit of DAB load output, which considers the impact of LC oscillation between ($L_p + L_s$) and $C_{s,Mij}$ on $V_{ds,Mij}$ during failure. The equivalent circuit for load output for AFEC is a constant current source [21]. The voltage transition between complementary MOSFETs are related by (1)-(3)

$$\sum_{i=1}^{4}\sum_{j=1}^{2} m_{ij}V_{ds,Mij} = V_{DC} \tag{1}$$

$$\sum_{i=1}^{2}\sum_{j=1}^{2} m_{ij}V_{ds,Mij} + \sum_{i=1}^{2}\sum_{j=1}^{2} m'_{ij}V_{ds,Dij} = \frac{V_{DC}}{2} \tag{2}$$

$$\sum_{i=3}^{4}\sum_{j=1}^{2} m_{ij}V_{ds,Mij} + \sum_{i=3}^{4}\sum_{j=1}^{2} m'_{ij}V_{ds,Dij} = \frac{V_{DC}}{2} \tag{3}$$

The snubber current across the SiC MOSFET and SiC JBS diode is calculated as follows (4)-(5)

$$V_{ds,Mij}(t_{k+1}) = R_s \times i_{s,Mij}(t_k) + \frac{(i_{s,Mij}(t_k) - i_{Cbs,Mij}(t_k)) \times \Delta t}{C_s, Mij} + V_{ds,Mij}(t_k) \tag{4}$$

$$V_{ds,Dij}(t_{k+1}) = R_{s,Dij} \times i_{s,Dij}(t_k) + \frac{(i_{s,Dij}(t_k) - i_{Cbs,Dij}(t_k)) \times \Delta t}{C_{D,ij}} + V_{ds,Dij}(t_k) \tag{5}$$

The m_{ij} is considered zero for the failed and turned-off switches. Using (1) - (5) and switching states from Table 3,

TABLE 3. Switching States of the 3L- NPC pole during normal operating conditions.

		Switching Patterns		
Pole output	M_{11}, M_{12}	M_{21}, M_{22}	M_{31}, M_{32}	M_{41}, M_{42}
$0.5V_{DC}$	ON	ON	OFF	OFF
0	OFF	ON	ON	OFF
$-0.5V_{DC}$	OFF	OFF	ON	ON

the snubber current during open switch failure across single MOSFET is calculated as follows (6)

$$i_{s,Mij}(t_k) = i_{s,Dij}(t_k) = \frac{I\left(C_{s,D}R_{s,D} - C_{s,T}R_{s,T}\right) e^{-\frac{C_{D.ij}t + 2C_{M,ij}t}{2C_{ds}C_{ms}R_{s,Dij} + C_{D.ij}C_{ms}R_{s,Dij}}}}{(2R_{s,D} + R_{s,M}) \times (C_{s,D} + 2C_{s,M})} \tag{6}$$

The snubber current during open switch failure across two series-connected MOSFETs is calculated by (7)

$$i_{s,Mij}(t_k) = i_{s,Dij}(t_k) = \frac{I(4R_{s,D}C_{s,D} - 8R_{s,T}C_{s,T})e^{-e^{-\frac{C_{s,D}t + 2C_{s,T}t}{2C_{s,D}C_{s,T}R_{s,D} + C_{s,D}C_{s,T}R_{s,T}}}}}{(R_{s,D} + 2R_{s,T}) \times (C_{s,D} + 2C_{s,T})} \tag{7}$$

The snubber current through DAB during single switch failure is calculated by (8)

$$i_{s,Mij}(t_k) = i_{s,Dij}(t_k) = \frac{I\,(8C_{sD}R_{sD})\,sin(\frac{1}{3\sqrt{((L_p+L_s)(C_{s,D}+C_{s,M}))}})e^{-\frac{C_{Dij}t + 2C_{Mij}t}{2C_{ds}C_{ms}R_{sDij}}}}{(2R_{sD} + 4R_{s,T}) \times (2C_{s,D} + 6C_{s,T})} \tag{8}$$

Similarly, the snubber current during failure across two series-connected MOSFETs is calculated by (9)

$$i_{s,Mij}(t_k) = i_{s,Dij}(t_k) = \frac{I\left((6C_{s,T}R_{s,T})sin(\frac{1}{3\sqrt{((L_p+L_s)(C_{s,D}+C_{s,M}))}})\right) e^{-\frac{C_{D.ij}t + 2C_{T,ij}t}{2C_{ds}C_{ms}R_{s,Dij}}}}{(2R_{s,D} + 4R_{s,T}) \times (2C_{s,D} + 6C_{s,T})} \tag{9}$$

Eq.(7) & (9) are valid for the failure across four SiC MOSFETs in 3L-NPC pole. The gate-source voltage of the failed switch is calculated by (10)

$$v_{gs}(t) = -V_{EE} + (V_{DD} + V_{EE}) \times (1 - e^{\frac{-t_k}{C_{iss}R_g}}) \tag{10}$$

The $i_{s,Mij}(t_k)$ evaluated using (6)-(9) is independent of $i_{bs,Mij}$ and $L_{b,Mij}$. Fig. 15 shows the commutation path of $i_{bs,Mij}$ through $C_{bs,Mij}$, during $V_{ds,Mij}$ transition. This transition time is utilized to determine the base plate current flowing through MOSFETs, which is computed as follows

$$i_{bs,Mij}(t_k) = C_{bs,Mij}\frac{\sum_{i=1}^{4}\sum_{j=1}^{2}\sum_{i=1}^{300} V_{ds,Mij}(t_{k+i}) + \sum V_{hs}(t_{k+1})}{\Delta t} \times m_{ij} \tag{11}$$

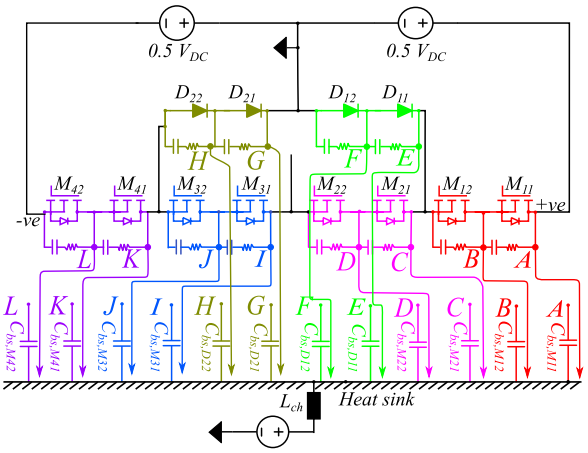


FIGURE 15. Base plate current ($i_{Cbs,Mij}$) conduction through $C_{bs,Mij}$ during switching transition.

where, m_{ij}=1 for MOSFETs witnessing switching transition.

The heat sink voltage just before the failure can be determined as follows

$$V_{hs}(t_0) = 0.5\ V_{DC} \tag{12}$$

The $V_{hs}(t_k)$ during the shutdown process is calculated as follows

$$V_{hs}(t_k) = V_{hs}(t_{k-1}) + C_{bs,Mij} \frac{\sum_{i=1}^{4}\sum_{j=1}^{2}\sum_{k=1}^{300} V_{ds,Mij}\,(t_{k+1}) - \sum_{k=1}^{300} V_{hs}\,(t_{k+1})}{\Delta t^2} \tag{13}$$

The voltage drop at inductance ($L_{b,Mij}$) after turn-off failure is calculated as follows

$$L_{b,Mij} \frac{i_{s,Mij}\,(t_{k+1}) - i_{s,Mij}\,(t_k)}{\Delta t} m_{ij} = V_{lb,Mij}(t_k) \tag{14}$$

The computation of the snubber current for the subsequent iteration is done as follows

$$i_{s,Mij}(t_k) = 0.5 \times i_{s,Mij}(t_{k-1}) + 0.5 \times C_{bs,Mij} \frac{\sum\sum_{k=1}^{300} V_{ds,Mij}\,(t_{k-1})}{\Delta t} \times m_{ij} \tag{15}$$

$$i_{s,Dij}(t_{k+1}) = 0.5 \times i_{s,Dij}(t_k) + 0.5 \times C_{bs,Dij} \frac{\sum\sum_{i=1}^{300} V_{ds,Dij}\,(t_{k-1})}{\Delta t} + \frac{\sum V_{hs}\,(t_k)}{\Delta t} \times m_{ij} \tag{16}$$

Eq.(17) evaluates the error (ϵ) between 0.5 V_{DC} and the sum of turn-off voltage across SiC MOSFETs and SiC JBS diodes

$$\sum_{i=1}^{i=2}\sum_{j=1}^{j=2} V_{ds,Mij}(t_r) + \sum_{i=1}^{i=2}\sum_{j=1}^{j=2} V_{lpi,j}(t_r) - 0.5V_{DC} = \epsilon \tag{17}$$

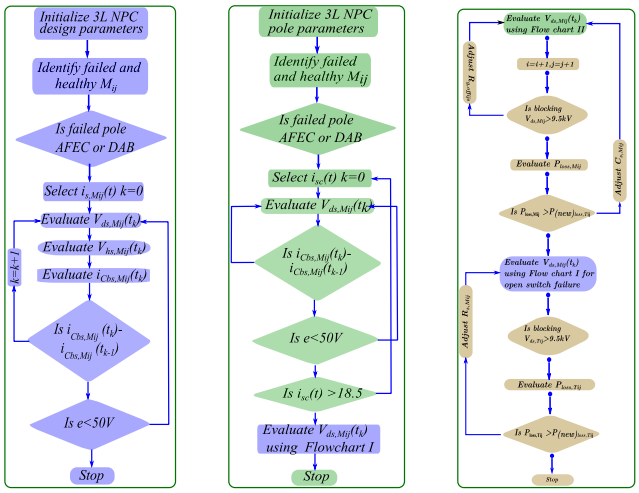


FIGURE 16. (a) Flow chart I depicting evaluation of V_{ds} during different open switch failures. (b) Flow chart II depicts the evaluation of V_{ds} during different turn-on switch failures. (c) Flow chart III depicts the Modification of design parameters ($R_{goff,ij}$,$C_{s,Mij}$ and $R_{s,Mij}$) to reduce overvoltage during shutdown of the affected 3L-NPC pole after switch failure.

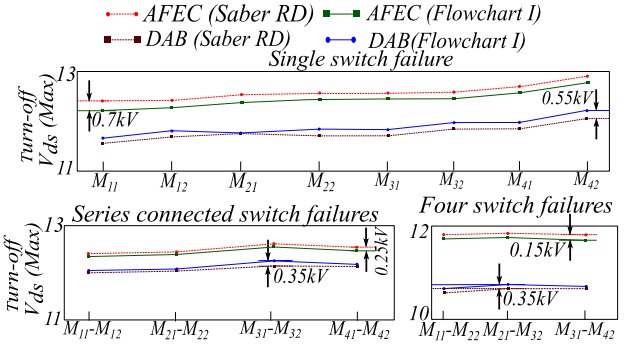


FIGURE 17. Saber Rd simulation data for maximum turn-off voltage during open switch failure.The results obtained from Flowchart II deviate from the simulation by 0.3%. (Y-axis: Maximum Blocking Voltage, X-axis: Notation of the failed MOSFET).

The t_r is updated for integral in (15)-(17) as follows

$$\sum_{i=1}^{i=2}\sum_{j=1}^{j=2} V_{ds,Mij}(t_r) = 0.5V_{DC}. \tag{18}$$

Fig. 13(b) shows the $V_{ds,M11}$ waveform calculated till ϵ < 50V, using Flowchart I illustrated in Fig. 16(a). Similarly, maximum turn-off $V_{ds,Mij}$ was plotted for different open switch failures in Fig. 17, which shows that the device turn-off voltage crosses 9.5kV (TVS diode rating) during each switch failure.

B. TURN-ON SWITCH FAILURE IN 3L-NPC POLE

The unexpected short circuit across MOSFETs or a false PWM logic signal may lead to turn-on switch failure. Fig. 18(a) shows the conduction path of inductive load current after the turn-on switch failure across series-connected M_{21} and M_{22} in DAB. The failure causes DC offset voltage, which

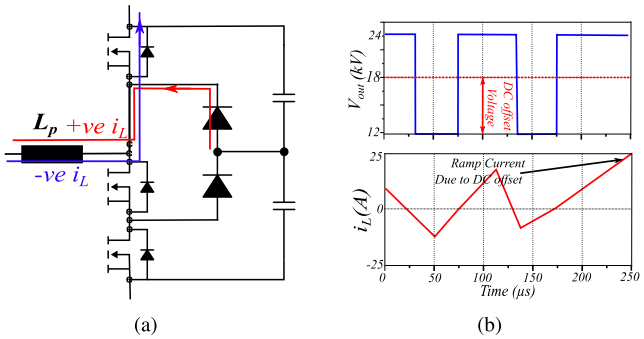


FIGURE 18. (a) Conduction path for load current during turn-on switch failure across Top Mid-MOSFETs (M_{21} & M_{22}) after converter shutdown.(b) 3L-NPC pole output voltage ($V_{out}(kV)$) and load current ($i_L(A)$) after turn-on failure. The output voltage has DC-offset component, which results in linearly increasing DC-offset current at load output.

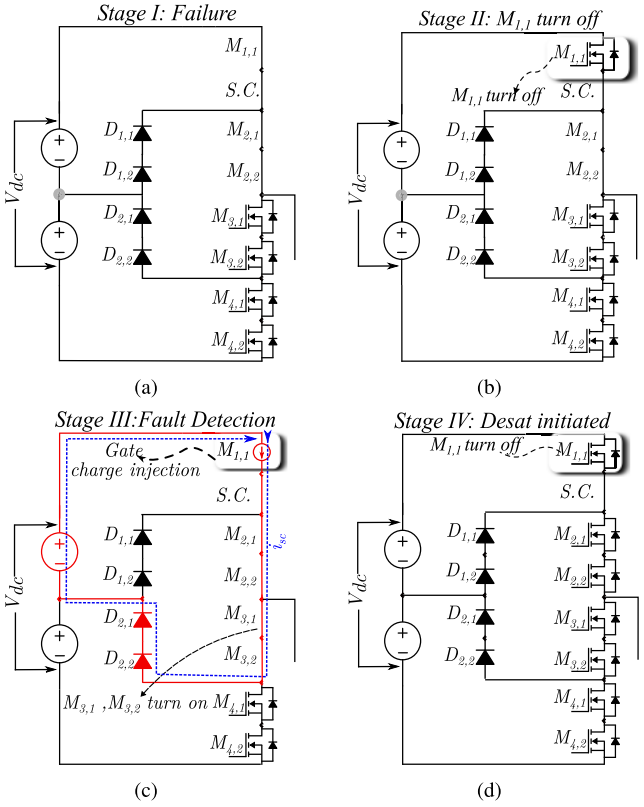


FIGURE 19. (a) Stage I: Initiation of turn-on failure in M_{12} (b)Stage II: Turn-off across M_{11} due to PWM (c) Stage III: Turn-on across M_{31} & M_{32}, leading to short circuit (d) Soft turn-off initiated by desat protection system.

leads to a linearly ramping current at the output terminal, as shown in Fig. 18(b). The current will saturate L_p and filter inductors, if the affected 3L-NPC pole is not turned off and disconnected from MV SST PCS.

Fig. 19 depicts the failure detection and shutdown of the 3L-NPC pole after false turn-on across M_{12}. Fig. 19(a) shows Stage I when the fault is initiated. The series-connected 10kV SiC MOSFET M_{11} turns off due PWM signal in Stage II, which is shown in Fig. 19(b). It results in 0.5 V_{DC} = 12kV being shared across M_{11}. Fig. 19(c) shows Stage III, when active clamp causes M_{11} to turn on, leading to a short circuit. The MOSFETs in the fault path have a soft turn-off after failure detection, as shown in Fig. 19(d).

The shutdown is followed by fault isolation of 3L-NPC pole, using S_1, S_2 and S_3, described in [35]. The timing waveform of turn-on switch failure and 3L-NPC pole shutdown is shown in Fig. 11(b). The fault current flows across six MOSFETs and two series-connected 10kV SiC JBS diodes. Fig. 20(a) shows an equivalent circuit of turn-on switch failure across M_{12}, after the complimentary M_{31}-M_{32} turns-on. Fig. 20(b) and Fig. 20(c) show the equivalent circuit of 3L-NPC pole during turn-on switch failure across two SiC MOSFETs and four SiC MOSFETs. A similar equivalent circuit can be derived for other turn-on switch failures at different locations in 3L-NPC pole, as illustrated in Fig. 9. The $i_{ds,Mij}$ during Stage III is calculated as follows

$$i_{ds,Mij} = g_M \times \left(v_{gs}(t_k) - v_{th}\right) + C_{oss} \times \frac{V_{ds,Mij}\,(t_{k+1}) - V_{ds,Mij}\,(t_k)}{t_{k+1} - t_k} + i_{s,Mij}(t_k) \quad (19)$$

Using (19) and (1)-(4), $i_{ds,Mij}$ is listed in Table 4 for different turn-on switch failures. The $i_{ds,Mij}$ is similar for turn-on failure across two MOSFETs and four MOSFETs in the 3L-NPC pole. Table 5 can be substituted in (1)-(4) & (19) for analytical expression of $V_{ds,Mij}$ and $i_{ds,Mij}$. The $0.5V_{DC}$ and $i_{ds,Mij}$ are related as follows

$$\frac{1}{2}V_{DC} = \sum_{i=1}^{4}\sum_{j=1}^{j=2}((L_{b,ij} + L_{mod})(\frac{i_{ds,Mij}(t_{k+1})}{\Delta t} - \frac{i_{ds,Mij}(t_k)}{\Delta t})) \quad (20)$$

Fig. 21(a) shows that V_{hs} oscillate between 23kV to 9.5kV, which leads to turn-off voltage mismatch across series-connected 10kV SiC MOSFETs. The analytical V_{hs} is calculated using (13) -(14). The t_{sf} is evaluated as follows

$$t_{sf} = (\frac{52}{v_{th,ij} + VEE}) \times R_{goff,ij} \times C_{iss,ij} \quad (21)$$

The soft turn-off interrupts fault current through the device channel. The V_{ds} transition after turn-off is calculated similarly to open circuit failure using (4)-(5). The Flowchart II illustrated in Fig. 16(b) evaluates $V_{ds,Mij}$ during shutdown after turn-on failure. The Saber RD simulation waveform for short circuit failure across M_{11}, shown in Fig. 21(b) validates $V_{ds,M11}$ obtained using Flowchart II. The flowchart was used to evaluate maximum turn-off V_{ds} during different turn-on switch failures, as illustrated in Fig. 22. The highest value is 12.7kV for $V_{ds,M41}$ during turn-on switch failure across M_{41} and M_{42}.

Table 5 lists over-current and fault detection time for different turn-on switch failures, calculated using $i_{sc,Mij}$ from Flowchart II. Fig. 23(a) illustrates the impact of R-C snubber on the $i_{sc,M11}$ and $i_{sc,M31}$. Snubber capacitors slow down

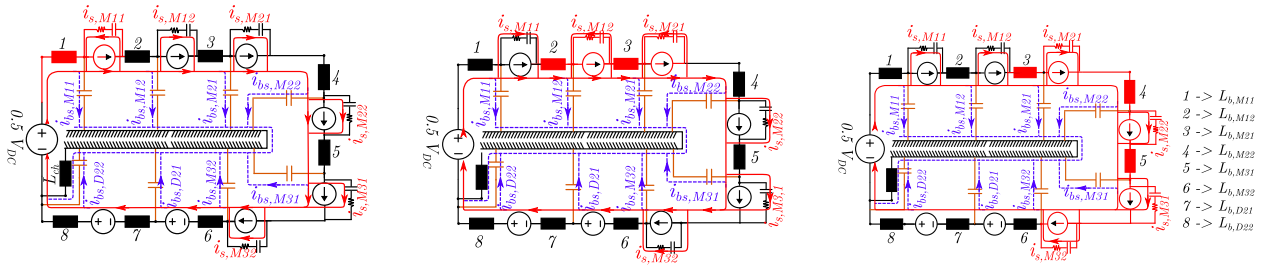


FIGURE 20. Equivalent circuit for short circuit in Stage III after detecting turn-on switch failure across (a) Single SiC MOSFET M_{12}. (b) Series-connected SiC MOSFET M_{11}-M_{12} (c) Four SiC MOSFET M_{11}-M_{22}.

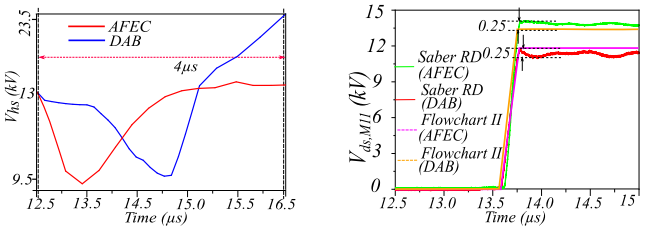


FIGURE 21. (a) Heat sink voltage during failure across switch M_{12} in 3L NPC AFEC and DAB pole.(b) Turn-off waveform of $V_{ds,M11}$ after turn-on failure across M_{12} in AFEC and DAB (maximum deviation:0.4%).

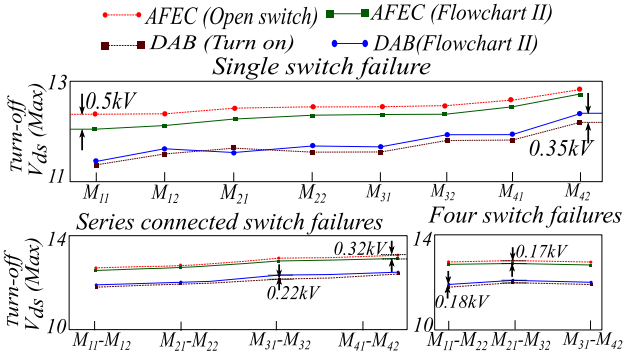


FIGURE 22. Saber Rd simulation data of maximum turn-off voltage mismatch during different turn-on switch failures in 3L-NPC pole. The results obtained from Flowchart II deviate from the simulation by 0.3%.

current surge, introducing a delay in the current rise, which reduces $\frac{dv}{dt}$ and $\frac{di}{dt}$, preventing high voltage overshoot due to $L_{b,ij}$. Fig. 23(b) shows the Saber simulated waveform of $i_{sc,M11}$ & $i_{sc,M31}$ during turn-on failure across series-connected M_{11} & M_{12}. The current rises rapidly during turn-on failure across series-connected 10kV SiC MOSFETs, due to the absence of any open switch in the path of the fault current.

III. MODIFICATION OF 3L-NPC PARAMETERS

Fig. 16(c) illustrates Flowchart III, used to modify design parameters for the 3L-NPC pole to limit the $V_{ds,Mij}$ within 9.5kV (TVS diode rating), following the shutdown of the MV SST PCS. The initial value of $t_{d,ij}$ is calculated to reduce to

TABLE 4. Drain current $i_{ds,Mij}$ during different turn on switch failures in 3L-NPC pole.

Type of Failure	Analytical expression
	Active Front End Converter
Single Switch	$(\frac{g_{m,ij}I_z t}{3R_{s,M}C_{oss}} - \frac{g_{m,ij}I_z t}{3(R_{s,M}C_{oss})^2})\, e^{(\frac{1}{R_{s,M}C_{s,M}} - \frac{1}{R_{s,M}C_{oss}})} + \frac{g_{m,ij}I_z + v_{th}}{3R_{s,M}C_{oss}}\, e^{(\frac{1}{R_{s,M}C_{s,M}} - \frac{1}{R_{s,M}C_{oss}})}$
Double Switch & Four Switch	$I_L e^{-\frac{\sum_{i=1}^{4}\sum_{j=1}^{j=2} R_{on,ij}}{\sum_{i=1}^{4}\sum_{j=1}^{j=2}(L_{b,ij}+L_{mod})}} + \frac{V_{DC}}{\sum_{i=1}^{4}\sum_{j=1}^{j=2} R_{on,ij}} \times (1 - e^{-\frac{\sum_{i=1}^{4}\sum_{j=1}^{j=2} R_{on,ij}}{\sum_{i=1}^{4}\sum_{j=1}^{j=2}(L_{b,ij}+L_{mod})}})$
	Dual Active Bridge
Single Switch	$(\frac{g_{m,ij}I_z t}{3R_{s,M}C_{ds}} - \frac{g_{m,ij}I_z t}{1.5(R_{s,M}C_{s,M})^2})\, e^{(\frac{1}{R_{s,M}C_{s,M}} - \frac{1}{R_{s,M}C_{oss}})} + \frac{0.5V_{DC}}{L_p+L_s} e^{-\frac{R_{s,M}+R_{s,D}}{L_p+L_s}}$
Double Switch & Four Switch	$\frac{V_{DC}}{\sum_{i=1}^{4}\sum_{j=1}^{j=2} R_{on,ij}} \times (1 - e^{-\frac{\sum_{i=1}^{4}\sum_{j=1}^{j=2} R_{on,ij}}{\sum_{i=1}^{4}\sum_{j=1}^{j=2}(L_{b,ij}+L_{mod})}}) + \frac{0.5V_{DC}}{L_p+L_s} e^{-\frac{R_{s,M}+R_{s,D}}{L_p+L_s}}$

TABLE 5. Over-current and fault detection time during turn-on failure.

Failure Type	t_{ov}	t_{ov}+t_{bl} +t_c	Failure Type	t_{ov}	t_{ov}+t_{bl} +t_c
M_{11}	25.65μs	28.65μs	M_{31}	35.65μs	38.65μs
M_{12}	35.23μs	38.23μs	M_{32}	42.65μs	45.65μs
M_{21}	29.65μs	32.65μs	M_{41}	28.71μs	31.71μs
M_{22}	31.23μs	34.23μs	M_{42}	32.71μs	32.71μs
M_{11}-M_{12}	18.41μs	21.41μs	M_{21}-M_{22}	20.73μs	23.73μs
M_{31}-M_{32}	17.42μs	20.42μs	M_{41}-M_{42}	19.67μs	22.67μs
M_{11}-M_{22}	19.41μs	22.41μs	M_{21}-M_{32}	20.73μs	23.73μs
M_{31}-M_{42}	18.42μs	21.42μs			

reduce V_{ds} mismatch during turn-on switch failure (22)

$$t_{d,ij}(0) = \left(\frac{i_L}{3} - C_{bs,Mij}\frac{(V_{hs}(t_{k+1}) - V_{hs}(t_k))}{\Delta t}\right) \quad (22)$$

The initial value of $R_{g-off,ij}$ is calculated as follows

$$R_{g-off,ij}(0) = \frac{1}{t_d} ln \frac{V_{th,ij}}{V_{DD} + V_{EE}} \quad (23)$$

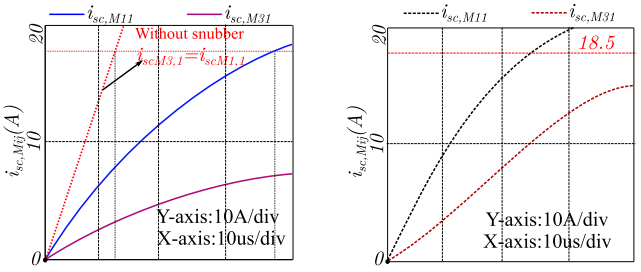


FIGURE 23. Short circuit current waveform ($i_{sc,M11}$ & $i_{sc,M31}$) obtained using Saber RD simulator for (a) Single turn-on failure across M_{12} (b) Turn-on failure across series-connected M_{21} & M_{22}.

The $R_{g,offij}(p)$ is adjusted to account for the effect of L_{ch} and $C_{bs,Mij}$ on the turn-off voltage mismatch as follows

$$\frac{R_{g,offij}\,(p+1)}{R_{g,offij+1}\,(p+1)} = \frac{R_{g,offij}\,(p)}{R_{g,offij+1}\,(p)}\left(1+\left(\frac{V_{ds,ij+1}(t_{300})-100}{V_{ds,ij+1}(t_{300})}\right)\right) \tag{24}$$

To reduce the voltage mismatch during turn-on switch failure across series connected MOSFETs, the $R_{s,Mij}$ is updated as follows

$$\frac{R_{s,Mij}\,(p+1)}{R_{s,Mij+1}\,(p+1)} = \frac{R_{s,Mij}\,(p)}{R_{s,Mij+1}\,(p)}\left(1+\left(\frac{V_{ds,ij+1}(t_{300})-100}{V_{ds,ij+1}(t_{300})}\right)\right) \tag{25}$$

where j=1, for 24 and 25.

The snubber capacitor values across devices are adjusted to minimize the difference in switching loss with modified parameters as follows

$$C_{sM,ij}\,(p+1) = C_{sM,ij}\,(p)\left(1+\left(\frac{P_{ds,ij}\,(p+1)-P_{ds,ij}\,(p)}{P_{s,ij}\,(p)}\right)\right) \tag{26}$$

where, $P_{ds,ij}(p)$ is evaluated as follows

$$P_{ds,ij}(p) = \sum_{k=1}^{300} i_{s,Mij}(t_{k+1})^2 R_{sM,ij}(p)(t_{k+1}-t_k)+ \tag{27}$$

where, $i_{g,Mij}$ is evaluated for condition when 3L-NPC pole is operating in normal state. The $R_{s,Mij}$, $C_{s,Mij}$ and $R_{goff,ij}$ during each iteration using Flowchart III, till (28) & (30) is satisfied

$$\frac{P_{loss}\,(p+1)-P_{loss}\,(p)}{P_{loss}\,(p)} < 0.1 \tag{28}$$

where P_{loss} is calculated as follows

$$P_{loss}(p) = \sum_{i=1}^{4}\sum_{j=1}^{2}\sum_{k=1}^{300} P_{ds,ij}(t_k) \tag{29}$$

TABLE 6. Comparison of turn-off v_{ds} using modified R-C snubber.

Figures	Turn-off V_{ds} (AFEC)			Turn-off V_{ds} (DAB)		
	Value	Flow-chart III	∇	Initial	Flow-chart III	∇
Fig. 25(a)	11.56kV	6.3kV	45.4%	10.1kV	6.5kV	35.64%
Fig. 25(b)	12.56kV	6.2kV	50.64%	10.9kV	6.0kV	44.9%
Fig. 25(c)	10.12kV	6.3kV	37.7%	11.2kV	7kV	27%
Fig. 25(d)	12.2kV	6.2kV	35%	11.5kV	6.8kV	40.8%
Fig. 25(e)	12.2kV	6.5kV	50.8%	11.9kV	6.8kV	42.2%
Fig. 25(f)	13kV	6.0kV	53.8%	11.5kV	6.0kV	47.8%

TABLE 7. The simulation data for different timing values to shut down the MV SST PCS.

Active Front End Converter						
	t_{AC}	t_{DC1}	t_{DC2}	Detection Time	t_{mid}	Shutdown Scheme
Fig. 25(a)	250ms	25ms	250ms	7.34ms	250ms	Fig. 20(a)
Fig. 25(b)	21.9ms	28ms	215ms	6.2ms	21.9ms	Fig. 20(c)
Fig. 25(c)	230ms	28ms	205ms	5.9ms	230ms	Fig. 20(c)
Fig. 25(d)	25.8ms	25ms	25ms	7.8ms	220ms	Fig. 20(c)
Fig. 25(e)	25.9ms	26ms	26ms	8ms	200ms	Fig. 20(c)
Fig. 25(f)	27ms	28ms	28ms	6.34ms	190ms	Fig. 20(c)
Dual Active Bridge						
	t_{AC}	t_{DC1}	t_{DC2}	Detection Time	t_{mid}	Shutdown Scheme
Fig. 25(a)	12ms	30.06ms	210ms	7.34ms	210ms	Fig. 20(b)
Fig. 25(b)	11ms	30.06ms	190ms	6.2ms	190ms	Fig. 20(b)
Fig. 25(c)	11.5ms	30.06ms	220ms	5.9ms	220ms	Fig. 20(b)
Fig. 25(d)	12ms	30.06ms	30.06ms	7.8ms	215ms	Fig. 20(b)
Fig. 25(e)	11ms	30.06ms	30.06ms	8ms	190ms	Fig. 20(b)
Fig. 25(f)	11.5ms	30.06ms	30.06ms	6.34ms	210ms	Fig. 20(b)

The delay parameters for each turn-off switch failure are evaluated as follows

$$\frac{t_{d,ij}(p+1)-t_{d,ij}(p)}{t_{d,ij}(p+1)} < 0.05 \tag{30}$$

where, $t_{d,ij}(0)$ is evaluated using (22).

IV. SIMULATION AND EXPERIMENTAL RESULTS

The Saber RD simulation results for a single open switch failure across M_{11} in AFEC are presented in Fig. 24(a). The turn-off transition across M_{31} is shown in Fig. 25(a). Due to the healthy functioning of Mid-switches, the affected pole can be used for balancing the mid-point voltage. The switches $M_{11}-M_{12}$ and $M_{41}-M_{42}$ are turned off, followed by $M_{21}-M_{22}$ and $M_{31}-M_{32}$. The time taken to reach the mid-point balance is within 5% of $0.5V_{DC}$, which is 250ms. To disconnect, the AC switch, the converter pole is disengaged at zero current crossings, followed by the disconnection of DC current interrupters [7]. Fig. 25(a) shows Saber RD result for $V_{ds,M22}$ after shutdown during the open switch failure across M_{21} in the DAB. To avoid overvoltage due to $\frac{di}{dt}$, the DC current interrupter is disengaged to reduce load current within the 1A, followed by disengaging the AC switch. The time constant due to L_{fl} and R_{load} is 500μs, causing the pole current to damp within 2.5ms [47]. Fig. 25(b) shows the $V_{ds,M21}$ and $V_{ds,M31}$ during open switch failure across M_{21}-M_{22} for AFEC and DAB. Fig. 25(c) shows the maximum $V_{ds,Mij}$ during failure across M_{21}-M_{32}.

The converter shutdown during turn-on switch failure across M_{12} is shown in Fig. 24(b). The 3L-NPC pole shutdown due to open switch failure across Mid-MOSFETs

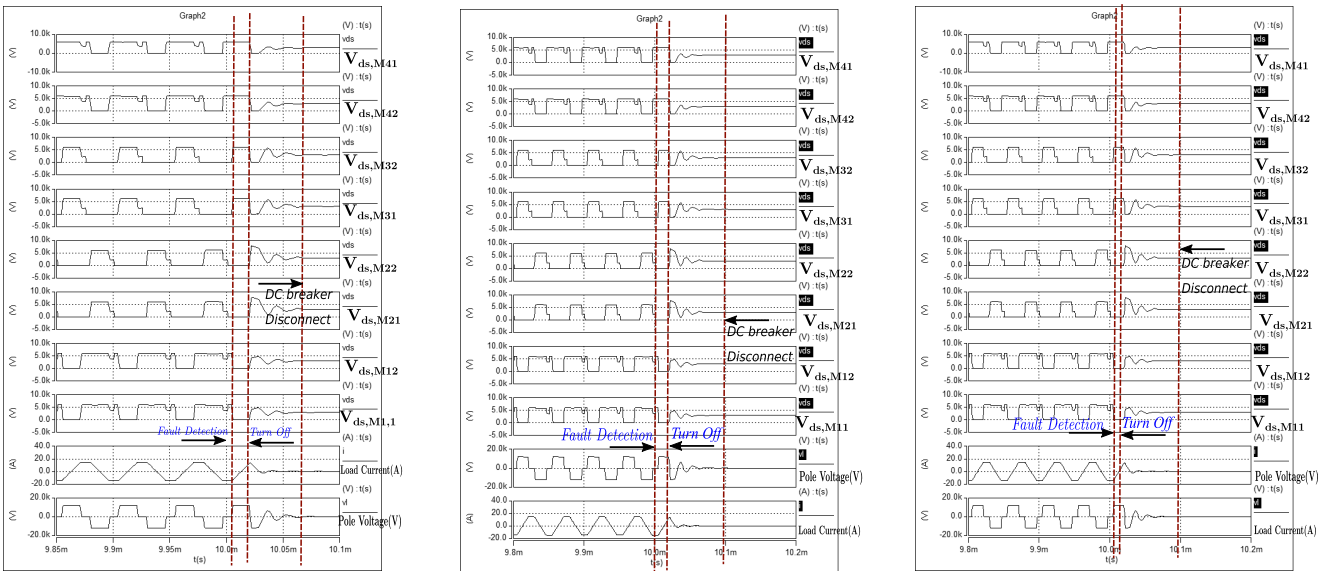


FIGURE 24. Shutdown of 3L-NPC converter pole simulated in Saber RD environment using MAST model of 10kV SiC MOSFETs and 10kV SiC JBS diodes for (a) Open switch failure across M_{11} in 3L-NPC pole operated using sine triangle PWM in AFEC (b) Turn-on switch failure across M_{12} in 3L-NPC pole operated using square wave PWM in DAB (c) Turn-on switch failure across M_{31}-M_{32} in 3L-NPC pole operated using square wave PWM in DAB.

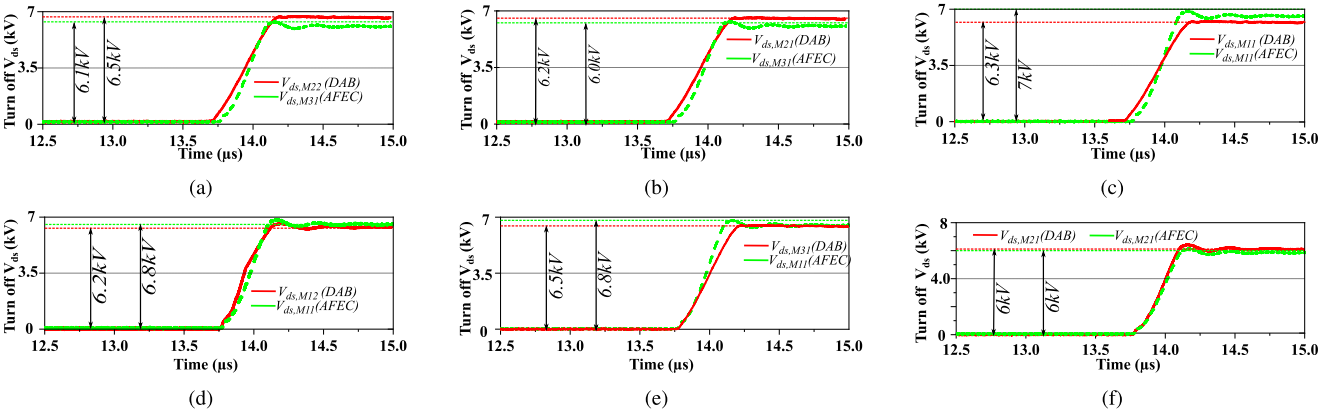


FIGURE 25. Turn off voltage across MOSFETs with maximum overvoltage during (a) Open switch failure across M_{11} in AFEC and across M_{21} in DAB (b) Open switch failure across M_{21} - M_{22} in AFEC and DAB. (c) Open switch failure across M_{21} - M_{32} in AFEC and DAB. (d) Single switch turn-on failure across M_{12} in AFEC and DAB (e) Turn-on switch failure across M_{31} - M_{32} in AFEC and DAB. (f) Turn on switch failure across M_{11} - M_{22} in AFEC and DAB.

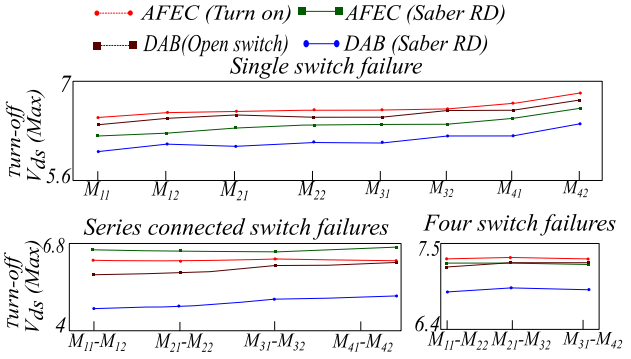


FIGURE 26. Maximum turn-off voltage mismatch during different open switch and turn-on failures in 3L-NPC pole with modified parameters listed in Table.8.

M_{21}-M_{32} is shown in Fig.24(c). Fig. 25(d), Fig. 25(e) and Fig. 25(f) shows maximum $V_{ds,Mij}$ during shutdown after turn-on failure across M_{12}, $M_{31}-M_{32}$ and $M_{11}-M_{22}$. Fig. 23 plots the maximum $V_{ds,Mij}$ during turn-on switch failures in AFEC and DAB, with the highest V_{ds} for 7.25kV across M_{21} in DAB. Table 6 shows the reduction in maximum $V_{ds,Mij}$ up to 53.8% due to modification $R_{g,offij}$, $R_{s,Mij}$ and $C_{s,Mij}$ using Flowchart III.

The fault isolation of affected 3L-NPC pole and MV SST PCS shutdown was simulated during switch failures using HIL setup with Xilinx FPGAs and the RTDS. The fault isolation of affected 3L-NPC pole and discharge of DC link capacitor in MV SST PCS is performed by S_1,S_2,S_3 and PWM generation using FTC scheme described in [35]. Fig. 27(a) shows the shutdown scheme of the MV SST PCS for open switch failure in Top MOSFETs (M_{11}-M_{12}) and Bottom MOSFETs (M_{31}-M_{32}) in AFEC. The Mid-MOSFETs can be turned to balance the mid-point voltage. Fig. 27(b) shows the MV SST PCS shutdown during switch failures across Mid-MOSFETs in DAB. Since the mid switches cannot be used for neutral point balancing, the disconnection

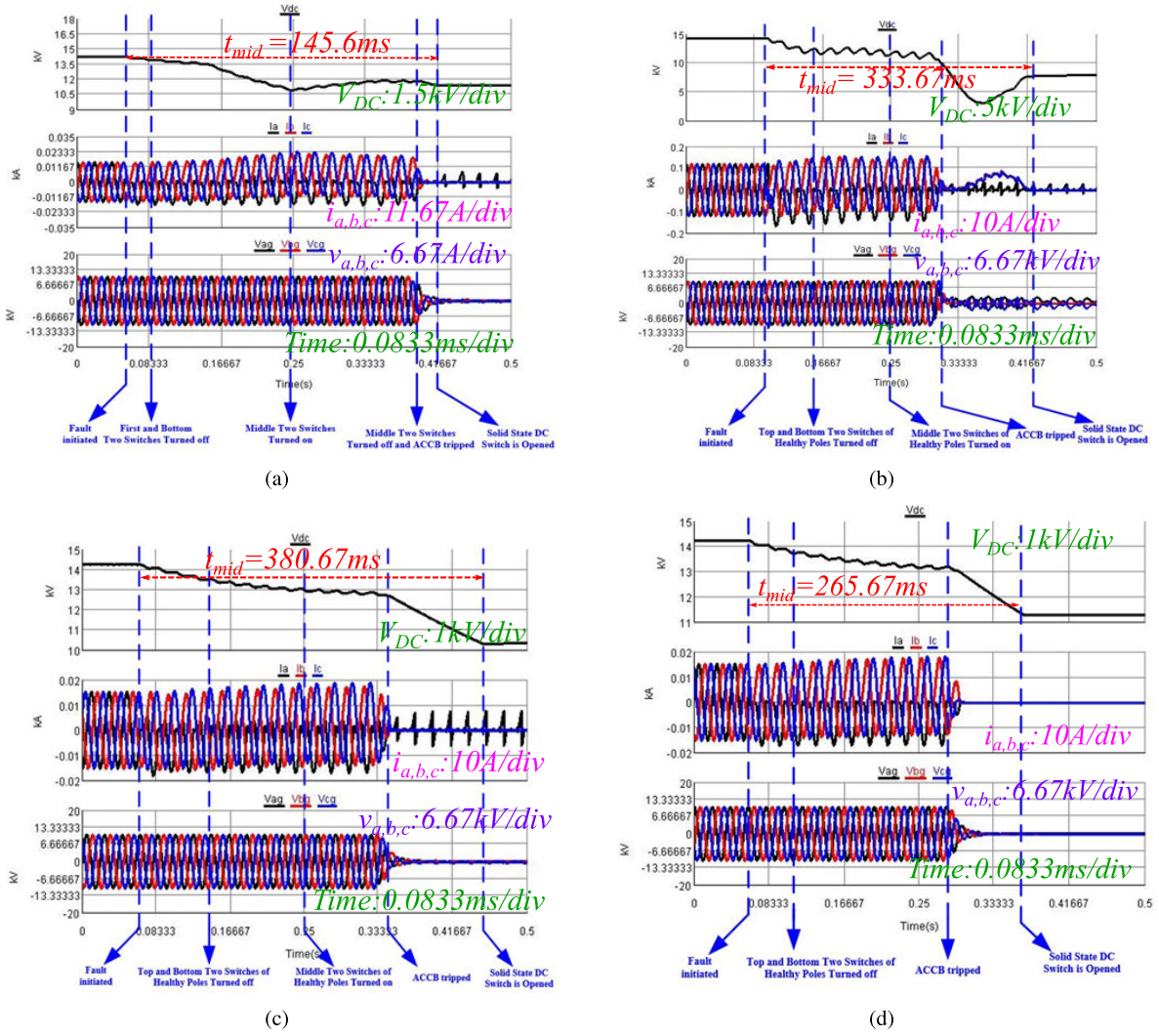


FIGURE 27. (a) Shut down scheme for open switch failure across M_{11},M_{12},M_{41}&M_{42} or turn-on switch failure across M_{21} -M_{32} in 3L-NPC AFEC pole. (b) Shut down scheme for the open switch or turn-on switch failure in the DAB pole. (c) Shut down scheme for open switch failure across M_{21} -M_{32} or turn-on switch failure across M_{11},M_{12},M_{41}&M_{42} in 3L-NPC AFEC pole (d) Converter shutdown using −ve sequence network as backup detection and protection scheme for open circuit switch fault at M_{11}.

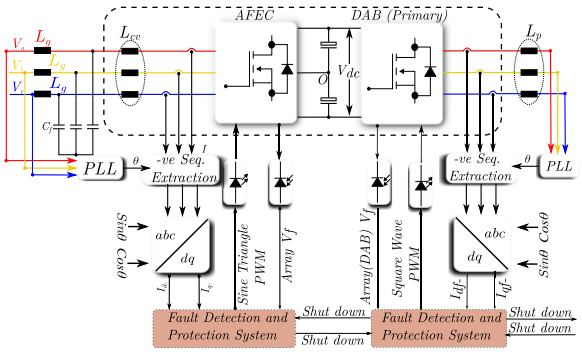


FIGURE 28. Fault protection mechanism with negative sequence extraction as backup protection scheme.

of the faulty phase from the rest of the system happens immediately. The healthy phases shut down after balancing the neutral point voltage within 5% of $0.5V_{DC}$. Fig. 27(c) shows the shutdown process during the open switch failure in Mid-MOSFETs of AFEC. The neutral point voltage is balanced by healthy phases and all AFEC poles are disconnected at zero current crossing. The t_{AC}, t_{DC1}, t_{DC2} and t_{mid} are listed in Table 7.

Fig. 28 illustrates the sensing and extraction of the negative sequence component for identifying switch failures in the 3L-NPC pole. In the event of a failure across M_{11} in AFEC, as depicted in Fig. 27(d), the converter undergoes shutdown through the detection of negative sequence current, should the de-saturation detection method fail to transmit the fault signal. Over-current detection via negative sequence current is activated with a programmed delay from the primary protection system, as described in Fig.29(a). This figure showcases the maximum response time of both the primary

TABLE 8. Values of 3L-NPC design parameters obtained from Flowchart III.

AFEC						DAB					
Variables	Value	Variables	Value	Variables	Value	Variables	Value	Variables	Value	Variables	Value
$R_{g,11}$	8Ω	$C_{s,M11}$	1.1 nF	$R_{g,12}$	12Ω	$R_{g,11}$	4Ω	$C_{s,M11}$	1 nF	$R_{g,12}$	7Ω
$R_{g,21}$	10Ω	$C_{s,M21}$	0.5 nF	$C_{s,M12}$	0.8 nF	$R_{g,21}$	10Ω	$C_{s,M21}$	0.63 nF	$C_{s,M12}$	0.5 nF
$R_{g,22}$	13Ω	$C_{s,M22}$	0.9 nF	$R_{g,31}$	14Ω	$R_{g,22}$	9Ω	$C_{s,M22}$	0.8 nF	$R_{g,31}$	12Ω
$C_{s,M31}$	1.5 nF	$R_{g,32}$	12Ω	$C_{s,M32}$	1.2 nF	$C_{s,M31}$	1.3 nF	$R_{g,32}$	10.5Ω	$C_{s,M32}$	0.95 nF
$R_{g,41}$	19Ω	$C_{s,M41}$	1.1 nF	$R_{g,42}$	8Ω	$R_{g,41}$	11Ω	$C_{s,M41}$	0.85 nF	$R_{g,42}$	23Ω
$C_{s,M42}$	0.8 nF	$R_{s,M11}$	4.7Ω	$C_{s,D11}$	2.4 nF	$C_{s,M42}$	0.9 nF	$R_{s,M11}$	16Ω	$C_{s,D11}$	1.2 nF
$R_{s,M12}$	2.2Ω	$C_{s,D12}$	1.2 nF	$R_{s,M21}$	1.2Ω	$R_{s,M12}$	2.5Ω	$C_{s,D12}$	0.9 nF	$R_{s,D21}$	12Ω
$R_{s,D11}$	2.3Ω	$R_{s,M22}$	2.1Ω	$R_{s,D12}$	3.5Ω	$R_{s,D11}$	2.3Ω	$R_{s,M22}$	2.1Ω	$R_{s,D12}$	3.5Ω
$R_{s,M31}$	0.9Ω	$C_{s,D21}$	2.4 nF	$R_{s,M32}$	0.8Ω	$R_{s,M31}$	0.9Ω	$C_{s,D21}$	2.8 nF	$R_{s,D32}$	8Ω
$C_{s,D22}$	1.2 nF	$R_{s,M41}$	1.3Ω	$R_{s,D21}$	2.3Ω	$C_{s,D22}$	1.2 nF	$R_{s,M41}$	1.3Ω	$R_{s,D21}$	2.3Ω
$R_{s,M42}$	1.1Ω	$R_{s,D22}$	3.5Ω			$R_{s,M42}$	3.1Ω	$R_{s,D22}$	5.5Ω		

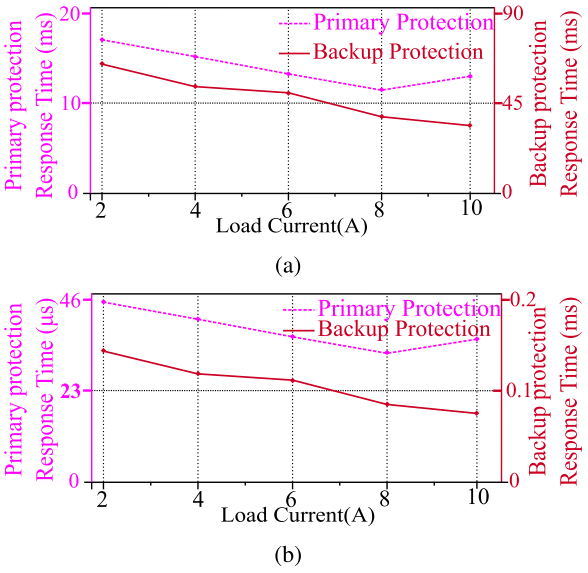


FIGURE 29. (a) Maximum response time from failure detection to the trip signal for switch failure in (a) AFEC (b) DAB.

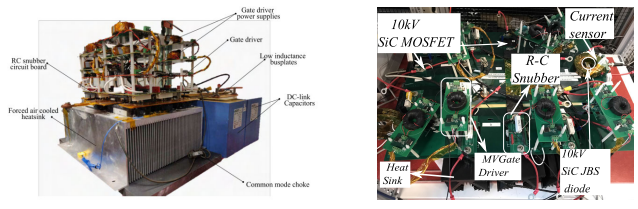


FIGURE 30. (a) 3L-NPC pole hardware as a building block of MV SST PCS (b) 3L-NPC pole hardware with modified design parameters.

and backup protection systems during M_{11} switch failure in AFEC, with the backup protection responding after a delay of 41ms during open switch failure and 28.1ms during turn-on switch failure. Fig. 29(b) outlines the maximum response time for the primary and backup protection systems in the case of switch failure across M_{11} in DAB. Notably, the response time is faster compared to AFEC, owing to the detection of switch failure within half of the operating duty cycle. The backup failure detection responds after a delay of 4 switching cycles (0.2ms) to prevent saturation in the DAB transformer post-failure.

TABLE 9. Performance metrics for assessing the effectiveness of modified 3L-NPC parameters.

Metric	3L-NPC pole (DAB)	3L-NPC pole (AFEC)
Experimental data		
Efficiency	99.2%	98.2%
DC Offset Voltage (DAB)	40V	12V
Maximum Voltage Mismatch	23V	28V
Specified limits (Using [2])		
Efficiency	98.8%	97.8%
DC Offset Voltage (DAB)	50V	50V
Maximum Voltage Mismatch	50V	50V

Fig. 30(a) provides a depiction of the 3L-NPC pole as a fundamental component of the MV SST PCS shown in Fig. 1(a). Experimental hardware for testing the 3L-NPC pole with modified design parameters is illustrated in Fig. 30(b), with the parameters listed in Table 8. Dynamic voltage balancing across M_{11} and M_{12} during hard switching operation in AFEC is shown in Fig. 31(a) under specific operating conditions. Similar results were obtained for soft-switched turn-off in DAB, as evidenced by Fig. 31(b).

Furthermore, Fig. 31(c) compares switching losses for series-connected SiC MOSFETs and SiC JBS diodes under modified parameters, with maximum losses for hard and soft switching operations measuring 42mJ and 5mJ, respectively. Fig. 31(d) illustrates the maximum turn-off voltage mismatch for different i_L. Table 9 presents experimental values of efficiency, DC offset, and maximum voltage mismatch in the 3L-NPC pole, all of which fall within specified limits.

TABLE 10. Comparative assessment of different literature on the efficiency and response time for primary and backup protection.

Active Front End Converter					
Existing Solution	Open Circuit: Response Time	Turn-on failure Response Time	Backup Protection: Response Time (Open circuit Failure)	Backup Protection: Response Time (Turn-on failure)	Efficiency: Normal operation
[16]- [20]	430ms	400ms	None	None	Not mentioned
[22]- [23]	350ms	300ms	None	None	Not mentioned
[35]	320ms	310ms	None	None	97.6
[15]	420ms	450ms	None	None	Not mentioned
This paper	46ms	16.9ms	86ms	45ms	98.2
Dual Active Bridge					
[24]	41.5ms	41.5ms	None	None	Not mentioned
This paper	30μs	30μs	0.2ms	0.2ms	99.2

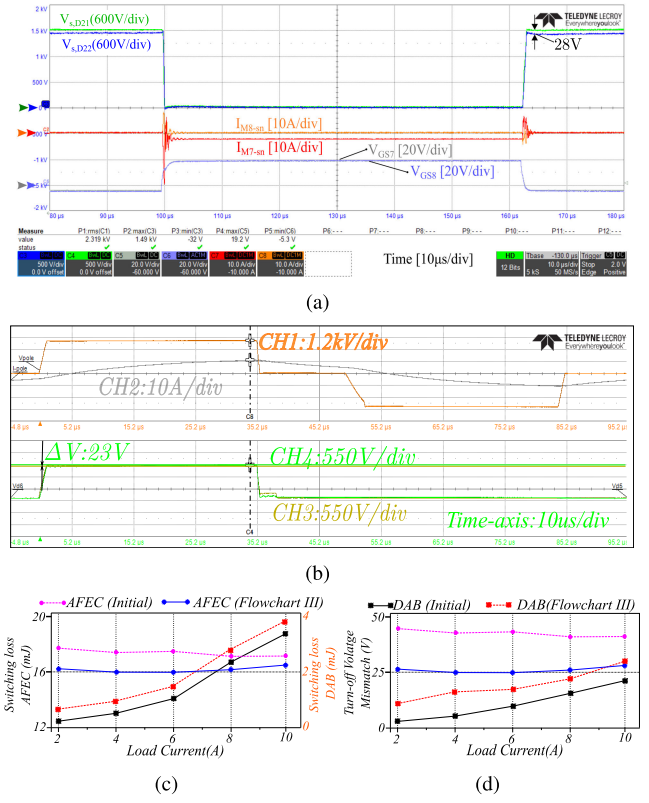


FIGURE 31. Experimental waveform at 7kV DC bus,10A load current for 3L NPC pole hardware showing Turn-off waveform for $V_{ds,M11}$ & and $V_{ds,M12}$ and voltage mismatch of (a) 28V in AFEC using sine triangle PWM (b)and 23V in DAB using 3L square wave. Comparison of switching loss and maximum turn-off voltage mismatch in (c) 3L-NPC AFEC pole and (d) 3L-NPC DAB pole for parameters listed in Table 9.

V. CONCLUSION

This paper introduces a methodology to detect open and turn-on switch failures and provide overvoltage protection for 10kV SiC MOSFETs in MV SST Power Conditioning Systems (PCS), enabled by 3P-3L NPC AFEC and DAB, using series-connected 10kV SiC MOSFETs and 10kV SiC JBS diodes. The methodology features an active voltage clamp at the gate terminal and desat detection for identifying abrupt open switch and turn-on switch failures. Furthermore, it calculates the turn-off timing for the series-connected MOSFETs through analytical modeling of $V_{ds,Mij}$ during turn-off after switch failures, by considering bus bar inductance, base plate capacitance, R-C snubber, and the common mode choke situated between the heat sink and the midpoint of the DC link capacitor. Modifications to $R_{g,offij}$, $R_{s,Mij}$, and $C_{s,Mij}$ are made to prevent overvoltage during turn-on switch failure while maintaining voltage balance and minimizing switching losses during normal operation. The $V_{ds,Mij}$ transition using $t_{d,ij}$ and modified values of $R_{g,offij}$, $R_{s,Mij}$, and $C_{s,Mij}$ is verified through Saber RD simulation results at rated 13.8kV AC/24kV DC level. The analytical results closely match the simulation results, with an accuracy of 99.4%. Additionally, the paper includes simulations for safe fault isolation of the 3L-NPC pole and MV SST PCS shutdown within a real-time environment using a Hardware-in-the-Loop (HIL) setup equipped with Xilinx FPGAs and the RTDS, operating at the 13.8kV AC/24kV DC level. The data obtained from the simulation result has been compared with existing methods in Table.10. The proposed method shows the lowest response time of 22ms for open switch failure and 16.9ms for turn-on switch failure in AFEC. Similarly, the response time for open switch and turn-on switch failure across DAB is 30μs. The back up failure protection method shows a higher response time compared to the primary protection system due to programmed delay in operation. Experimental results, conducted at a 7kV DC bus by incorporating the modified $R_{g,offij}$, $R_{s,Mij}$, and $C_{s,Mij}$ demonstrate turn-off voltage mismatch across 10kV SiC MOSFETs, DC offset at the pole output terminal and operating efficiency within the limits, as specified in Table 9. The future work could optimize the delay calculation period to achieve the design of overvolatge protection system by reducing the iterations for determining heat sink voltage(V_{hs}) and base plate capacitance current (i_{cbs}). r

ACKNOWLEDGMENT

The authors would like to thank Dr. Mike Turner and Davis Thakaran from Saber Synopsis for their invaluable assistance in conducting the Saber RD simulation, utilizing the MAST model for 10kV SiC MOSFETs and 10kV SiC JBS diodes.

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