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RESEARCH ARTICLE

Novel Phase Shift Angle Compensation Method of DAB Converter Considering Parasitic Capacitance of SiC MOSFET

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ABSTRACT This study proposes a novel method to compensate phase shift angle of dual active bridge (DAB) converters by considering the parasitic capacitance of SiC metal-oxide-semiconductor field-effect transistors (MOSFETs). In general, the DAB converter bidirectionally transfers power between the primary and secondary sides using a phase shift angle. The conventional methods calculate the phase shift angle with an assumption of the instantaneous changes in the voltage and current. However, SiC MOSFETs used in a DAB converter have parasitic capacitances such as the input, output, and reverse transfer capacitance which affect the voltage and current leading to inaccurate phase shift angle calculation. For instance, the input parasitic capacitance delays the voltage slew rate between the drain and the source of the SiC MOSFET. Moreover, during the dead time, the output parasitic capacitance of the SiC MOSFET and leakage inductance in the DAB converter resonate, delaying the slew rates of both current and voltage. Therefore, this study analytically quantifies the effect of parasitic capacitances on the performance of the SiC DAB converter and proposes a novel phase shift angle compensation method. The proposed method was validated through simulations and experiments with a 4-kW SiC DAB converter prototype.

INDEX TERMS DAB converter, single phase shift, SiC MOSFET, parasitic capacitance.

I. INTRODUCTION

Owing to environmental problems and energy resource allocation, renewable energy, electric vehicles, and microgrids have gained substantial attention. A bidirectional power converter plays a vital role in these distributed energy resources, capable of controlling the power flow among various energy sources. In addition to the bidirectional power flow, galvanic isolation among energy sources is of paramount importance as the system needs to meet the safety and reliability standards (e.g., IEEE 519-2022) and have relatively simple system reconfiguration for optimal operation [1], [2].

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Dual active bridge (DAB) converters have garnered considerable attention for their high efficiency and high power density with galvanic isolation through the high-frequency transformer. The primary and secondary sides of transformers have full-bridge structures, and an inductor is connected in series with the transformer to provide additional inductance [3], [4]. The full-bridge switching structures in the primary and secondary sides use Si MOSFETs or IGBTs as switching devices. Recently, SiC MOSFETs have replaced the existing Si MOSFETs and IGBTs due to their low on-state resistance and low switching losses even at high voltages. Therefore, SiC based DAB converter can deliver a high output voltage at a high switching frequency leading to high power density without compromising system efficiency [5], [6].

In MOSFETs, the gate is insulated by a thin silicon oxide film. Thus, MOSFETs have inherent capacitance between the gate and drain, gate–source, and drain–source. The input ($C_{iss} = C_{gd} + C_{gs}$), output ($C_{oss} = C_{ds} + C_{gd}$), and reverse transfer ($C_{rss} = C_{gd}$) capacitances of a MOSFET are essential factors affecting its electrical characteristics. The parasitic capacitance of a MOSFET affects its switching speed and switching losses. The parasitic capacitance which is connected in parallel to the MOSFET and operates similar to a snubber capacitor, also affects the zero-voltage switching (ZVS) performance. A study was conducted to estimate the minimum current requirement for the ZVS of the DAB converter according to the capacitor connected in parallel with the MOSFET [7], [8], [9].

DAB converter generally ignores transformer magnetizing inductance and device parasitic capacitance and calculates ZVS range using phase shift angle, output power, and turn ratio of the transformer. The ZVS region represents the range in which the designed converter can operate stably. However, due to the influence of magnetizing inductance and device parasitic capacitance, it may deviate from the ZVS region or reduce the operating range in actual operation. Therefore, setting the correct parameters is important when designing a DAB converter [10], [11], [12], [13].

DAB converter typically uses single-phase shift (SPS) control using a phase shift between the primary and secondary phases because SPS easily provides the ZVS and can simply control power transmission through the phase shift of the full-bridge switching elements at both ends. The SPS method transfers power through the voltage difference across the inductor during the phase shift between the primary and secondary sides.

To improve the SPS method, the method for controlling inductor current using a trapezoidal or triangular was proposed. The extended phase shift (EPS) method uses the phase shift between the primary and secondary sides and the phase shift between the upper and lower parts of the primary-side switching element. The dual-phase shift (DPS) method has been proposed to improve the EPS and simultaneously control the upper and lower switches of the primary and secondary full-bridge sides [14], [15], [16], [17], [18], [19], [20], [21].

Importantly, the fundamental power transfer principle of the SPS, EPS, and DPS methods is the voltage difference across the inductor. However, SiC MOSFETs used for switching have parasitic capacitance as the input, output, and reverse transfer, and parasitic capacitances are charged and discharged according to the switching operation. The output parasitic capacitance resonates with the inductor during the dead time used for switching safety. Therefore, the voltage changes between the drain and the source of SiC MOSFET are delayed, and the voltage difference in the inductor is not an ideal square wave but a quasi-square or a trapezoidal-like wave. In addition, the input parasitic capacitance delays voltage change between the drain and source of SiC MOSFET [22], [23], [24]. These parasitic components can cause a significant mismatch between the estimated power and the measured power transfer. Therefore, it is critical to consider the parasitic components when it comes to estimating the phase shift angle to transfer power by the DAB converter.

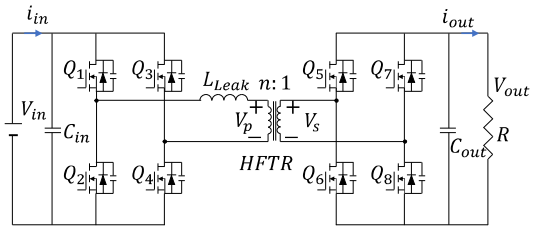

FIGURE 1. DAB DC-DC converter.

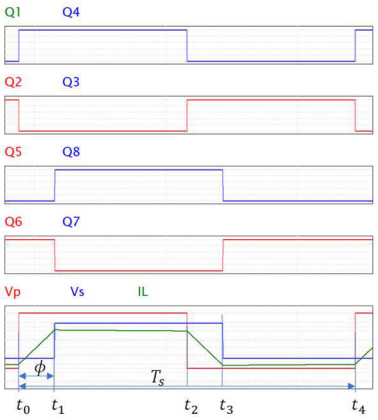

FIGURE 2. Switching state by the conventional SPS method.

In this study, we analyze the effect of SiC MOSFET parasitic capacitance on the performance of the DAB converter with the SPS method and propose a novel phase shift angle compensating method considering the parasitic capacitance of the SiC MOSFETs.

The conventional SPS method which is generally used for controlling the DAB converter, calculates the phase shift angle using the ideal DAB parameters without considering the delay caused by the parasitic capacitance of the MOSFET. Therefore, the phase shift angle calculated by conventional SPS has an error when compared to the phase shift angle required to obtain the rated output of the DAB converter. The method proposed in this paper is to analyze the influence of MOSFETs parasitic capacitance and compensate for this influence. In this way, the accuracy of the phase shift angle used to control and design conventional DAB converters can be improved.

The phase shift angle with improved accuracy can be used as a parameter for DAB design and as a reference value for closed-loop control. The control characteristics using the proposed phase shift angle in the paper are compared and analyzed with the control characteristics using the conventional phase shift angle. Additionally, the accuracy of the proposed method is verified by comparing it with the phase shift angle obtained through closed-loop control.

TABLE 1. Symbol list used equation.

Symbol	Unit	Quantity
ΔI_L	A	Change in Leakage Inductance Current
ϕ	Degree	Phase Shift Angle
Z_s	Ω	Leakage Inductance Impedance
L_{leak}	μH	Leakage Inductance
V_p	V	Primary Voltage
V_s	V	Secondary Voltage
V_L	V	Leakage Inductance Voltage
n		Turn Ratio of High Frequency Transformer (HFTR)
f	Hz	Switching Frequency
P	W	Power

The rest of the paper is organized as follows: Chapter 2 describes the conventional SPS method for DAB Converter; Chapter 3 presents the proposed SPS method considering the parasitic capacitance; Chapter 4 presents the simulation and experiment; Chapter 5 concludes the paper.

II. CONVENTIONAL SPS METHOD DAB CONVERTER

A DAB converter is shown in Fig. 1 which consists of a full-bridge switch at both ends, a high-frequency transformer, and an inductor.

The power flow is determined by the phase shift angle (ϕ) between the primary- and secondary-side full-bridge switches.

Fig. 2 shows the switching state, voltage, and current according to the conventional SPS control. Table 1 lists the symbols used in these calculations.

The inductor current generated by the phase shift angle can be calculated as follows:

Mode 1: $t_0 \sim t_1$

$$\Delta I_L = \frac{\phi}{Z_s}\left(V_p + nV_s\right) = \frac{\phi V_L}{Z_s}$$
$$i\left(t_1\right) = i\left(t_0\right) + \Delta I_L \tag{1}$$

Mode 2: $t_1 \sim t_2$

$$\Delta I_L = \frac{\pi - \phi}{Z_s}\left(V_p - nV_s\right) = \frac{\left(\pi - \phi\right) V_L}{Z_s}$$
$$i\left(t_2\right) = i\left(t_1\right) + \Delta I_L \tag{2}$$

because $i\left(t_0\right) = -i(t_2)$

$$i\left(t_0\right) = -i\left(t_2\right) = \frac{1}{2Z_s}\left(-\pi V_p + nV_s\left(\pi - 2\phi\right)\right) \tag{3}$$

$$i\left(t_1\right) = \frac{1}{2Z_s}\left(\left(2\phi - \pi\right) V_p + \pi nV_s\right) \tag{4}$$

The average value of the inductor current and power can be calculated using (3) and (4), as follows:

$$I_{L\_avg} = \frac{nV_s}{2\pi^2 fL_{leak}}\phi\left(\pi - \phi\right) \tag{5}$$

$$P = I_{L\_avg}V_p = \frac{nV_pV_s\phi\left(\pi - \phi\right)}{2\pi^2 fL_{leak}} \tag{6}$$

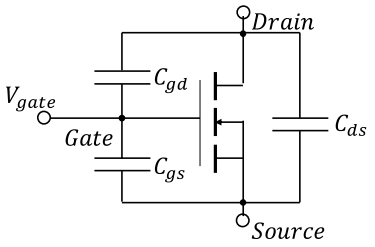

FIGURE 3. Switching state by the conventional SPS method.

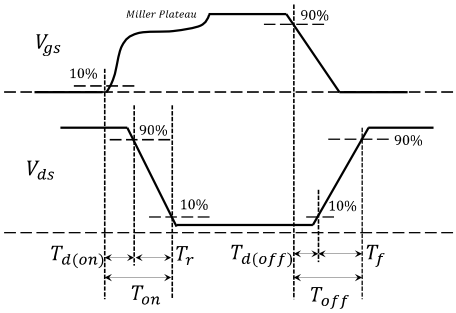

FIGURE 4. V_{gs} and V_{ds} waveforms of the MOSFET.

The phase shift angle is calculated using (6), expressed as follows.

$$\phi = \frac{\pi}{2}\left(1 - \sqrt{1 - \frac{8fL_{leak}P}{nV_pV_s}}\right) \tag{7}$$

Equation (1) and (2) assume that the primary and secondary voltages for calculating the change in inductor current change instantaneously, as shown in Fig. 2.

III. PROPOSED SPS METHOD CONSIDERING PARASITIC CAPACITANCE OF SiC MOSFET

Fig. 3 shows the equivalent circuit of a regular MOSFET with parasitic capacitance. The gate–drain capacitance, C_{gd}, and gate–source capacitance, C_{gs}, are primarily determined by the structure of the gate electrode. The drain–source capacitance, C_{ds}, is determined by the vertical p-n junction.

The input ($C_{iss} = C_{gd} + C_{gs}$), output ($C_{oss} = C_{ds} + C_{gd}$), and reverse transfer ($C_{rss} = C_{gd}$) capacitances of the power MOSFET are essential factors. The parasitic capacitance of the MOSFET changes according to the voltage between the drain–source, V_{ds}.

The parasitic capacitance C_{iss}, C_{oss} and C_{rss} of a SiC MOSFET can be calculated and measured by measuring V_{ds} and the current flowing through the MOSFET. The V_{ds} of the MOSFET is changed from 0 to a specific voltage, and the parasitic capacitance is calculated using the changed value during turn-on or turn-off time. This parasitic capacitance is expressed based on the V_{ds} voltage [25], [26], [27].

Fig. 4 shows the gate–source voltage V_{gs} and the drain–source voltage V_{ds} waveforms of the MOSFET. When the gate voltage is input, current flows through the gate and charges C_{gs} and C_{gd}. While the gate voltage rises to the

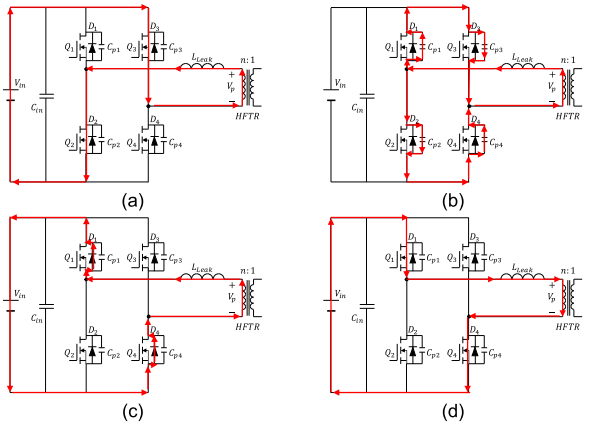

FIGURE 5. Current path during the dead time. (a) State 1. (b) State 2-1. (c) State 2-2. (d) State 3.

threshold voltage (V_{th}), C_{gs} and C_{gd} are charged in parallel, and when V_{gs} exceeds V_{th}, the drain current flows and C_{gs} and C_{gd} are continuously charged. As V_{gs} increases, the drain current continues to increase and V_{ds} decreases, resulting in a Miller plateau where V_{gs} remains constant due to the Miller effect. Subsequently, both C_{gs} and C_{gd} are charged in the oversaturation region [22], [23], [24].

The time from when the gate–source voltage V_{gs} rises by 10% or more until the drain–source voltage V_{ds} reaches 90% is called turn-on delay time $T_{d(on)}$. Rise time (T_r) represents the time it requires for the drain–source voltage to change from 90% to 10%. The total turn-on time (T_{on}) of the MOSFET is the time sum of the turn-on delay and rise time.

When the gate signal goes low, C_{iss}starts discharging and V_{gs} gradually decreases. Turn-off delay time ($T_{d(off)}$) is the delay time from when the gate voltage is below 90% to when V_{ds} becomes 10%. The V_{ds} increases gradually from 10% to 90%, and this time is called fall time (T_f). The turn-off time (T_{off}) is the sum of the turn-off delay time and the fall time. Therefore, C_{iss} directly affects the turn-on and turn-off delays by charging and discharging the MOSFET. C_{oss} is an important factor for ZVS as it affects the circuit resonance.

The MOSFET used in the DAB converter uses the dead time to prevent an arm-short between the upper and lower MOSFETs. The current flows by the energy stored in the inductor through the freewheeling diode (D_1, D_2, D_3, D_4) and parasitic capacitance ($C_{p1}, C_{p2}, C_{p3}, C_{p4}$) of the MOSFET during dead time.

Fig. 5 shows the current path of the primary side and when the output parasitic capacitance is also considered.

Fig. 6 shows the relationship between the delay time of the MOSFET and the DAB output when only the freewheeling diode is considered (Case 1) because the influence of parasitic capacitance is negligible, when the parasitic capacitance of the MOSFET is also considered (Case 2) because the parasitic capacitance becomes a significant enough to affect the performance of DAB converter. In Fig. 6, t_5 to t_{12} are as follows:

$t_5 \sim t_8$: Dead time of primary
$t_5 \sim t_6$: MOSFET3 turn-off delay time ($T_{d(off)1}$)

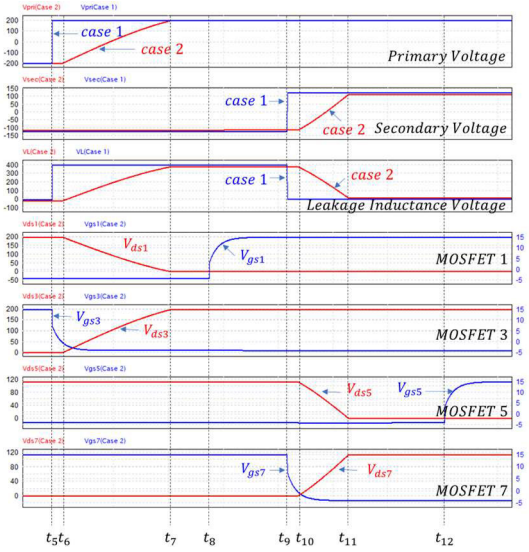

FIGURE 6. Voltage characteristics of cases 1 and 2 for dead time.

$t_6 \sim t_7$: Delay time due to MOSFET1, 3 output parasitic capacitance and leakage reactance resonance (T_{p1})
$t_7 \sim t_8$: ZVS operation by Freewheeling diode of MOSFET1
t_8 : MOSFET1 Turn-on
$t_9 \sim t_{10}$: MOSFET7 Turn-off delay time ($T_{d(off)2}$)
$t_{10} \sim t_{11}$: Delay time due to MOSFET5, 7 output parasitic capacitance and leakage reactance resonance (T_{p2})
$t_{11} \sim t_{12}$: ZVS operation by freewheeling diode of MOSFET5
t_{12} : MOSFET5 Turn-on

During primary and secondary deadtime, turn-off delay time ($T_{d(off)1}, T_{d(off)2}$) due to input parasitic capacitance and delay time (T_{p1}, T_{p2}) due to resonance of output parasitic capacitance and leakage reactance occur. When the MOSFET is turned on, the turn-on delay ($T_{d(on)}$) of the MOSFET does not appear because ZVS operation is performed by the output parasitic capacitance and the freewheeling diode during the dead time.

Additionally, the transient time during which the leakage inductance voltage changes is equal to the delay time due to the resonance of the output parasitic capacitance and the leakage inductance.

The leakage inductance voltage (V_L) in Fig. 7 has the maximum voltage during the phase shift angle (ϕ) of the primary and secondary voltages and has the minimum voltage during no phase shift angle ($\pi - \phi$). When the turn ratio of the transformer used in the DAB converter is n, $k(k = V_{in}/nV_{out})$ is the ratio between the output voltage considering the turn ratio (n) and the input voltage, and if k is not equal to 1, the current stress and circulating current become substantially large [13], [28]. Therefore, when k is set to 1, the leakage

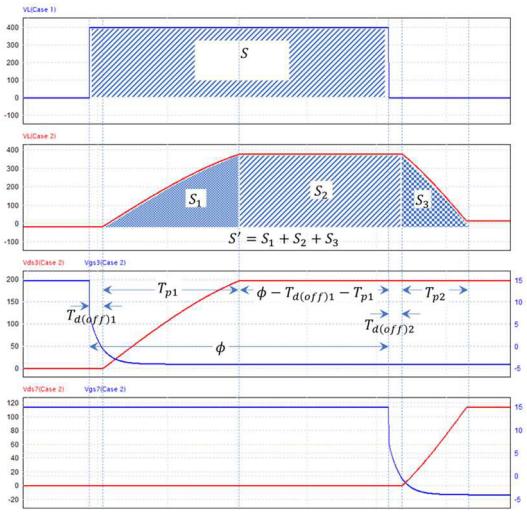

FIGURE 7. Leakage inductance voltage for the phase shift angle.

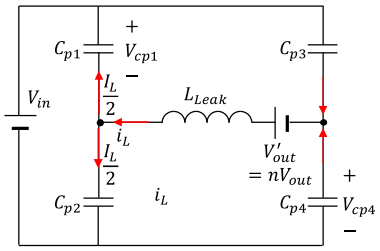

FIGURE 8. Primary side equivalent circuit at state 2-1.

inductance voltage is as follows:

$$0 \sim \phi : V_L = V_p + nV_s \tag{8}$$

$$\phi \sim (\pi - \phi) : V_L = 0 \tag{9}$$

According to (8) and (9), the change in leakage inductance current appears during the phase shift angle ϕ; therefore, the change in the leakage inductance current is as follows:

$$\Delta I_L = \frac{\phi(V_p + nV_s)}{Z_s} = \frac{\phi V_L}{Z_s} \propto \phi \; and \; V_L \tag{10}$$

Fig. 7 shows the leakage inductance voltage during the phase shift angle shown in Fig. 6. S represents the area created by the phase shift angle and the leakage inductance. The area S of Case 1 which does not consider parasitic capacitance, differs from that of Case 2 which considers parasitic capacitance. Therefore, the delay in the voltage change must be compensated to produce the identical output as in the conventional SPS method when parasitic capacitance is considered.

In Fig. 7, there are two reasons for delaying the change in V_L. The first is the primary-side delay time (T_{p1}) and the secondary-side delay time (T_{p2}) caused by the resonance of the output parasitic capacitance and leakage inductance, and the second is the primary and secondary turn-off delay times ($T_{d(off)1}$, $T_{d(off)2}$).

A. DELAY TIME BY OUTPUT PARASITIC CAPACITANCE

Fig. 8 shows the primary side equivalent circuit at state 2-1 in Fig. 5, wherein the current flows through the primary side of the DAB with the output parasitic capacitance during the dead time as an equivalent circuit.

In Fig. 8, if Q_2 and Q_3 are active in the previous switching state, then C_{p1} and C_{p4} are charged with the switching open state and have voltages V_{cp1} and V_{cp4}.

When all switches are open at the dead time, C_{p1} and C_{p4} start discharging, and C_{p2} and C_{p3} charge.

Each leg was connected in parallel according to the current path, and the output parasitic capacitances of the upper and lower sides were connected in series. Assuming that the size of each output parasitic capacitance is the same ($C_{p1} = C_{p2} = C_{p3} = C_{p4} = C_{pri}$), the primary side output parasitic capacitance is C_{pri}.

The resonance frequency generated by the output parasitic capacitance and leakage inductance can be expressed by the following equation:

$$f_{1o} = \frac{1}{2\pi\sqrt{L_{Leak}C_{pri}}} \tag{11}$$

During the dead time, the energy of the leakage inductance and the output parasitic capacitance or snubber capacitor must be equal, or the energy of the output parasitic capacitance or the snubber capacitor must be higher to operate the stable ZVS.

Using these conditions, the energy of the output parasitic capacitance can be expressed as follows:

$$EL_{leak} = \frac{1}{2}L_{leak}I_L^2 = EC_p \tag{12}$$

where, EL_{leak} is the energy stored in leakage inductance and EC_p is the energy stored in parasitic capacitance.

The leakage inductance current is the same as the current flowing through C_{p1} and C_{p2} when the output parasitic capacitance is the same; thus, the following current equation can be obtained:

$$I_{cp1} = I_{cp2} = I_{cp} = \frac{I_L}{2} \tag{13}$$

In this condition, the maximum voltages of all MOSFETs are the same ($V_{cp1} = V_{cp2} = V_{cp3} = V_{cp4} = V_{cpp} = V_{in}$).

The current flowing through the output parasitic capacitance is calculated using the voltage across the output parasitic capacitance as follows:

$$I_{cp} = C_{pri}\left(\frac{dV_{cpp}}{dt}\right) \tag{14}$$

The inductor current can be expressed by (13) and (14) as follows:

$$I_L = 2I_{cp} = 2C_{pri}\frac{dV_{cpp}}{dt} \tag{15}$$

The energy transferred to the output parasitic capacitance is expressed by the voltage and inductor current as follows:

$$EC_p = V_{cpp}I_L T_{d1} = \int_0^{T_{d1}} \left(V_{cpp}I_L\right) dt$$

$$= \int_0^{T_{d1}} \left(V_{cpp}2C_{pri}\frac{dV_{cpp}}{dt}\right) dt = 2C_{pri}V_{cpp}^2 \tag{16}$$

The MOSFET voltage can be expressed as follows by (12) and (16) indicating the energy stored in the output parasitic capacity.

$$\frac{1}{2}L_{leak}I_L^2 = 2C_{pri}V_{cpp}^2 \tag{17}$$

$$V_{cpp} = \sqrt{\frac{L_{Leak}I_L^2}{4C_{pri}}} \tag{18}$$

Equation (18) represents the maximum value of the voltage generated by the resonance of the leakage inductance and output parasitic capacitance during the dead time. During resonance, the voltage changes like a sine wave; thus, it can be expressed as:

$$v_{cpp}(t) = V_{cpp}\sin(2\pi f_{1o}t) \tag{19}$$

Equation (20) represents the output parasitic capacitance satisfying (18).

$$C_{pri} = \frac{L_{Leak}I_L^2}{4V_{cpp}^2} = C'_{pri} \tag{20}$$

The output parasitic capacitance C'_{pri} in (20) represents the capacitance corresponding to all energy transferred from the leakage inductance during the dead time and has a large value. However, the output parasitic capacitance of the actual MOSFET is exceedingly small. When this value is substituted in C_{pri}, V_{cpp} becomes larger than the input voltage V_{in}.

However, because the voltage by charging the capacitance cannot be higher than the supply voltage V_{in}, current flows only while the output parasitic capacitance is being charged. Therefore, (19) can be expressed as (20) as input voltage. Equation (22) represents the delay time T_{p1} calculated using (20).

$$V_{in} = V_{cpp}\sin(2\pi f_{1o}T_{p1}) \tag{21}$$

$$T_{p1} = \frac{\sin^{-1}\left(\frac{V_{in}}{V_{cpp}}\right)}{2\pi f_{1o}} \tag{22}$$

T_{p2} which represents the effect of the secondary-side output parasitic capacitance, can be expressed as

$$L'_{Leak} = \frac{L_{Leak}}{n^2} \tag{23}$$

$$V_{cps} = \sqrt{\frac{L'_{Leak}(nI_L)^2}{4C_{sec}}} \tag{24}$$

$$f_{2o} = \frac{1}{2\pi\sqrt{L'_{Leak}C_{sec}}} \tag{25}$$

$$V_{out} = V_{cps}\sin(2\pi f_{2o}T_{p2}) \tag{26}$$

$$T_{p2} = \frac{\sin^{-1}\left(\frac{V_{out}}{V_{cps}}\right)}{2\pi f_{2o}} \tag{27}$$

B. DELAY TIME BY INPUT PARASITIC CAPACITANCE

During the dead time, if the off signal is input to the gate of the MOSFET, as shown in Fig. 4, the input parasitic capacitance is discharged, and the drain–source voltage does not change until the gate–source voltage is lower than the threshold voltage. Therefore, V_L which causes a change in the inductor current by the phase shift angle, is delayed by the primary-side turn-off delay time ($T_{d(off)1}$) and extended by the secondary-side turn-off delay time ($T_{d(off)2}$). Input parasitic capacitance has less dependency on drain–source voltage than the output parasitic capacitance [27], [29], [30]. Since SiC MOSFETs are generally controlled using a fixed voltage range and circuit by the gate driver, the turn-off delay time by the input parasitic capacitance uses the data sheet value of SiC MOSFET.

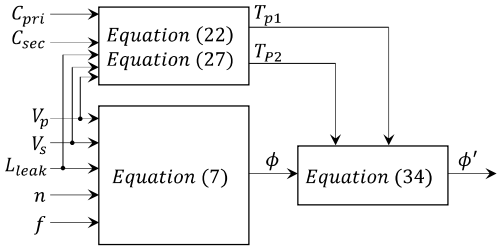

FIGURE 9. Control block diagram for compensated phase shift angle ϕ'.

Equations (28) and (32) express the area of the leakage inductance voltage in Cases 1 and 2, respectively, as shown in Fig. 7.

Since two MOSFETs are connected in series during the dead time, the maximum value of the sine waves of S_1 and S_3, representing the area at the dead time, is twice the maximum voltage of the MOSFET. S_2 is equal to that in (30) considering all delay times by the input/output parasitic capacitance.

For the leakage inductance currents of Cases 1 and 2 to be the same, (28) and (32) must have the same values.

$$S = V_L\phi \tag{28}$$

$$S_1 = 2V_{cpp}\int_0^{T_{p1}}\sin(2\pi f_{1o}t)\,dt \tag{29}$$

$$S_2 = V_L\left(\phi' - T_{d(off)1} - T_{p1} + T_{d(off)2}\right) \tag{30}$$

$$S_3 = 2V_{cps}\int_0^{T_{p2}}\sin(2\pi f_{2o}t)\,dt \tag{31}$$

$$S' = S_1 + S_2 + S_3 \tag{32}$$

Thus, the proposed phase shift angle ϕ'considering the parasitic capacitance is as follows:

$$S = S' \tag{33}$$

$$\phi' = \frac{S - S_1 - S_3}{V_L} + T_{d(off)1} + T_{p1} - T_{d(off)2} \tag{34}$$

Fig. 9 shows control block diagram for compensated shift angle ϕ'.

IV. SIMULATION AND EXPERIMENT RESULTS

A. SIMULATION RESULTS

The Level-2 MOSFET model in PSIM can be consider the intrinsic and parasitic components. Table 2 attributes to the Level-2 MOSFET in PSIM [31].

TABLE 2. Attributers for level-2 MOSFET In PSIM [31].

Parameters	Description
Vbreakdown (drain-source)	Maximum drain–source voltage without causing avalanche breakdown, in V.
On Resistance *RDS(on)*	On resistance $R_{DS(on)}$ of the MOSFET, in Ohm.
Gate Threshold Voltage VGS(th)	Threshold voltage of the gate-to-source voltage, in V, above which, the MOSFET starts conducting.
Internal Gate Resistance	Internal gate resistance, in Ohm.
Transconductance	Transconductance g_m of the MOSFET.
Capacitance *Cgs*	Gate-to-source intrinsic capacitance, in F.
Capacitance *Cgd*	Gate-to-drain intrinsic capacitance, in F.
Capacitance *Cds*	Output capacitance between drain and source, in F.
Diode Forward Voltage	Forward voltage of the anti-parallel diode, in V.
Diode Resistance	ON resistance of the anti-parallel diode, in Ohm

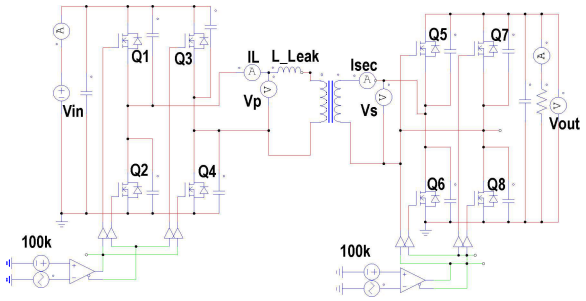

FIGURE 10. PSIM model of DAB converter with Level-2 MOSFET for simulation.

TABLE 3. Terms for simulation.

Parameter	Unit	Specification
Input Voltage: V_{in}	V	450
Output Voltage: V_{out}	V	281.25
Power: P_{in}, P_{out}	W	3,164
Switching Frequency: f_{sw}	kHz	100
Transformer turn ratio: n		1.6
Leakage Inductance: L_{Leak}	μH	53

Fig. 10 shows that the PSIM model of DAB converter consists of Level-2 MOSFET for simulating the proposed method.

Table 3 shows the conditions for the characteristic analysis. In Fig. 11, the parasitic capacitance corresponding to Table 3 is shown in Table 4.

Fig. 12 shows the comparison of output characteristics according to the size of parasitic capacitance of MOSFET. The output characteristics according to the size of the parasitic capacitance were compared using two SiC MOSFET models as follows. SiC MOSFET I is the model used for the experiment in this paper, and SiC MOSFET II is a model designed so small that the parasitic capacitance is negligible.

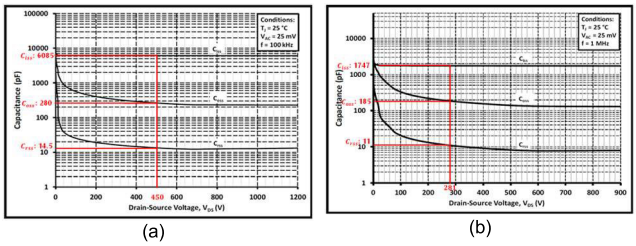

FIGURE 11. Nonlinearity of parasitic capacitance by the drain–source voltage [32], [33]. (a) C3M0016120K: Primary SiC MOSFET. (b) C3M0030090K: Secondary SiC MOSFET.

TABLE 4. Parasitic capacitance of MOSFET according to V_{ds}.

Parameter	Unit	Value	Parameter	Unit	Value
$C_{iss}\|_{V_{DS}=450V}$	pF	6,085	$C_{iss}\|_{V_{DS}=281}$	pF	1,747
$C_{oss}\|_{V_{DS}=450V}$	pF	280	$C_{oss}\|_{V_{DS}=281}$	pF	185
$C_{rss}\|_{V_{DS}=450V}$	pF	14.5	$C_{rss}\|_{V_{DS}=281}$	pF	11

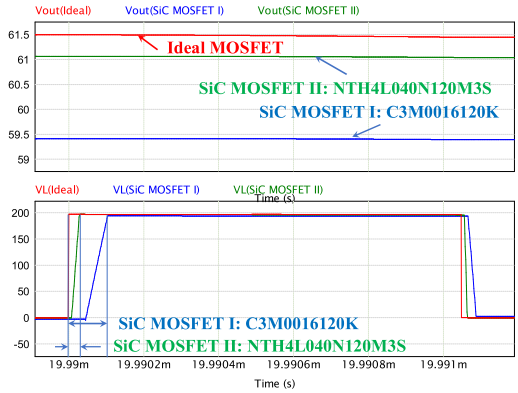

FIGURE 12. Comparison of output characteristics according to the size of parasitic capacitance of MOSFET.

TABLE 5. Comparison of output voltage according to the size of parasitic capacitance of MOSFET.

Model	Output Voltage [V]	Ratio [%]
Ideal MOSFET	61.54	100
SiC MOSFET I	59.41	96.6
SiC MOSFET II	61.06	99.3

1) SiC MOSFET I

Wolfspeed C3M0016120K (C_{iss}: 6,085 pF, C_{oss}: 230 pF)

2) SiC MOSFET II [34]

Onsemi, NTH4L040N120M3S (C_{iss}: 1,700 pF, C_{oss}: 80 pF)

In Fig 12, SiC MOSFET II with low parasitic capacitance has a lower delay time than SiC MOSFET I and has almost similar output characteristics to ideal MOSFETs.

Table 5 shows the comparison of output characteristics in Fig. 12. SiC MOSFET II with low parasitic capacitance had a value of 99.3% of the output voltage of the ideal MOSFET, but the output voltage of SiC MOSFET I with high parasitic capacitance was 96.4% of the ideal MOSFET output voltage.

TABLE 6. Specifications of the experimental devices and components.

Device and Components	Specification
Primary-side SiC MOSFET	Wolfspeed, C3M0016120K
Secondary-side SiC MOSFET	Wolfspeed, C2M0030090K
High Frequency Transformer	L_{leak}: 53 μH, $Turn\ Ratio$: 1.6: 1

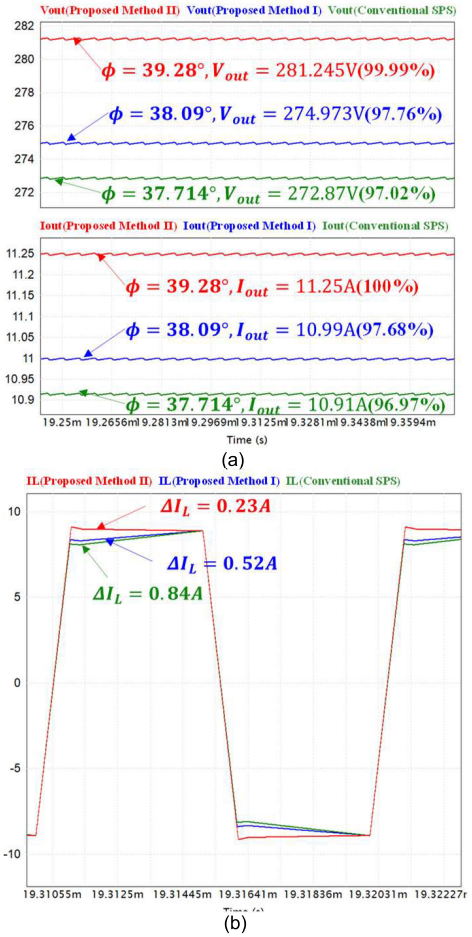

FIGURE 13. Comparison of control characteristics (V_{in} = 450V). (a) Output voltage and current. (b) Leakage inductance current.

TABLE 7. Specifications of the DAB converter.

Parameter	Specifications
Input Voltage Range	100~ 500 V_{dc}
Output Voltage Range	62.5~312.5 V_{dc}
Output Power Rating	4 kW
Switching Frequency	100 kHz

Therefore, a compensation method according to the size of the parasitic capacitance is required.

To analyze the influence of MOSFET output and input parasitic capacitance, the method proposed in the paper was compared according to the following two conditions.

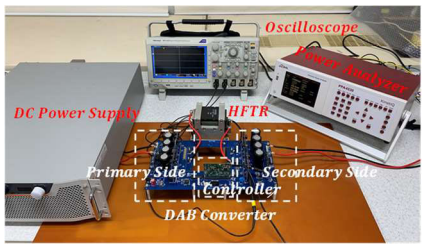

FIGURE 14. Experimental devices for performance analysis.

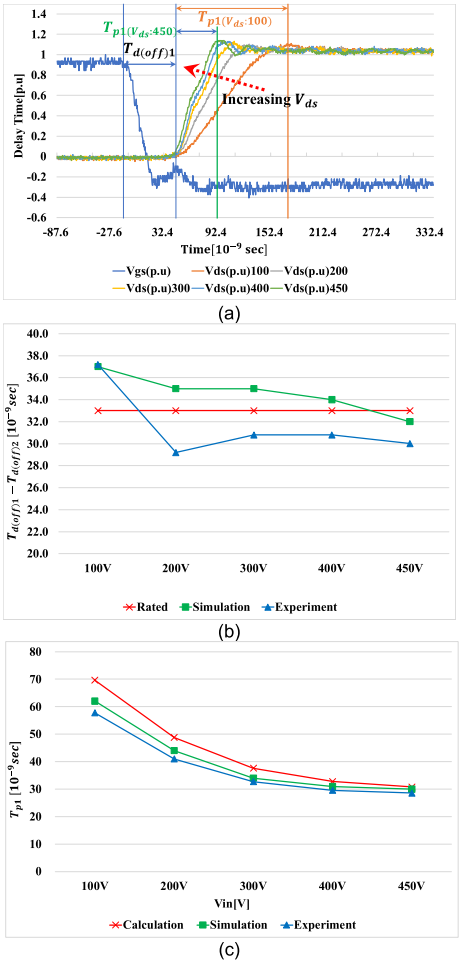

FIGURE 15. Characteristics of the gate–source voltage (V_{gs}) and the drain–source voltage (V_{ds}). (a)V_{gs} (p.u) and V_{ds} (p.u). (b)$T_{d(off)}$. (c) T_{d1}.

3) Proposed Method I

Compensated phase shift angle considering only the output parasitic capacitance (C_{oss}) of MOSFET

4) Proposed Method II

Compensated phase shift angle considering both the output parasitic capacitance (C_{oss}) and input parasitic capacitance (C_{iss}) of MOSFET

The compensated phase shift angle calculation (Proposed Method I) considering only the output parasitic capacitance (C_{oss}) is expressed as follows:

$$\phi' = 1058.19 \times 10^{-9}\text{s} = 38.09^{\circ} \tag{35}$$

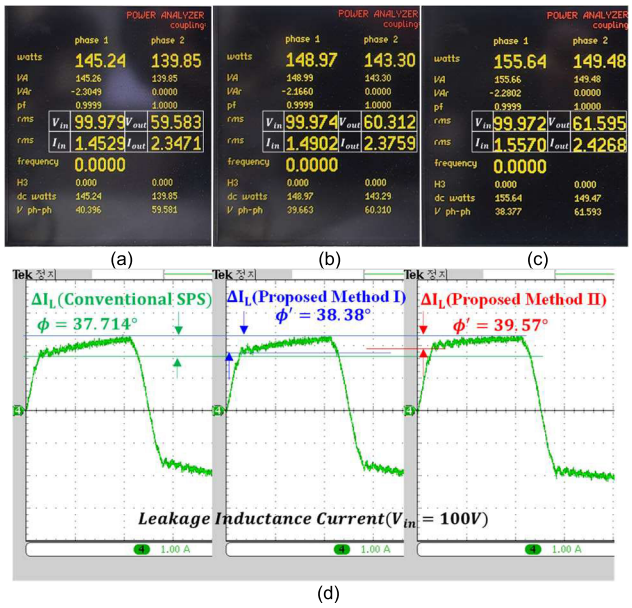

FIGURE 16. Input and output characteristics of the DAB Converter ($V_{in} = 100V$). (a) SPS. (b) Method I. (c) Method II. (d) Leakage inductance current.

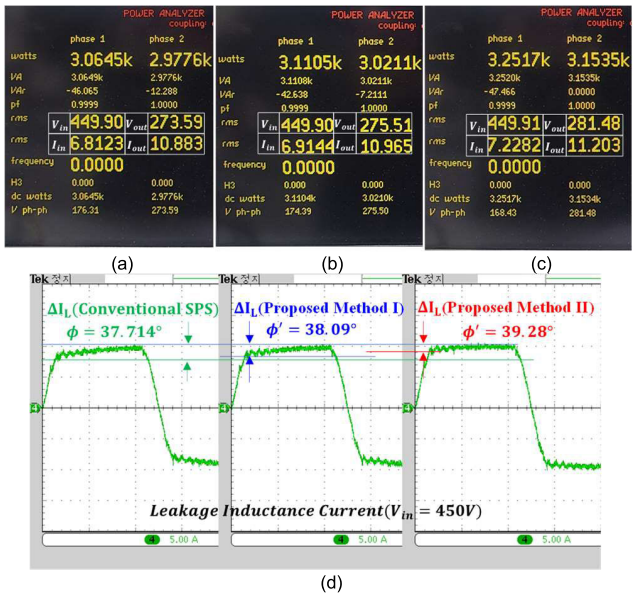

FIGURE 17. Input and output characteristics of the DAB converter ($V_{in} = 450V$). (a) SPS. (b) Method I. (c) Method II. (d) Leakage inductance current.

The compensated phase shift angle calculation (Proposed Method II), considering the parasitic capacitance of input (C_{iss}) & output (C_{oss}) is expressed as follows:

$$\phi' = 1091.19 \times 10^{-9}\text{s} = 39.28° \tag{36}$$

Fig. 13 shows the control characteristics under the conditions listed in Table 3. In Fig. 13(a), when controlled by the conventional SPS method, the effect of parasitic capacitance on the switching is not compensated; thus, it has the lowest accuracy. The accuracy slightly increased when only the output parasitic capacitance was considered (Method I), and the highest accuracy was obtained when both the input and output parasitic capacitances were considered (Method II).

When no phase shift occurs between the primary and secondary side, as the value of k representing the voltage ratio of the DAB converter reaches closer to one, the leakage inductance current change becomes smaller.

Therefore, in Fig. 13(b), the change in leakage inductance current of Method II which has the output voltage closest to the secondary rated value, is the smallest.

B. EXPERIMENT RESULTS

Fig. 14 shows the experiment configuration. Table 6 shows the primary devices and components used for the experiment.

Table 7 shows the primary specifications of the DAB converter.

The experiment analyzed the characteristics when the input voltage was changed from 100 to 450 V.

Fig. 15 shows the characteristics of the gate–source voltage (V_{gs}) and drain–source voltage (V_{ds}) when the input voltage is changed. Fig. 15 (a) shows the turn-off delay time ($T_{d(off)1}$) by the input parasitic capacitance and the delay

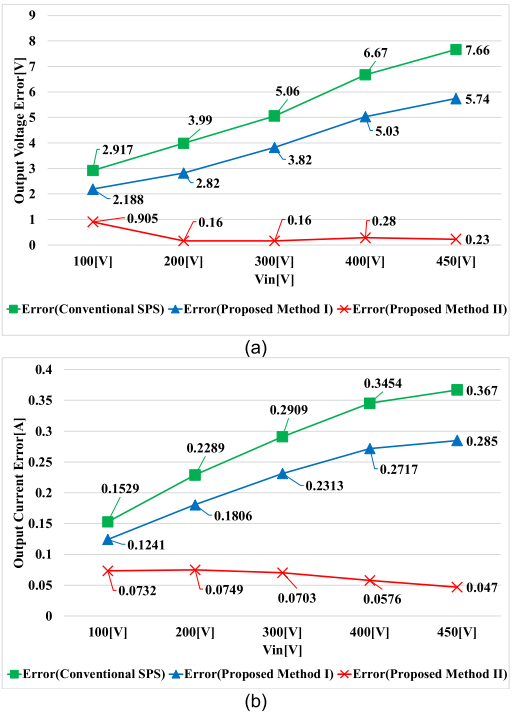

FIGURE 18. Errors in the output voltage and output current. (a) Output voltage error. (b) Output current error.

time (T_{p1}) by the output parasitic capacitance. $T_{d(off)1}$ barely changes despite changing the voltage because the input parasitic capacitance has low dependency on voltage. However, T_{p1} changes as the output parasitic capacity vary with voltage.

Fig. 15(b) shows the difference ($T_{d(off)1} - T_{d(off)2}$) between the primary and secondary sides of the turn-off delay time caused by the charging and discharging of the input parasitic

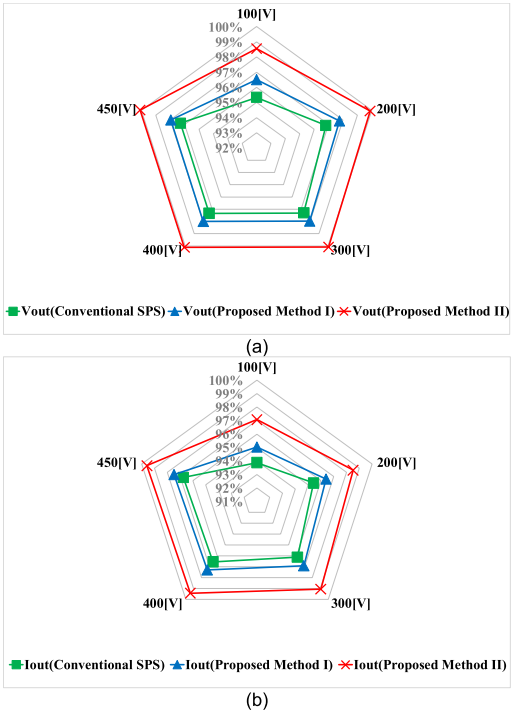

FIGURE 19. Comparison of output voltage and current accuracy. (a) Output voltage accuracy. (b) Output current accuracy.

TABLE 8. Output voltage of the DAB converter.

V_{in}[V]	Rated V_{out}[V]	Conventional	Proposed	
		SPS V_{out} [V]	Method I V_{out} [V]	**Method II V_{out} [V]**
100	62.5	59.583	60.312	**61.595**
200	125	121.01	122.18	**124.84**
300	187.5	182.44	183.68	**187.66**
400	250	243.33	244.97	**250.28**
450	281.25	273.59	275.51	**281.48**

TABLE 9. Output current of the DAB converter.

V_{in}[V]	Rated I_{out}[A]	Conventional	Proposed	
		SPS I_{out} [A]	Method I I_{out} [A]	**Method II I_{out} [A]**
100	2.5	2.3471	2.3759	**2.4268**
200	5	4.7711	4.8194	**4.9251**
300	7.5	7.2091	7.2687	**7.4297**
400	10	9.6546	9.7283	**9.9424**
450	11.25	10.883	10.965	**11.203**

capacitance of the MOSFET. The results obtained through experiments and simulations are similar to the rated values (Rated) presented in the datasheet because the turn-off delay time is approximately constant, as shown in Fig. 15(a).

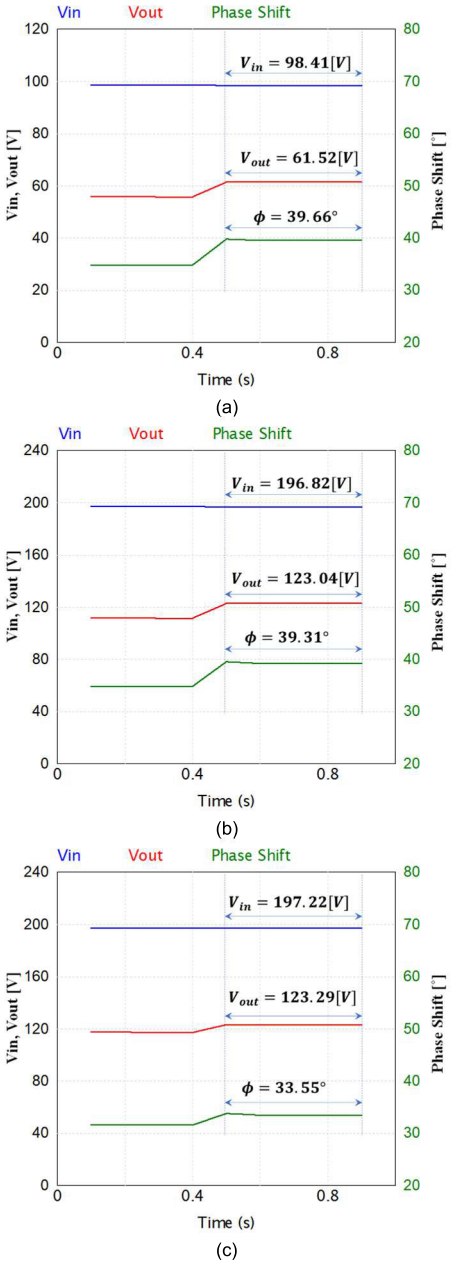

FIGURE 20. DAB converter output characteristics by closed loop control (simulation result). (a) V_{in}= 100V, R_L= 25Ω, (b) V_{in}= 200V, R_L= 25Ω, (c) V_{in}= 200V, R_L= 28Ω.

Fig. 15(c) shows the delay time (T_{p1}) characteristics caused by the resonance of the output parasitic capacitance and the leakage inductance. Comparing the results of experiments and simulations with those calculated by (34), the results appear substantially close as the input voltage increases. Since the size of the parasitic capacitance changes considerably as the voltage is lowered, the errors are relatively larger at lower voltages, but as the voltage becomes higher, the results of experiments and simulations are closer to the calculated results.

Fig. 16 and 17 show the input and output characteristics when the input voltage is 100 and 450 V, respectively.

TABLE 10. Phase shift angle comparison result.

	V_{in} = 100 V R_L = 25 Ω	V_{in} = 200 V R_L = 25 Ω	V_{in} = 200 V R_L = 28 Ω
Conventional SPS	37.71° (92.2%)	37.71° (94.7%)	32.48° (95.1%)
Proposed Method II	39.57°(96.7%)	39.37°(98.8%)	33.42°(97.8%)
Simulation	39.66°(96.7%)	39.31°(98.8%)	33.55°(98.2%)
Experiment	40.90°	39.79°	34.15°

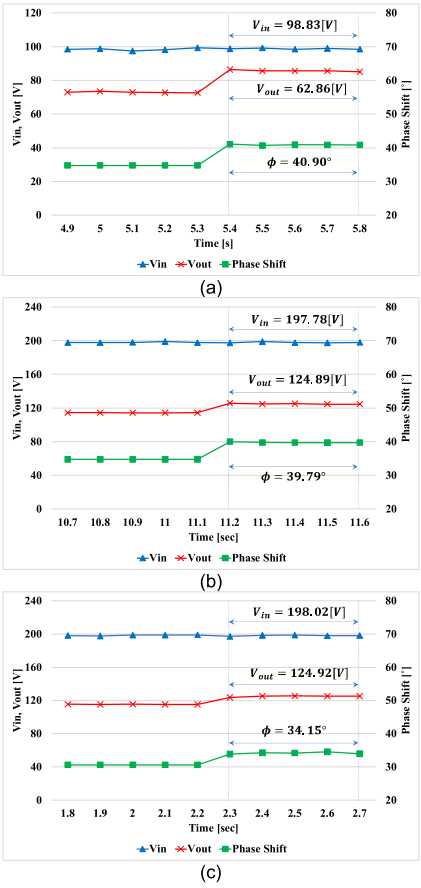

FIGURE 21. DAB converter output characteristics by closed loop control (experiment result). (a) V_{in}= 100V,R_L= 25Ω, (b) V_{in}= 200V,R_L= 25Ω, (c) V_{in}= 200V,R_L= 28Ω.

Fig. 16(a) and 17(a) show the conventional SPS method, Fig. 16(b) and 17(b) show the input and output characteristics when only the effect of the output parasitic capacitance is considered (Method I), and Fig. 16(c) and 17(c) show the input and output characteristics when both the input and output parasitic capacitances are considered (Method II).

Fig. 16(d) and 17(d) show the leakage inductance current comparison. When the phase angle is compensated considering all the parasitic capacitance, the current change in the leakage inductance is the smallest.

Tables 8 and 9 are the results of comparing the output voltage and current characteristics when the input voltage is varied from 100 to 450 V.

Fig. 18 shows the error between the rated values and the output values in Tables 8 and 9. When the input voltage rises, the voltage and current errors increase when the conventional SPS and output parasitic capacitance are considered, but the error of output voltage and current when the phase shift angle is compensated by considering both the input and output parasitic capacitances decrease. Fig. 19 shows the accuracy comparison according to Tables 8 and 9.

When the phase shift angle is compensated through (36), the accuracy of the output voltage and current becomes the highest.

When the input voltage is 450 V, the accuracy of the proposed method is close to 100% (voltage 100%, current 99.5%). The method presented in the paper improved the existing SPS method (output voltage error: 97.2%, output current error: 96.7%) by about 3%.

C. CLOSED LOOP CONTROL RESULTS

Fig. 20 and 21 show the results of simulation and experiment, respectively, when the DAB converter is controlled by the closed loop method. Fig. 20, 21 (a) and (b) show the characteristics of input voltage change from 100 V to 200 V when the load resistance is 25 Ω. Fig. 20, 21 (b) and (c) show the response characteristics when the load resistance is changed to 28 Ω at the same voltage.

Table 10 shows the comparison of the phase shift angle calculated by the method proposed in the paper and the phase shift angle by the closed loop method in Fig. 20 and 21.

V. CONCLUSION

This study proposed a novel phase shift angle compensation method of the DAB converter considering the parasitic capacitance of SiC MOSFET. MOSFETs have an inherent parasitic capacitance due to their electrical structure. The input parasitic capacitance is charged and discharged when a signal is input to the gate, and a time delay occurs in this process.

A DAB converter has a full-bridge-type switching part at both ends, inductor, and transformer. The dead time was used to prevent the arm-short in the full bridge applied to both ends. During this dead time, the leakage inductance of the inductor and transformer and the output parasitic capacitance of the SiC MOSFET resonated and affected the control characteristics of the DAB according to this resonance phenomenon.

Therefore, in this study, the delay time was calculated considering the input and output parasitic capacitances of the SiC MOSFET. A method of compensating for the phase shift using this delay time was proposed. For the proposed method, simulations and experiments using an actual DAB were performed under changing voltage and parasitic capacitance conditions.

When the phase shift angle was compensated by considering both the output and input parasitic capacitances with the method presented in the paper, the accuracy of the output voltage and current became almost 100% and was improved by 3% compared to the conventional SPS method.

The proposed in this paper was very close to the phase shift angle obtained through closed loop control.

This improvement in accuracy was expected to significantly contribute to the performance improvement of bidirectional charging and discharging systems for e-mobility, aircraft, and precision systems using DC source.

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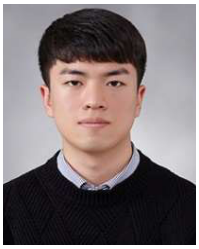

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