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TOPICAL REVIEW

Realizing Joint Communication and Sensing RF Receiver Front-Ends: A Survey

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ABSTRACT Joint Communication and radio Sensing (JC&S) has gained significant attention over the past few years. The advantages of this technology include reduced cost, size and power consumption. With further advancements in JC&S systems, it can potentially be used in next-generation cellular networks, internet-of-things and upcoming applications such as Industry 4.0, where a single system is capable of performing a wide variety of functions or tasks. The inclusion of this technology will result in improved performance and safety of the systems. Even though communication and radio sensing make use of a similar Radio Frequency (RF) front-end, the specifications for both these technologies mainly differ in terms of bandwidth and linearity. In this survey, a detailed study of the specifications of radar and communication systems was conducted. For the RF front-end to operate efficiently in both radar and communication modes, there must be reconfigurability in terms of frequency, bandwidth, gain and linearity. In this survey, we investigated different frequency, bandwidth, gain and linearity reconfigurable low noise amplifier (LNA) and down-conversion mixer architectures. The merits and demerits of each architecture are discussed and a summary of the performance of the reconfigurable LNAs and down-conversion mixers in the literature is presented. Finally, possible topologies for JC&S are deduced based on their performance.

INDEX TERMS Frequency reconfiguration, joint communication and sensing, multi-mode LNA, multi-mode down conversion mixers, reconfigurable RF front-end, variable gain, CMOS.

I. INTRODUCTION

Joint Communication and radio Sensing (JC&S) has attracted significant attention in recent years and is expected to be one of the key features of future 6G wireless networks [1], [2]. JC&S allows the efficient use of the limited spectrum and also, offers the possibility of sharing hardware resources. The advantages can be seen in the cost, size, power consumption, performance and safety of the system. Reconfigurability and tuning of hardware will play an important role in meeting the diversity of needs and enabling the reuse of hardware whenever possible, thus fully utilizing its benefits. With programmable circuitry, JC&S can be better supported in future networks and applications, without adding overheads.

To date, communication and sensing technologies have been mostly studied and developed separately. Wireless communication technologies allow the transmission of data and information between the sender and receiver through wireless channels while, radio sensing (e.g. Radar) refers to the detection of objects/targets, their location, movements, speed, shape and environment. Current state-of-the-art communication technologies employ half-duplex communication techniques whereas, the full-duplex mode is mostly used for mono-static radars and, the half-duplex mode in pulsed radar. However, both communication and radar rely on the same physical phenomenon of sending and receiving electromagnetic waves. Hence, potentially the same

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spectrum, hardware and signal waveforms can be used for both the purposes. As shown in Fig. 1, the same signal is transmitted to convey information from A to B and it will also be reflected by the objects in the vicinity. These reflected signals can be processed at A to estimate the position and velocity of the objects, while sending communication data to B which can be not just limited to the object information.

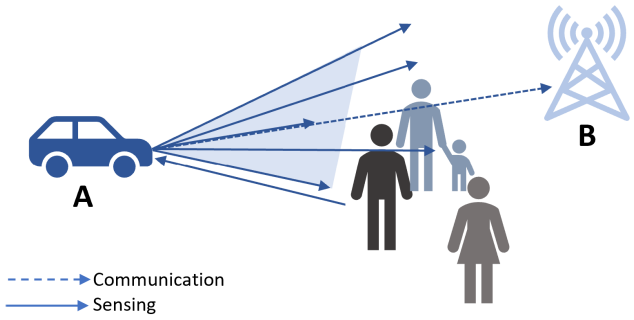

FIGURE 1. Application of JC&S.

However, combining these two technologies requires finding a shared solution in terms of the hardware, waveforms transmission, reception and modulation techniques. A survey of modulation schemes that support JC&S is given in [3]. There are several approaches for combining radar and communication systems. An existing radar system can be used to add communication functionalities to it [4], [5]. Alternatively, radar functionalities can be added to a communication system or a co-designed system can be developed [6]. The different transmit-receive techniques possible in JC&S, considering the current state of the art are: 1) half-duplex communication with half-duplex radar 2)half-duplex communication with full-duplex radar, and 3)full-duplex communication with full duplex radar. A half duplex communication with half duplex radar for JC&S system model was proposed in [7] using zero-padded Orthogonal Frequency Division Multiplexing (ZP-OFDM). This method used the guard interval between symbols for radar detection and environment sensing while, the rest of the symbol was used for communication. The second technique involving half-duplex communication and full-duplex radar was mentioned in [4], where a joint Frequency Modulated Chirp Waveform (FMCW) for both communication and radar was proposed. The communication link was operated in Time Division Duplex (TDD) mode. Chirp pulse position modulation was used in [5] where communication information was encoded using time shifts in the transmitted signals. This enables a system architecture in which it is possible to obtain sensing data while having spectral access between users to perform other functions, including communications. These modes require the receiver to work in both radar mode and communication mode, which have different specifications when it comes to the Radio Frequency (RF) front-end.

A number of front-end JC&S architecture implementations are already listed in literature. Most of such architectures concentrate on the modulation of the waveforms and use the same front-end in both modes. An FMCW waveform with data modulated into it with Frequency Shift Keying (FSK) was proposed in [8]. Reference [9] proposed a system where wireless communication and sensing functions are fully integrated and sequentially arranged in time domain using a time-agile modulation scheme. In radar mode, the signal splits into two halves using a Substrate Integrated Waveguide (SIW) whereas in the communication mode, the Local Oscillator(LO) is unmodulated. Reference [10] uses a Direct Digital Synthesizer (DDS) to generate a modulated waveform which separates the radar and communication modes in time domain. Switched architectures were proposed in [11] and [12], where the input to the mixer decides the mode of operation. A reconfigurable architecture could be a key element in realizing hardware reuse. Such a transceiver architecture was proposed in [13] with reconfigurabilty embedded in LNA, Power Amplifier (PA), up and down converters and analog baseband blocks. Such a system also needs a dual-mode analog-to-digital converter (ADC), reconfigurable digital processing unit and a switched architecture. A combined radar and communication receiver still needs a unified framework with concrete list of applications and Key Performance Indicators (KPIs). One of the main benefit of a joint receiver front-end is the possibility of hardware reuse. Even though the different specifications in radar and communication make it difficult to use the same design for both modes, separate hardware for the two modes as in [14] will require a larger area and higher costs. Shared hardware will facilitate the integration of this technology into applications which demand smaller form factors and hence, future applications will benefit more from a co-design approach [15].

The L-band (1 GHz-2 GHz), S-band (2 GHz-4 GHz), C-band (4 GHz-8 GHz) and the millimeter wave (mmWave) band (30 GHz-300 GHz) have already seen coexisting radar and communication systems. The mmWave band is expected to become busier owing to the increasing interest of the wireless community with regard to the mmWave wave communications [16]. The co-design opportunities are more at mmWave frequencies and hence, a key enabler for a combined front-end. As new applications and use-cases evolve, there is an increasing need to include sensing capabilities in the communication ecosystem which further propels the demand to use mmWave bands in targetted 6G networks [13].

As the need for higher data rates increased, last decades saw communication systems moving to Complementary Metal Oxide Semiconductors (CMOS) and Fully Depleted Silicon-On-Insulator (FDSOI) processes. Radar chipsets however owing to higher output power requirements and simpler baseband processing, still use Gallium Arsenide (GaAs) or Silicon Germanium (SiGe) Heterojumction Bipolar Transistor (HBT) processes along with CMOS processes. Potentially, advanced CMOS, FDSOI (45nm and lower) and SiGe BiCMOS nodes can be used for the realization of low cost JC&S receiver front-ends [13]. With 6G, the carrier

frequency is expected to go to sub-THz range and the f_T and f_{max} of the transistors will play an important role in the selection of the technology. The lower nodes provide very high f_T and f_{max}. The 45nm and 28/22nm nodes have the highest f_T and f_{max} in the range of 350 GHz-400 GHz [17]. The reported f_T and f_{max} in 22nm FDSOI technology referenced to the top metal layer is 240 GHz and 230 GHz respectively [18]. SiGe BiCMOS technology provides the possibility to extend f_T and f_{max} for higher sub-THz carrier frequencies in the range of 700 GHz and beyond. It is also reported that Partially Depleted (PD) SOI, FDSOI and SiGe technologies show better performance than bulk CMOS at D-band [17].

Some of the KPIs of an RF front-end include bandwidth, gain, noise figure (NF) and linearity of the system. These requirements differ in communication and radar, as well as in the full-duplex and half-duplex modes. A summary of the requirements for each modes is presented in Table 1.

All modes of operation require a high gain to mitigate path losses which also accounts for a larger range in the case of radar. It is also important to make use of the full-scale range of the ADC and the signal must be amplified to avoid losing any bits in ADC quantization. Usually, radar requires a larger absolute bandwidth compared to communication applications for better range resolution and context-aware use of frequency bands. Noise can affect the overall sensitivity of a system. A lower NF requirement is more stringent in the case of communication than for radar. A lower NF can contribute to a higher detection range of the radar, while reducing the bit error rate (BER) in wireless communications. The linearity requirements for radar are significantly higher than those for communication. In the case of close object detection, the incoming signal can saturate the LNA, leading to non-linearities and hence, radar applications require a higher IP1dB requirement. In the full-duplex mode, self-interference from the transmit antenna can saturate the LNA, hence, a higher linearity receiver is required in both the radar and communication modes. A combined JC&S receiver front-end would also demand high resolution ADCs.

To provide a quantitative example, we consider the 5G NR n257 band which is centered at 28GHz for communication and radar. The 3GPP specification for 5G NR user equipment in power class 4 limits the maximum transmitter output power to 23 dBm and the maximum Effective Isotropic Radiated Power (EIRP) to 43 dBm [19]. For simplicity, we assume that the self-interference in full-duplex communication and radar is negligible owing to self-interference cancellation techniques in the antenna, RF, baseband and digital domains. The sensitivity of the receiver (P_{sens}) at room temperature is given by:

$$P_{sens} = -174\,\text{dBm/Hz} + NF + 10\log_{10}(BW) + SNR_{min} \quad (1)$$

A receiver with a minimum Signal to Noise Ratio (SNR_{min}) of 5 dB and Bandwidth (BW) of 100 MHz has a P_{sens} of −84 dBm, which is the minimum signal level that a receiver can detect with acceptable quality. The Free Space Path Loss (FSPL) is given by:

$$FSPL = 20\log_{10}(d) + 20\log_{10}(f) + 20\log_{10}\left(\frac{4\pi}{c}\right) - G_{Tx} - G_{Rx} \quad (2)$$

where d is the distance between antennas, f is the frequency, c is the speed of light, G_{Tx} is the gain of the transmitter antenna and G_{Rx}, the gain of the receiver antenna.

Considering the maximum EIRP, the path loss sustained by a communication signal at a carrier frequency of 28 GHz for a distance of 1 km and 0.5 km for receiver antenna gain of 20 dB are 101.4 dB and 95.4 dB respectively. This causes the power received at the input of the LNA to be −52.4 dBm for a distance of 500 m. In the case of a radar receiver, it must be able to detect close targets depending on the application. The attenuation that occurs owing to path loss in a radar receiver, that needs to detect an object at 1 m distance is 47.4 dB, considering a fully reflective object completely in the path of the radar beam. Therefore, for the same assumptions as the communication receiver, the output power received at the LNA is −4.4 dBm, which is significantly different from the communication scenario. The power received at the LNA increases as the distance decreases and that will demand very high linearity in case of applications like gesture recognition. In addition, radar signals typically involve short durations and high power signals transmitted at regular intervals. This can also increase the linearity requirements. This causes a substantial difference in the linearity requirements of the communication and radar receivers.

Frequency tunability in conventional communication receivers facilitates multi-band and multi-standard receivers.

TABLE 1. Requirements of radar and communication front-ends in full-duplex and half-duplex modes.

Half-duplex Mode		Full-duplex mode	
Radar	**Communication**	**Radar**	**Communication**
• High gain	• High gain	• High gain	• High gain
• High absolute bandwidth	• Low absolute bandwidth	• High absolute bandwidth	• Low absolute bandwidth
• Relaxed NF requirement	• Low NF	• Relaxed NF requirement	• Low NF
• High 1 dB compression point (IP1dB)	• Relaxed IP1dB requirement	• High IP1dB	• High IP1dB

A wide-band system is subjected to large interferers and out-of-band blockers, which reduces the sensitivity of the overall system. Multi-band systems operating in multiple narrow bands ensure noise and interference reduction, resulting in increased sensitivity and selectivity of the receiver. Frequency tunability facilitates band selectivity and isolation. Additionally, dynamic frequency tuning can reduce the impact of interference and improve the overall performance of the system. The transmitter can periodically measure the power level and interference levels, when not actively transmitting, in order to understand the spectrum usage and thereby change the transmit frequency to a different carrier frequency if needed. This requires frequency tuning at the receiver side. The bandwidth of short-range automotive radars ranges from 1 GHz-5 GHz whereas that of communication applications varies between a few hundred megahertz. Thus, for a JC&S system, frequency tuning would mean tunability in both frequency and bandwidth.

The question to be addressed here is whether to design a receiver that provides high gain, high linearity, low NF and high absolute bandwidth for JC&S applications, while considering power consumption. This point has been addressed in [20] with an example of an LNA. Fig. 2 shows the performance variations of a reconfigurable LNA. To answer the question above, to attain the best performance in all the parameters, one would have to design an LNA with a higher power consumption. The next component in the front-end receiver chain is the down-conversion mixer. The third-order intercept point (IIP3) and the IP1dB of the mixer are usually the limiting factors that determine the overall linearity of the receiver. Since the LNA provides sufficient gain, the linearity of the mixer affects the overall linearity and sensitivity of the receiver more than the LNA linearity. Hence, we studied the state-of-the-art highly linear and reconfigurable mixer architectures. The reconfigurability is addressed in frequency, gain and linearity.

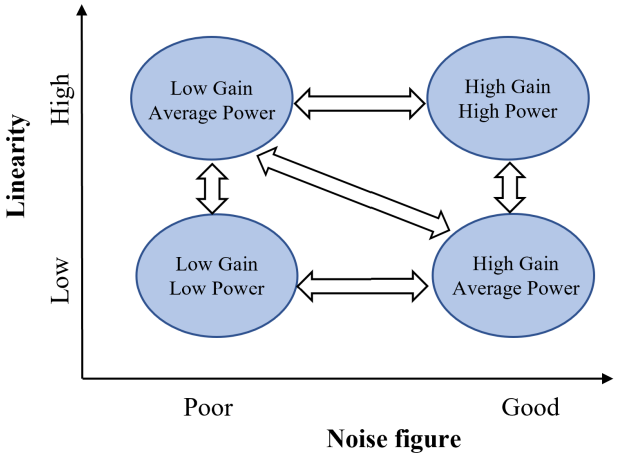

FIGURE 2. Performance matrix of a reconfigurable LNA [20].

The remainder of this paper is organized as follows. Section II compares the state-of-the-art radar and communication receivers and outlines the difference in specifications for both technologies. Sections III and IV explain the various frequency reconfigurable and variable gain LNA architectures respectively. Their advantages and disadvantages are also discussed along with a comparison of the previously published reconfigurable LNAs. Section V explains the possible topologies for a JC&S recconfigurable mixer. Finally, section VI concludes the study.

II. STATE-OF-THE-ART RADAR AND COMMUNICATION RECEIVERS

It is important examine the actual implementations of radar and communication receivers and deduce the differences in specifications and performances. Here, we look at a few state-of-the-art receivers that are specifically designed for radar and communication applications. Table 2 compares the performance of the radar and communication receivers in similar frequency bands. Implementations in the E band were considered for comparison.

The main difference between radar and communication receivers can be observed in the linearity and noise figure requirements. As discussed in the previous section, radar demands higher linearity whereas communication receivers require a lower NF and a comparably higher gain. Even though the table shows a larger bandwidth for communication applications, in reality, the bandwidth requirement is less when compared to that of radar in most applications and does not require multi Gbps (Giga bits per second) data rates.

Multi-functional RF systems and front-ends are the focal points for facilitating spectral convergence and hardware sharing [5]. For a half-duplex JC&S receiver, this would mean that the receiver can operate in the low gain-high linearity radar mode and high gain-low linearity communication mode. However, for a full-duplex JC&S receiver, the receiver must provide high linearity and gain simultaneously. This requirement can be relaxed and converted to a multi-mode

TABLE 2. Comparison of radar and communication receiver specification.

Radar Receiver						
Ref	Tech	Freq. (GHz)	BW (GHz)	Gain (dB)	NF (dB)	IP1dB (dBm)
[21]	40nm CMOS	76.5	1	17	8.7-14	-7.4
[22]	45nm CMOS	78.5	5	-	13.8	-10
[23]	65nm CMOS	78.5	5	15	10-11	1
[24]	45nm CMOS	78.5	4	-	18	-7
[25]	65nm CMOS	78.5	4	26.2	15.3	-8.5
Communication Receiver						
[26]	28nm CMOS	75	27.5	30.8	7.3-9.1	-30.7
[27]	45nm SOI	67	16	27.1	3.6-5	-21.5
[28]	28nm CMOS	75.1	12.5	28	8.3-10	-25
[29]	28nm CMOS	79	8	35	6.2-7	-32.5
[30]	130nm SiGe	73	5	70	6-7	-19.6

front-end if radar sensing happens in short intervals and most (e.g. 95%) of the time is dedicated to communication and hence, preserving an almost full-duplex operation.

III. FREQUENCY RECONFIGURABLE LNAs

Frequency-reconfigurable LNAs enable multi-band, multi-mode operation of JC&S while ensuring the selectivity and sensitivity of the receiver. Bandwidth tuning ensures multi-mode operations where a larger bandwidth is needed in the radar mode than in the communication mode. The frequency of operation also affects the choice of matching elements which will affect the topology used for frequency reconfigurability. Also, one main challenge of designing a frequency reconfigurable LNA is to attain the same results in terms of gain, linearity, NF and power while switching the frequency bands.

Various frequency-tunable LNA architectures have been proposed in the literature. In this survey, we look at cost-effective and area-effective architectures. Reconfigurability can be achieved by designing many LNAs, placing them as an array and switching between different frequencies using a multiplexer switch as in [31]. Three parallel paths were provided for each band and each path was switched on using a digital control in [32]. However, this would require larger area and power depending on the number of bands that the design has to cover. Therefore, in this survey, we examine designs with tunability inherent in the design, which facilitates reduction in the overall area and cost.

Tunability in frequency can be achieved by tuning the input or output matching networks as shown in Fig. 3. Fig. 4 and Fig. 5 shows the different possibilities listed in literature for input tunability and output tunability in the matching network of frequency tunable LNAs, respectively. Input tunability can be achieved by tuning the gate inductor, L_g as shown in Fig. 4.(a) and output tuning can be attained by tuning the output matching network as shown in Fig. 5.(a). Typically, one or more techniques are applied to design tunable LNAs. Also, the techniques depend a lot on the frequency of operation. As the frequency of operation shifts to higher mmWave bands, designs with transmission line matching will become more prominent. Table 3 summarizes the advantages and disadvantages of techniques used in frequency-reconfigurable LNAs. The methods are described in the following subsections. Table 4 summarizes the performance of frequency-tunable LNAs reported in the literature.

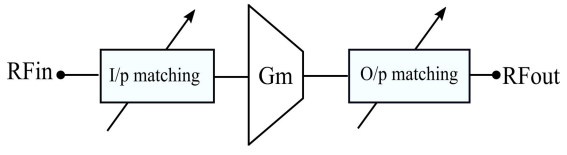

FIGURE 3. General concept of frequency tunable LNAs.

A. SWITCHED MULTI-TAP TRANSFORMER

The switched multi-tap transformer as shown in Fig. 4.(b) is typically used in the input matching network of a common-source (CS) LNA. The operating frequency of a CS LNA can be controlled by changing the value of the series gate inductor, L_g or the source degeneration inductor L_s or the C_{gs} of the transistor in Fig. 4.(a). Changing L_g or C_{gs} changes the imaginary part of the input impedance, and hence, multi-mode LNA input matching usually makes use of changing/switching L_g. The use of a transformer saves area and can be used as a tunable inductor. As reported in [33] and [34], the series gate inductor of the CS configuration is replaced by a multi-tap transformer to realize a multi-mode LNA. The transformer has a primary, L_1 and a secondary, L_2 inductor. L_2 is divided into two sections, L_{s1} and L_{s2} which have different coupling coefficients, k_a and k_b respectively as shown in Fig. 4.(b). Each section of the secondary can be open, shorted or terminated with a capacitor resulting in different operating frequencies and hence, matching. This method also has the flexibility to work for narrow band and wide band matching. The segments in the secondary inductor have to be switched on/off using switches and the parasitics associated with the switches can cause a shift in the matching frequency and can also cause additional losses. The on-resistance and the off-capacitance of the switches can limit the gain of the circuit as we move to the mmWave frequencies. In addition to multi-tap transformers, an n-winding transformer can also be used for frequency tuning. A 3-winding transformer load was used in [35]. The 3-winding transformer as load provides 3 parallel paths providing the flexibility to be used in a wide-band, high frequency band and low frequency band mode. The input matching network provides wide-band matching. Because of the 3 parallel signal paths and output matching networks, the area and power consumption of this design are comparatively higher.

B. SWITCHED MULTI-TAP INDUCTOR

Similar to the switched multi-tap transformer topology, the multi-tap inductor, as depicted in Fig. 4.(c), comes with switching elements, which can cause frequency deviations due to parasitic elements [52], [55]. Each switching frequency must be matched in the output matching network as well. This method supports only coarse tuning of the frequency, facilitating easy reconfigurations. Other techniques have to be implemented in the case of fine tuning. A switched inductor using substrate shield inductor was used for input matching in [54]. The inductance was varied by changing the coupling to the ground shield. Switched multi-tap inductors can also be used in the output frequency tuning network, as in [53], where a complimentary switched capacitor array is used to switch the inductors.

C. TUNABLE FLOATING INDUCTOR

This architecture as shown in Fig. 4.(e) achieves tunability by scaling the gate inductance by adding an amplifier in the feedback-loop of the input matching network [37]. The inductor value changes depending on the amplifier gain. This method provides continuous input tuning but can cause a frequency shift at the input and can also result in increased power consumption.

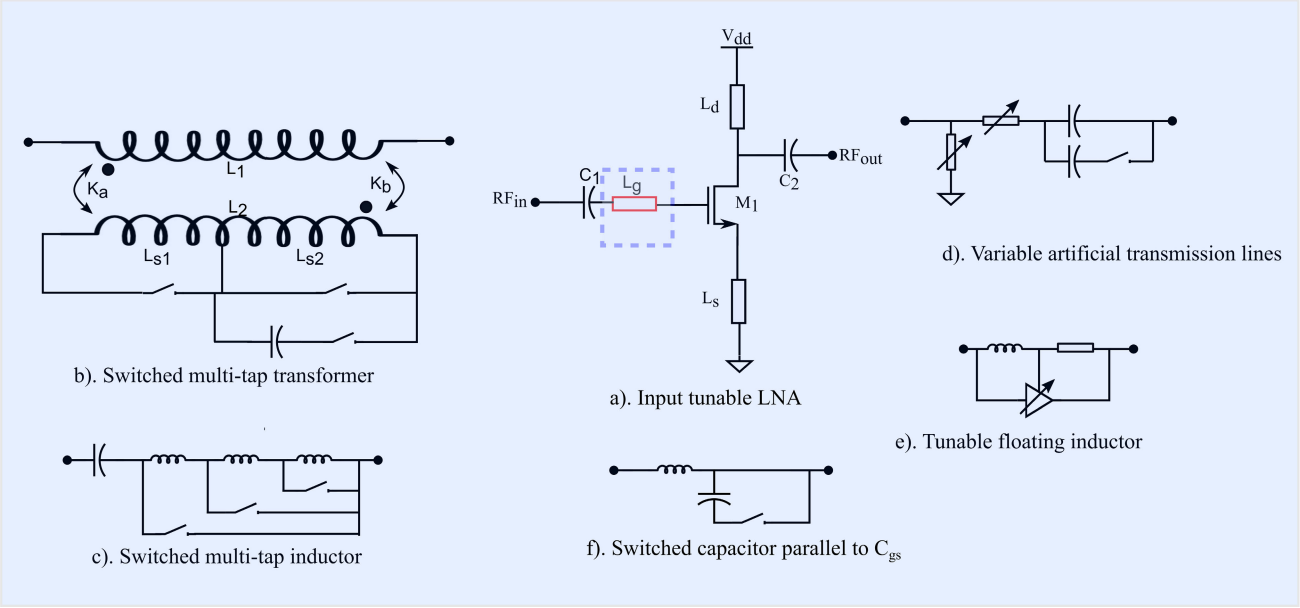

FIGURE 4. Input tunable LNA topologies.

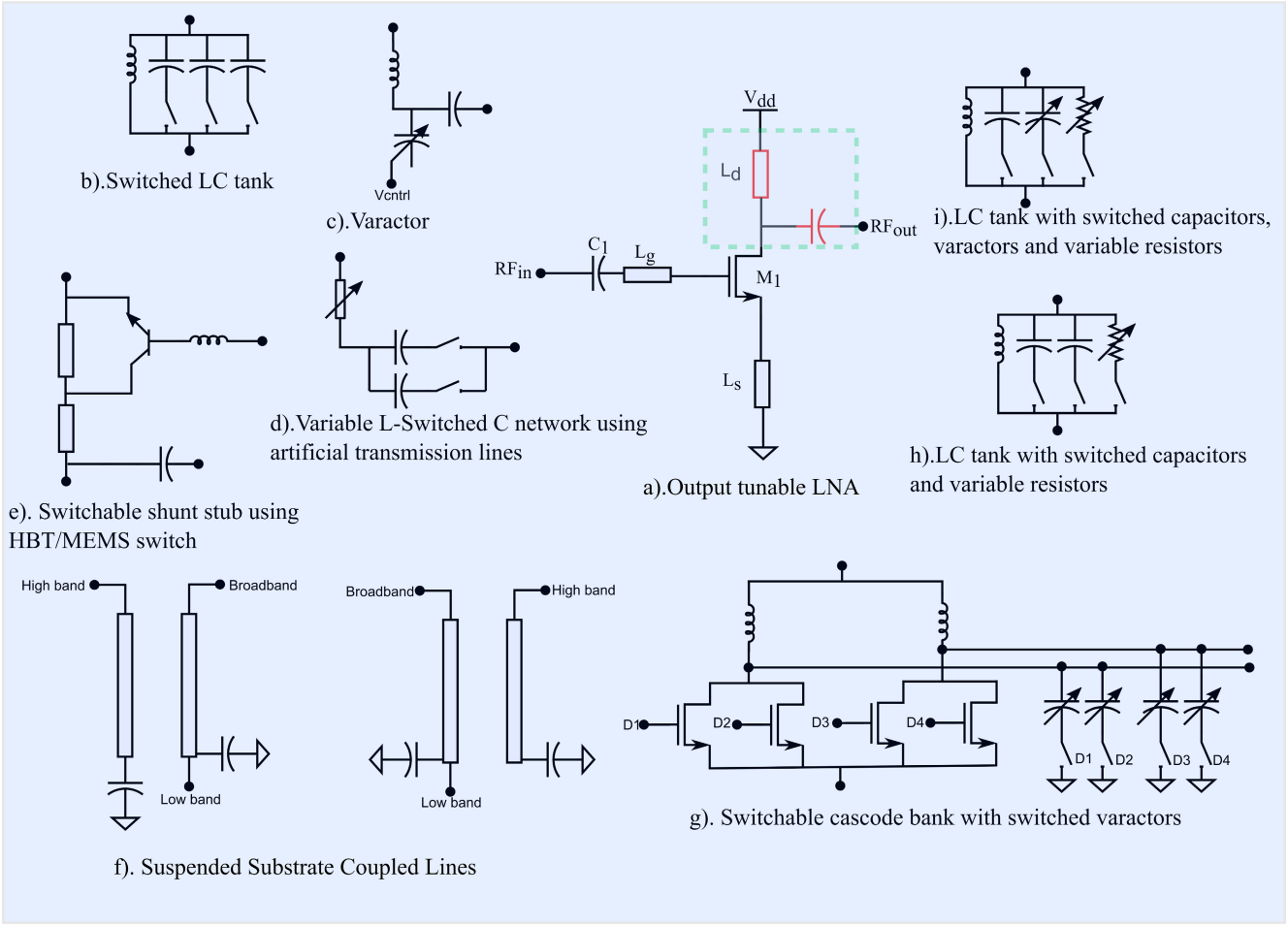

FIGURE 5. Output tunable LNA topologies.

TABLE 3. Advantages and disadvantages of frequency reconfigurable LNA techniques proposed in literature.

References.	Section	Technique	Advantages	Disadvantages
[33], [34], [35]	III-A	Switched multi-tap transformer with CMOS switches	• Flexible frequency switching • Possibility of narrow band and wide band matching	• Use of parasitic capacitances for tuning can cause frequency deviation • Higher area and power [35]
[36]	III-B	Switched inductors	• Wide frequency tunability	• Comparatively higher NF • Switch parasitics • Complicated wideband input inductor design • Lower gain at higher frequencies
[37]	III-C	Tunable floating inductor	• Continuous tuning	• Can cause mismatch at the input • Can result in increased power consumption
[38]	III-D	Switched capacitor parallel to C_{gs}	• Less area	• Switch parasitics • Can cause gain degradation
[20]	III-E	LC resonance tank with multi-tapped switched inductors and varactors	• Coarse and fine tuning possibility • Highly reconfigurabile	• Switch parasitics can change resonant frequency • Low Quality-factor (Q-factor) of the varactors might degrade the gain
[39]	III-E	LC resonance tank with switched substrate shield inductors and switched capacitors	• Less area	• Switch parasitics can change resonant frequency • High NF • Low gain • Complexity of providing effective ground for the shield inductor
[40]	III-E	RLC tank with RC tuning and varactor	• Coarse and fine tuning possibilities • Tunable bandwidth and tunable centre frequency	• Need of a digital interface
[41], [42]	III-F	Varactor	• Continuous tuning	• Parasitics can affect the tuning range • Low Q-factor of the varactors might degrade the gain • Need for broadband input matching
[43]	III-G	Variable artificial transmission lines and switched capacitors	• Highly reconfigurable • Compact area	• Large number of control pins and hence require a digital interface
[44], [45], [46], [47]	III-I	Tunable stub using HBT/MEMS switch	• Less area	• Switch parasitics and losses • Less flexibility in tuning
[48], [49], [50], [51]	III-J	Suspended Substrate Coupled Lines (SSCL)	• Switch-free architecture	• Introduce additional insertion loss that may affect performance • Large area
[52]	III-B, III-F,III-H	Switched input inductor, switched capacitor/varactor and inductors tank, switched cascode bank	• Highly reconfigurable	• No measurement data • Switch paracitics can change resonant frequency • While switching capacitors, the quality factor of the inductor cannot be kept the same across frequency bands
[53]	III-B, III-E	LC resonance tank with multi-tapped switched inductors at the output matching	• Complementary switch capacitor array to mitigate the degrading Q-factor of the inductor across frequency bands	• Comparatively higher NF
[54]	III-B, III-J	Switched substrate shield inductors at the input and variable length transmission lines at output	• Good matching in both frequency bands	• Switch non-linearities • Complexity of providing effective ground for the shield inductors
[55]	III-B, III-E	Switched multitap inductor at the input and switched capacitors at the output	• Use of phase change RF switch with low on resistance	• Switch fabrication on another process and is integrated into chip

TABLE 4. Performance comparison with previously published frequency tunable LNAs.

Ref	Tech	Vdd [V]	Note	Freq [GHz]	BW [GHz]	Gain [dB]	NF [dB]	IP1dB [dBm]	IIP3 [dBm]	Pdc [mW]	Area [mm^2]
[33]	130nm CMOS	1.2	Single band	2.8	-	16.1	1.7	-13.6**	-4	6.4	0.728
				3.3	-	14.2	3	-11.6**	-2		
				4.6	-	14.2	3.7	-12.8**	-3.2		
			Concurrent multi-band	2.05	-	14.9	4	-11.6**	-2		
				5.65	-	14.9	4.8	-13.8**	-4.2		
			Wide band	7.5	6.5	3 - 15.6	4.0 - 5.3	-14.6 ~-10.8**	-5 ~-1.2		
[20]	130nm CMOS	1	Single band	2.4	-	22.1	2.8	-27.8**	-18.2	4.6	0.498
				3.43	-	22.6	2.2	-24.9**	-15.3		
				3.96	-	24	2.4	-28.1**	-18.5		
				4.49	-	22.6	2.5	-28.3**	-18.7		
				5.4	-	24.8	3.1	-30**	-20.4		
[41]	100nm GaAs	1	Continuous tuning	28	4.6	25.1	2.4	-18.3	-8.8	74	1.6
				39	3	27.7	2.8	-17	-8.5		
[43]	120nm SiGe	0.8	Digitally controlled stepped tuning	28-39	-	12.5	-	-8*	-	45	0.08***
[52]	180nm CMOS	1.5	Single band	1.9	-	15	1.6	-25.8**	-16.2	3	-
				2.4	-	22.6	2.8	-27.9**	-18.3	3.4	
				3.5	-	24	2.7	-26.7**	-17.1	3.4	
				5.2	-	22.6	3.1	-29.2**	-19.6	5.3	
[48]	150nm GaAs	2.5	Single band	8 - 10#	-	25 - 25.2	1.28 - 1.41	-23.5	-	190	3.6
				12 - 20#	-	20.1 - 28	1.23 - 1.51	-17.9	-	227.5	
[45]	130nm SiGe	2.5	Single band	28	-	16.2	2.8	-12	-	8.2	0.23
				60	-	15	3.4	-7	-	21	
[37]	130nm CMOS	1.2	Continuous tuning	1.9 - 2.4	-	10-14	3.2 - 3.7	-6.7	-	14	0.52
[46]	130nm SiGe	-	Single band	125	-	18.2	7	-17.3****	-	36.8	0.257
				143	-	16.1	7.7	-15.9****	-		
[47]	250nm SiGe	2.5	Single band	51 - 60#	9	18.7 - 21	6.8 - 7.3	-	-	40	0.78
				66 - 78#	12	21.3 - 23	7.6 -8.4	-	-		
[36]	28nm CMOS	1	Single band	24	3.4	29.9	5.63	-40	-	25.6	0.84
				33	3.1	32.4	4.55	-42	-		
				50	14.8	14.8	5.96	-34	-		
[38]	130nm CMOS	1.5	Single band	1.8	-	14.54	1.75	-16	-	7.5	0.544
				2.14	-	16.6	1.97	-5.8	-		
[40]	SiGe HBT	0.3	Continuous tuning with possibility for BW tuning	3 - 6	-	36	4.3	-	-	18	2.1
[49]	65nm CMOS	1.2	Single band	18 - 24#	-	27 - 27.2	0.85 - 1.05	-17	0	16.5	0.56
				25 - 40#	-	25 - 27	0.95 - 1.2	-16	0	17.4	
[53]	180nm CMOS	1.8	Single band	2.4	-	15	6.5	-12.6**	-3	14.6	1.39
				3.5	-	17	7.6	-14.6**	-5	27.7	
				5.2	-	15.4	8.5	-8.6**	1	27.7	
[35]	22nm FDSOI	1.2 1.8	Single band	21.5-26.5#	-	32.4	2.7	-39.4*		35	0.74***
				27.5-33#	-	33	2.3	-39.2*			
			Wide band	21.6-34.2#	-	32	2.3	-38**			
[50]	150nm GaAs		Single band	2.5-8#	5.5	20.3-22.1	1.38-1.53	-	-	128.4	3
				6-18#	12	20.2-22.7	1.64 -1.97	-	-	237.2	
[51]	150nm GaAs	2	Single band	39	-	24.3	3.9	-17.5*	-	64.7	3.04
				48	-	18.8	4.8	-11.9*	-	61.4	
[39]	45nm SOI		Single band	22	-	8.5	3.8	-11	-	15.5	0.317
				39	-	12.9	4.9	-16	-	15.5	
[54]	65nm CMOS	1,2	Single band	28	9	20.1	3	-15.6	-6	28.5	0.157***
				39	16	14.9	4.7	-11	-2	28.5	
[55]	130nm CMOS	1.2	Single band	3	-	21.2	2.5	-	-12.5	7.2	-
				5	-	21.9	2.7	-	-13.5	3.6	

*Calculated from OP1dB, **Estimated from IP1dB= IIP3-9.6, ***excluding pads, ****simulated, #Frequency range is reported instead of center frequency

D. SWITCHED CAPACITOR PARALLEL TO C_{GS}

This architecture as shown in Fig. 4.(f) realizes band tunability by switching an extra capacitor parallel to C_{gs} [38]. This configuration attains reconfigurability while requiring less area. The gain of the LNA can degrade due to the extra capacitance and the parasitics associated with the switch can affect the frequency of operation.

E. LC/RLC RESONANCE TANK

LC or RLC tank matching is usually a part of the output matching network and there can be different combinations of this circuit, as shown in Fig. 5.(b,i,h). One can use switched multi-tap inductors, switched capacitors, varactors or combinations of these [20], [40], [52]. Switched multi-tap inductors and switched capacitors provide coarse tuning which makes it possible to switch the frequency band, whereas, varactors can be used for fine tuning the frequency. Additionally, with an RLC load with variable resistance, the bandwidth of the circuit can be tuned while maintaining a constant center frequency [40]. For the switched multi-tap transformer, one must consider the losses and frequency shifts that can arise with the switches for this output matching topology. A magnetically tuned variable inductor along with switched capacitors were used in [39] for frequency tunability. The input wideband tuning was achieved using a transformer. The variable inductor was realized using inductors with metal shield ground where the inductance is varied by controlling the intensity of the induced current to the ground which depends on the coupling strength between the main coil and the ground shield.

F. VARACTOR

Varactors as shown in Fig. 5.(c) enable continuous tuning of the frequency [41], [42] and can be used with both input and output matching networks. They can also be used in conjunction with other frequency matching techniques such as LC resonance tanks, to facilitate fine tuning of the matching frequency, while occupying very less area. However, additional parasitics in the circuit can affect the overall tuning range of the varactor. In addition, the quality factor of the varactor has a clear effect on the gain of the LNA and one must take this into consideration during the design.

G. VARIABLE ARTIFICIAL TRANSMISSION LINES

Artificial transmission lines are implemented as slow-wave coplanar waveguides with a switched shunt capacitor to the ground as shown in Fig. 6. For large tunable ranges and fine tuning, multiple stages of the matching network are used which results in a large number of control bits requiring a digital control interface. By switching C_L, the unit length capacitance of the segment can be varied, which further results in the variation of the characteristic impedance. The switches must be carefully designed and in [43], triple-well nMOS devices were preferred over Heterojunction Bipolar Transistors (HBTs) because of the lower current consumption per unit cell. For each configuration of the operating frequency range, the output matching also needs to be adjusted. In [43], artificial transmission lines were used in conjunction with switched capacitors at the input and output matching circuits as in Fig. 4.(d) and Fig. 5.(c) respectively.

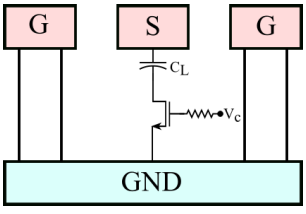

FIGURE 6. Variable transmission line unit cell cross section.

H. CASCODE BANK

This topology uses a switched cascode structure as in [52]. It also has the option of switching the transistor width in the individual cascode branches for gain variations. Since, there are multiple load branches, it would mean that there are multiple load inductors, which would increase the overall area of the circuit. In addition, this topology requires additional tunable elements such as switched capacitors/varactors as shown in Fig. 5.(g) and buffer stages which have to be carefully designed considering the paracitics.

I. TUNABLE STUB

This method uses a tunable stub to switch between frequencies. The stub is made tunable using a switch, which changes the stub's length when turned on and off, as in Fig. 5.(e). The switch can be realized using an HBT switch [44], [45] or an RF Microelectromechanical Systems (MEMS) switch [46], [47]. The switches have on and off losses and must be designed for minimum losses. Reference [44] reported an on-loss as low as 1dB at 60GHz and off-loss of 0.7 dB at 28GHz. MEMS switches have advantages over other switches because of their low static power consumption but their switching speed is relatively low when compared to other active devices [56].

J. SUSPENDED SUBSTRATE COUPLED LINES (SSCL)

This topology realizes a switch-less architecture that uses of an inter-stage and output-stage SSCL for frequency tuning as shown in Fig. 5.(f). This requires a broadband input stage and the signal is then divided into two parallel single band stages by the inter-stage SSCL [48], [49], [50]. The split signals are amplified by the high-band and low-band stages and the output stage SSCL combines the amplified single-band signals at the output. The coupled line also provided the required matching. This architecture consumes large area and the coupled lines introduce insertion losses which can affect the overall performance of the LNA. A single-pole-double-throw (SPDT) switch was used in [50] to switch between bands at the output. Reference [51] uses a broadband common-source stage and two parallel

common-gate stages one of which supports the high frequency mode and the other, low frequency mode. The signal is combined using a coupled-line-based diplexer at the output stage.

IV. GAIN TUNABLE LNAs

JC&S receivers are expected to work in a high gain-low linearity mode and a low gain-high linearity mode enabling the communication and radar mode respectively. Variable gain amplifiers are a widely discussed topic and in this survey, we look at designs that emphasize on a low noise design. The variable-gain amplifier designs that use an attenuator at the succeeding stage are not considered in this study as they often tend to increase the power consumption of the overall system. Instead, we focussed on designs with built-in gain tunable architectures. In addition, variable-gain LNAs can replace the variable-gain amplifiers in the RF chain resulting in an overall power reduction. Table 5 summarizes the advantages and disadvantages of the variable-gain LNAs reported in the literature. Table 6 presents a the performance summary of the LNAs discussed in this section and compares the gain and linearity ranges achieved by each technique.

A. TUNABLE TRANSISTOR WIDTH

Many gain-tunable architectures in the literature rely on switched-transistor methodologies, through which the effective width and thus, the transconductance of the transistor can be modified. Fig. 7 shows the schematic of an LNA with size-switchable input transistor. This makes it possible to tune the gain in discrete steps and operate in low-gain and high-gain modes. This can also be used in conjunction with other gain-variable topologies, as in [57] which additionally makes use of current tuning and back gate switching. In [20] and [52], the switched transistor widths are at different ratios and is switched ON through digital control. This topology also allows the tuning of linearity and achieves maximum linearity at the lowest gain state. The disadvantages of this architecture lie in the switches used. The switching delays and insertion losses associated with the switches must be considered which can also change the matching of the circuit.

B. VARIABLE BIASING

A straight forward approach to gain tuning is to vary the bias of the transistors as shown in Fig. 8. This method as in [58], [59], [60], and [61] attains a very good range in gain and linearity tuning but can cause the transistors to leave the optimum operating region depending on the bias voltage. Transistors in the triode region will affect the NF and isolation. Variable biasing can be applied as in [59] where bias tuning is performed for multiple input transistors and it can be applied independently to each transistor to achieve greater tunability.

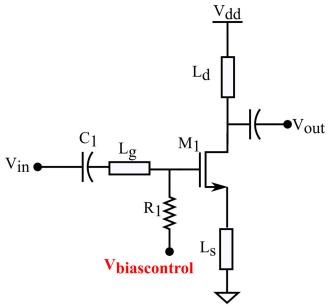

FIGURE 8. Schematic of an LNA with bias control.

C. CASCODE CURRENT STEERING

In this architecture, the added current steering transistor M3 in Fig. 9 when turned on, route a part of the drain current of M2 from the supply to the steering transistors rather than through the load thereby achieving tunability in gain [62], [63], [64], [65], [66], [67], [68]. This method has very small effect on the overall matching of the circuit under all gain modes and the DC current remains almost a constant. It also consumes a smaller area while providing more power gain at higher frequencies. The topology can be either single current steering or a switched one, allowing more tunability. This method can be used either to digitally switch between gains or to use it for continuous gain variation by changing the steering voltage between the highest and lowest usable values. This circuit introduces a phase variation and would require a phase-compensation network. Additionally, the NF of the LNA can be affected in the low-gain configuration.

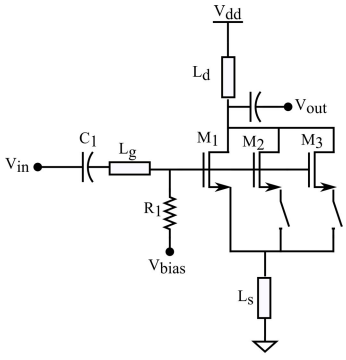

FIGURE 7. Schematic of an LNA with input size tunable transistor.

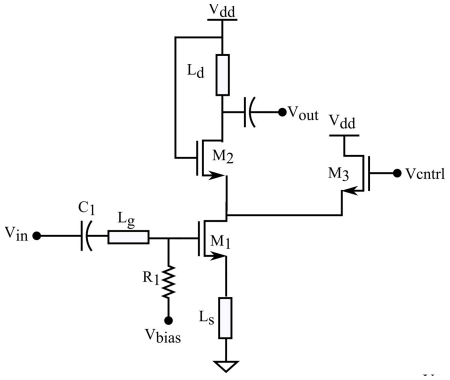

FIGURE 9. Schematic of a cascode LNA with current steering.

TABLE 5. Advantages and disadvantages of gain tunable LNA techniques proposed in literature.

References.	Section	Technique	Advantages	Disadvantages
[69], [52], [20]	IV-A	Digital switching ON and OFF transistors	• Good gain and linearity tuning	• Switch non-linearities
[58], [59], [60], [61], [70]	IV-B	Bias point tuning	• Good gain and linearity tuning	• The transistors may leave the perfect operating region
[43], [71], [62], [63], [64], [65], [66], [67], [68]	IV-C	Cascode current steering	• Large gain tunability • Constant DC current and less impact on matching • Suitable for high frequency applications	• Introduces a phase change • Increased noise figure • Decrease in OP1dB with gain reduction
[72], [73], [74], [75]	IV-D	Body biasing/ backgate control	• Possibility for continuous gain tuning • Ultra-low power operation with backgate biasing	• Higher NF with reverse body bias
[76]	IV-E	Tunable coupling coefficient based transformers	• Continuous tuning • Large tunable range • No frequency shift with tunability • Small area due to compact transformer • Low variation in power consumption and NF during gain tunability	• Tunability in linearity is not known • Complicated transformer implementation • Introduces a phase shift which needs to be compensated with additional circuitry
[36], [77]	IV-F	Tunable resistive load	• Good gain tunability	• Comparitevely higher NF • Susceptabile to Process, Voltage, Temperature (PVT) variations
[78], [79]	IV-G	Tunable Negative feedback capacitor	• Good gain tunability • No bias current variation with gain variation • OP1dB is kept constant	• Higher noise figure
[57]	IV-A, IV-C, IV-D	Tunable transistor width through current steering and back-gate switching	• Low, medium and high power modes • Overall low power • Less area	• Lesser tunability in linearity values
[80]	IV-B, IV-F	Tunable resistive loads and bias current tuning	• Good gain and linearity tuning	• High power • Susceptible to PVT variations
[81]	IV-H, IV-F	Resistive feedback and variable resistor in parallel with the load inductor	• Good continuous gain and linearity tuning	• Non-linearities in feedback path • Linearity tuning range is lesser than gain tuning range • Comparatively high NF

Even though the IP1dB of the LNA increases with reduction in the gain, OP1dB degrades with reduction in gain.

D. BACKGATE CONTROL

The threshold voltage of a MOSFET is a function of the bulk-source voltage. This implies that changing the body bias of the transistor can be used to achieve a dynamic threshold voltage. This can be used to change the transconductance of the transistor and hence, the gain as shown in Fig. 10. The backgate control is more effective with FDSOI technologies than with conventional CMOS processes. Backgate control also allows best power performance as reported in [72] where it can be used for very low power operations while not compromising on the overall performance of the LNA. Forward body biasing was used in [73] to relax the supply voltage requirements while ensuring the operation of the transistors in the saturation region.

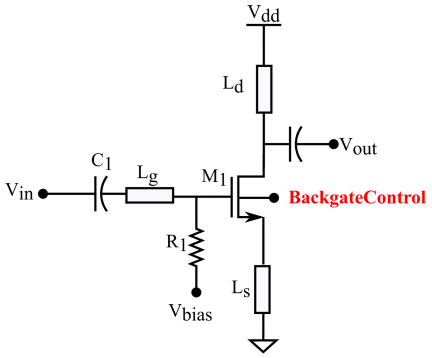

FIGURE 10. Schematic of a LNA with backgate control.

E. TUNABLE COUPLING COEFFICIENT BASED TRANSFORMERS

This architecture makes use of tunable-coupling coefficient based transformers as shown in Fig. 11. The tunable coupling

TABLE 6. Performance comparison with previously published variable gain LNAs.

Ref	Tech	Vdd [V]	Note	Freq [GHz]	BW [GHz]	Max Gain [dB]	NF [dB]	IP1dB [dBm]	IIP3 [dBm]	Pdc [mW]	Area [mm^2]	Gain Range [dB]	IP1dB/ IIP3 Range [dBm]
[57]	28nm FDSOI	1.2	Low power	2.4	4	16.8	6.6	-25.6^{c}	-16	0.35	0.0015	6.1	1.2
			Mid power		5.2	19.4	5.4	-26.4^{c}	-16.8	0.9			
			High power		4.5	22.9	3.6	-26.8^{c}	-17.2	2			
[20]	130nm CMOS	1	Low Gain	3.96	-	11	4	-19.3^{c}	-9.7	3.1	0.498	13	8.8
			Mid gain		-	11.7	4.6	-19.7^{c}	-10.1	3.6			
			High gain		-	24	2.4	-28.1^{c}	-18.5	4.6			
[76]	65nm CMOS	1	Continuous tuning	28	12	18.2	3.9 - 4.1	-15	-	9.8	0.16	6.2	-
[43]	120nm SiGe	2.5	Digital gain steps	28-39	-	12.5	-	-8*	-	45	0.08	18	-
[78]	180nm CMOS	0.6	Continuous tuning	2.8	-	10	4	-9.6^{c}	0	0.6	0.9	6	-
[58]	28nm CMOS	0.9	Continuous tuning	82.3^{h} 81.2^{l}	28.3^{h} 30.7^{l}	29.6^{h} 18^{l}	6.4-8.2^{h} 7.8-9.8^{l}	-28.1^{h} -12.3^{l}	-	31.3^{l} 11.7^{l}	0.254	11.6	15.8
[80]	40nm CMOS	1.1	Digital gain steps	27.1^{h} 27.8^{l}	7.4^{h} 9.3^{l}	27.1^{h} 18.4^{l}	3.3-4.3^{h} 3.4-4.4^{l}	-21.6^{h} -13.4^{l}	-12.6**^{h} -4.9**^{l}	31.4^{l} 21.5^{l}	0.26	8.7	8.2
[69]	28nm CMOS	0.9	Digital gain steps	79	10	23.8^{h} 19.3^{l}	4.9^{h} 5.6^{l}	-18.5^{h} -15^{l}	-	35^{h} 28^{l}	0.147	4.5	3.5
[60]	180nm CMOS	1.5	High, mid and low gain modes	5.7	-	16.4^{h} 8^{l}	3.5^{h} 6^{l}	-	-	3.2	0.583	8.4	-
[61]	130nm CMOS	-	Continuous tuning	62	-	13.5	6.8	-	-	-	0.45	13	-
[52]	180nm CMOS	1.5	Digital gain steps	5.2	-	16	3.1	-29.2^{c}	-19.6	5.3	-	8.5	-
[81]	65nm CMOS	1.2	Continuous tuning	4.5-5.5	-	23^{h} 3^{l}	2^{h} 6^{l}	-16.1^{ch} 0.4^{cl}	-6.5^{h} 10^{l}	16	0.043	20	16.5
[71]	90nm CMOS	1	Continuous tuning	26-30.5 33.8-40.6	-	21.5	4.7	-25.5*	-	17.9	0.45	9.8	-
[36]	28nm CMOS	1	Continuous tuning	24	3.4	29.9	5.63	-40	-	26.5	0.22***	35.4	-
[59]	65nm CMOS	1.3	Continuous tuning	52-61	8	25	4.8	-22	-	26-47	0.26	17	-15
[82]	65nm CMOS	1	Digital control	17-24	-	13.3	2.8-3.8	-14	-	4.2	0.23	6.8	-
[62]	90nm CMOS	2	Continuous tuning	71-76	-	14	-	-	-	36	0.726	30	-
[70]	65nm CMOS	-	Continuous tuning	30-34.5	-	20.8	3.71	-20.4	-	16.5-26.7	0.39	10.6	-
[74]	22nm FDSOI	0.9	Continuous tuning	152	10.8	18	7.5-9.3	-17.0	-	17.5-27.5	0.09***	9	8.2
[64]	40nm CMOS	1.5,1	Continuous tuning	146-151	-	21.2	8.1	-28.5	-	34-46	0.24***	12.5	-
[72]	22nm FDSOI	0.8	Continuous tuning	30.1	7.2	16	5.5-6.3	-28.8	-	0.41-0.97	0.083***	8	7.8
[65]	90nm CMOS	2.5	Continuous tuning	68.8-87.6	-	23.7	5.3	-23.5*	-	55	0.57	19.1	-
[66]	90nm CMOS	2	Digital Control	38	-	18.89	6.74	-20	-	15.62	0.203	10.49	13
[77]	45nm SOI	-	Continuous control	29	-	23	2.7	-19.2	-9.3	28	0.252***	15	-
[73]	65nm CMOS	1.2	Continuous control	24.25	12.5	11.4	4.7-6.4	-	-	2.16	0.3***	16.4	-
[68]	55nm CMOS	2	Continuous control	6.5-12	-	20.7	3.26	-12.2	-	75	0.98	18	7.2
[67]	55nm CMOS	1.8	Continuous control	5.5	1	19	3.26-18	-18.6^{c}	-9	27	0.56	38	9
[63]	90nm CMOS	1.4, 1.2	Continuous control	73.7-87.8	14.1	26.1	4.8	-31.9^{h} -26^{l}	-	23	0.52	17	5.9
[79]	40nm CMOS	1.1	Digital control	60	10	19.8	5.98^{h} 7.54^{l}	-29.5	-	18	0.22	13.3	12.5

*calculated from OP1dB, **Calculated from OIP3, ***excluding pads, ****simulated , *h*-max gain mode, *l*-min gain mode, *c*-calculated from IP1dB=IIP3-9.6

coefficient in X_{vg} changes the matching of the second stage, thus enabling a continuous gain variation of the LNA. This method alleviates the problems of the high power consumption and increase in NF variation that can occur with other tunable approaches. It also attains continuous gain tunability, and the frequency shift during tuning is negligible. Reference [76] uses a switched substrate-shield layout technique to achieve a tunable low-loss coupling coefficient.

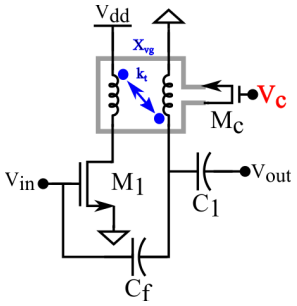

FIGURE 11. Schematic of a tunable LNA with tunable coupling coefficient based transformers.

F. TUNABLE RESISTIVE LOADS

This gain-variable architecture makes use of resistive loads that are either tunable or switchable as shown in Fig. 12. Tunable resistive loads use active CMOS resistors whereas, the switchable topology uses parallel resistive loads that can be controlled digitally [80], [81]. One must consider the associated switch losses and the higher NF. They are also susceptible to PVT variations.

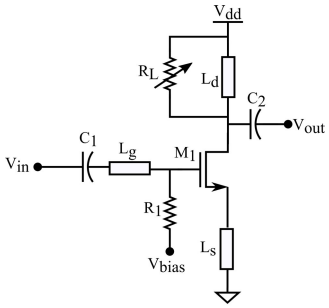

FIGURE 12. Schematic of a LNA with tunable resistive load.

G. TUNABLE NEGATIVE FEEDBACK CAPACITOR

This technique is similar to the cascode current steering technique, except for the capacitor between the current steering transistor and the cascode configuration as shown in Fig. 13 which is equivalent to a negative-feedback variable capacitor [78]. The gain of the cascode transistor can be adjusted by changing the gate voltage of the M3 using V_{cntrl}. Since the current doesn't flow into C_B, there is no bias current variation with gain variations. The OP1dB is preserved with gain variation in this configuration.

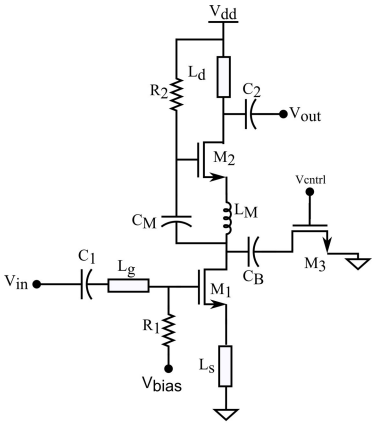

FIGURE 13. Schematic of a cascode LNA with tunable negative feedback capacitor.

H. RESISTIVE FEEDBACK

A resistor is used in a negative feedback configuration, as in [81], which helps control the gain in a continuous manner as depicted in Fig. 14. The additional resistor may increase the overall NF of the circuit. In addition, the circuit is susceptible to PVT variations.

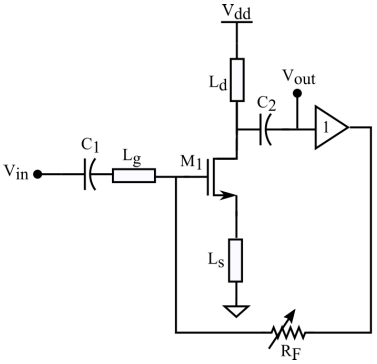

FIGURE 14. Schematic of a LNA with resistive feedback.

V. MULTI-MODE MIXERS

The previous two sections described the possible topologies for frequency and gain reconfigurable LNAs. However, for a reconfigurable front-end, the tunability of down conversion mixer may prove to be vital for optimum performance. Frequency tunability in a mixer can be achieved by varying the RF and LO matching networks. The matching requirements at the LO port are generally relaxed, because the LO signal is typically very strong. The input-tuning methodologies presented in Section III can be used for tuning the frequency matching of the mixer. In addition to those techniques, an LC ladder is a possible architecture for frequency tuning in mixers. While the LNA primarily influences the NF of the receiver, the down-conversion mixer assumes a critical role in determining the linearity of the receiver. In the case of JC&S receivers, the linearity of the receiver plays a crucial factor, particularly in radar mode and, more specifically, during close target detection. Ensuring high linearity is important in such scenarios, while

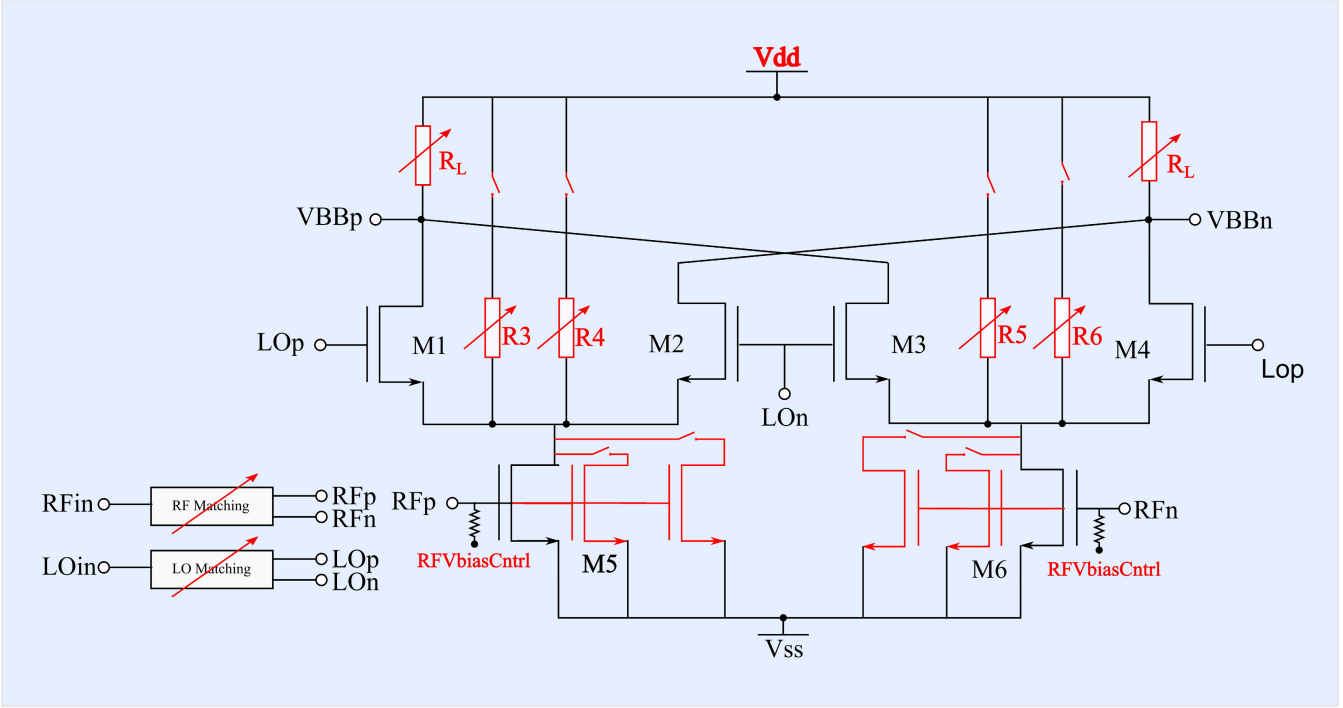

FIGURE 15. General concept of a tunable Gilbert cell mixer.

the gain of the mixer is only secondary. On the contrary, in communication mode, gain is of utmost importance while linearity becomes a less prominent concern. Hence the mixer also needs to function in a multi-mode scenario ensuring the operation in communication and radar modes.

Current mixer-tunable architectures focus mainly on gain and linearity tunability. The mixer also employs similar variability architectures as those used by the LNA, such as, DC bias tuning, transistor width tuning, body bias tuning and current tunability. Tunability can be implemented in the mixer core or can be attained by a variable gain amplifier stage [83] or an attenuator, which results in increased power consumption. Active and passive variable-gain mixers or a combination of both [84] and [85] have been discussed in the literature. Passive mixers with controllable transconductance and transimpedance stages can be used for variable gains as in [86].

Gilbert cell mixer architecture is one of the most commonly used architecture in the active mixer category. It can also be such that an Operational Transconductance Amplifier (OTA) was used in conjunction with a Gilbert-type switching core and an Intermediate frequency (IF) / baseband load [87], [88]. For simplicity, we examined gain tunable topologies in an active Gilbert cell mixer circuit.

Fig. 15 shows the possible tunable approaches in a Gilbert cell mixer. The tunable methods are highlighted in red. The approximate conversion gain of the Gilbert cell mixer is given by (3) [89].

$$CG = \frac{2}{\pi} g_m.R_L \tag{3}$$

where g_m is the transconductance of the RF transistors and R_L is the load resistance. Hence, gain reconfigurability can be achieved by either tuning the load resistor R_L in Fig. 15 or by scaling the current consumption, which changes the g_m of the RF transistors. One method to change the current is to change the bias of the RF transistors M5 and M6 in Fig. 15 using RFVbiasCntrl. Another method is to change the RF transistor widths (M5 and M6) using switches. This may come with additional design changes in the LO transistors too. The current through the RF transistors can also be changed through current bleeding branches (R3, R4, R5 and R6). For tunability, each branch can be digitally controlled using switches or the resistors can be implemented as MOS resistors whose values change with their gate voltage. The gain variability can also be achieved by scaling the supply voltage and the body bias of the transistors. However, scaling the supply voltage can affect the overall circuit bias. FDSOI technologies provide more flexibility with body biasing and can be used to change the transconductance of the transistors, leading to a tunability in the conversion gain. The performance comparison of the tunable multi-mode mixers is summarised in Table 7.

VI. SUMMARY AND CONCLUSION

In this study, a comprehensive survey of various LNA and down-conversion mixer architectures that can facilitate JC&S applications was carried out. It is clear from the analysis that communication and radar modes demand different bandwidths, gains and linearity requirements. An extensive and comparative study of techniques that provide tunability in

TABLE 7. Performance comparison with previously published tunable mixers.

Ref	Tech	Vdd [V]	Note	Freq [GHz]	Conv. Gain [dB]	NF [dB]	IP1dB [dBm]	IIP3 [dBm]	LO-RF Isolation [dB]	Pdc [mW]	Area [mm^2]
[90]	130nm CMOS	1.2	Digital control with transistor width tuning and fine tuning using resistor load	2-10	24^h 9^l	8^h 23^l	-19^h -4^l	-12^h 3.5^l	<62	18-2.4	0.19*
[91]	180nm CMOS	1.8	Tunable resistor load	5.25	-28.02^l - 6.21^h	18.81	-16	-3.94	57.35	7.2	-
[92]	180nm CMOS	0.4-1.8	Body bias, supply voltage and current bleeding tuning	2.5	13.8^l 24.2^h	17.1	-22	-11	<30	2	0.93
[86]	130nm CMOS	1.8	Passive mixer with tunable transconductance and transimpedance stages	0.7-2.3	3.5^l 20.5^h	15.3^l 8.03^h	-	8.5^l 1^h	-	5.58-10.08	0.705
[87]	130nm CMOS	1.2	Changing the transconductance of the OTA	1-12	1.2^l 17^h	11	-3.7^l -11^h	8.6^l 2^h	70	1.8^l 5.9^h	0.105*
[88]	130nm CMOS	1.8	Changing the transconductance of the OTA	0.7-2.6	8^l 26^h	9.1^l 18.1^h	-	8.5^l	-	8.82-14.04	0.456
[93]	130nm CMOS	1.2	LO and load switching	0.5-7	7.8^l 16.8^h	15.1^l -8.9^h	-3.46^l -16^h	10.33^l -3.55^h	-	2.4^l 9.6^h	0.08*
[94]	130nm CMOS	1.2	Tuning the current bleeding transistors	57-64	7.5^l 15.1^h	15.4^l 11^h	-5^h -9^h	5.3^l	-	16	0.456
[95]	130nm CMOS	1, 1.69	Active-passive combined	30-38	-1.5^l 4.3^h	21^l 25.7^h	4^l -1^h	-	-	10.4	0.458

*excluding pads, *h*-max gain mode, *l*-min gain mode

frequency, bandwidth, gain and linearity and its performance with respect to the KPIs was performed. A short summary of the analysis is provided below:

- Transitioning to sub-THz range frequencies necessitates careful consideration of technology selection, as it significantly influences system performance. This will push the need to move to lower CMOS and FDSOI technology nodes. Additionally, SiGe BiCMOS technology is a viable option, offering capabilities required for systems operating at sub-THz range frequencies
- The mode of frequency tuning will greatly depend on the frequency of operation. As we move to higher frequencies, designers will have to rely on techniques that uses transmission lines.
- The most frequently used technique for frequency tuning is switchable architecture. However, the main disadvantage of this technique lies in the non-linearities associated with switches. The switches come with insertion losses and the associated parasitics can change the resonant frequency. The reconfigurability is high in this topology and there is often a need for a digital interface.
- Varactors offer a simple solution with respect to area and continuous frequency reconfigurability. However, the low Q-factor of the varactor can affect the overall gain of the circuit. Additionally, the parasitics in the circuit can compromise the entire tuning range.
- Variable artificial transmission lines and tunable stubs provide reconfigurability while occupying less area. The tunability is high in the case of artificial transmission lines whereas, it is limited for tunable stubs.
- Bandwidth tunability can be achieved using switched multi-tap transformers at the input or with tunable resistors in the output matching network. The use of resistors may result in PVT variation.
- Gain variability can be achieved by simple techniques such as variable biasing and backgate biasing. However, with variable biasing, there is a chance of transistors going out of saturation and thereby increasing the noise of the LNA. In addition, this can affect the matching at different gain values. Backgate tuning is more relevant with FDSOI technologies and can be employed for very low-power operations without compromising the performance of the LNA.
- Gain variability with switched transistors come with the inherent non-linearities associated with the switches. The architectures which use resistors for gain tuning are prone to PVT variations.
- The current steering architecture provides very good tuning with respect to gain and linearity. The NF and matching variations are low compared to those of the other topologies. However, the power remains almost a constant in all modes since the DC current remains the same in all gain modes. This must be kept in mind if one intends to achieve power saving in the low gain mode. Even though the IP1dB of the LNA increases with a lower gain, the OP1dB of the LNA tends to degrade in the low gain mode. This can be fixed using the tunable negative feedback capacitor technique which is very similar to the cascode current steering itself.
- Multi-mode mixers can use input frequency-tunable architectures and gain-tunable topologies such as variable biasing, changing RF transistor width, backgate biasing and load resistor tuning. In addition, tuning can be performed with current-injection resistors in the Gilber cell mixer topology.

This topical survey provides a simplified tool and platform to compare the possible multi-mode LNA and mixer architectures for the development of a multi-mode RF receiver front-end towards a realizable JC&S system in terms of RF hardware.

REFERENCES

[1] C. De Lima, D. Belot, R. Berkvens, A. Bourdoux, D. Dardari, M. Guillaud, M. Isomursu, E.-S. Lohan, Y. Miao, A. N. Barreto, M. R. K. Aziz, J. Saloranta, T. Sanguanpuak, H. Sarieddeen, G. Seco-Granados, J. Suutala, T. Svensson, M. Valkama, B. Van Liempd, and H. Wymeersch, "Convergent communication, sensing and localization in 6G systems: An overview of technologies, opportunities and challenges," *IEEE Access*, vol. 9, pp. 26902–26925, 2021.

[2] M. Nemati, Y. H. Kim, and J. Choi, "Toward joint radar, communication, computation, localization, and sensing in IoT," *IEEE Access*, vol. 10, pp. 11772–11788, 2022.

[3] L. G. de Oliveira, B. Nuss, M. B. Alabd, A. Diewald, M. Pauli, and T. Zwick, "Joint radar-communication systems: Modulation schemes and system design," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 3, pp. 1521–1551, Mar. 2022.

[4] S. Dwivedi, A. N. Barreto, P. Sen, and G. Fettweis, "Target detection in joint frequency modulated continuous wave (FMCW) radar-communication system," in *Proc. 16th Int. Symp. Wireless Commun. Syst. (ISWCS)*, Aug. 2019, pp. 277–282.

[5] A. Herschfelt, A. R. Chiriyath, S. Srinivas, and D. W. Bliss, "An introduction to spectral convergence: Challenges and paths to solutions," in *Proc. 1st IEEE Int. Online Symp. Joint Commun. Sens. (JC&S)*, Feb. 2021, pp. 1–6.

[6] R. S. Thoma, C. Andrich, G. D. Galdo, M. Dobereiner, M. A. Hein, M. Kaske, G. Schafer, S. Schieler, C. Schneider, A. Schwind, and P. Wendland, "Cooperative passive coherent location: A promising 5G service to support road safety," *IEEE Commun. Mag.*, vol. 57, no. 9, pp. 86–92, Sep. 2019.

[7] S. H. Dokhanchi, A. N. Barreto, and G. Fettweis, "A half-duplex joint communications and sensing system using ZP-OFDM," in *Proc. 2nd IEEE Int. Symp. Joint Commun. Sens. (JC&S)*, Mar. 2022, pp. 1–6.

[8] J. Marin, M. Bernhardt, M. Heino, and T. Riihonen, "Monostatic FMCW radar architecture for multifunction full-duplex radios," in *Proc. 55th Asilomar Conf. Signals, Syst., Comput.*, Oct. 2021, pp. 640–644.

[9] L. Han and K. Wu, "24-GHz integrated radio and radar system capable of time-agile wireless communication and sensing," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 3, pp. 619–631, Mar. 2012.

[10] L. Han and K. Wu, "Radar and radio data fusion platform for future intelligent transportation system," in *Proc. 7th Eur. Radar Conf.*, Sep. 2010, pp. 65–68.

[11] S. George, P. Sen, A. N. Barreto, and G. Fettweis, "Reconfigurable E-band receiver development for joint communication and sensing," in *Proc. IEEE 12th Latin Amer. Symp. Circuits Syst. (LASCAS)*, Feb. 2021, pp. 1–4.

[12] F. Bozorgi and P. Sen, "A compact reconfigurable power splitter enabling a full-duplex integrated transceiver employed for joint communication and radar sensing," in *Proc. 20th Eur. Radar Conf. (EuRAD)*, Sep. 2023, pp. 367–370.

[13] P. Sen, A. Harutyunyan, M. Umar, and S. Kamal, "Joint communication and radar sensing: RF hardware opportunities and challenges—A circuits and systems perspective," *Sensors*, vol. 23, no. 18, p. 7673, 2023.

[14] G. N. Saddik, R. S. Singh, and E. R. Brown, "Ultra-wideband multifunctional communications/radar system," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 7, pp. 1431–1437, Jul. 2007.

[15] P. Sen, F. Bozorgi, A. Harutyunyan, A. N. Barreto, A. Nimr, and G. Fettweis, "RF front-ends for ISAC—Design challenges and potential solutions," in *Integrated Sensing and Communications*. Singapore: Springer, 2023, pp. 507–535.

[16] F. Liu, C. Masouros, A. P. Petropulu, H. Griffiths, and L. Hanzo, "Joint radar and communication design: Applications, state-of-the-art, and the road ahead," *IEEE Trans. Commun.*, vol. 68, no. 6, pp. 3834–3862, Jun. 2020.

[17] A. Bandyopadhyay, "Differentiated silicon technologies for mmWave 5G and 6G applications (invited)," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Mar. 2023, pp. 1–4.

[18] M. S. Dadash, S. Bonen, U. Alakusu, D. Harame, and S. P. Voinigescu, "DC-170 GHz characterization of 22 nm FDSOI technology for radar sensor applications," in *Proc. 13th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Sep. 2018, pp. 158–161.

[19] *NR; Base Station (BS) Radio Transmission and Reception*, document G. T. 38.104, 2019.

[20] C.-T. Fu, C.-L. Ko, C.-N. Kuo, and Y.-Z. Juang, "A 2.4–5.4-GHz wide tuning-range CMOS reconfigurable low-noise amplifier," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 12, pp. 2754–2763, Dec. 2008.

[21] T. Arai, T. Usugi, T. Murakami, S. Kishimoto, Y. Utagawa, M. Kohtani, I. Ando, K. Matsunaga, C. Arai, and S. Yamaura, "A 77-GHz 8RX3TX transceiver for 250-m long-range automotive radar in 40-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 56, no. 5, pp. 1332–1344, May 2021.

[22] K. Dandu et al., "2.2 High-performance and small form-factor mm-wave CMOS radars for automotive and industrial sensing in 76-to-81 GHz and 57-to-64 GHz bands," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 64, Feb. 2021, pp. 39–41.

[23] T. Fujibayashi, Y. Takeda, W. Wang, Y.-S. Yeh, W. Stapelbroek, S. Takeuchi, and B. Floyd, "A 76- to 81-GHz multi-channel radar transceiver," *IEEE J. Solid-State Circuits*, vol. 52, no. 9, pp. 2226–2241, Sep. 2017.

[24] B. P. Ginsburg et al., "A multimode 76-to-81 GHz automotive radar transceiver with autonomous monitoring," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 158–160.

[25] T. Ma, Z. Chen, J. Wu, W. Zheng, S. Wang, N. Qi, and B. Chi, "A CMOS 76–81 GHz 2TX 3RX FMCW radar transceiver based on mixed-mode PLL chirp generator," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, 2018, pp. 83–86.

[26] M. Vigilante and P. Reynaert, "On the design of wideband transformer-based fourth order matching networks for *E*-band receivers in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 2071–2082, Aug. 2017.

[27] J. Moody, S. Lepkowski, and T. Forbes, "A 67 GHz 23 mW receiver utilizing complementary current reuse techniques," in *Proc. 17th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Sep. 2022, pp. 292–295.

[28] M. Vigilante and P. Reynaert, "A coupled-RTWO-based subharmonic receiver front end for 5G *E*-band backhaul links in 28-nm bulk CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 10, pp. 2927–2938, Oct. 2018.

[29] D. Guermandi, Q. Shi, A. Medra, T. Murata, W. Van Thillo, A. Bourdoux, P. Wambacq, and V. Giannini, "A 79 GHz binary phase-modulated continuous-wave radar transceiver with TX-to-RX spillover cancellation in 28 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2015, pp. 1–3.

[30] R. Levinger, R. B. Yishay, O. Katz, B. Sheinman, N. Mazor, R. Carmon, and D. Elad, "High-performance E-Band transceiver chipset for point-to-point communication in SiGe BiCMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 4, pp. 1078–1087, Apr. 2016.

[31] A. Geis, Y. Rolain, G. Vandersteen, and J. Craninckx, "A 0.045 mm^2 0.1–6 GHz reconfigurable multi-band, multi-gain LNA for SDR," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, May 2010, pp. 123–126.

[32] G. Chararas, A. Stefanou, A. Hatzopoulos, and V. F. Pavlidis, "A novel design methodology for modular, digitally controlled, multiband, mmWave LNAs," in *Proc. 12th Int. Conf. Modern Circuits Syst. Technol. (MOCAST)*, Jun. 2023, pp. 1–4.

[33] X. Yu and N. M. Neihart, "A 2–11 GHz reconfigurable multi-mode LNA in 0.13 μm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2012, pp. 475–478.

[34] X. Yu and N. M. Neihart, "Analysis and design of a reconfigurable multimode low-noise amplifier utilizing a multitap transformer," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 3, pp. 1236–1246, Mar. 2013.

[35] M. G. Bardeh, J. Fu, N. Naseh, J. Paramesh, and K. Entesari, "A mm-wave wideband/reconfigurable LNA using a 3-winding transformer load in 22-nm CMOS FDSOI," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2023, pp. 121–124.

[36] C.-J. Liang, C.-W. Chiang, J. Zhou, R. Huang, K.-A. Wen, M. F. Chang, and Y.-C. Kuan, "A tri (K/Ka/V)-band monolithic CMOS low noise amplifier with shared signal path and variable gains," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Aug. 2020, pp. 333–336.

[37] M. El-Nozahi, E. Sanchez-Sinencio, and K. Entesari, "A CMOS low-noise amplifier with reconfigurable input matching network," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 5, pp. 1054–1062, 2009.

[38] H. Song, H. Kim, K. Han, J. Choi, C. Park, and B. Kim, "A sub-2 dB NF dual-band CMOS LNA for CDMA/WCDMA applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 3, pp. 212–214, Mar. 2008.

[39] R. A. Shaheen, T. Rahkonen, and A. Pärssinen, "Millimeter-wave frequency reconfigurable low noise amplifiers for 5G," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 2, pp. 642–646, Feb. 2021.

[40] Z. Zou, M. Hosseini, R. Kwende, S. Raman, and J. C. Bardin, "A frequency and bandwidth reconfigurable 3–6 GHz cryogenic SiGe BiCMOS LNA with a power consumption of $\leq$ 2.9 mW," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2021, pp. 653–656.

[41] Z. Wang, D. Hou, P. Zhou, H. Li, Z. Li, J. Chen, and W. Hong, "A Ka-band switchable LNA with 2.4-dB NF employing a varactor-based tunable network," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 4, pp. 385–388, Apr. 2021.

[42] C.-R. Wu, H.-H. Hsieh, L.-S. Lai, and L.-H. Lu, "A 3–5 GHz frequency-tunable receiver frontend for multiband applications," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 9, pp. 638–640, Sep. 2008.

[43] R. B. Yishay and D. Elad, "A compact frequency-tunable VGA for multi-standard 5G transceivers," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Aug. 2020, pp. 325–328.

[44] A. A. Nawaz, J. D. Albrecht, and A. Ç. Ulusoy, "A 28-/60-GHz band-switchable bidirectional amplifier for reconfigurable mm-wave transceivers," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 7, pp. 3197–3205, 2020.

[45] A. A. Nawaz, J. D. Albrecht, and A. Ç. Ulusoy, "A Ka/V band-switchable LNA with 2.8/3.4 dB noise figure," *IEEE Microw. Wireless Compon. Lett.*, vol. 29, no. 10, pp. 662–664, Oct. 2019.

[46] J. Heredia, M. Ribo, L. Pradell, S. T. Wipf, A. Goritz, M. Wietstruck, C. Wipf, and M. Kaynak, "A 125–143-GHz frequency-reconfigurable BiCMOS compact LNA using a single RF-MEMS switch," *IEEE Microw. Wireless Compon. Lett.*, vol. 29, no. 5, pp. 339–341, May 2019.

[47] A. Ç. Ulusoy, M. Kaynak, T. Purtova, B. Tillack, and H. Schumacher, "A 60 to 77 GHz switchable LNA in an RF-MEMS embedded BiCMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 22, no. 8, pp. 430–432, Aug. 2012.

[48] C. Xie, Z. Yu, and C. Tan, "An X/Ku dual-band switch-free reconfigurable GaAs LNA MMIC based on coupled line," *IEEE Access*, vol. 8, pp. 160070–160077, 2020.

[49] R. Vignesh, P. Gorre, H. Song, and S. Kumar, "A K/Ka-band switchless reconfigurable 65 nm CMOS LNA based on suspended substrate coupled line," *IEEE Access*, vol. 10, pp. 33449–33464, 2022.

[50] Z. Wang, M. Chen, X. Li, X. Tang, X. Li, and Y. Wang, "A 2.5-to-18 GHz reconfigurable LNA with 1.38-to-1.97 dB NF using switchable diplexer and low-noise oriented input," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2023, pp. 131–134.

[51] B. Ko, S. Lee, W. Seo, T. Sim, S. Kim, M.-S. Kim, and J. Kim, "A 39/48 GHz switchless reconfigurable low noise amplifier usingcommon gate and coupled-line-based diplexer," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 70, no. 11, pp. 4028–4032, Nov. 2023.

[52] A. T. Phan and R. Farrell, "Reconfigurable multiband multimode LNA for LTE/GSM, WiMAX, and IEEE 802.11.a/b/g/n," in *Proc. 17th IEEE Int. Conf. Electron., Circuits Syst.*, Dec. 2010, pp. 78–81.

[53] W.-C. Li, C.-S. Wang, and C.-K. Wang, "A 2.4-GHz/3.5-GHz/5-GHz multi-band LNA with complementary switched capacitor multi-tap inductor in 0.18 μm CMOS," in *Proc. Int. Symp. VLSI Design, Autom. Test*, Apr. 2006, pp. 1–4.

[54] H.-H. Chen and Z.-M. Tsai, "Ka-/K-band frequency-reconfigurable single-input differential-output low-noise amplifier for 5G applications," *IEEE Microw. Wireless Technol. Lett.*, vol. 33, no. 9, pp. 1297–1300, Sep. 2023.

[55] R. Singh, G. Slovin, M. Xu, T. E. Schlesinger, J. A. Bain, and J. Paramesh, "A reconfigurable dual-frequency narrowband CMOS LNA using phase-change RF switches," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 11, pp. 4689–4702, Nov. 2017.

[56] J. Danson, C. Plett, and N. Tait, "Using MEMS capacitive switches in tunable RF amplifiers," *EURASIP J. Wireless Commun. Netw.*, vol. 2006, no. 1, pp. 1–9, Dec. 2006.

[57] T. Taris, J. Desevedavy, F. Hameau, P. Audebert, and D. Morche, "Inductorless multi-mode RF-CMOS low noise amplifier dedicated to ultra low power applications," *IEEE Access*, vol. 9, pp. 83431–83440, 2021.

[58] M. Vigilante and P. Reynaert, "A 68.1-to-96.4 GHz variable-gain low-noise amplifier in 28 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Jan. 2016, pp. 360–362.

[59] D. Bierbuesse and R. Negra, "60 GHz variable gain & linearity enhancement LNA in 65 nm CMOS," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Aug. 2020, pp. 163–166.

[60] Y. S. Wang and L. H. Lu, "5.7 GHz low-power variable-gain LNA in 0.18 μm CMOS," *Electron. Lett.*, vol. 41, no. 2, pp. 66–68, Jan. 2005.

[61] Y. Kim and Y. Kwon, "A 60 GHz cascode variable-gain low-noise amplifier with phase compensation in a 0.13 μm CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 22, no. 7, pp. 372–374, Jul. 2012.

[62] C.-C. Kuo, Z.-M. Tsai, J.-H. Tsai, and H. Wang, "A 71–76 GHz CMOS variable gain amplifier using current steering technique," in *Proc. IEEE Radio Freq. Integr. Circuits Symp.*, Jun. 2008, pp. 609–612.

[63] Y. Wang, T.-Y. Chiu, C.-C. Chien, W.-H. Tsai, and H. Wang, "An E-band high-performance variable gain low noise amplifier for wireless communications in 90-nm CMOS process," *IEEE Microw. Wireless Compon. Lett.*, vol. 32, no. 9, pp. 1095–1098, Sep. 2022.

[64] I. Kim, W. Kim, and S. Hong, "A D-band variable-gain LNA with triple-inductive coupling gm-boosting," in *Proc. IEEE Int. Symp. Radio-Freq. Integr. Technol. (RFIT)*, Aug. 2022, pp. 194–196.

[65] Y. Wang, C.-N. Chen, Y.-C. Wu, and H. Wang, "An E-band variable gain low noise amplifier in 90-nm CMOS process using body-floating and noise reduction techniques," in *Proc. 13th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Sep. 2018, pp. 277–280.

[66] Y.-T. Chang, Y.-N. Chen, and H.-C. Lu, "A 38 GHz low power variable gain LNA using PMOS current-steering device and Gm-boost technique," in *Proc. Asia–Pacific Microw. Conf. (APMC)*, Nov. 2018, pp. 654–656.

[67] C.-M. Lo, S.-F. Chao, C.-C. Chang, and H. Wang, "A fully integrated 5–6 GHz CMOS variable-gain LNA using helix-stacked inductors," in *Proc. Eur. Microw. Integr. Circuits Conf.*, Sep. 2006, pp. 348–351.

[68] H. Gao, N. Li, M. Li, S. Wang, Z. Zhang, Y.-C. Kuan, X. Yu, Q. J. Gu, and Z. Xu, "A 6.5–12 GHz balanced variable gain low-noise amplifier with frequency-selective non-foster gain equalization technique," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Aug. 2020, pp. 321–324.

[69] A. Medra, V. Giannini, D. Guermandi, and P. Wambacq, "A 79 GHz variable gain low-noise amplifier and power amplifier in 28 nm CMOS operating up to 125°C," in *Proc. 40th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2014, pp. 183–186.

[70] S. Lee, J. Park, and S. Hong, "A Ka-band phase-compensated variable-gain CMOS low-noise amplifier," *IEEE Microw. Wireless Compon. Lett.*, vol. 29, no. 2, pp. 131–133, Feb. 2019.

[71] K.-C. Chang, Y. Wang, and H. Wang, "A broadband variable gain low noise amplifier covering 28/38 GHz bands with low phase variation in 90-nm CMOS for 5G communications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2021, pp. 764–767.

[72] M. Spasaro and D. Zito, "Sub-mW 30 GHz variable-gain LNA in 22 nm FDSOI CMOS for low-power tapered mm-wave 5G/6G phased-array receivers," in *IEEE MTT-S Int. Microw. Symp. Dig.*, 2022, pp. 723–726.

[73] H. Chen, H. Zhu, L. Wu, Q. Xue, and W. Che, "A CMOS low-power variable-gain LNA based on triple cascoded common-source amplifiers and forward-body-bias technology," in *IEEE MTT-S Int. Microw. Symp. Dig.*, May 2021, pp. 1–3.

[74] P. J. Artz, P. Scholz, T. Mausolf, and F. Gerfers, "A fully-differential 146.6–157.4 GHz LNA utilizing back gate control to adjust gain in 22 nm FDSOI," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2022, pp. 611–614.

[75] M. Rack, L. Nyssens, Q. H. Le, D. K. Huynh, T. Kämpfe, J.-P. Raskin, and D. Lederer, "A compact 120 GHz LNA in 22 nm FD-SOI with back-gate controllable variable-gain," in *Proc. 18th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Sep. 2023, pp. 386–389.

[76] S. N. Ali, M. A. Hoque, S. Gopal, M. Chahardori, M. A. Mokri, and D. Heo, "A continually-stepped variable-gain LNA in 65-nm CMOS enabled by a tunable-transformer for mm-wave 5G communications," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2019, pp. 926–929.

[77] S. Li, T.-Y. Huang, Y. Liu, H. Yoo, Y. Na, Y. Hur, and H. Wang, "A millimeter-wave LNA in 45 nm CMOS SOI with over 23 dB peak gain and sub-3 dB NF for different 5G operating bands and improved dynamic range," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2021, pp. 31–34.

[78] J.-Y. Hsieh and K.-Y. Lin, "A 0.6-V low-power variable-gain LNA in 0.18-μm CMOS technology," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 1, pp. 23–26, Jan. 2020.

[79] Y.-T. Chang and H.-C. Lu, "A *V*-band low-power digital variable-gain low-noise amplifier using current-reused technique with stable matching and maintained OP1dB," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 11, pp. 4404–4417, Nov. 2019.

[80] M. Elkholy, S. Shakib, J. Dunworth, V. Aparin, and K. Entesari, "A wideband variable gain LNA with high OIP3 for 5G using 40-nm bulk CMOS," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 1, pp. 64–66, Jan. 2018.
[81] S. Popuri, V. S. R. Pasupureddi, and J. Sturm, "A tunable gain and tunable band active balun LNA for IEEE 802.11ac WLAN receivers," in *Proc. 42nd Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2016, pp. 185–188.
[82] M. Yaghoobi, M. Yavari, and H. Ghafoorifard, "A 17-to-24 GHz low-power variable-gain low-noise amplifier in 65-nm CMOS for phased-array receivers," *Circuits, Syst., Signal Process.*, vol. 38, no. 12, pp. 5448–5466, Dec. 2019.
[83] C. C. Boon and X. Yi, "A 10–67 GHz 1.44 mW 20.7 dB gain VGA-embedded downconversion mixer with 40 dB variable gain range," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 7, pp. 466–468, Jul. 2014.
[84] T. T. Nguyen, K. Fujii, and A.-V. Pham, "A 7–42 GHz dual-mode reconfigurable mixer with an integrated active IF balun," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2017, pp. 2018–2021.
[85] N. Gupta, A. Dutta, and S. G. Singh, "A low/high band highly linearized reconfigurable down conversion mixer in 65nm CMOS process," in *Proc. Nordic Circuits Syst. Conf. (NORCAS), NORCHIP Int. Symp. Syst.-Chip (SoC)*, Oct. 2015, pp. 1–4.
[86] K. Bao, X. Fan, L. Tang, Z. Hua, and Z. Wang, "A CMOS reconfigurable passive mixer with digitally-controllable gain," in *Proc. IEEE Int. Symp. Radio-Freq. Integr. Technol.*, Aug. 2014, pp. 1–3.
[87] J. Xu, C. E. Saavedra, and G. Chen, "A 12 GHz-bandwidth CMOS mixer with variable conversion gain capability," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 10, pp. 565–567, Oct. 2011.
[88] X. Fan, C. Gu, J. Tao, and Z. Hua, "A reconfigurable 0.7–2.6 GHz wideband mixer for multi-mode multi-standard receivers in 0.18 μm RF CMOS," in *Proc. IEEE MTT-S Int. Microw. Workshop Ser. Adv. Mater. Processes RF THz Appl. (IMWS-AMP)*, Jul. 2015, pp. 1–3.
[89] B. Razavi and R. Behzad, *RF Microelectronics*, vol. 2. New York, NY, USA: Prentice-Hall, 2012.
[90] M. Wang and C. E. Saavedra, "Reconfigurable broadband mixer with variable conversion gain," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2011, pp. 1–4.
[91] J.-Y. Hsieh and S.-Y. Lee, "Theoretical analysis and implementation of a variable gain even harmonic mixer," in *Proc. Int. Symp. VLSI Design, Autom. Test (VLSI-DAT)*, Apr. 2007, pp. 1–4.
[92] C.-H. Wu and H.-T. Chou, "A 2.4GHz variable conversion gain mixer with body bias control techniques for low voltage low power applications," in *Proc. Asia–Pacific Microw. Conf.*, Dec. 2009, pp. 1561–1564.
[93] M.-M. Mohsenpour and C. E. Saavedra, "Highly linear reconfigurable mixer designed for environment-aware receiver," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2017, pp. 1–4.
[94] V. Kolios and G. Kalivas, "A 60 GHz down-conversion mixer with variable gain and bandwidth in 130 nm CMOS technology," in *Proc. 5th Int. Conf. Modern Circuits Syst. Technol. (MOCAST)*, May 2016, pp. 1–4.
[95] M.-H. Li, C.-N. Chen, Y. Wang, and H. Wang, "A 30-to-38 GHz active and passive combined down-conversion variable gain mixer with low OP1dB variation in 65-nm CMOS," in *Proc. 16th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Apr. 2022, pp. 55–58.

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