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RESEARCH ARTICLE

Enhanced Dynamic Regulation in Buck Converters: Integrating Input-Voltage Feedforward With Voltage-Mode Feedback

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ABSTRACT DC-DC buck converters in automotive and aerospace applications are often required to handle large disturbances in their input supply and abrupt variations in their loads. This paper proposes a systematic method to combine input-voltage feedforward (IVFF) and voltage-mode feedback (VFB) controllers, aiming to enhance the closed-loop performance of these DC-DC converters. This method relies on the stability boundary locus approach to help select the proper control parameters that achieve strong dynamic stability across the full operating range regardless of practical implementation challenges. Also, an optimization approach is employed to minimize the passive components' area within the compensator, achieving a 79% reduction in integration size compared to conventional designs. The controller was fabricated in a 0.35-μm CMOS technology, occupying a core area of 0.438 mm^2. The prototype chip was experimentally tested to regulate a buck converter that leverages an e-GaN half-bridge while operating at 1 MHz. Measurement results show a remarkable closed-loop performance against line and load variations, reaching up to $\pm$80 V/ms and $\pm$535 mA per 150 μs, respectively. The output remains stable, showcasing very small ($<$ 100 mV) to non-existent spikes and fast recovery periods. In addition, the system shows fast startup times ($<$ 100 μs) with small overshoots ($<$ 1%) observed at the output. The system power efficiency, tested across various loads, peaks at 95.14% while operating at 695 mA load current. It is shown that the combined-controller approach entirely eliminates transient voltage spikes, offering up to 100% improvement in dynamic performance over a standalone VFB controller.

INDEX TERMS Buck converter, controller design, DC-DC converter, dynamic regulation, feedforward, GaN half-bridge, high-voltage circuits, stability boundary locus, voltage-mode feedback.

I. INTRODUCTION

DC-DC buck converters are widely utilized in aerospace and automotive applications to drive and control electro-hydraulic actuators, such as solenoid valves [1], [2], [3]. Power buses within such systems are subject to transient overvoltage surges, often triggered by adjustments to the power bus's load [4], [5]. Ensuring stable output voltage (V_o) and current (I_o) in the face of such surges and line and load variations is crucial for overall system reliability [6], [7]. This emphasizes the need for robust controllers, designed for effective closed-loop

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performance, guaranteeing optimal dynamic and steady-state regulation.

Considerable research has been directed towards the design of controllers with robust rejection capabilities, especially for line variations [8], [9]. The developed techniques vary based on sensed state-variables, sensing mechanisms, and control signal generation. Notable examples include current-mode feedback control, sliding-mode control, one-cycle control, reset-integral control, and feedback linearization control, all of which can be adapted to mitigate the overvoltage surges. However, these techniques have several limitations including conditional instabilities, undesirable harmonics, complexity, reduced performance, and potential overvoltage issues [9], [10], [11], [12], [13]. More about these techniques is reviewed in Section II.

A promising solution to address these limitations lies in the combination of input-voltage feedforward control (IVFF) and voltage-mode feedback control (VFB) [15]. While both techniques individually possess limitations, notably, IVFF does not consider component tolerances and conduction losses [16], and VFB lacks information on the input voltage (V_g) causing large V_o transients [17], their combination can potentially mitigate line and load variations, free from the limitations above. This combination (FF-FB) has been presented in [18], where IVFF is combined with a simple VFB, and in [19], where IVFF is combined with a lag-lead voltage-mode controller for the regulation of a buck converter. Both studies, based on simulations, showed better immunity to line variations. However, neither study offered experimental verification, and they only examined variations of limited magnitudes ($\Delta V_g = 1$V to 4V). In addition, they did not analyze the impact of IVFF on VFB's dynamics.

To our knowledge, the internal dynamics of this combined approach and its impact on DC-DC converters' stability have remained unexplored in the literature. Our prior work in [15] introduced an initial analysis of combining IVFF with a voltage-mode PI controller for buck converter regulation. It was found that changes in the IVFF gain strongly affect the control performance, impacting the closed-loop system's phase margin, gain margin, and feedback bandwidth. This can lead the buck system's response to transition from an overdamped state to an underdamped (unstable) state. Ideally the IVFF gain is constant and independent of V_g, which makes the converter dynamically isolate the output from the input [20]. However, in practical implementations, the IVFF gain shifts with V_g variations when using a nonlinear conventional ramp generator [21]. To address this issue, more linearized ramp generators can be used, as in [22] and [23], but at the cost of circuit complexity and imperfect linearity. Therefore, a systematic method is essential to integrate both IVFF and VFB, ensuring the appropriate selection of control parameters and maintaining closed-loop dynamic stability across the operating range of interest. Other challenges lie in designing the VFB's compensator due to the large passive components' size, typically necessitating off-chip implementation. This can compromise the controller's accuracy and performance due to increased parametric uncertainties [24], [25].

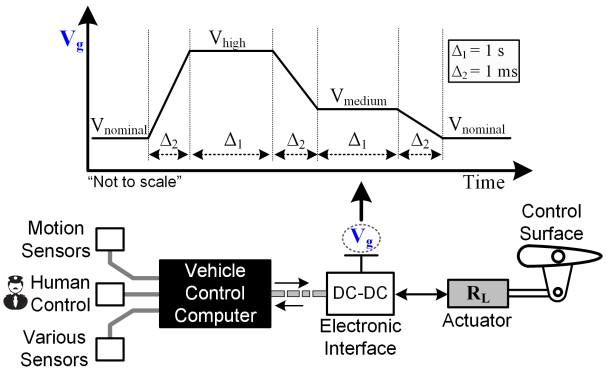


FIGURE 1. A vehicle's control system comprising a DC-DC converter with unregulated supply experiencing an overvoltage surge event.

In this paper, we propose a method to combine IVFF and VFB, leveraging the stability boundary locus approach (SBL) [26] to select optimal control parameters and to visualize the system's stability regions. Furthermore, our method addresses the challenges posed by the varying IVFF gain, ensuring a robust controller even when employing a nonlinear ramp generator. We also adopted the approach proposed in [17] to optimize the VFB's compensator footprint allowing full integration and avoiding delays and wiring parasitics related to off-chip components that degrade the system's efficiency. This paper contributes:

- A systematic method for selecting optimal control parameters to ensure stability of DC-DC buck converters regulated with combined IVFF and VFB controllers and subject to heavy and abrupt line and load variations, while considering nonlinearities of the circuit implementations.
- A detailed analysis of the design challenges imposed by the various circuit blocks constituting the combined controller (FF-FB), such as the analog compensator and the sawtooth generator circuits.
- A fully-integrated FF-FB controller implemented using a 0.35-μm CMOS process technology that minimizes the compensator's layout area considerably.
- Experimental verification of the closed-loop steady-state and dynamic performances of a buck converter regulated by the fabricated combined controller prototype.
- Dynamic performance comparison between the proposed combined controller and a standalone VFB controller to show the achieved improvement.

The paper is organized as follows. Section II reviews the relevant control techniques and the background application. Section III details the proposed method for combining IVFF and VFB. Section IV presents circuit implementations of the combined controller along with a brief illustration of the optimization approach used to reduce the on-chip area of

the passive components. Section V presents the controller prototype's test setup and results when regulating a buck converter. Finally, Section VI concludes the paper.

II. BACKGROUND AND LITERATURE REVEIW

Electronic interfaces in automotive applications, such as the vehicle's control system shown in Fig. 1, are often realized as DC-DC converters [17]. These converters draw their V_g supply from unregulated power buses susceptible to unwanted events such as transient overvoltage surges. Figure 1 depicts a typical overvoltage surge [6], where V_g shifts between three levels ($V_{nominal}$, V_{medium}, and V_{high}) in fast transitions as low as 1 ms. The system's capability to tolerate such surges is crucial to maintain reliable operation. Following is a review of various control techniques with competitive dynamic performance that can address this challenge. This review also examines the limitations of each technique.

First is the current-mode feedback control (CFB) that has two control loops: one to manage the inductor's current (I_L) and another to regulate V_o. CFB's strength lies in its instant response to changes in V_g, thus, achieving a stable V_o immune to line variations [27], [28]. Yet, it suffers from conditional instabilities requiring an artificial ramp to prevent possible oscillations at duty cycles ≥ 0.5 [10]. The slope of this ramp must match I_L's falling slope, which is hard to achieve during a transient event, otherwise, the rejection capability to line variations degrades [29]. CFB also requires a fast and precise current sensor, such as the Hall-effect sensor [30], which is costly and difficult to design [31]. Another technique, known for its fast response and robustness to disturbances, is the sliding-mode control (SMC). Instead of using a pulse width modulation (PWM) scheme, SMC directly drives the on/off state of the power switches, leading to a variable switching frequency (F_{sw}) and hard-to-eliminate harmonics [32], [33]. Efforts were reported to have SMC with fixed F_{sw} by using a hysteresis band comparator [11], or a PWM scheme [34], or system's state variables to create an adaptive sliding surface [32]. However, all these approaches come at the cost of reduced performance, lower robustness, and a complicated closed-loop structure that is hard to implement. Other control schemes, like one-cycle control (OCC) [29] and reset-integral control (RIC) [35], focus on filtering out the line variations, overlooking the actual V_o and leading to a low control performance in the presence of load variations and parasitic losses. An attempt in [28] to combine the features of different control types yielded a method merging OCC with voltage-mode feedback based on the SMC principles and operating with fixed F_{sw}. But, it is hard to reach optimum control parameters, and extending such method to other converter topologies is challenging [28]. Moreover, control schemes based on OCC or similar methods rely on sensing the switching node voltage (V_{sw}), which can experience large oscillations or large negative forward-voltage drops [36], [37]. Therefore, feeding V_{sw} to the low-voltage (LV) control circuits can potentially cause overvoltage problems. Another

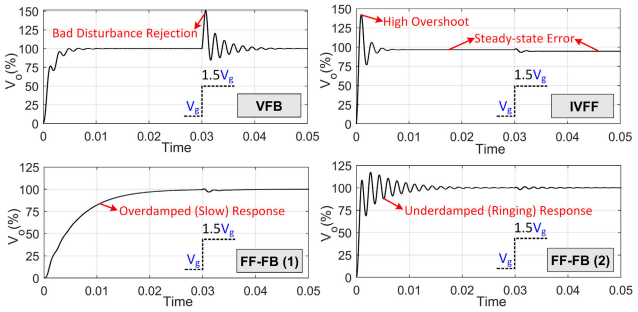


FIGURE 2. Transient response of a buck converter to a line variation step (from V_g to $1.5V_g$) using different less than ideal control schemes.

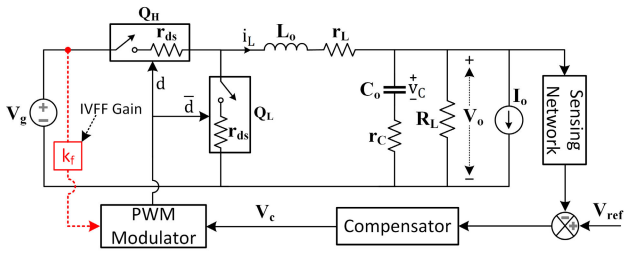


FIGURE 3. Simplified diagram of a non-ideal DC-DC buck converter regulated with IVFF and VFB controllers.

technique, the feedback linearization control (FLC), seeks to cancel out system nonlinearities and improve its disturbance rejection. However, its complex mathematical nature often requires the use of high-performance digital processors [13], [14]. Moreover, considering our application where analog control is the primary focus, integrating FLC into analog circuits becomes highly challenging due to the complexity associated with representing the inverse nonlinear dynamics.

IVFF was also introduced as a theoretical concept to reduce V_o's sensitivity to disturbances in V_g [38]. The IVFF's PWM modulator can be realized by either modulating the sawtooth signal's slope or its peak amplitude. The former results in variable F_{sw}, considered undesirable, leading designers to favor the latter with fixed F_{sw}. Adopting the latter, [10] introduced a general method to construct IVFF-based PWM modulators for various DC-DC converters using elements such as an integrator with reset, a comparator, and a one-shot pulse generator. Later, [16] and [39] applied that method for buck and boost converters, providing good immunity to line variations. However, only using IVFF is insufficient as it does not account for component tolerances and switching delays in the physical system [16], [35], resulting in steady-state errors as shown in Fig. 2. An added error signal from an external feedback, is essential for refining IVFF, ensuring DC stability and a reliable start-up regardless of supply disturbances [27]. Typically, a standalone VFB can deliver adequate performance, but relying solely on VFB is also insufficient to filter out line variations. This is because VFB lacks information on V_g, and it only responds to errors in V_o that occurs later after the V_g disturbance [15], which results in significant V_o transients, as shown in Fig 2. Combining IVFF and VFB

TABLE 1. Buck converter parameters.

Parameter	Value	Parameter	Value (Range)
V_o	28V	V_g	36 V - 115 V
L_o	24 µH	r_L	37 mΩ
C_o	33 µF	r_C	2.7 mΩ
r_{ds}	25 mΩ	R_L	25 Ω - 150 Ω

is expected to merge their benefits and mitigate individual limitations. However, proper control parameter selection is crucial to prevent potential closed-loop instability with varying IVFF gain, as shown in Fig. 2.

Several studies focused on the challenge of integrating the VFB's compensator with reduced on-chip area, often by employing more complex circuit designs. For instance, [40] proposed a type-III compensator using a transconductance amplifier (OTA) and a differential difference amplifier, achieving significant on-chip area reduction compared to conventional type-III. In [41], a type-II was integrated using a capacitor and a resistor, complemented by four OTAs and sensing I_L's AC ripple. Meanwhile, [42] used highly-linear OTAs and capacitance multipliers comprising high-gain amplifiers to replace resistors and capacitors, respectively, for effective integration of type-III compensators.

III. CONTROLLER DESIGN METHODOLOGY

In this Section, each step of the proposed method, to design the combined controller, is explained in detail. The method is applied to a synchronous buck converter, with F_{sw} of 1 MHz, whose simplified diagram, including the parasitic components, is depicted in Fig. 3. The first step is to define the converter's power-stage parameters followed by deriving its dynamic model. Afterwards, we choose the appropriate controller structure based on the system complexity and then select its fixed parameters. Lastly, the SBL approach is utilized to visualize the system stability and properly select the variable control parameters that guarantee optimal dynamic performance across the full operating range.

A. DEFINING THE CONVERTER'S PARAMETERS

The parameters of the buck converter (Fig. 3) are summarized in Table 1. The output filter inductor (L_o) is 24 μH and has DC resistance value (r_L) of 37 mΩ. The output filter capacitor (C_o) is 33 μF and has an equivalent series resistance (ESR) value (r_C) of 2.7 mΩ. The power-stage half-bridge is composed of two EPC2010C power transistors (Q_H, Q_L) with on-resistance (r_{ds}) of 25 mΩ. The input voltage (V_g) in the target application [6] ranges from 36 V to 115 V with a nominal value of 36 V. The nominal V_o is 28 V. Finally, the load resistance (R_L) ranges from 25 Ω to 150 Ω with a nominal value of 56 Ω.

B. DERIVING THE CONVERTER'S DYNAMIC MODEL

The widely used state-space averaging (SSA) technique is employed to derive the steady-state and dynamic models of the buck power-stage. This technique is divided into three stages: (1) formulation, (2) averaging, and (3) linearization, originally reported in [43] and further explained in [44] and [45]. It is also worth noting that a refined version of SSA was reported in [46]. The steady-state V_o is expressed in (1):

$$V_o = \frac{DR_L}{\eta} \mathrm{x} V_g \tag{1}$$

where D is the duty cycle and η is equal to $(R_L + r_{ds} + r_L)$. The most important transfer function (TF) in the dynamic model is the duty cycle-to-output voltage, $G_{dv}(s)$, which is expressed in (2) in terms of the converter's parameters.

$$G_{dv}(s) = \frac{\frac{R_L r_C V_g (R_L + r_L + r_{ds})}{\eta L_o (R_L + r_C)} \left(s + \frac{1}{C_o r_C}\right)}{s^2 + \frac{L_o + R_L C_o (r_C + \eta - R_L) + r_C C_o (\eta - R_L)}{L_o C_o (R_L + r_C)} s + \frac{\eta}{L_o C_o (R_L + r_C)}} \tag{2}$$

The other TFs describing the dynamic model, such as the input voltage-to-output voltage, $G_{vv}(s)$ and the output current-to-output voltage, $G_{iv}(s)$, which can be found in [44], do not contribute directly to the controller design, however, they can

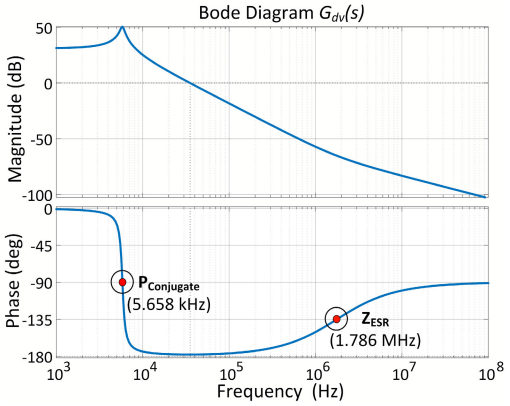


FIGURE 4. Bode diagram of $G_{dv}(s)$ for the nominal buck converter highlighting the conjugate pole and ESR zero frequencies.

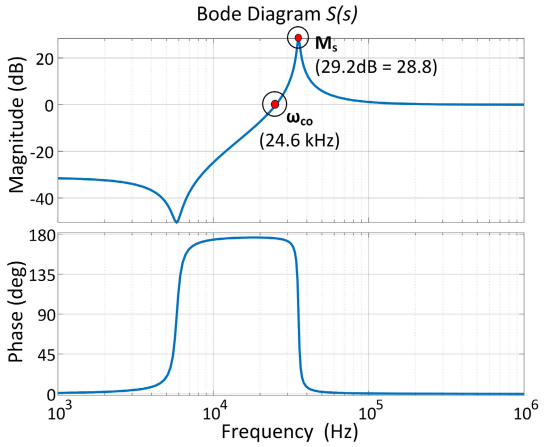


FIGURE 5. Bode diagram of $S(s)$ for the nominal buck converter in case of a unity feedback and a unity modulator's gain.

be used to evaluate the system response. The VFB structure is chosen based on the complexity and shape of $G_{dv}(s)$. The parameters from Table 1, at the nominal operating point ($V_g = 36$ V, $R_L = 56\ \Omega$), are used to obtain the numeric representation of $G_{dv}(s)$ as expressed in (3):

$$G_{dv}(s) = \frac{4049.8(s + 1.122\text{x}10^7)}{s^2 + 3237s + 1.264\text{x}10^9} \tag{3}$$

Apparently, $G_{dv}(s)$ consists of one zero and two complex conjugate poles, located at 1.786 MHz and 5.658 kHz, respectively, as shown in Fig. 4. It is worth noting that pole locations deviate (by $< 0.1\%$) from their nominal values across the full range of V_g and R_L combinations. Given this negligible change, we can assume that using the nominal system is representative of all the other combinations.

C. CHOOSING THE FEEDBACK CONTROLLER STRUCTURE

The VFB controller structure plays a pivotal role in the converter's closed-loop operation. Its parameters are selected to ensure optimal phase margin (ϕ_M), gain margin (A_M), and bandwidth (BW) to achieve reliable dynamic performance. Also, when considering controller robustness, it is important to account for the sensitivity of the closed-loop system to parametric changes and line variations. This sensitivity, represented by $S(s)$ in (4), shows the impact of the feedback on the output [47], where $G_C(s)$ is the compensator's TF and $L(s)$ is the system's open-loop gain.

$$S\,(s) = \frac{1}{1 + G_C(s)G_{dv}(s)} = \frac{1}{1 + L(s)} \tag{4}$$

In the buck converter under study, r_C is very small ($\sim 2.7\ \text{m}\Omega$), leading to a high-frequency zero (Z_{ESR}) that does not benefit the converter in boosting ϕ_M as shown in Fig. 4. In addition, assuming $G_C\,(s) = 1$, the maximum sensitivity (M_s), defined by (5) and highlighted in Fig. 5, reaches 28.8. This is clearly higher than commonly reported values of 1.1 to 2 [47], [48], compromising the disturbance rejection post the crossover frequency (ω_{co}). Therefore, at least a 2$^{\text{nd}}$ order controller is essential to appropriately shape $S(s)$ and introduce a low-frequency zero to boost ϕ_M. A type-III compensator, serving as the VFB controller, is adopted to enhance both the ϕ_M and BW of the closed-loop system and properly shape $S(s)$ [49]. Its TF is shown in (6) and it comprises one pole at the origin (ω_{p0}), two additional poles (ω_{p1}, ω_{p2}), and two zeroes (ω_{z1}, ω_{z2}).

$$M_s = max\,|S\,(s)| = max\left|\frac{1}{1 + L\,(s)}\right| \tag{5}$$

$$G_C(s) = \frac{\left(\frac{s}{\omega_{z1}} + 1\right)\left(\frac{s}{\omega_{z2}} + 1\right)}{\frac{s}{\omega_{p0}}\left(\frac{s}{\omega_{p1}} + 1\right)\left(\frac{s}{\omega_{p2}} + 1\right)} \tag{6}$$

The SBL approach facilitates the effective combination of IVFF and VFB by graphically representing IVFF's impact on the closed-loop system stability. This aids in selecting the optimal VFB parameters to achieve enough stability while maintaining M_s within the 1.1 to 2 range. However, this approach only yields two equations. Thus, one of the two zeros in $G_C\,(s)$, ω_{z1}, is treated as a variable for phase shaping, and the pole ω_{p0}, which significantly affects the speed of the controller [49], is chosen as the second variable. The other parameters (ω_{z2}, ω_{p1}, ω_{p2}) of $G_C(s)$ are chosen to be fixed.

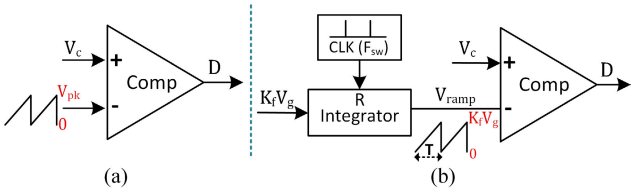


FIGURE 6. Diagram of the PWM modulator for a buck converter: (a) without IVFF, and (b) with IVFF.

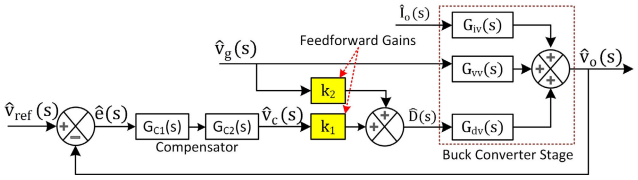


FIGURE 7. Complete dynamic model of the closed-loop buck converter system with combined IVFF and VFB.

D. SELECTING THE COMPENSATOR'S FIXED PARAMETERS

To simplify the parameter selection process, $G_C(s)$ can be considered as two cascaded controllers, $G_{C1}\,(s)$ and $G_{C2}(s)$, without any loss of generality [25]. Both $G_{C1}(s)$ and $G_{C2}\,(s)$ are defined in (7), where the parameters k_p and k_i are equal to ω_{p0}/ω_{z1} and ω_{p0}, respectively.

$$G_{C1}\,(s) = \frac{(k_p s + k_i)}{s},\ G_{C2}\,(s) = \frac{\left(\frac{s}{\omega_{z2}} + 1\right)}{\left(\frac{s}{\omega_{p1}} + 1\right)\left(\frac{s}{\omega_{p2}} + 1\right)} \tag{7}$$

As noted, the parameters of $G_{C1}(s)$ are graphically determined using the SBL approach, while those of $G_{C2}(s)$ adhere to a fixed criterion based on the pole-zero locations and the frequency response of $G_{dv}(s)$ of the nominal system. In our buck converter, $G_{dv}(s)$'s phase rolls quickly to –180° post the conjugate pole ($\text{P}_{\text{Conjugate}}$), as shown in Fig. 4. So, ω_{z2} is selected at this frequency to provide a 90° phase boost and prevent the descent to –180°. For high-frequency robustness and noise attenuation, ω_{p1} is selected to cancel the high-frequency Z_{ESR}. Finally, ω_{p2} is selected at half of F_{sw} (equal to 0.5 MHz) of the buck converter system to maintain higher closed-loop BW.

E. APPLYING THE STABILITY BOUNDARY LOCUS APPROACH

Before applying the SBL approach to select the variable parameters, the PWM modulator's dynamic model is derived at first to account for its contribution in $L(s)$.

1) MODULATOR'S DYNAMIC MODEL

For a standalone VFB, a typical PWM modulator is used. This modulator comprises a comparator with the control voltage (V_c) on its $+ve$ input and a fixed-amplitude sawtooth signal (V_{ramp}) with amplitude (V_{pk}) on its $-ve$ input, as shown in Fig. 6(a). In this case, D is equal to V_c divided by the peak change in V_{ramp} as in (8). Thus, the modulator's small-signal model can be represented by a constant gain (k), which is the inverse of V_{pk} as given in (9).

$$D = \frac{V_c}{\Delta V_{ramp}} = \frac{V_c}{V_{pk}} \tag{8}$$

$$k = \frac{\partial D}{\partial V_c} = \frac{1}{V_{pk}} \tag{9}$$

On the other hand, when IVFF and VFB jointly regulate the buck converter, V_{pk} is designed proportional to V_g [10], as shown in Fig. 6(b). Consequently, D rapidly changes to counteract variations in V_g, adjusting the generated PWM cycle-by-cycle as defined in (10). The small-signal model for this modulator is derived from the first-order terms in the Taylor series expansion of (10), as given in (11). The hat symbol $\hat{()}$ denotes small-signal values. This model is represented by two gains, k_1 and k_2, defined in (12), which correlate the small changes in D to those in V_c and V_g, respectively. Here, k_f is the IVFF scaling factor.

$$D = \frac{V_c}{\Delta V_{ramp}} = \frac{V_c}{k_f V_g} \tag{10}$$

$$\hat{D} = \frac{\partial D}{\partial V_c}\hat{V}_c + \frac{\partial D}{\partial V_g}\hat{V}_g = k_1\hat{V}_c + k_2\hat{V}_g \tag{11}$$

$$k_1 = \frac{1}{k_f V_g}, k_2 = \frac{-V_c}{k_f V_g^2} = -\frac{D k_f V_g}{k_f V_g^2} = \frac{V_o}{V_g^2} \tag{12}$$

The full dynamic model of the buck converter system combining both IVFF and VFB is shown in Fig. 7. The buck power-stage is represented by the three TFs: $G_{dv}(s)$, $G_{vv}(s)$, and $G_{iv}(s)$. The compensator is represented by $G_{C1}(s)$ and $G_{C2}(s)$ given in (7), while the IVFF-based PWM modulator is represented by the two gains (k_1 and k_2). Past studies often overlooked the impact of IVFF on the open-loop gain $L(s)$, leading to the independent design of VFB and IVFF. However, IVFF does influence $L(s)$, particularly as its gain k_1 forms part of $L(s)$ as seen in (13). This gain varies with the value of V_g and k_f as per (12), which can result in an unstable system if not considered in the VFB design.

$$L(s) = k_1 G_{C1}(s)\, G_{C2}(s) G_{dv}(s) \tag{13}$$

2) STABILITY BOUNDARY LOCUS APPROACH

The SBL approach [26] is used to analyze the closed-loop system, aiming to identify the possible (k_p, k_i) combinations that achieve a specific level of stability with ϕ_M and A_M exceeding certain values. In addition, the effect of combining IVFF with VFB on the stability can be visualized, enabling the selection of optimal control parameters. The dynamic model, shown in Fig. 7, is used to derive the system closed-loop TF from $\hat{V}_{ref}(s)$ to $\hat{V}_o(s)$, as defined in (14).

$$\frac{\hat{V}_o(s)}{\hat{V}_{ref}(s)} = \frac{L(s)}{1+L(s)} = \frac{k_1 G_{C1}(s)\, G_{C2}(s)\, G_{dv}(s)}{1 + k_1 G_{C1}(s)\, G_{C2}(s)\, G_{dv}(s)} \tag{14}$$

The TFs, $G_{C2}(s)$ and $G_{dv}(s)$, are combined to form the system TF, $G_{sys}(s)$, given in (15). Here, N_e and N_o are the numerator's even and odd terms, respectively, while D_e and D_o are the denominator's even and odd terms, respectively. Using (7), (14), and (15), the closed-loop characteristic polynomial is derived in (16), given that s is substituted by $j\omega$, where j is the imaginary unit and ω stands for the angular frequency. An additional term in (16), the gain-phase tester ($A_M.e^{-j\phi_M}$), is added to ensure that the loci resulting from the SBL approach define the boundaries for ϕ_M and A_M.

$$G_{sys}(s) = G_{C2}(s)\, G_{dv}(s) = \frac{N(s)}{D(s)} = \frac{N_e + j\omega N_o}{D_e + j\omega D_o} \tag{15}$$

$$1 + A_M e^{-j\phi_M} k_1 \left(\frac{j\omega k_p + k_i}{j\omega}\right)\left(\frac{N_e + j\omega N_o}{D_e + j\omega D_o}\right) = 0 \tag{16}$$

To determine the stabilizing (k_p, k_i) pairs ensuring a Hurwitz stable closed-loop system with specific ϕ_M and A_M, the characteristic polynomial is expanded. Equating its real and imaginary parts to 0 provides two equations. Solving these for k_p and k_i yields the boundary loci equations defined below in (17):

$$k_p = \frac{X(\omega)\, U(\omega) - Y(\omega)\, R(\omega)}{k_1.\left(Q(\omega)\, U(\omega) - R(\omega)\, S(\omega)\right)}$$

$$k_i = \frac{Y(\omega)\, Q(\omega) - X(\omega)\, S(\omega)}{k_1.\left(Q(\omega)\, U(\omega) - R(\omega)\, S(\omega)\right)} \tag{17}$$

where the terms Q, R, S, U, X, and Y are defined below in (18):

$$\begin{aligned} Q(\omega) &= A_M\left(\omega N_e \sin\phi_M - \omega^2 N_o \cos\phi_M\right) \\ R(\omega) &= A_M\left(N_e \cos\phi_M + \omega N_o \sin\phi_M\right) \\ S(\omega) &= A_M\left(\omega N_e \cos\phi_M + \omega^2 N_o \sin\phi_M\right) \\ U(\omega) &= A_M(\omega N_o \cos\phi_M - N_e \sin\phi_M) \\ X(\omega) &= \omega^2 D_o \\ Y(\omega) &= -\omega D_e \end{aligned} \tag{18}$$

From (17), it is clear that the IVFF gain k_1 impacts the boundary loci's computation. For a desired ϕ_M, we set A_M to one in (17), while for a desired A_M, we set ϕ_M to zero in (17) to neutralize the phase-gain tester's exponential term. For the buck case, we can derive generalized expressions for the boundary loci by parameterizing $G_{dv}(s)$ as shown in (19).

$$G_{dv}(s) = \frac{a_1 s + a_0}{b_2 s^2 + b_1 s + b_0} \tag{19}$$

Due to the complex algebraic manipulations required, a simple MATLAB® script is used to solve for the boundary loci, Loc(k_p, k_i), using the parametrized forms of $G_{C2}(s)$ and $G_{dv}(s)$. This yields the locus Loc($k_{p-\phi_M}$, $k_{i-\phi_M}$) for ϕ_M

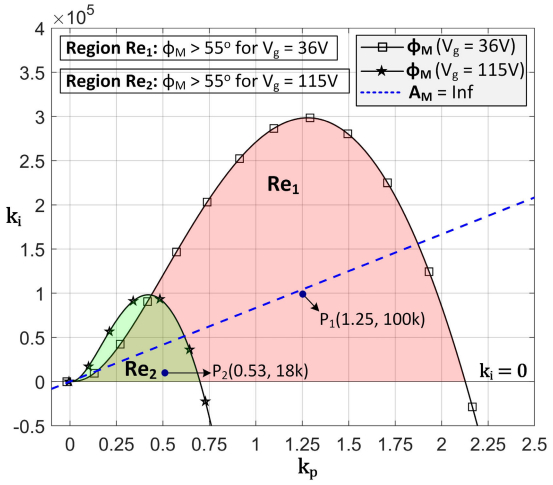


FIGURE 8. Boundary loci for $\phi_M \geq 55°$ and $A_M = \text{Inf}$ at different values of V_g (which corresponds to different IVFF gain values).

and the locus $\text{Loc}(k_{p-A_M}, k_{i-A_M})$ for A_M, which are denoted by (20) and (21), respectively:

$$k_{p-\phi_M} = \frac{C_3C_4 - \omega^2 C_1C_2}{\omega k_1\left(\omega^2+\omega_{z2}^2\right)\left(a_0^2+a_1^2\omega^2\right)}$$
$$k_{i-\phi_M} = \frac{C_5C_4 - \omega^2 C_6C_2}{\omega k_1\left(\omega^2+\omega_{z2}^2\right)\left(a_0^2+a_1^2\omega^2\right)} \tag{20}$$

$$k_{p-A_M} = \frac{C_4\left(-a_1\omega^2+a_0\omega_{z2}\right) - \omega^2 C_2\left(a_0\omega + a_1\omega\omega_{z2}\right)}{A_M\omega k_1\left(\omega^2+\omega_{Z2}^2\right)\left(a_0^2+a_1^2\omega^2\right)}$$
$$k_{i-A_M} = \frac{\omega^2 C_4\left(a_0+a_1\omega_{z2}\right) + \omega^3 C_2\left(-a_1\omega^2+a_0\omega_{z2}\right)}{A_M\omega k_1\left(\omega^2+\omega_{z2}^2\right)\left(a_0^2+a_1^2\omega^2\right)} \tag{21}$$

where the coefficients $C_1$to C_6 are defined in (22) below:

$$C_1 = \begin{pmatrix} a_1\omega^2\sin\phi_M + a_0\omega\cos\phi_M - \\ a_0\omega_{z2}\sin\phi_M + a_1\omega\omega_{z2}\cos\phi_M \end{pmatrix}$$
$$C_2 = \begin{pmatrix} b_0\omega_{p1} + b_0\omega_{p2} - b_1\omega^2 - \\ b_2\omega^2\omega_{p1} - b_2\omega^2\omega_{p2} + b_1\omega_{p1}\omega_{p2} \end{pmatrix}$$
$$C_3 = \begin{pmatrix} a_0\omega_{z2}\cos\phi_M - a_1\omega^2\cos\phi_M + \\ a_0\omega\sin\phi_M + a_1\omega\omega_{z2}\sin\phi_M \end{pmatrix}$$
$$C_4 = \begin{pmatrix} b_0\omega^3 - b_2\omega^5 + b_1\omega^3\omega_{p1} + \\ b_1\omega^3\omega_{p2} - b_0\omega\omega_{p1}\omega_{p2} + b_2\omega^3\omega_{p1}\omega_{p2} \end{pmatrix}$$
$$C_5 = \begin{pmatrix} \omega\sin\phi_M\left(-a_1\omega^2+a_0\omega_{z2}\right) - \\ \omega^2\cos\phi_M\left(a_0+a_1\omega_{z2}\right) \end{pmatrix}$$
$$C_6 = \begin{pmatrix} \omega\cos\phi_M\left(-a_1\omega^2+a_0\omega_{z2}\right) + \\ \omega^2\sin\phi_M\left(a_0+a_1\omega_{z2}\right) \end{pmatrix} \tag{22}$$

The parameters of $G_{dv}(s)$ and $G_{C2}(s)$ are substituted back in (20) and (21), noting that the value of k_1 varies with V_g and that it is computed based on the parameters of the sawtooth generator circuit designed later in Section IV-B. ϕ_M is set to 55°, while A_M is set to Inf, which implies that $L(s)$'s phase will never cross −180°. Afterwards, ω is varied from 0 to 2.5M to draw the boundary loci at $V_g = 36$ V and 115 V, as shown in Fig. 8. These loci, combined with the $k_i = 0$ line, divide the (k_p, k_i) plane into stable and unstable regions relative to selected values of ϕ_M and A_M [26]. Thus, by sampling a (k_p, k_i) pair from each region and checking the roots of the characteristic polynomial, stable and unstable regions are identified. For instance, in Fig. 8, at $V_g = 36$ V, pairs from the shaded region (Re_1), as P_1, are guaranteed to achieve $\phi_M \geq 55°$, while at $V_g = 115$ V, pairs from the shaded region (Re_2), as P_2, are guaranteed to achieve $\phi_M \geq 55°$. Pairs below the dashed line guarantee A_M to be Inf. Hence, the shaded areas below this dashed line in Fig. 8 guarantee both $\phi_M \geq 55°$ and A_M as Inf for the respective V_g values.

From Fig. 8, it is evident that as V_g decreases (increases), the stability region (where $\phi_M \geq 55°$) expands (shrinks) to include (exclude) pairs of (k_p, k_i) that achieve the required stability. This is attributed to the IVFF gain ($k_1 = 1/k_f V_g$) which results in an open-loop gain $L(s) = G_C(s)G_{dv}(s)/k_f V_g$ that varies with changes in V_g or k_f. The V_g term (from k_1) is cancelled with the V_g term in the numerator of $G_{dv}(s)$, shown in (2), achieving the main objective of IVFF: making $L(s)$ independent to V_g. However, a residual V_g-dependence still exists through k_f. This factor is equal to $\alpha\beta$, where α is a constant representing the resistive divider used to scale down V_g, while β is a variable signifying the transfer characteristics of the sawtooth generator used to implement the IVFF. Thus, the effective part of the IVFF gain (k_1) is β, which decreases nonlinearly with V_g if conventional sawtooth generators are used as will be detailed later in Fig. 13 of Section IV. This causes the system's dynamic stability to partially depend on V_g, potentially leading to stability and performance issues if not considered in the combined controller design.

F. SELECTING THE COMPENSATOR'S VARIABLE PARAMETERS

The selection criteria for the control parameters, k_p and k_i, is based on the dynamic properties of the closed-loop system, namely ϕ_M, A_M, BW, and M_s, ensuring a robust controller that remains stable despite $L(s)$ variations with V_g. Firstly, ϕ_M and A_M should be at least higher than 55° and 10, respectively, for sufficient stability [49]. Secondly, the BW is constrained by a lower bound of $3f_0$ (17 kHz) and an upper bound of $F_{sw}/2$ (500 kHz), where f_0 is the resonance frequency of the output filter. This lower bound ensures having enough system gain to counteract oscillations at f_0 and is recommended to be more than one-tenth of F_{sw}. Meanwhile, the upper bound is based on the system physical limitations and to reduce susceptibility to high-frequency noise. Lastly, M_s should be smaller than 2 for robustness against input disturbances and insensitivity to process variations [25], [47].

In Fig. 8, the (k_p, k_i) pairs in Re_1 (excluding those in Re_2), such as P_1, violates the ϕ_M constraint at $V_g = 115$ V and thus are not selected for $G_{C1}(s)$. However, parameters of $G_{C1}(s)$ are selected from pairs in Re_2 below the A_M locus to satisfy all the stability requirements. First, a value from the respective k_i range in Fig. 8 is arbitrarily selected (18k), and k_p is varied while monitoring the dynamic properties like

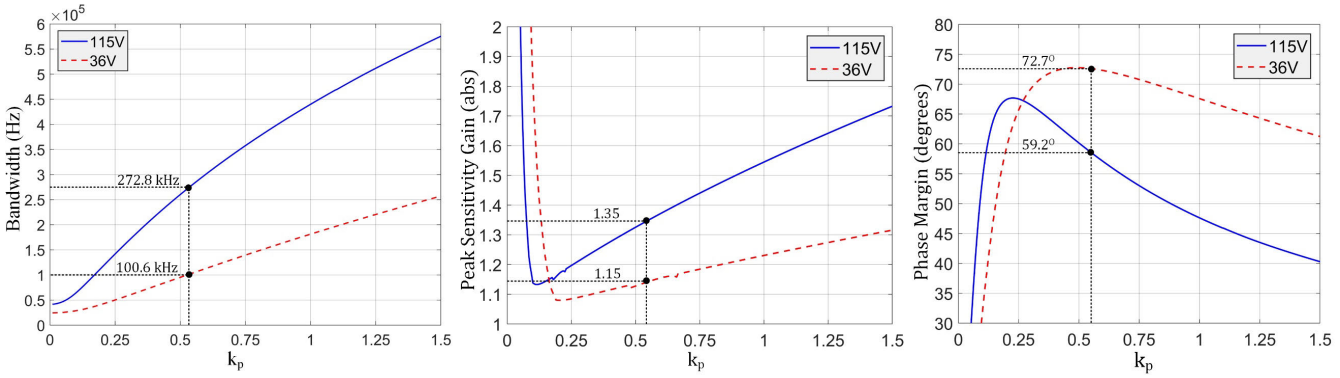
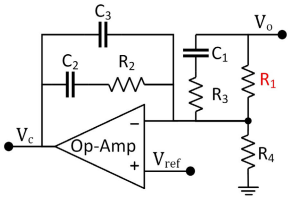


FIGURE 9. Plots of the closed-loop dynamic properties (bandwidth, peak sensitivity, and phase margin) at a fixed k_i of 18000 and a variable k_p.



(a)

Passive Components & $G_C(s)$ Parameters

R_1	2.270 MΩ	C_3	265.0 fF
R_2	1.203 MΩ	k_p	0.53
R_3	7.196 kΩ	k_i	18000
R_4	81.04 kΩ	ω_{p1}	11.22*10^6 rad/s
C_1	12.40 pF	ω_{p2}	3.14*10^6 rad/s
C_2	24.52 pF	ω_{z2}	35.55*10^3 rad/s

(b)

FIGURE 10. (a) Typical analog realization of type-III compensator using an op-amp [49]. (b) Summary of the selected $G_C(s)$ parameters and the on-chip passive components' values after optimizing the area.

ϕ_M, BW, and M_s as shown in Fig. 9. The proper k_p value is then selected so that the dynamic properties are satisfied at the V_g corner values (36 V, 115 V). Thus, point P_2 ($k_p = 0.53$, $k_i = 18$k) is selected from Fig. 8. At $V_g = 36$ V, ϕ_M, A_M, BW, and M_s are 72.7°, Inf, 100.6 kHz, and 1.15, respectively, while at V_g =115 V, they are 59.2°, Inf, 272.8 kHz, and 1.35, respectively. Finally, it is recommended for the dynamic properties to exhibit a minimal variation relative to the k_p parameter around the selected P_2, ensuring a robust controller, as observed in Fig. 9.

IV. CIRCUIT AND SYSTEM DESIGN

In this Section, we present the circuit design procedure for implementing the proposed combined controller using the AMS 0.35-μm CMOS technology. This technology supports the integration of various active and passive devices with voltage ratings from 3.3 V to 120 V. Additionally, we employ an optimization technique to minimize the on-chip foot-print of the compensator's passive components.

A. VOLTAGE-MODE FEEDBACK (COMPENSATOR)

The typical analog implementation of a type-III compensator is depicted in Fig. 10(a). It is composed of an op-amp, three capacitors, and four resistors. Usually, designers prefer to place the passive components off-chip to save silicon area and lower the fabrication cost. However, off-chip components are bulky, have increased parametric uncertainties, and can inject significant noise degrading the controller's accuracy and the system's reliability [41]. Accordingly, the technique we proposed in [17] is used to minimize the area of the passive components to allow fully integrating the compensator. Given that (23) represents the TF of the compensator in Fig. 10(a), we can redefine the parameters of $G_C(s)$, reported earlier in (6) and summarized in Fig. 10(b), in terms of the passive components' values: (C_1, C_2, C_3) and (R_1, R_2, R_3) by mapping to (23). The mapping result is shown in (24), assuming that $R_1 \gg R_3$ and $C_2 \gg C_3$.

$$G_C(s) = \frac{V_c(s)}{V_o(s)} = \frac{(1+sC_1(R_1+R_3))(1+sC_2R_2)}{sR_1(C_3+C_2)(1+sC_1R_3)\left(1+sR_2\frac{C_2C_3}{C_2+C3}\right)} \tag{23}$$

$$\omega_{z1} = \frac{1}{R_2C_2}, \omega_{z2} \approx \frac{1}{R_1C_1}$$
$$\omega_{p1} = \frac{1}{R_3C_1}, \omega_{p2} \approx \frac{1}{R_2C_3}, \omega_{p0} \approx \frac{1}{R_1C_2} \tag{24}$$

Given that the compensator's poles and zeros are already selected, with some algebra, all passive components can be designed based on R_1's value as indicated in (25). Hence, the on-chip area of these components is also a function of R_1. In (25), the ratio (0.0357) between R_4 and R_1 is set based on the nominal V_o value (28 V) to be scaled down to 1 V in the range of the voltage reference signal (V_{ref}).

$$R_4 = 0.0357R_1 \quad R_2 = \frac{\omega_{p0}}{\omega_{z1}}R_1 \quad R_3 = \frac{1}{\omega_{p1}C_1} = \frac{\omega_{z2}}{\omega_{p1}}R_1$$
$$C_1 = \frac{1}{\omega_{z2}R_1} \quad C_2 = \frac{1}{\omega_{p0}R_1} \quad C_3 = \frac{1}{\omega_{p2}R_2} = \frac{\omega_{z1}}{\omega_{p2}\omega_{p0}R_1} \tag{25}$$

By modeling each passive component's layout area, we can optimize R_1 to minimize the compensator's area. Capacitors and resistors from AMS are selected based on their voltage ratings and surface density. High-voltage (HV) capacitors use the "CWPM" type, while low-voltage (LV) capacitors (C_2 and C_3) use the "CPOLY" type. Area models for each

capacitor type are then derived in terms of the capacitance value (C_{val}) as in (26), where m_{1-3} are constants calculated based on guard ring dimensions, area of metal contacts at the capacitor's terminals, and capacitance per unit area.

$$\text{Area}_{\text{Cap}} = \frac{C_{val}}{m_3} + m_1\sqrt{\frac{C_{val}}{m_3}} + m_2 \tag{26}$$

High-value resistors (R_1, R_2, and R_4) use the "RPOLYH" type, while low-value resistors (R_3) use the "RPOLY1" type. Similarly, area models for each resistor type are derived in terms of the resistance value (R_{val}) and the number of bends (N) as defined in (27), where m_{4-7} are constants calculated based on guard ring dimensions, physical spacings between bends, and sheet resistance value.

$$\text{Area}_{\text{Res}} = (m_4 + m_5 N)\left(m_6 + \frac{R_{val}}{m_7\,(N+1)}\right) \tag{27}$$

Now, the total area is determined as a function of R_1 and the number of bends (N_i) for each resistor (R_i), represented as AreaTotal $= f(R_1, N_1, N_2, N_3, N_4)$. Using MATLAB®'s optimization toolbox, this nonlinear multivariable function is minimized to get the smallest possible area. The numerical results are then used to obtain the passive components' final values (reported in Fig. 10(b)), achieving a compensator with very small on-chip area. Figure 11 plots the total area versus R_1 based on the predicted N_i values, highlighting a calculated minimum area of 0.225 mm^2 at $R_1 = 2.27$ MΩ. Notably, a ±15% deviation from this optimal R_1 value retains a similar total area. Compared to the recommended R_1 value of 200 kΩ by Texas Instruments [49], our optimal R_1 value of 2.27 MΩ achieved a significant reduction in the total area of the passive components by 79% (1.072 mm^2 to 0.225 mm^2). While translating this area reduction directly into monetary savings is challenging within the scope of our academic research project, it is important to note that such reduction would positively impact the non-recurring engineering and volume fabrication costs in a commercial context. To our knowledge, there is no system-related negative impact from choosing R_1 outside the range mentioned in [49]. However, the realized actual area is 0.296 mm^2, which is slightly higher than the predicted area in Fig. 11. The reason is that some resistors, such as R_1 and R_4, are divided into smaller parts for matching purposes. Also, floor-planning of different components and circuit blocks results in a slight increase in the area. For detailed area optimization insights, see [17].

B. INPUT-VOLTAGE FEEDFORWARD

The IVFF controller, which is a major part of our proposed solution, comprises two main blocks as illustrated in Fig. 12. The first block, a resistive divider, is used to scale down V_g to signal V_x below 3.3 V. Its dynamic model representation is a constant (α) equal to the scaling factor, as defined in (28). The second block, the sawtooth generator, generates a sawtooth signal with its peak proportional to V_x's value. Its dynamic model representation is a variable (β) which links the change in the sawtooth amplitude V_{pk} to the change in V_x, as defined

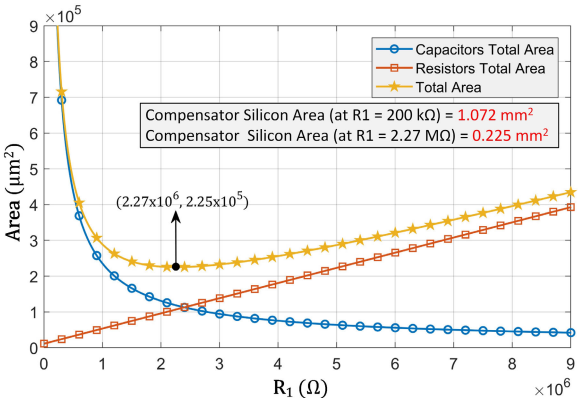


FIGURE 11. Calculated on-chip area of the passive components composing the type-III compensator (using predicted values of N_i).

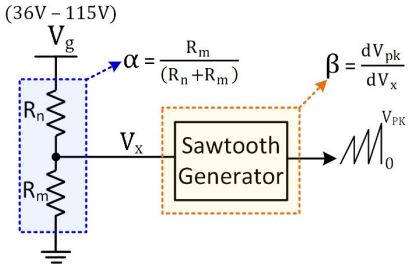


FIGURE 12. The IVFF implementation comprising a resistive divider block and a sawtooth generator block.

in (29). These two gains combined form the IVFF scaling factor $k_f = \alpha\beta$, central to shaping the stability region as explained in Section III. Thus, proper implementation and parameter selection for these blocks are crucial to guarantee the system's stability.

$$\alpha = \frac{R_m}{R_n + R_m} \tag{28}$$

$$\beta = \frac{dV_{pk}}{dV_x} \tag{29}$$

For optimal feedforward compensation, V_{pk} should be linearly proportional to V_g, making β constant. Nevertheless, most real-world sawtooth generators are nonlinear in nature resulting in a variable β. While some research, like [22] and [23], aims for sawtooth generators with linear characteristics, these designs are often more complex, in addition, deviations from perfect linearity still exist. For this reason, we have adopted the traditional sawtooth generator circuit from [50], and the inherent nonlinearity is handled during the controller design stage as explained in Section III.

The sawtooth generator circuit is depicted in Fig. 13(a). It is basically a controlled integrator with a reset switch (M_{N0}). The signal V_x is processed through an op-amp, creating a proportional current using resistor R_t. This current is mirrored using M_{P1} and M_{P0} to charge capacitor C_t. Paired with the narrow-pulse generator, M_{N0} discharges C_t and resets the output V_{saw} to zero in sync with the rising edge

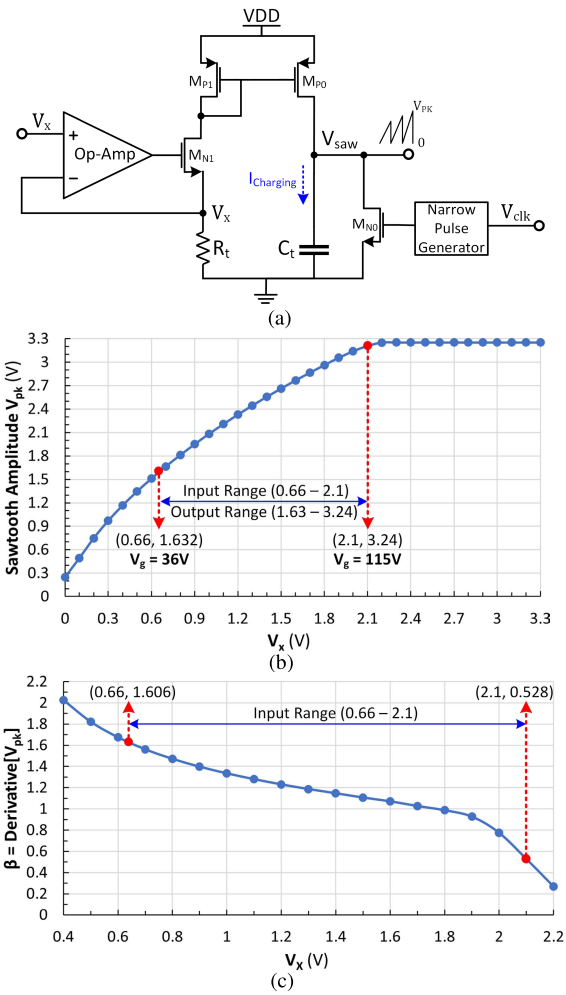


FIGURE 13. (a) Circuit diagram of the classic sawtooth generator. (b) Simulated transfer characteristics highlighting the input range of importance. (c) Transfer characteristics' derivative representing β in the factor k_f.

of the input clock (V_{clk}). This outputs a sawtooth signal matching the V_{clk} frequency with an amplitude controlled by the input V_x (i.e., the current $I_{Charging}$ and the capacitor C_t). The limits of the common-mode input-voltage range of the designed op-amp are 0.2 V and 2.34 V. This requires the value of V_x to be within such range for linear operation and to set the voltage-drop on M_{N1} and M_{P1} so that they operate in saturation. Consequently, the resistors R_n and R_m, in Fig. 12, are adjusted to 500 kΩ and 9.3 kΩ, respectively, making $\alpha = 0.01926$, hence scaling down V_g from (36 V – 115 V) to (0.66 V – 2.1 V). The values of R_t and C_t are set to 60 kΩ and 12 pF, respectively, so that V_{pk} approaches VDD of 3.3 V at the upper limit of V_x, enhancing the modulator's noise immunity. Figure 13(b) shows the simulated transfer characteristics demonstrating the scaled input range and the corresponding V_{pk} range. The nonlinearity of the sawtooth generator is shown in Fig. 13(c), where β changes from 1.606 to 0.528 when V_g changes from 36 V to 115 V (corresponding to the two stability regions seen in Fig. 8).

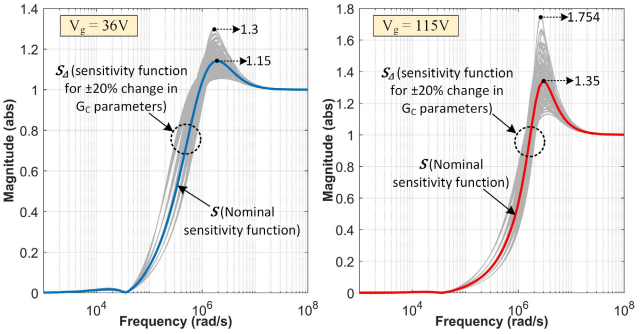


FIGURE 14. Sensitivity functions (S: nominal, S_Δ: all combinations of ±20% change in the $G_C(s)$ parameters).

C. ROBUSTNESS-FRAGILITY ANALYSIS OF THE CONTROLLER

Designed linear controllers have exact parameter values, which are difficult to achieve due to passive components tolerances and numerical approximations. Fragility analysis is used to assess the impact of controller parameter variations on system robustness. In [51], the delta-epsilon-robustness-fragility index ($FI_{\Delta 20}$), defined in (30), was introduced to measure the loss of robustness due to ±20% variations of the nominal $G_C(s)$ parameters. This index categorizes controllers into robustness fragile ($FI_{\Delta 20} > 0.5$), robustness nonfragile ($0.1 < FI_{\Delta 20} \leq 0.5$), and robustness resilient ($FI_{\Delta 20} \leq 0.1$).

$$FI_{\Delta 20} = \left(\frac{M_{s\Delta 20}}{M_{so}} - 1 \right) \tag{30}$$

where M_{so} is the sensitivity function's peak value for the nominal system, and $M_{s\Delta 20}$ is the sensitivity function's peak value for ±20% change in the controller's component values. Figure 14 plots the sensitivity function for 729 combinations for ±20% variations in the controller's passive components (S_Δ), shown in Fig. 10(a), and for the nominal system (S). $FI_{\Delta 20}$ is calculated to be 0.13 at V_g of 36 V and 0.3 at V_g of 115 V. This makes our designed controller robust nonfragile across its operating range, which is sufficient to obtain robust performance against process variations.

D. VOLTAGE CLAMPS AND SR FLIP-FLOP

The complete block diagram of the developed controller chip, interfacing an external buck converter, is shown in Fig. 15. Two voltage-clamps are used to isolate HV from LV circuitry by limiting the propagating signal to 3.3 V. One clamp is placed at the VFB side (right) and the other is placed at the IVFF side (left). Both clamps are composed of ESD diodes that can clamp a voltage up to 80 V. A dual-input analog MUX is used to define two modes of operation: the feedback-only mode (FB) utilizes an external fixed-peak sawtooth signal V_{ramp}, while the combined feedforward-feedback mode (FF-FB) utilizes the on-chip generated variable-peak sawtooth signal V_{saw}. This structure allows us to compare the performance of the proposed controller in its ability to improve

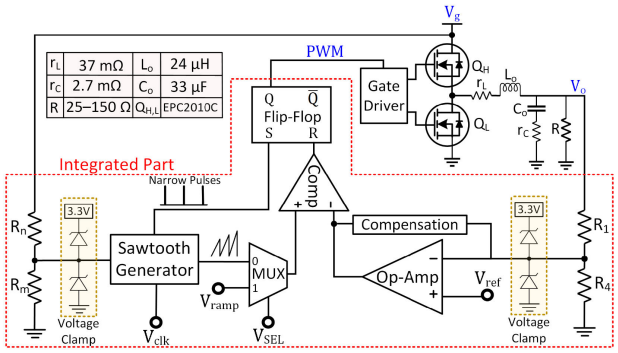


FIGURE 15. Block diagram of the controller chip interfacing an external buck converter power-stage.

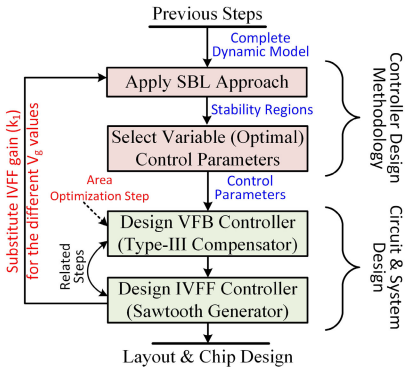


FIGURE 16. Flowchart relating the controller design to circuit design.

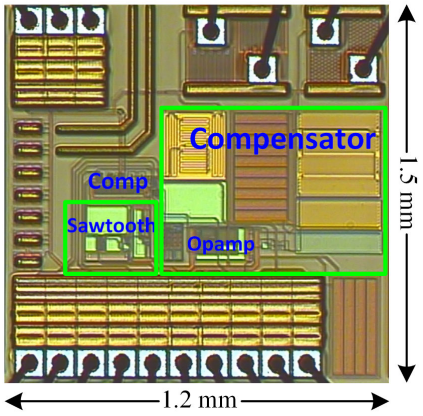


FIGURE 17. Micrograph of the fabricated die (1.2 mm x 1.5 mm) combining VFB and IVFF controllers.

transient immunity to line variations against the use of a standalone VFB.

The start of the PWM signal duty-cycle is defined by setting an SR flipflop using the narrow pulses from the sawtooth generator block. Afterwards, the sawtooth signal is compared to the slow-moving control signal V_c. When the former exceeds the latter, the comparator resets the flipflop to define the duty-cycle's end. The flipflop ensures that there is only one pair of set-reset events per switching cycle [52]. Consequently, the modulator cannot change the PWM signal state until the onset of the following clock pulse, which increases the modulator's noise immunity to avoid jitter and instability.

E. REMARKS ON CONTROLLER AND CIRCUIT DESIGN

To address the stability issues that arise from integrating VFB and IVFF, the controller design methodology proposed in Section III must consider the inherent nonlinearities of the IVFF implementation presented in Section IV. Figure 16 provides a flowchart illustrating the relation between the controller and the circuit design processes and showing the steps taken to ensure a stable and reliable controller design. Assuming the closed-loop system's dynamic model is complete, the SBL approach is applied to identify stability regions within which the optimal (variable) control parameters are selected. It is crucial that this step incorporates the variable IVFF gain (k_1) determined by the sawtooth circuit implementation, which impact the shape of the generated stability regions. As shown in Fig.16, the IVFF and VFB designs proceed concurrently, given that the IVFF design plays a role in the selection of the control parameters critical for constructing the type-III compensator (VFB core).

V. EXPERIMENTAL RESULTS AND DISCUSSION

The proposed combined controller was fabricated in a HV 0.35-μm CMOS process. The micrograph of the integrated chip is shown in Fig. 17. The total chip area, including the IO PADs, is 1.8 mm^2, while the core area of the controller circuit, including the passive components, is 0.438 mm^2. The controller chip is set up for the regulation of a DC-DC buck converter whose parameters are summarized in Table 1. In the reported experiments, the V_g signal experiences line variations between 36 V and 115 V in 1 ms transitions, as illustrated in Fig 1. The converter's switching frequency is maintained at 1 MHz.

The experimental setup adopted to test and characterize the performance of the fabricated chip is shown in Fig. 18. The EPC9003C board represents the open-loop power-stage carrying a gate driver, a half-bridge made of two e-GaN power transistors of type EPC2010C, and a low-pass filter comprising C_o and L_o. Three parallel capacitors are used to implement C_o to reduce the effective r_C, and the output voltage ripple, while handling higher output currents at low losses. The fabricated chip is wire-bonded to a DIP package that is assembled on a custom designed PCB. The Chroma programmable AC power source 61501 is used to generate the required line variations. The DC electronic load EL34243A is used to obtain the desired loads ranging from 25 Ω to 200 Ω and to apply the load variations test as well. To characterize the full performance of the proposed controller, we present measurements of the system's transient response to line variations (Fig. 19 and Fig. 20) and load variations (Fig. 24), the system's start-up response (Fig. 22), the steady-state line and load regulation, and the system's power efficiency (Fig. 27).

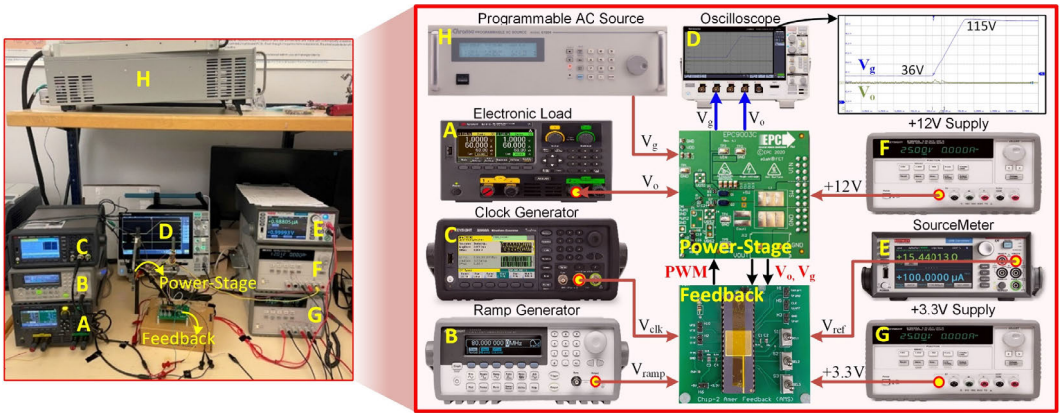


FIGURE 18. Experimental setup to evaluate the combined controller prototype chip within a DC-DC buck converter system. It highlights the EPC9003C board used as a power-stage, the designed PCB carrying the controller chip, and the equipment used in the reported experiments.

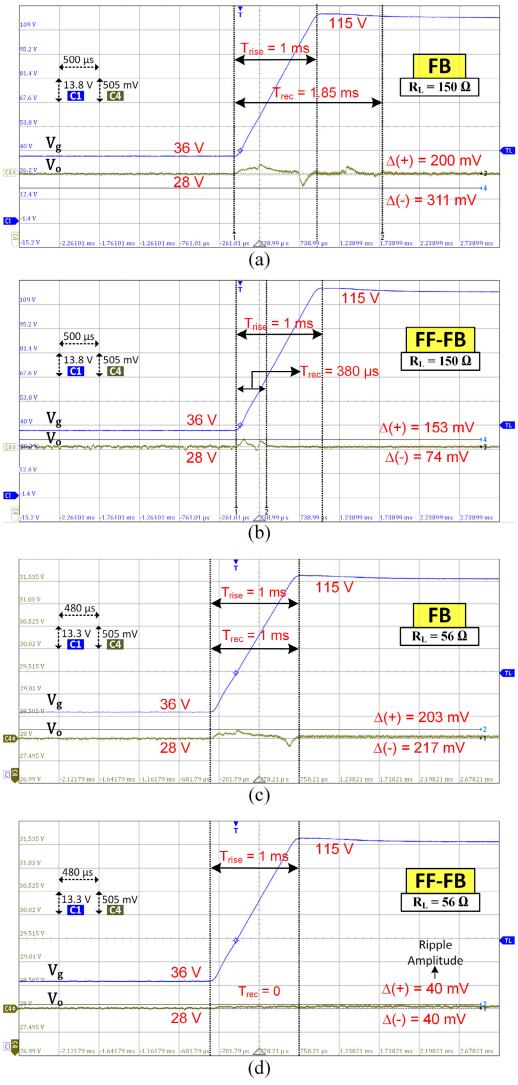


FIGURE 19. Closed-loop V_o response to 1 ms rising transition of V_g from 36 V to 115 V at $R_L = 150\ \Omega$: (a) with FB and (b) with FF-FB, and at $R_L = 56\ \Omega$: (c) with FB and (d) with FF-FB.

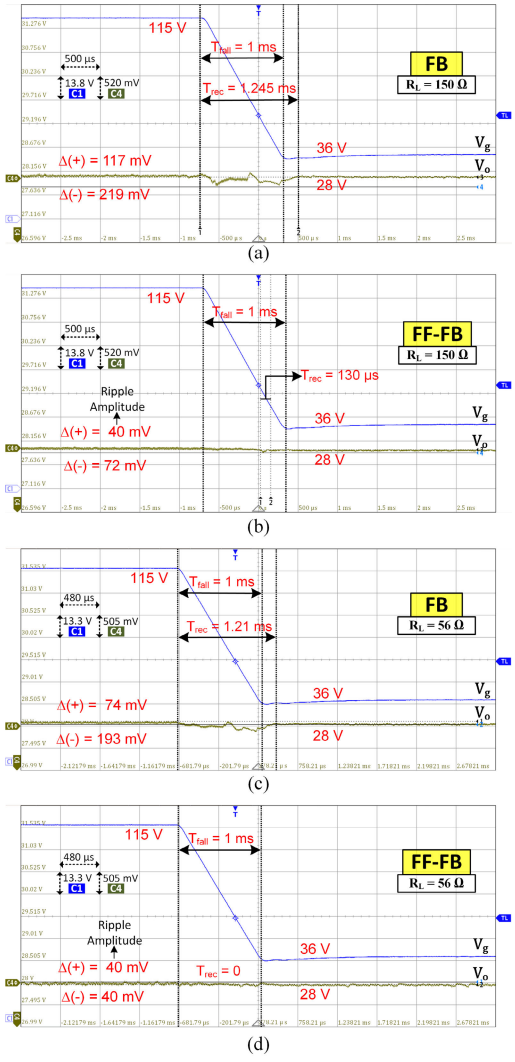


FIGURE 20. Closed-loop V_o response to 1 ms falling transition of V_g from 115 V to 36 V at $R_L = 150\ \Omega$: (a) with FB and (b) with FF-FB, and at $R_L = 56\ \Omega$: (c) with FB and (d) with FF-FB.

To test the transient immunity of the combined controller against line variations, the closed-loop V_o response was measured during 1 ms rising and falling V_g transitions (36 V $\leftrightarrow$ 115 V). The measurements were performed at various loads

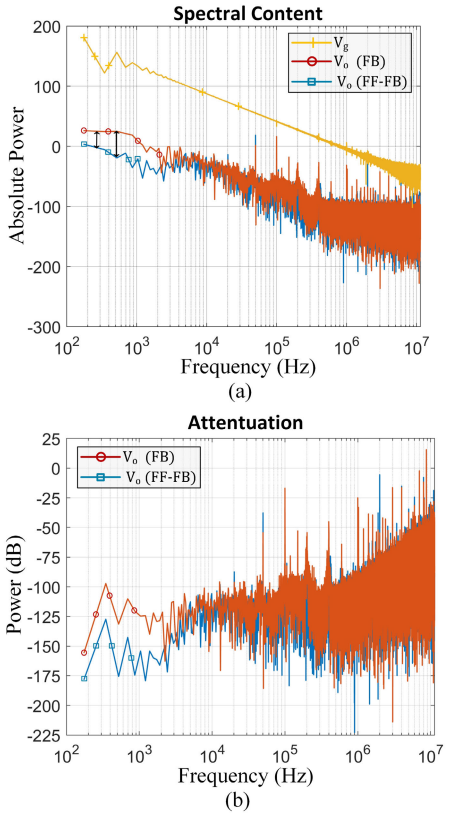


FIGURE 21. (a) Absolute spectral power of the V_g and V_o signals from Fig. 19(c, d). (b) The frequency attenuation achieved at V_o with respect to V_g using both controller modes: FB and FF-FB.

(R_L = 150 Ω, 75 Ω, and 56 Ω) in two operating modes: using only feedback (FB) and using the combined controller (FF-FB). Figure 19 captures the results during the rising transition of V_g. In FB mode, V_o displayed voltage spikes up to ±311 mV from the 28 V baseline and long recovery times (T_{rec}) up to 1.85 ms, as shown in Fig. 19(a, c). Conversely, FF-FB mode resulted in notably reduced or no spikes and very short T_{rec} down to zero, as shown in Fig. 19(b, d). Figure 20 captures the results during the falling transition of V_g. In FB mode, V_o displayed spikes up to ±219 mV and long T_{rec} up to 1.355 ms, as shown in Fig. 20(a, c). Conversely, FF-FB mode resulted in very small or no spikes and very short T_{rec} down to zero, as shown in Fig. 20(b, d). Overall, FF-FB mode achieved superior transient immunity against line variations by either significantly reducing the voltage spikes amplitude and the recovery time or by entirely eliminating all spikes. It should be noted that the spikes that were considered eliminated had an amplitude as large as the output ripple voltage amplitude (∼ 40 mV).

Due to the lack of the necessary tools, performing direct frequency domain measurements was challenging. Hence, to provide insights into the system's frequency characteristics, we adopted an indirect approach. The closed-loop V_o responses for the rising transition of V_g at R_L = 56 Ω, shown in Fig. 19(c, d), were sampled and extracted for further analysis in the frequency domain. The MATLAB®'s

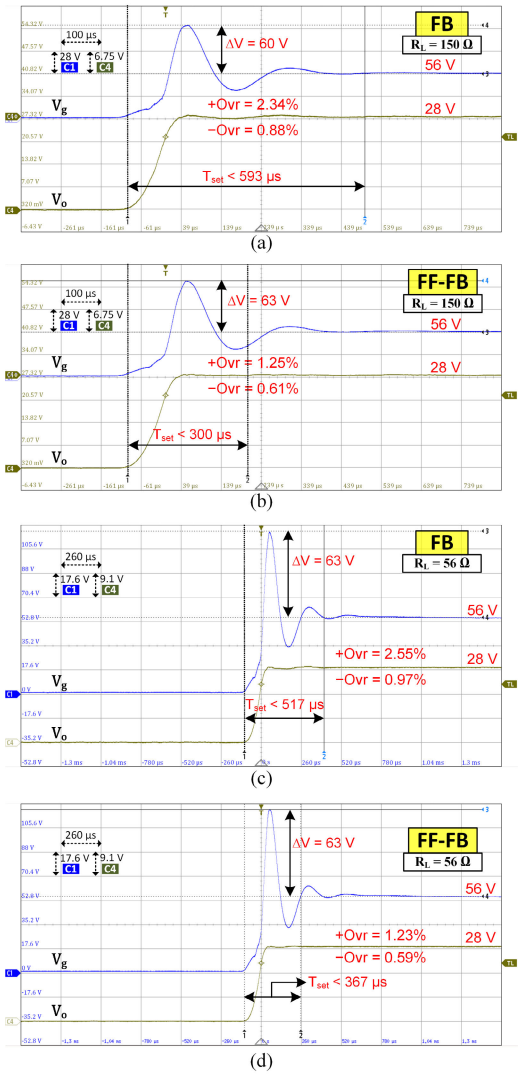


FIGURE 22. Closed-loop V_o startup response for V_g of 56 V at R_L = 150 Ω (a) with FB and (b) with FF-FB, and at R_L = 56 Ω (c) with FB and (d) with FF-FB.

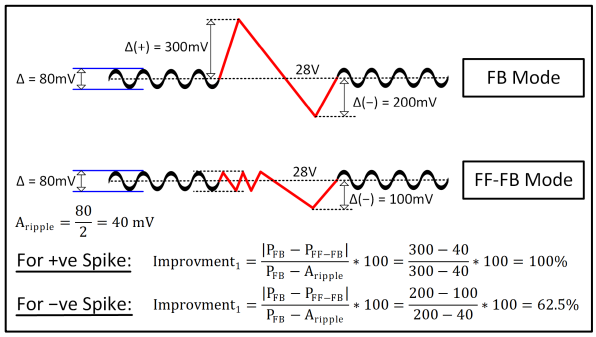


FIGURE 23. Example of improvement calculation for ±ve spikes using the formula in (31) for existing ripple voltage in both features.

spectral analysis tool is used to quantify the frequency content inherent in each signal. This tool uses the Discrete Fourier Transform to convert time-series waveforms into their frequency counterparts. Figure 21(a) shows the absolute spectral

TABLE 2. Summary of the improvement in transient response achieved by using the combined controller.

Response Type	Rising Transition		Falling Transition		Startup	
R_L = 150 Ω						
Measurement Type	FB / FF-FB	Improvement	FB / FF-FB	Improvement	FB / FF-FB	Improvement
Overshoot (+ve Spike)	(200 / 153) mV	29.4 %(1)	(117 / 40) mV	100 %(1)	(2.34 / 1.25) %	46.6 %(2)
Undershoot (−ve Spike)	(311 / 74) mV	87.5 %(1)	(219 / 72) mV	82.1 %(1)	(0.88 / 0.61) %	30.7 %(2)
Recovery (Settling) Time	(1.85 / 0.38) ms	79.5 %(2)	(1.245 / 0.13) ms	89.6 %(2)	(593 / 300) µs	49.4 %(2)
R_L = 75 Ω						
Measurement Type	FB / FF-FB	Improvement	FB / FF-FB	Improvement	FB / FF-FB	Improvement
Overshoot (+ve Spike)	(230 / 40) mV	100 %(1)	(169 / 40) mV	100 %(1)	(1.9 / 1.22) %	35.8 %(2)
Undershoot (−ve Spike)	(319 / 40) mV	100 %(1)	(200 / 60) mV	87.5 %(1)	(0.76 / 0.41) %	46.1 %(2)
Recovery (Settling) Time	(1.825 / 0) ms	100 %(2)	(1.355 / 0.09) ms	93.4 %(2)	(528 / 289) µs	45.3 %(2)
R_L = 56 Ω						
Measurement Type	FB / FF-FB	Improvement	FB / FF-FB	Improvement	FB / FF-FB	Improvement
Overshoot (+ve Spike)	(203 / 40) mV	100 %(1)	(74 / 40) mV	100 %(1)	(2.55 / 1.23) %	51.8 %(2)
Undershoot (−ve Spike)	(217 / 40) mV	100 %(1)	(193 / 40) mV	100 %(1)	(0.97 / 0.59) %	37.1 %(2)
Recovery (Settling) Time	(1 / 0) ms	100 %(2)	(1.21 / 0) ms	100 %(2)	(517 / 367) µs	39.2 %(2)

(1) Calculated using the formula in (31), (2) Calculated using the formula in (32)

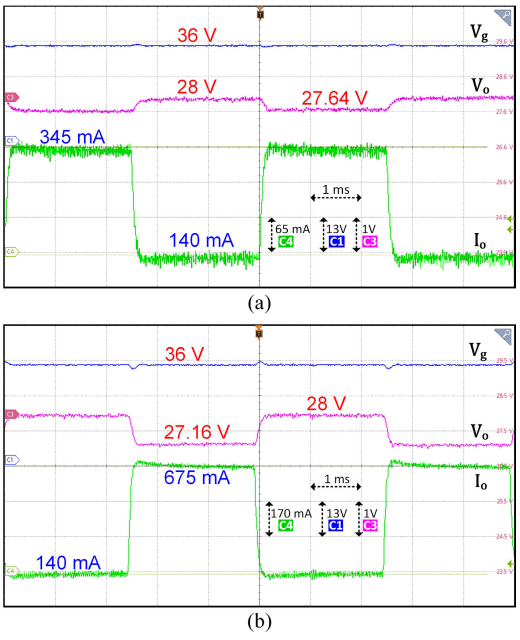


FIGURE 24. Closed-loop V_o response as R_L undergoes 150 μs transitions: (a) 200 Ω ↔ 80 Ω and (b) 200 Ω ↔ 40 Ω.

power content of the V_g and V_o signals. It indicates that during the FF-FB mode of operation, frequencies near DC were attenuated by 25 dB to 50 dB more than when using the FB mode. The attenuation of the different input frequencies achieved by both controllers is plotted with respect to V_g in Fig. 21(b), emphasizing the improved immunity to line variations achieved by FF-FB mode.

The closed-loop V_o startup response was also measured with V_g set to 56 V at various loads (R_L = 150 Ω, 75 Ω, and 56 Ω). Figure 22 shows the measurement results for the startup response for both FB and FF-FB modes. In FB mode, V_o had an overshoot (+Ovr) as high as 2.55% and an undershoot (−Ovr) as low as 0.97% from the 28 V baseline with a settling time (T_{set}) up to 593 μs, as shown in Fig. 22(a, c). In FF-FB mode, V_o had a reduced +Ovr (< 1.25%) and −Ovr (< 0.61%) with T_{set} < 367 μs at different R_L as shown in Fig. 22(b, d). Clearly, the system achieved better startup response with reduced +Ovr, −Ovr, and T_{set} at the different loads while operating in FF-FB mode. It is notable also that the performance of both modes was very good in terms of the fast, almost critically damped, startup regardless of the big +Ovr (∼ 63 V) and −Ovr (∼22 V) in V_g.

To quantify the improvement achieved by operating in the FF-FB mode over the FB mode, the different features (+Ovr, −Ovr, T_{set}, ±ve spikes, T_{rec}) of the measured transient responses for both modes were extracted and summarized in Table 2. Afterwards, the improvement for the ±ve spike features of both falling and rising transitions is calculated using (31), where P_{FB} is a feature of a FB mode response, P_{FF-FB} is the same feature of an FF-FB mode response, and A^{+}_{ripple} is the measured amplitude of the ripple voltage (∼ 40 mV). The improvement for the rest of the features is calculated using (32). In (31), the term A^{+}_{ripple} is subtracted in the denominator as it represents a common value found in both P_{FB} and P_{FF-FB}. Figure 23 shows an example of calculating the improvement using the formula in (31) for clarification. The calculated improvements at the different loads (R_L = 150 Ω, 75 Ω, and 56 Ω) are summarized in Table 2 as well. The FF-FB mode shows up to 100% improvement in most of the cases compared to the FB mode.

$$\text{Improvement}_1 = \frac{|P_{FB} - P_{FF-FB}|}{P_{FB} - A^{+}_{ripple}} \text{x}100\% \quad (31)$$

$$\text{Improvement}_2 = \frac{|P_{FB} - P_{FF-FB}|}{P_{FB}} \text{x}100\% \quad (32)$$

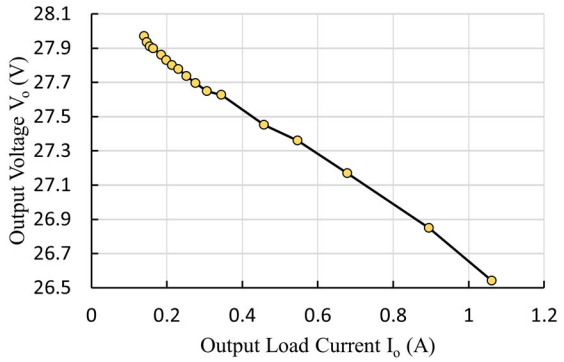


FIGURE 25. Closed-loop steady-state measurement of V_o versus I_o at nominal $V_g = 36$ V.

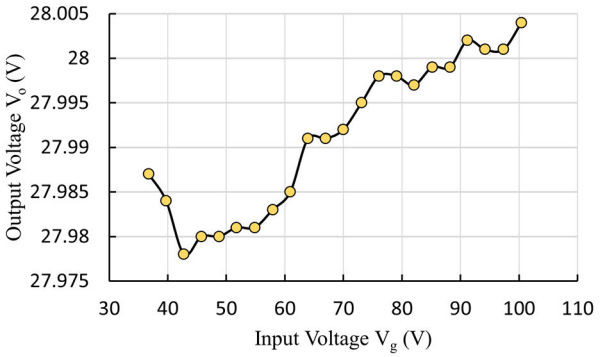


FIGURE 26. Closed-loop steady-state measurement of V_o versus V_g at nominal $R_L = 56$ Ω.

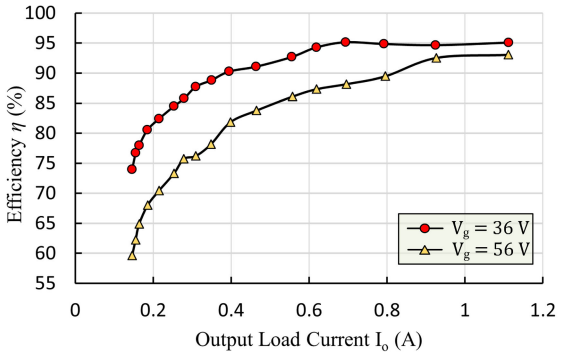


FIGURE 27. Measured closed-loop system efficiency at $V_g = 36$ V and $V_g = 56$ V across the required I_o range (140 mA - 1.1 A).

The closed-loop V_o transient response was also tested against load variations taking place in 150 μs transitions with V_g set to 36 V. Figure 24(a) shows that V_o changed by 0.36 V during a (200 Ω ↔ 80 Ω) load variation which corresponds to a 205 mA change in I_o. While Fig. 24(b) shows that V_o changed by 0.84 V during a (200 Ω ↔ 40 Ω) load variation which corresponds to a 535 mA change in I_o. Clearly, the closed-loop system was stable during the load variations test, and it eliminated any ±ve spikes in V_o. The change in V_o reflects the steady-state load regulation performance of the system which is further characterized in Fig. 25.

To characterize the steady-state load regulation of the closed-loop system, V_o is measured at different values of I_o ranging from 140 mA to 1.1 A (i.e., $R_L = 200$ Ω to 25 Ω) at fixed V_g of 36 V, as shown in Fig. 25. The change in V_o is $\Delta V_o = 27.97 - 26.54 = 1.43$ V, which corresponds to a change in R_L from 200 Ω to 25 Ω. Thus, the steady-state load regulation is calculated based on (33) [12], and is equal to 4.98%, where $V_{o-nominal}$ is the nominal output voltage (28 V). This change in V_o can be avoided by changing V_{ref}, according to the load value, to put V_o back at 28 V.

$$\text{Load Regulation (\%)} = \frac{\Delta V_o}{V_{o-nominal}} \text{x} 100\% \qquad (33)$$

To characterize the steady-state line regulation of the closed-loop system, V_o is measured at different values of V_g ranging from 36 V to 100 V at $R_L = 56$ Ω (i.e., at $I_o = 0.5$ A), as shown in Fig. 26. It is observed that the value of V_o decreases first and then increases as the value of V_g increases. The maximum change found in the output voltage is $\Delta V_o = 28.004 - 27.978 = 0.026$ V, while the maximum change found in V_g is $\Delta V_g = 100 - 36 = 64$ V. Therefore, the steady-state line regulation per 1 V change of V_g is calculated based on (34) [12], and is equal to 0.00146 %/V.

$$\text{Line Regulation(\%/V)} = \frac{\Delta V_o}{V_{o-nominal}} \text{x} \frac{1}{\Delta V_g} \text{x} 100\%/\text{V} \quad (34)$$

The efficiency of the closed-loop system (η) is evaluated at different V_g values (36 V and 56 V) across the required range of I_o from 140 mA to 1.1 A, corresponding to R_L values from 200 Ω to 25 Ω, and depicted in Fig. 27. A peak η of 95.143% is achieved at V_g of 36 V and I_o of 695 mA. However, η degrades as V_g increases. The main source of this efficiency drop is the Miller coupling via the gate-drain capacitance of the e-GaN power transistors (Q_H, Q_L) in the half-bridge. This coupling causes peak currents into the power transistor's gate, increasing the risk of partial unintended turn-on due to the employed unipolar gate driving scheme. This results in small shoot-through currents diminishing the efficiency [53]. Such issue can be addressed by adopting bipolar or three-level gate driving architectures, as reported in [54].

Finally, the performance of the buck converter system is summarized and compared with similar works in literature in Table 3. This table starts by listing the system design parameters (V_g, V_o, F_{sw}, R_L) and the type of control used. In [55], CFB control is used, while both [41] and [56] use VFB control. Although [41] introduces a new compensator to reduce the integration area, our proposed controller's area is comparable thanks to the area-optimization step performed. Afterwards, the table shows the transient and steady-state performances summary. Our system stands out with a robust transient response, experiencing no spikes during step changes in R_L or V_g. However, the steady-state load regulation is slightly higher due to the IR drop in the electronic load wiring, which probably affects the actual V_o value seen by the VFB. Overall, our system performs well,

TABLE 3. Summary of buck converter and controller performance.

Reference	[55]	[41]	[56]	This Work
Technology	FPGA	0.35	0.25 HV	0.35 HV
Controller	CFB	VFB	VFB	VFB + IVFF
F_{sw} (MHz)	0.2	1	0.5	1
V_g (V)	33 - 55	3.6	9 - 21	**36 - 115**
V_o (V)	28	2.5	6	28
R_L (Ω)	10 - 1000	2.5 - 50	30 - 300	25 - 200
Core Area (mm^2)	N/A	0.38[(A)]	1.22[(A)]	**0.438**
Phase Margin[(B)]	60°	65°	76°	72.7°
Bandwidth (kHz)	N/A	200	N/A	100
Line Reg.[(C)(D)] (mV/V)	1.14[(A)] @ 2.8A	12 @ 500mA	5.4 @ 500mA	0.406 @ 500mA
Load Reg.[(B)(E)] (%)	0.25[(A)]	0.4	0.3	4.98
Line Transient[(C)] (V) ± Spike (mV) T_{rec} (µs)	33 ↔ 55 ± 240 2500[(A)]	N/A	N/A	**36 ↔ 115** **± 1**[(F)] **1**[(F)]
Load Transient[(B)](mA) ± Spike (mV) T_{rec} (µs)	Δ = ± 1400 ± 280 1500	Δ = ± 950 ± 48 80 - 85	Δ = ± 980 ± 250 26 - 30	**Δ = ± 535** **± 1**[(F)] **1**[(F)]
Peak Efficiency (%)	N/A	94 @ 500mA	86.4 @ 500mA	**95.143 @ 659mA**
FOM	N/A	0.63	3.30	**57.48**

[(A)] Estimated value, [(B)] At nominal V_g, [(C)] At nominal R_L, [(D)] Law = $\Delta V_o/\Delta V_g$, [(E)] Law = $\Delta V_o/V_{o-nominal} * 100$, [(F)] Value is set to 1 as no ±ve spikes are detected.

achieving the highest figure of merit (FOM) when compared to other works, according to (35). The used FOM considers the different system performance metrics in a way where higher values indicate better overall performance.

$$FOM = \frac{\text{(Peak Efficiency) (Step Load Change)}}{\text{(Line Reg.) (Load Reg.) } (T_{rec} x F_{sw}) \text{ (Core Area)}} \quad (35)$$

VI. CONCLUSION

In this paper, we introduced a systematic method to merge and integrate input-voltage feedforward (IVFF) and voltage-mode feedback (VFB) controllers. This method effectively addresses the closed-loop dynamic challenges and stability issues stemming from such combination. It uses the stability boundary locus technique to analyze the impact of the IVFF gain variations on system stability. This analysis guides the selection of the VFB control parameters, ensuring robust controller performance even when conventional sawtooth generators are used. Our comprehensive approach not only handles the controller design but also optimizes the passive components comprising the type-III compensator, achieving full integration while minimizing the Silicon area footprint. Furthermore, the designed controller was proved to be robust and non-fragile against process variations. Our controller prototype, fabricated using the AMS 0.35-μm technology, was tested while regulating a synchronous DC-DC buck converter, showing excellent transient immunity to overvoltage surges of up to 115 V (80 V/ms) and abrupt load variations of up to 535 mA/150μs across a wide range of loads (25 Ω ↔ 150 Ω). Comparative tests between our combined controller and a standalone VFB revealed a significant improvement in transient performance reaching up to 100% (complete suppression of unwanted transients).

As a future work, uncertainty in the DC-DC converter's components will be considered to design more robust controllers. In addition, we plan to extend the design method for higher-order DC-DC converters to handle input supply spikes or surges above or under the nominal output value. Moreover, incorporating an integrated three-level gate driver is a planned step to optimize the driving process of the e-GaN power transistors.

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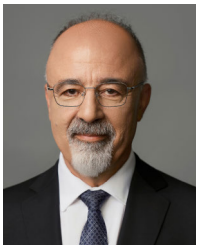

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