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RESEARCH ARTICLE

Benchmarking of Multi-Bridge-Channel FETs Toward Analog and Mixed-Mode Circuit Applications

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ABSTRACT In this study, for the very first time developing of n- and p-type 3-D single-channel (SC) FinFET and gate-all-around (GAA) Multi-Bridge-Channel FETs (MBCFET) like nanowire FET (NWFET) and nanosheet FET (NSFET) are benchmarked towards device and circuit levels which are emulated with International Road map for Devices and Systems (IRDS) for sub-5-nm technology nodes. Compared to the FinFET, the MBCFETs exhibits higher ON-current (I_{ON}), switching ratio (I_{ON}/I_{OFF}), lower subthreshold-swing (SS) and drain-induced barrier lowering (DIBL). Except for extended parasitic capacitances (C_{para}), our benchmarking results show that the NWFET and NSFET achieve the high-performance (HP) and low-power (LP) goals of IRDS. Furthermore, the NSFET delivers superior performance towards DC and analog/RF metrics. The cut-off frequency (f_T) and gain bandwidth product (GBW) are higher (because of high I_{ON}) in the case of NSFET, even though the capacitive effect is significant. Further, the logic circuit applications like CMOS inverter and ring oscillator (RO) circuits are analyzed and compared in detail. The CMOS inverters propagation delays (τ_p) is reduced to 31% from FinFET to NWFET and 12% from NWFET to NSFETs is noticed. Also, the NWFET and NSFET based ROs offer 39% and 56% high oscillation frequency (f_{osc}) compared to that of FinFET counterpart. Finally, the single stage current mirror performance and operational transconductance amplifiers (OTA) gain and common mode rejection ratio (CMRR) are carried out towards analog and mixed-mode circuit applications.

INDEX TERMS CMRR, CMOS inverter, IRDS, GAAFET, operational transconductance amplifier (OTA), ring oscillator.

I. INTRODUCTION

The FinFET became the promising architecture at sub-22-nm nodes as it offered robust gate control over the channel and enabled scaling to the 7-nm technology node. Also, the FinFET played a remarkable role in high-performance (HP) applications. The FinFETs are still being used and more prominently used at the 7-nm technology node, as per the foundry publications (N7) [1], [2]. However, it is shown that the FinFET is incapable of downscaling further as it became challenging to maintain the device's electrostatic control in future technology nodes. To maintain good electrostatics, a thinner fin is necessary. However, this reduces carrier mobility and causes threshold voltage (V_{th}) fluctuation [3], [4], [5]. The GAA Multi-Bridge-Channel FET (MBCFET) [4] like nanowire FET and nanosheet

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FET (NSFET) architectures emerged as potential candidates for sub-5-nm nodes to improve the performance [6], [7], [8], [9], [10], [11]. Therefore, physically based 3D simulations are essential for assessing the performance of these devices. The GAA NWFET exhibits superior electrostatic integrity at sub-5-nm nodes. However, due to the reduced channel area, the drive current is limited in NWFET and restricts its usage for HP applications. In 2017, IBM proposed the construction of stacked NSFETs, which outperformed FinFETs and stacked NWFETs [12]. For a given active width, NSFETs may have a smaller parasitic capacitance, resulting in a better C_{eff}–I_{eff} relationship. Hence, for scaling sub-5-nm technology nodes, NSFET emerged as a viable contender [12]. Meanwhile, silicon (Si) NSFET has been established to improve effective channel widths (W_{eff}) for higher current drivability while ensuring optimum electrostatics through gate-all-around (GAA) architecture. Moreover, NSFET modulates the drive current by varying NS width, which allows CMOS layout compatibility designs [13]. Although some works compared FinFET, NW and NSFET with a single channel [14], three-channel [15], [16], four-channel [17], two-channel (Bulk and SOI) [18], [19], however very few have compared FinFET, nanowire and two-channel SOI NSFET with equal effective widths (i.e., same area or equal footprint) for sub-5-nm nodes towards IRDS goals in the literature for both p- and n-type FETs. In GAA FETs with multiple vertically stacked silicon NWFET and NSFET, the desired performance in DC, analog, and RF applications can be achieved [14], [15]. Although three, four, five and more channel NSFETs have larger I_{ON} than the FinFETs, due to their larger effective width (W_{eff}), it will degrade the gate capacitance (C_{gg}), overlap, and outer-fringing capacitances arising from more channels [20]. Thus, in the proposed design, two-channel NSFET is focused for sub-5-nm nodes. Moreover, GAA NSFETs is a transition step between FinFET and NWFET designs because of their higher performance and adaptive minimal fabrication technique [16]. Additionally, NSFETs have also been developed to improve the W_{eff} of channels, enabling larger current drivability under an equal footprint while retaining good electrostatics [17], [18], [19]. The NSFET's broader design compared to the NW enables better transistor performance at higher power levels. [20].

Several works devoted to study the performance of FinFET, NW and NSFETs like I-V characteristics of bulk [21] and SOI [22], [23] FinFET, NW, and NSFET architectures. However, the p- and n-type FETs benchmark comparison by keeping in view of 2025 International Roadmap for Devices and Systems (IRDS) goals [24] towards DC and analog/RF performance needs to be explored in detail for sub-2-nm nodes. Thus, in this study, both p- and n-type FETs are designed for FinFET, NW and NSFET architectures with equal W_{eff}. Moreover, to analyze analog and mixed-mode circuit behavior of emerging FETs at sub-5-nm technology nodes we show the CMOS inverter propagation delay (τ), switching current (I_{SC}), energy-delay product (EDP), power-delay product (PDP) and the ring oscillator (RO) frequency of oscillation (f_{OSC}) performance for the first time. The manuscript is constructed as follows: The device dimensions and physical models are demonstrated in section II. In section III, DC and analog/RF FOMs comparison is performed for FinFET, NWFET, and NSFET. Section IV describes the circuit level comparison of FinFET, NW and NSFETs and benchmarking with IRDS. Section V describes the conclusion of the results and performances.

TABLE 1. Device parameters.

Device Parameter	FinFET	NWFET	NSFET
Gate Length (L_{G})	16 nm	16 nm	16 nm
F_{W}/NW_{W}/NS_{W}	6 nm	7 nm	10 nm
Channel height (F_{H}/NW_{T}/NS_{T})	27 nm	8 nm	5 nm
EOT	0.78 nm	0.78 nm	0.78 nm
Spacer dielectric	Nitride	Nitride	Nitride
Source/drain Length (L)	12 nm	12 nm	12 nm
Length of underlap spacer	5 nm	5 nm	5 nm
Source/drain doping	2×10^{19} cm^{-3}	2×10^{19} cm^{-3}	2×10^{19} cm^{-3}
Channel doping	1×10^{15} cm^{-3}	1×10^{15} cm^{-3}	1×10^{15} cm^{-3}
Effective Width (W_{eff})	60 nm	60 nm	60 nm
Gate work function	4.685 eV	4.47 eV	4.456 eV

II. DEVICE STRUCTURE AND SUMULATION METHODOLOGY

All the results of FinFET, NWFET and NSFET are simulated through the Cogenda Visual TCAD simulator 25. Table. 1 lists the device characteristics and dimensions that were employed in the simulations. A gate length of 16 nm is predicted to fall under sub-5-nm technology node range by IRDS 2025 [24] targets. For FinFET a channel height of 27 nm and fin width of 6 nm is chosen, which cannot be scaled beyond 7-nm-node due to severe fin bending issues [18]. An optimized width of 6 nm for FinFET and 7 nm width for NWFET are considered towards larger saturation currents [18]. For NSFET an optimized height of 5 nm and 10 nm width is considered accordance with [7]. For a better comparison an equal V_{th} of 275 mV is maintained, near to IRDS 2025 target (∼212 mV) by tuning gate work function. The effective widths (W_{eff}) of p- and n-type of FinFET ($W_{\text{eff}} = 2\text{F}_{\text{H}}+\text{F}_{\text{W}}$), NWFET ($W_{\text{eff}} = 2\times(2\text{NW}_{\text{W}}+2\text{NW}_{\text{H}})$) and NSFETs ($W_{\text{eff}} = 2\times(2\text{NS}_{\text{W}}+2\text{NS}_{\text{H}})$) [26] are maintained equal of 60 nm. All the structures are maintained an EOT of 0.78 nm with a high-k gate stack combination with SiO_2 and HfO_2. The doping of 2×10^{19} cm^{-3} in source and drain and 1×10^{15} cm^{-3} for the channel is considered for both n and p-type FETs.

An equal metal gate height of 60 nm is taken for FinFET, NW, and NSFETs. The spacers are fundamental to improve the subthreshold performance and are a prerequisite for sub-10-nm devices [26]. Due to the closer proximity of the source and drain contacts in the sub-20-nm region, the electrical behaviour of FETs starts to deteriorate. With higher DIBL, the gate has inadequate control on the channel region,

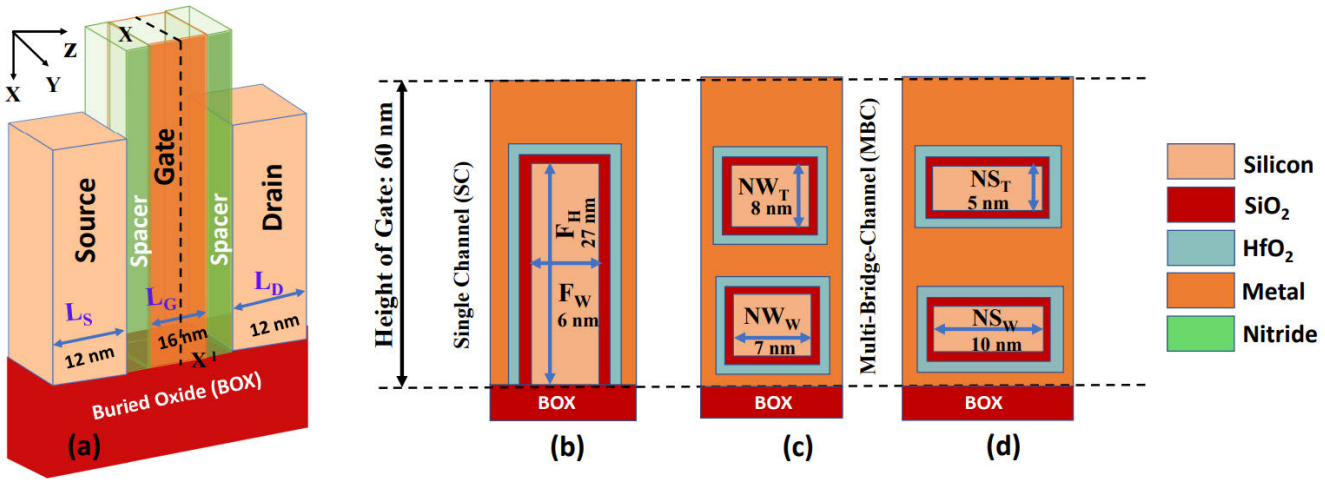

FIGURE 1. (a) 3-D schematic and 2-D cut views of (b) FinFET (c) NWFET and (d) NSFET (MBCFET).

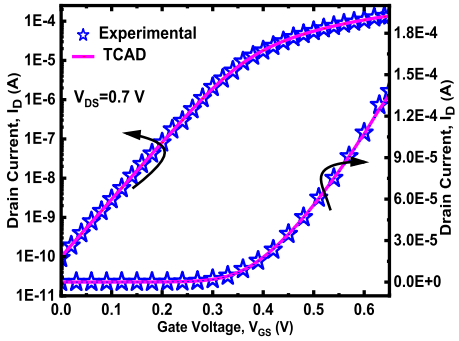

FIGURE 2. The calibration of TCAD simulation models with the experimental results of NSFET (MBCFET).

resulting in higher I_{OFF}, lower I_{ON}, lower I_{ON}/I_{OFF}, and SS deterioration [26]. The proposed FinFET, NWFET and NSFETs are maintained with nitride spacer to mitigate series resistance and parasitic capacitance effects [26]. The simulation of a 3D quantum-mechanically corrected device is carried out in detail by solving a series of density-gradient drift-diffusion equations. To account for carriers' lifetime and current densities, the Auger model is invoked. To consider generation and recombination effects, Shockley-Read-Hall models are incorporated. To account for bandgap narrowing effects due to heavy doping, Schenk's model and for velocity saturation effects, Caughey-Thomas models are involved. All the device parameters are initially validated through the non-equilibrium Greens function approach. To consider interface mobility degradation phenomena, the thin-layer mobility model is invoked. Fig. 2 depicts the calibration of transfer characteristics of the MBC GAA NSFET with the Visual TCAD simulation approach [27]. In addition, the NWFET is well also well calibrated with experimental results of [5] and shown in our recent works [3]. For gate and drain voltages, the simulated I_D–V_{GS} curve shows a good match with the experiment results. This demonstration ensures that the simulation analysis effectively captures the NSFETs short channel physics.

III. RESULT ANALYSIS AND DISCUSSION

Fig. 3(a)-(c) show the I_D-V_{GS} characteristics of FinFET, NW, and NSFET in log and linear scale at $|V_{DS}| = 0.7$ V and $|V_{DS}| = 0.05$ V for both n- and p-type FETs. For a fair comparison, the V_{th} of FinFET, NWFET and NSFETs are matched by modifying the gate work function. Fig 3(d)-(f) show the I_D-V_{DS} characteristics of FinFET, NW, and NSFET at various V_{GS}. The NSFET exhibits the highest output characteristics, followed by NWFET and FinFET.

A comparison of I_{ON}, I_{OFF}, I_{ON}/I_{OFF} for p and n-type FinFET, NWFET, and NSFETs are depicted in Fig. 4. The I_{ON} is extracted at $V_{DS} = V_{GS} = 0.7$ V for n-type FETs and $V_{DS} = V_{GS} = -0.7$ V for p-type FETs. Figure 4(a) shows that n-type NWFET and NSFET exhibit higher modulation in I_{ON} compared to FinFET. The I_{ON} of 0.482 mA/μm, 2.6 mA/μm, and 2.9 mA/μm with n-type FETs and 0.435 mA/μm, 2.03 mA/μm, and 2.32 mA/μm with p-type FETs are noticed with FinFET, NWFET, and NSFETs respectively. Moreover, compared to p-type FETs, the n-type FETs exhibit better I_{ON} due to better electron mobility. The NWFET exhibits a rise in I_{ON} of 5.39× with n-type and 4.6× with p-type compared to FinFET. Moreover, from NWFET to NSFET, a marginal rise in I_{ON} of 1.1× with n-type and 1.14× with p-type is observed. Both NW and NSFETs exhibit better I_{ON} compared to IRDS HP requirements. Furthermore, the FinFET, NWFET, and NSFETs show better performance compared to IRDS LP requirements. Figure 4(b) shows the I_{OFF} with p- and n-type FinFET, NW, and NSFETs. The I_{OFF} of 37.3 pA/μm, 34 pA/μm, and 31.5 pA/μm with n-type FETs and 109 pA/μm, 36.5 pA/μm, 33.3 pA/μm with p-type FETs is noticed. The variation in I_{OFF} is higher for FinFET compared to NWFET and NSFETs due to trigate nature. Moreover, higher gate drain induced drain leakage for p-type FETs at low V_{GS} is due to higher junction gradient of boron penetrating/diffusing into FinFET, NWFET and NSFET channels [13]. A fall of 1.09× with p-type and 2.98× with n-type is noticed from FinFET to NW. Furthermore, 1.07× with n-type and 1.09× p-type from NW to

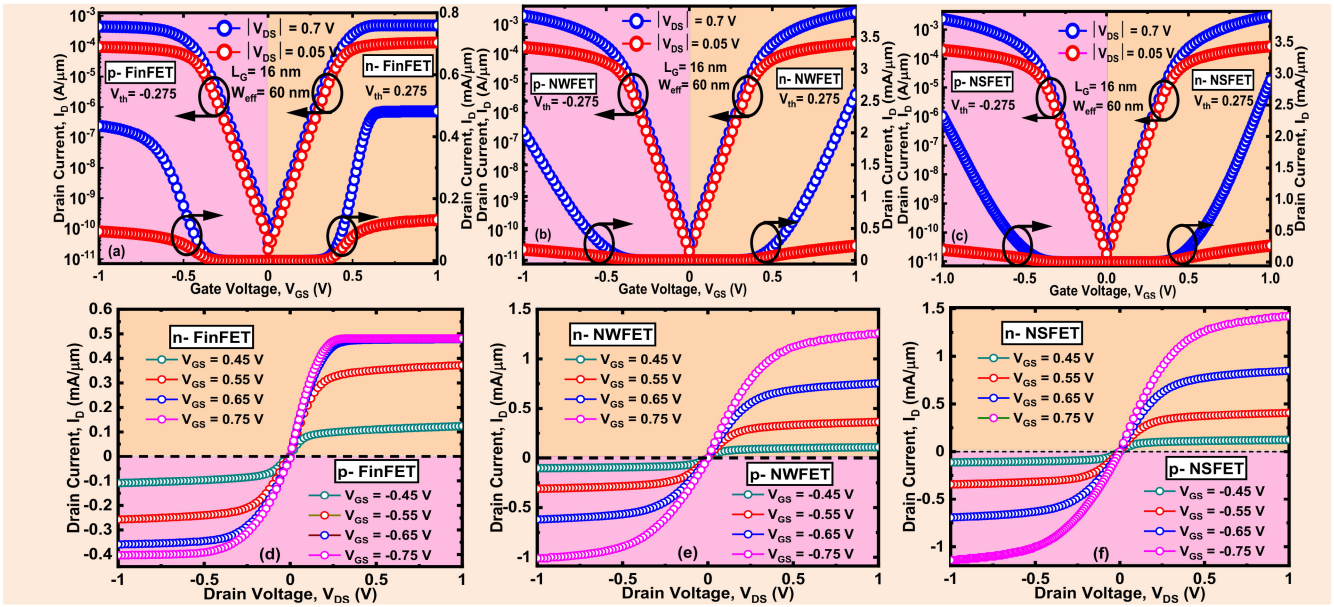

FIGURE 3. (a, b and c) Transfer characteristics (I_D-V_{GS}) (d, e and f) Output characteristics (I_D-V_{DS}) of FinFET, NW and NSFET (MBCFET).

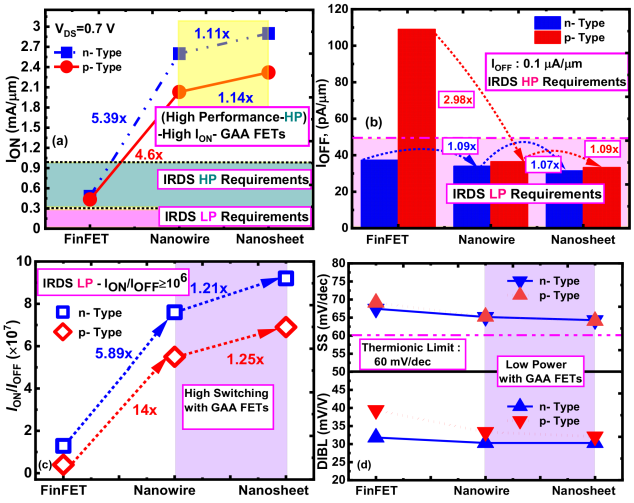

FIGURE 4. (a) I_{ON} (b) I_{OFF} (c) I_{ON}/I_{OFF} (d) SS and DIBL of FinFET, NW and NSFET (MBCFET).

NSFET is noticed. Except for p-type FinFET, the I_{OFF} shows better performance with NWFET and NSFETs compared to IRDS LP requirements. Figure 4(c) depicts the I_{ON}/I_{OFF} ratio of FinFET, and NWFET and NSFETs at $V_{DS} = 0.7$ V. An I_{ON}/I_{OFF} ratio of 1.29×10^7, 7.6×10^7, and 9.2×10^7 with n-type and 3.9×10^6, 5.5×10^7, and 6.9×10^7 with p-type are obtained with FinFET, NWFET and NSFET respectively. The NWFET and NSFET exhibit the highest I_{ON}/I_{OFF} ratio with n-type FET. Even for FinFET, the $I_{ON}/I_{OFF} > 10^7$ is possible due to higher work function of 4.6 e V is considered while matching threshold voltages (V_{th}) with NWFET and NSFET. The SS and DIBL are the fundamental DC metrics to estimate subthreshold performance at lower technology nodes.

The expressions for DIBL and SS are [26]:

$$DIBL\ (mV/V) = \left| \frac{V_{th1} - V_{th2}}{V_{DS1} - V_{DS2}} \right| \quad (1)$$

$$SS = \left[\frac{\partial log_{10} I_D}{\partial V_{GS}} \right]^{-1} \quad (2)$$

The DIBL is calculated by using (1), where V_{th1} and V_{th2} are the threshold voltages extracted at V_{DS} of 0.7 V and 0.05 V, respectively, at $N \times (W_{eff}/L_G) \times 10^{-7}$ A using the constant current method, where 'N' denotes the number of channels. As evident from Fig 4(d), the NWFET and NSFETs show a fall in SS and DIBL with p- and n-type compared to FinFET due to better electrostatic integrity by GAA architecture. Both GAA NWFET and NSFETs exhibit SS near to thermionic limit of 60 mV/dec.

The various analog/RF performance metrics of FinFET, NWFET, and NSFETs are compared for both p- and n-type FETs. The transconductance (g_m) is considered as one of the crucial analog metrics for device evaluation, which relates the change in drain current to the corresponding change in V_{GS}. The g_m is a measure of the device speed and higher g_m values are preferred for better performance of logic operations. Moreover, for devices with higher g_m, the gate transfer efficiency will be high. Furthermore, the amplifying capacity of the device is also determined by g_m. From figure 5(a), it is noticed that NSFET exhibits the highest g_m compared to NWFET and FinFET. The device offers a g_{mMax} of 2.63 mS/μm, 5.75 mS/μm, and 6.53 mS/μm with n-type FETs, and 1.51 mS/μm, 4.38 mS/μm, and 5.04 mS/μm with p-type FETs for FinFET, NWFET, and NSFETs respectively. Compared to p-type FETs, the n-type FETs exhibit better g_m and ensures better gain and amplifying capabilities.

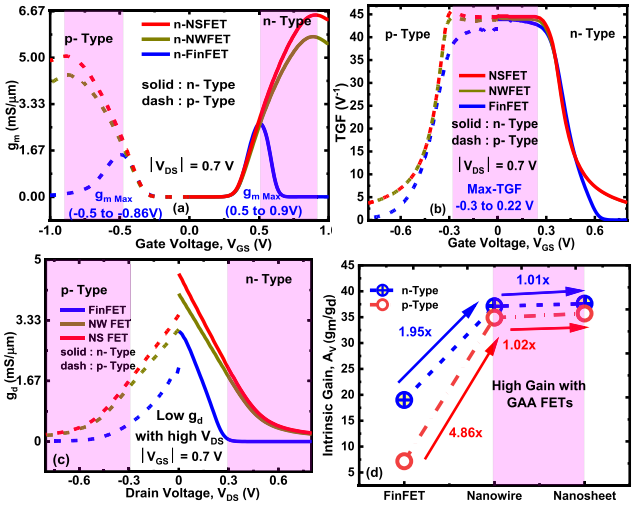

FIGURE 5. (a) g_m (b) TGF (c) g_d (d) A_V of p and n-type FinFET, NW and NSFET (MBCFET).

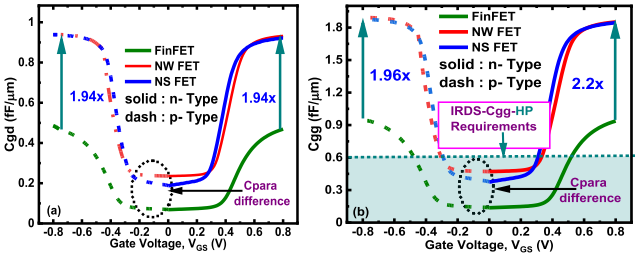

FIGURE 6. (a) C_{gd} (Miller Capacitance) and (b) C_{gg} characteristics of n- and p-type FinFET, NW and NSFET (MBCFET) at V_{DS} = 0.05 V.

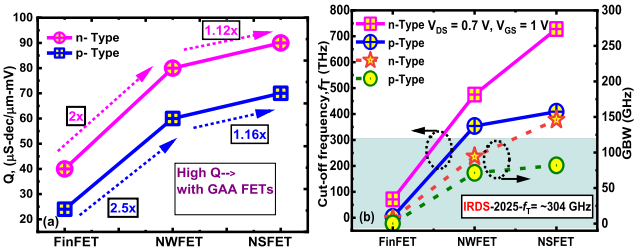

FIGURE 7. (a) Quality factor (Q), (b) f_T and GBW characteristics of n- and p-type for FinFET, NW and NSFET (MBCFET).

A maximum operating voltage of g_m to obtain the highest gain (A_V) is found around 0.5 to 0.9 V for n-type and around -0.5 to -0.86 V for p-type NWFET and NSFETs, respectively. The transconductance generation factor (TGF) $= g_m/I_D$ of a device determines how well a drain current is used to achieve an acceptable g_m and accessible A_V per unit power dissipation. Figure 5(b) depicts the TGF values at $V_{DS} =$ 0.7 V. The device with the highest TGF value can function at lower voltages without losing performance. Moreover, TGF is often used to estimate the power necessary to attain high speeds. The NSFET exhibits a marginal increment in TGF compared to NWFET and FinFET devices due to more g_m. The TGF of 41.8 V^{-1}, 43.9 V^{-1}, 44.5 V^{-1} for p-type and 43.9 V^{-1}, 44.1 V^{-1}, 44.6 V^{-1} for n-type FinFET, NWFET, and NSFET respectively are obtained. The maximum TGF is obtained from around -0.3 V to 0.22 V for all three devices.

For analog circuit design perspective, g_d is an important metric, and its variation with V_{DS} is illustrated in Fig. 5(c). Moreover, for the shorter channel, the influence of V_{DS} on the channel is high. Hence, it is fundamental to estimate the behaviour of g_d on FinFET, NWFET, and NSFET. The NSFET exhibits higher g_d compared to NWFET and FinFET. Moreover, p-type FinFET, NWFET, and NSFET show lower g_d compared to n-type FETs and ensures better gain. The intrinsic gain ($A_V = g_m/g_d$) depicts the overall performance of a device and is shown in Fig 5(d). It can be observed that for FinFET and NWFET, the A_v decreases due to the significant dependence of I_D on V_{DS}. Moreover, a slight increment of 1.95× from FinFET to NWFET and 1.01× from NW to NSFET in n-type is observed. Whereas an increment of 4.86× from FinFET to NWFET and 1.02× from NW to NSFET for p-type is observed. Higher amount of A_v is noticed from FinFET to NWFET due to better g_m.

To understand the AC performance, the total effective capacitance of FinFET, NW, and NSFETs are calculated and depicted in Fig. 6(a)-(b). The total gate intrinsic capacitance (C_{intr}) is the sum of the gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}). The C_{gd} is miller capacitance or parasitic capacitance. The $C_{gg} = (C_{intr} + C_{para})$ and C_{gd} values are low for FinFET compared to NW and NSFETs. Unlike FinFETs, in GAA NSFETs the outer fringing capacitances dominate due to larger NS width. Moreover, C_{gg} and C_{gd} are almost similar for NW and NSFETs. According to IRDS requirements, the C_{gg} for HP applications is 0.6 fF/μm. The FinFET shows lower C_{gg}, whereas NW and NS exhibit a rise over HP requirements. The p-type FETs have larger parasitic capacitances compared to n-type due to diffusion of boron into the channel deeper than phosphorus [20]. Furthermore, the C_{para} is more for NWFET and NSFET compared to FinFET in the OFF state. The quality factor Q = (g_m/SS) [12], determines the qualitative behaviour of a device and its behaviour with FinFET, NWFET and NSFETs is depicted in Fig 7(a). A rise in Q of 2.5× with n-type and 2× with p-type from FinFET to NWFET is noticed. Furthermore, an increment in Q of 1.12× with n-type and 1.16× with p-type from NWFET to NSFET is noticed. Higher improvement is noticed from FinFET to NWFET and NSFETs due to the better electrostatic integrity offered by the GAA structure. Higher Q obtained with NSFET is due to improved g_m and lower SS. The cut-off frequency (f_T) and gain-bandwidth product (GBW) are crucial metrics for the RF performance of any MOS device. The f_T comparison of FinFET, NWFET and NSFET for both n-type and p-type FETs is illustrated in Fig. 7(b). Larger width by NSFET of 10 nm invokes more carriers and offers high I_{ON}. Compared to FinFET and NWFET, the NSFET shows better f_T due to the larger I_{ON}. Moreover, the n-type FETs dominate p-type FETs in f_T due to better g_m.

The GBW indicates a MOS device's constant gain operation region [28]. The GBW product determines the device's constant gain region. The significance of GBW on FinFET,

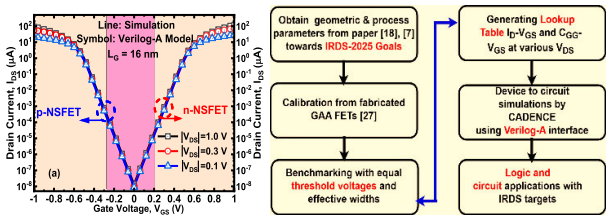

FIGURE 8. (a) Calibration of Verilog-A model characteristics with TCAD simulation results (b) process followed from TCAD to circuit level simulation.

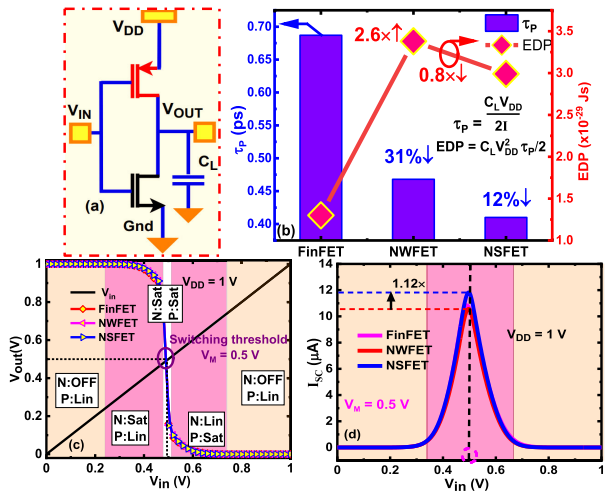

FIGURE 9. (a) Inverter schematic diagram (b) Propagation delay (T_p) and Energy-delay product (EDP) (c) DC response and (d) Switching current (I_{SC}) of CMOS inverter for FinFET, NW and NSFET (MBCFET).

NWFET, and NSFETs is shown in Fig. 7(b). The GBW for NSFET is higher than NWFET and FinFET due to higher g_m. Moreover, NSFET exhibits better performance than NWFET and FinFET for both n and p-type FETs. The GBW of n-type FinFET, NWFET, and NSFETs are 6.7 GHz, 94 GHz, and 146 GHz, respectively. For p-type FETs, the GBW deteriorates compared to n-type FETs with 1.42 GHz, 71 GHz, and 82 GHz for FinFET, NWFET and NSFET, respectively. Finally, it is proved that chosen NWFET and NSFET design metrics meet multiple IRDS goals towards logic and RF performance.

IV. CIRCUIT LEVEL ANALYSIS

The circuit level simulations for FinFET, NWFET and NSFETs are done using a look-up table-based Verilog-A model in the CADENCE simulator [29]. The parallel simulations are carried out using the VisualFab tool to obtain currents and capacitances at different drain voltages for all the devices. The I_D-V_{GS} characteristics from both TCAD and CADENCE tools are depicted in Fig. 8(a) and are matched well. The steps followed from device to circuit level simulations are shown in Fig. 8(b).

The inverter schematic diagram is shown in Fig. 9(a). The sum of both n-FET and p-FET's C_{gg} is considered as the load capacitance (C_L) [30]. The propagation delay of the inverter for FinFET, NWFET and NSFETs is shown in Fig. 9(b).

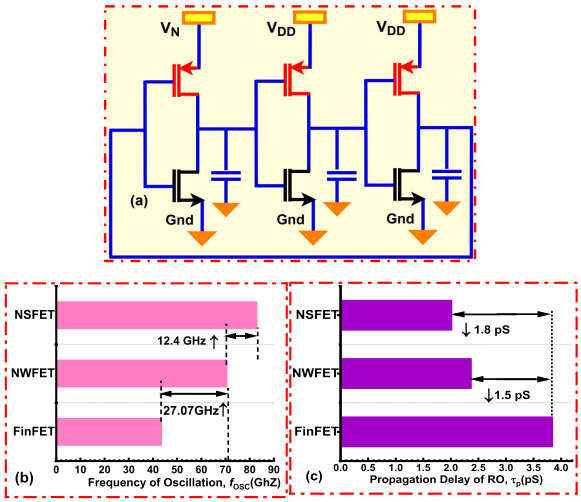

FIGURE 10. (a) 3- stage ring oscillator (RO) (b) Frequency of oscillation (f_{OSC}) (c) Propagation delay (τ_p) of FinFET, NWFET and NSFET (MBCFET) respectively.

The average propagation delay (τ_P) is calculated using the formula shown in Figure 9(b) [31], where I and C_L are the average current and the load capacitance, respectively. As τ_p α $C_L \times (1/I_{ON}$ (n-FET) $+ 1/I_{ON}$ (p-FET)) [32], the significant rise in "I" for NSFET is predominant compared to a marginal rise in C_L, which leads to a fall in τ_p for NSFET based inverter. The τ_p declined by 31% from FinFET to NWFET and 12% from NWFET to NSFET. Also, the energy delay product (EDP) calculated as show in Fig. 9(b) [26]. An increment of 2.8× in EDP is observed from FinFET to NWFET due to marginal fall in τ_p and significant rise in "C_L" and a decrement of 0.8× observed from NWFET to NSFET due to significant fall in τ_p and marginal rise in C_L.

The output characteristics of inverters are depicted in Fig. 9(c), and the switching threshold V_M is noticed at 0.5 V. Moreover, various operating regions of both p and n-type FETs in the inverter are shown in Fig. 9(c). Further, the switching current (I_{SC}) of the CMOS inverter is depicted in Fig. 9(d) for FinFET, NW and NSFETs at $V_{DD} = 1$ V. The static current (at $V_{in} = 0$ V, $V_{in} = V_{DD}$V) is less than 10 pA, resulting in significantly lower static power dissipation and improved energy efficiency for all the FinFET, NW and NSFET based inverters. Similar I_{SC} has been observed for FinFET and NW based inverters at switching threshold voltage. However, an increment of 1.12× in I_{SC} is observed for NSFET based inverter compared to FinFET and NW based inverters. Fig. 10a shows the 3-stage ring oscillator (RO) schematic diagram. Fig. 10b shows the f_{OSC} of FinFET, NW and NSFETs respectively. Compared to FinFET, the NWFET exhibits 27.07 GHz rise in f_{OSC} and compared to NWFET, the NSFET exhibits 12.4 GHz rise in f_{OSC}. Fig. 10c depicts the propagation delay (τ) of the 3-stage RO circuit of FinFET, NWFET and NSFET. A fall of 1.5 pS and 1.8 pS is noticed from FinFET to NW and NSFET respectively. Thus, the NSFET based circuits outperform in circuit applications and ensure further scaling of the device.

TABLE 2. Comparision of emerging fet with literature.

Examined Features	[24]	[12]	[14]	[33]	[34]	[35]	[36]	This work
Explored devices	NSFET	FinFET, NW and NSFET	FinFET, NW and NSFET	NSFET	NWFET	NSFET	NSFET	FinFET, NW and NSFET
Technology node	Sub-5-nm	Sub-5-nm	Sub-5-nm	7-nm	Sub-5-nm	Sub-2-nm	Sub-2-nm	Sub-5-nm
IRDS Benchmarking	No	Yes	No	No	No	Yes	Yes	Yes
p- and n-type	No	No	No	Yes	No	No	Yes	Yes
Circuit for DC and transient analysis	Yes	No	No	Yes	Yes	Yes	Yes	Yes
Circuit implementation (Digital, analog and mixed)	CMOS inverter and RO	--	--	CMOS inverter, SRAM	CMOS inverter and resistive load inverter, common source amplifier	Resistive load inverter and RO	CMOS inverter	CMOS inverter, RO, current mirror, OTA

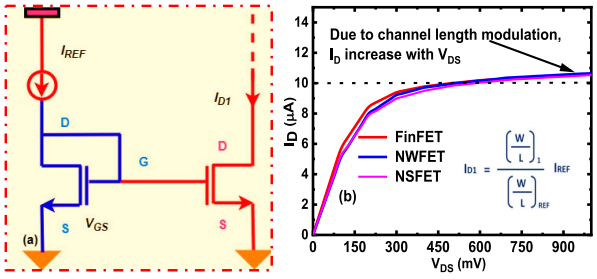

FIGURE 11. (a) Single stage current mirror schematic (b) I_D vs V_{DS} of current mirror with FinFET, NWFET and NSFET (MBCFET) respectively.

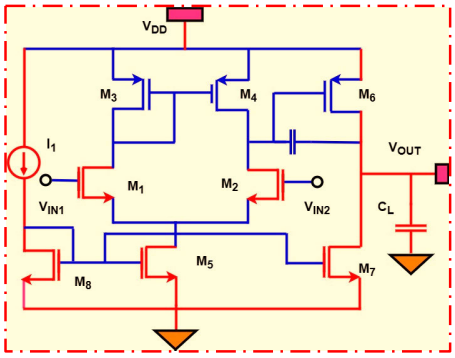

FIGURE 12. The schematic of operational transconductance amplifier (OTA).

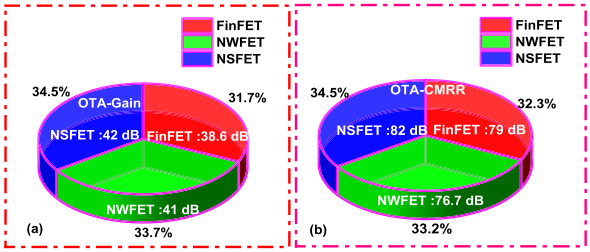

FIGURE 13. (a) The operational transconductance amplifier (OTA) gain and (b) common mode rejection ratio (CMRR) comparison for FinFET, NWFET and NSFET (MBCFET).

In an integrated circuits the current mirrors are an integral part to maintain constant currents instead of varying loads. Fig. 11(a) depicts the current mirror V_{DS} with I_{DS} with FinFET, NWFET and NSFET respectively. For current mirror circuit we have assumed $V_{DD} = 1$ V and I_{ref} of 10 μA. For FinFET, NWFET and NSFET almost have $I_{D1} = I_{ref}$, when V_{DS} approaching 1 V. However, the NSFET has constant output compared to NWFET and FinFET which shows NSFETs robustness for driving analog circuit applications (Fig. 11(b)).

The operational transconductance amplifier (OTA) is one of the fundamental components of any electronic circuit as it increases the output current with respect to the applied differential input voltage. Figure 12 depicts the schematic of OTA. In many circuits it can also be serves as voltage-controlled current source in many of the circuits. Figure 13 shows the performance comparison of FinFET, NWFET and NSFET towards gain (Fig. 13(a)) and CMRR (Fig. 13(b)) respectively. Compared to FinFET and NWFET, the NSFET (MBCFET) exhibits better gain and CMRR and can be feasible for ultra-lower power analog and mixed-mode circuit applications. The contribution of our study is highlighted with comparison of existing FETs in the latest literature is depicted in Table 2. Thus, the comparison of GAA FETs is presented towards device and circuit perspective with satisfying IRDS 2025 goals.

V. CONCLUSION

This article demonstrates the performance comparison of FinFET and GAA NWFET, and NSFET (MBCFET) at both

device and circuit levels. Various crucial DC and analog/RF FOMs are compared and benchmarked with IRDS guidelines. The NSFET exhibits better DC and analog performance compared to NW and FinFET. Compared to FinFET and NWFET, NSFET offers more g_m, TGF, Q, and intrinsic gain. Circuit level comparison has been made for circuits like inverter and ring oscillator. The NSFET based inverter offers the lowest propagation delay despite having more gate capacitances. Also, the NWFET and NSFET based ring oscillators outperform with an oscillation frequency of 70.46 GHz and 82.86 GHz, respectively. The performance benchmarking reveals that NSFET is a potential candidate to continue the scaling for sub-5-nm node technologies. Moreover, the circuits like OTA and current mirror performance for NSFET is better which can be feasible for ultra-lower power analog and mixed circuit applications. Finally, various parameters reach the IRDS goals with NSFET which ensures its robustness for continued scaling.

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