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RESEARCH ARTICLE

The Artificial Neuron: Built From Nanosheet Transistors to Achieve Ultra Low Power Consumption

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ABSTRACT The performance of semiconductors has greatly improved due to the miniaturization of the transistor. To shrink the size of a transistor, the channel length must be decreased. Short-channel effects become noticeable as the gate length is reduced. Short-channel effects are observable at dimensions below 7 nm as a consequence of the shorter gate length. However, nanosheet structures have been proposed to replace FinFET and nanowire transistors at the 7 nm and 3 nm technological nodes. The purpose of this research is to construct an artificial neuron based on nanosheet transistors and evaluate its spiking behaviour and power consumption. We are building a regular Axon Hillock and our proposed neuron model using GPDK 45 nm and nanosheet transistor 20 nm technology. The simulation results clearly show that the nanosheet transistor consumes less power than the GPDK 45 nm transistors. Furthermore, we verified the validity of our suggested neuron model by performing Monte Carlo simulation, PVT analysis, AC response, noise response and layout. Additionally, the proposed neuron was tested with a variety of input currents, including pulse current, ramp current, sinusoidal current, and arbitrary current, and their associated spike patterns were recorded. According to our research, nanosheet-based Axon Hillock consumes 156 fW, and our proposed neuron consumes 1.9 pW of power.

INDEX TERMS Neuromorphic, nanosheet, gate all aruond, FinFET, nanowire, neuron, spiking patterns, axon hillock, end of Moore's law.

I. INTRODUCTION

Significant progress has been made in the semiconductor sector to improve device performance. This is made possible by reducing the size of the transistor. By decreasing the size of the device, the number of transistors on the chip can be enhanced. Miniaturising a transistor requires shortening its channel length. As the length of the channel gets shorter, the distance between the source and drain will get closer together. As the gate length decreases, the gate has less control over the channel, allowing short-channel effects (SCE), self-heating effects (SHEs), and leakage currents to occur. When the channel length is on the same scale as the widths of the depletion layers at the source and drain junctions, short-channel effects are observed. Impact ionisation, velocity saturation/mobility degradation, drain-induced barrier lowering (DIBL), drain punch through, surface scattering, channel length modulation, threshold voltage roll-off, and drain punch through are all examples of short channel effects. Leakage current arises because of tunnelling through the gate oxide. Multiple-gate devices like FinFET, GAA Nanowire, and nanosheet transistors as shown in Figure 1 have been developed to address this issue [1].

When compared to FinFETs and gate-all-around nanowire transistors, nanosheet transistors are more advantageous due to their smaller footprint, low power consumption, and high speed. The drive current delivered by nanosheet transistors is much higher than that of FinFET technology within the same footprint. By stacking nanosheets, an effective channel width is created, which boosts the device's drive current capability.

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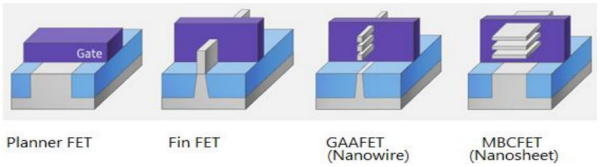
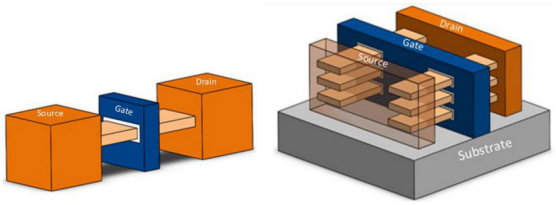


FIGURE 1. Evaluation of transistors [4] from planner FET to nanosheet Transistors.

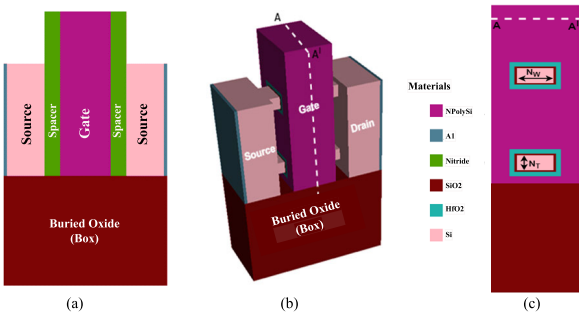


(a) Single (b) Vertically stacked

FIGURE 2. Single and vertically stacked nanosheet transistor [5].

TABLE 1. Comparison between FinFET, NWFET, NSFET [7].

S.No	Electrical Parameters	FinFET	NWFET	NSFET
1	Id sat (uA)	13.13	16.36	18.61
2	Ion lin (uA)	6.24	8.70	9.91
3	Ion Sat (uA)	23.05	30.98	35.89
4	Ioff lin (pA)	42.8	22.27	10.28
5	Ioff sat (pA)	77.50	50.76	18.68
6	Vt lin(-) (mV)	188.30	213.41	224.71
7	Vt sat(-) (mV)	171.99	188.44	210.63
8	SS lin (mV/Dec)	74.38	75.82	72.12
9	SS sat (mV/Dec)	70.99	74.85	72.15



(a) (b) (c)

FIGURE 3. (a) NSFET with Nitride spacer (b) 3D NSFET (c) 2D Cross section of NSFET [1].

Due to its ability to overcome the FinFET's physical limitations and fabrication hurdles, the nanosheet transistor has recently garnered a great deal of attention. The nanosheet transistor is also called the Multi Bridge Channel FET (MBCFET) [2], [3]. Under the 7*nm* technological node, nanosheet structures have been proposed as a replacement for FinFET and nanowire transistors. When compared to FinFET and NWFET, NSFET is the nano-dimension transistor best suited for the new 3 *nm* node technology because of its ideal electrical properties, such as sub-threshold swing SS, DIBL, and threshold voltage (VT). Switching to an NSFET solves most of the problems associated with a FinFET, including the need for constant scaling down, short channel regression, manufacturing complexity, and restricted device performance. It has been observed that the utilisation of NSFET is a suitable alternative for FinFET and nanowire transistors [4]. Mismatches in I_{ON} current seem to have less of an effect on NSFETs than NWFETs [6]. So, these NSFETs will undoubtedly be at the forefront of the semiconductor device industry for the foreseeable future.

The article is organized as follows: In Section II, the electrical properties of nanosheet transistors are examined. Section III focuses on the input and output characteristics of nanosheet transistors. The implementation of the Axon Hillock circuit and its spiking patterns are addressed in Section IV. Section V delves into the proposed neuron model, covering its layout, Monte Carlo simulation, AC response, noise response, PVT analysis, spiking behavior, and power consumption. Section VI discusses potential difficulties and restrictions associated with nanosheet transistors. Section VII outlines future research opportunities in neuromorphic computing using nanosheet transistors, Finally Section VIII addresses the anticipated applications of nanosheet based neurons.

II. NSFET STRUCTURE AND ITS ELECTRICAL PROPERTIES

The effects of channel orientations and widths on the electrical characteristics of p-type vertically stacked NSFETs with Si and Ge have been studied. It was discovered that p-type NS-FETs with vertically stacked nanosheets exhibit higher I_{ON} current when compared with single NSFETs. In addition, the orientation of the Si and Ge channels is a significant factor in influencing the I_{ON} current of the NSFET [5].

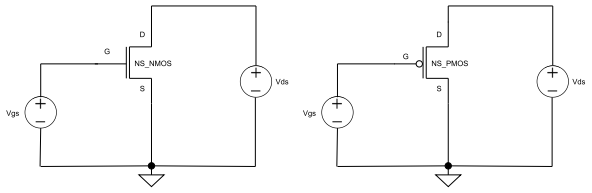
Figure 2 depicts the orientation of a single nanosheet FET and a nanosheet FET that has been stacked vertically. The vertically stacked NSFETs are a potential successor to the trigate FinFETs in terms of ongoing scaling difficulties [7]. NSFETs are well-suited to demanding computing requirements due to their versatility and compatibility with a wide range of materials [5].

To model sophisticated devices at the extreme scaling limit, even at 3 *nm* gate length, a TCAD-based technique is proposed in Ref. [7]. Devices with gate-all-around FET and FinFET structures, as well as horizontally stacked NSFETs and NWFETs, have been designed using this method; the results are listed in Table 1.

Cogenda Genius, a 3D TCAD simulator, is used to create the NSFET device structure in this work. Each sheet of the 3D NSFET is 5 *nm* thick, 10 *nm* width and 16 *nm* gate length. Doping concentrations of $10^{20}cm^{-3}$ and $10^{15}cm^{-3}$ are applied to the n-type source/drain and p-type channel sections, respectively. A 5 *nm* long nitride spacer is kept throughout the simulations to enhance the sub threshold behaviour [1]. In Figure 3(a), we can see a nitride-spaced 2D NSFET. Figure 3(b) depicts a three-dimensional model of an

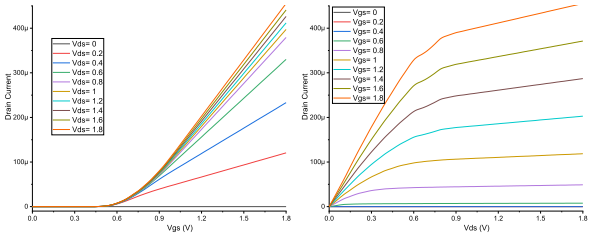
TABLE 2. Device parameters used in simulation [1].

S.No	Device Parameter	Value
1	nanosheet Thickness (*nm*)	5-9
2	nanosheet Width (*nm*)	10-50
3	Gate Length (*nm*)	5-20
4	Source/Drain Doping (cm-3)	1020
5	Channel Doping	5-20
6	EOT (*nm*)	0.78
7	Spacer Dielectric	Nitride
8	Source/Drain Length (*nm*)	12
9	Underlap Spacer Length (*nm*)	5
10	Work function of gate (eV)	4.6
11	Height of gate (*nm*)	60

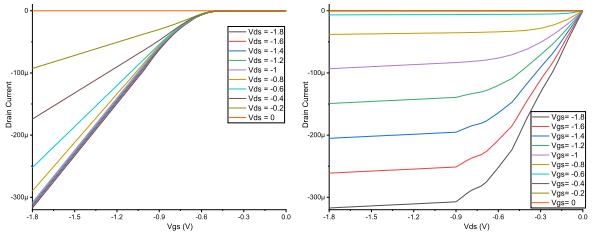


(a) NSNMOS biasing (b) NSPMOS biasing

FIGURE 4. Nanosheet MOSFET ((a) NMOS, (b) PMOS) circuit biasing for examining input and output characteristics.



(a) Input characteristics of NSNMOS (b) Output characteristics of NSNMOS



(c) Input characteristics of NSPMOS (d) Output characteristics of NSPMOS

FIGURE 5. Nanosheet MOSFET's input and output characteristics.

NSFET constructed from stacked nanosheets, and Figure 3(c) shows 2D cross sectional view of an NSFET.

It has been discovered that switching ratio, DIBL, and subthreshold swing (SS) deteriorate when the size of the nanosheet is increased. As width and thickness rise towards 50 *nm* and 9 *nm*, analogue/RF FOMs such as transconductance (gm), output conductance (gds), cutoff frequency (fT), Transconductance frequency product (TFP), and Gain bandwidth product (GBW) increase. However, when the physical dimensions of the NSFET grow larger, the intrinsic gain, as well as gain frequency product (GFP) and gain transconductance frequency product (GTFP), become lower [8]. The information regarding the various parameters taken into consideration for the simulation is presented in Table 2.

III. INPUT AND OUTPUT CHARACTERISTICS OF NSFET

This section describes the input and output characteristics of the nanosheet nmos/pmos transistors. The device was initially conceived in the Visual TCAD programme. The Visual Fab parallel simulation platform is then used to get the DC and AC properties. The lookup tables are constructed from the collected characteristics. The Cadence Virtuoso tool is used to build the symbol based on lookup tables and the VerilogA model, which is then used in schematic diagrams.

By adjusting V_{ds} from 0 to 1.8 Volts as shown in Figure 4(a), the input characteristics of a nanosheet nmos transistor are obtained between V_{gs} and I_d. Cadence Virtuoso is used to run the simulation, and the resulting plot can be seen in Figure 5(a). Whereas the output characteristics is obtained between V_{ds} and I_d by varying V_{gs} from 0 to 1.8 Volts. Figure 5(b) presents the graph that was produced as a result.

Similarlly, the input characteristics of a nanosheet pmos transistor can be achieved between V_{gs} and I_d by altering V_{ds} from 0 to −1.8 Volts, as illustrated in Figure 4(b). The simulation is carried out with the assistance of Cadence Virtuoso, and the resulting plot can be found in the Figure 5(c). Whereas the characteristics of the output can be found between V_{ds} and I_d by adjusting V_{gs} anywhere from 0 to −1.8 Volts. The graph that was produced as a result can be seen in Figure 5(d).

TABLE 3. Comparison of power consumption in NSFET and MOSFET technologies.

GPDK 45 *nm*		nanosheet	
nmos	pmos	NSnmos	NSpmos
14.8 nW	4.8 mW	537 pW	456 pW

As can be seen in Figure 5, the input and output characteristics of nanosheet FETs have characteristics that are quite close to those of conventional metal oxide FETs. As a result, in this work, we are going to propose a neuron that is based on nanosheet field effect transistors and compare the results with a neuron that is based on conventional field effect transistors. The Table 3 shows that compared to conventional nmos and pmos, the power consumption of nanosheet MOSFET is reduced.

IV. AXON HILLOCK USING NANOSHEET TRANSISTOR

The injected current I_{in} into the circuit will integrate and fire a spike when the membrane voltage (V_{mem}) reaches the threshold voltage. The further current injection will produce a sequence of spikes. On the other hand, when the membrane voltage is less than the threshold voltage, the circuit remains in quiescent state. i.e., no spike is generated. V_0 is the initial voltage on V_{mem} before the feedback sequence. The output voltage V_{spike} can be increased by increasing the input voltage through V_{mem}. When the output voltage is raised, it forces current to flow back through C_f, raising the

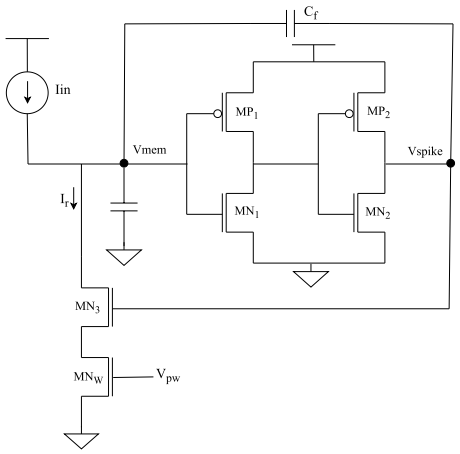


FIGURE 6. Axon hillock circuit proposed by carver mead.

TABLE 4. Comparison of power consumption in axon hillock circuit using NSFET and MOSFET technologies.

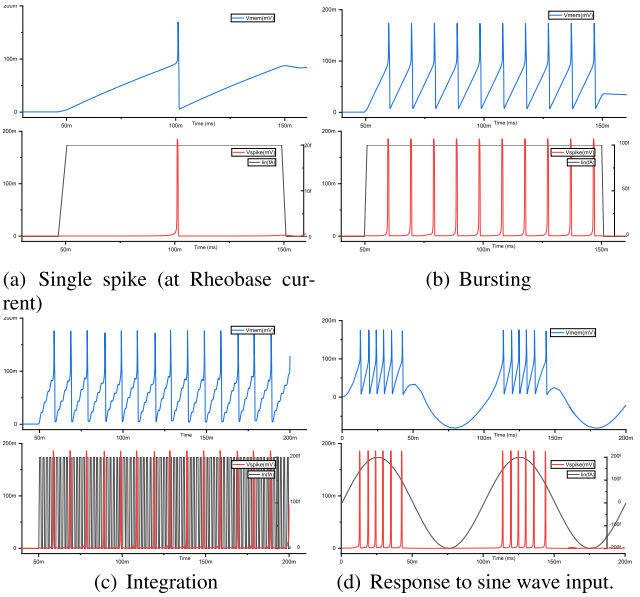
	GPDK 45 *nm*		nanosheet	
S.No	Iin	Power	Iin	Power
1	0	591 fW	0	2.3 fW
2	2 pA, 1ms	1.23 pW	20 fA	15.8 fW
3	1.1 pA	1.73 pW	100 fA	27.3 fW
4	100 pA	13.3 pW	1 pA	156 fW
5	1.2 pA, 10Hz Sine wave	240 fW	200 fA	15.9 fW

input voltage, which in turn raises the output voltage more rapidly. There will be a spike at V_{spike} once the positive feedback begins to take effect. The maximum value of V_{mem} is given by the capacitive-voltage divider relation. Voltage-dependent sodium channels are responsible for the positive feedback in a biological axon hillock. The objective of the MN_3 and MN_W transistors is to allow the current to flow to ground when the output is high, thus resetting the neuron. The voltage at node V_{mem} is discharged by MN_3 via MN_W. Action potential pulse duration is controlled by MN_W and V_{pw}. The Voltage-dependent potassium channels serve as the reset transistors in a real neuron. This circuit shown in Figure 6 is originally proposed by Carver and Ismail [9] and it is affected by static power dissipation through inverters. Hence this circuit consumes high amount of power. The Figure 7 displays membrane voltage and its corresponding spike output for various input currents.

Using GPDK 45 *nm* technology and nanosheet transistors of 20 *nm*, the Axon Hillock circuit was built. Table 4 details the power consumption of both studies. As can be seen in Table 4, both the input current required to cause the spike and the power required by the circuit are drastically reduced when using a nanosheet transistor.

V. PROPOSED NEURON USING NANOSHEET FET

This proposed neuron model is able to reproduce spikes without compromising the biological features of genuine neurons. To put it simply, genuine neurons are dynamical systems. As a dynamical system, the proposed neuron model



(a) Single spike (at Rheobase current) (b) Bursting

(c) Integration (d) Response to sine wave input.

FIGURE 7. Simulation results of the axon hillock utilizing nanosheet transistors.

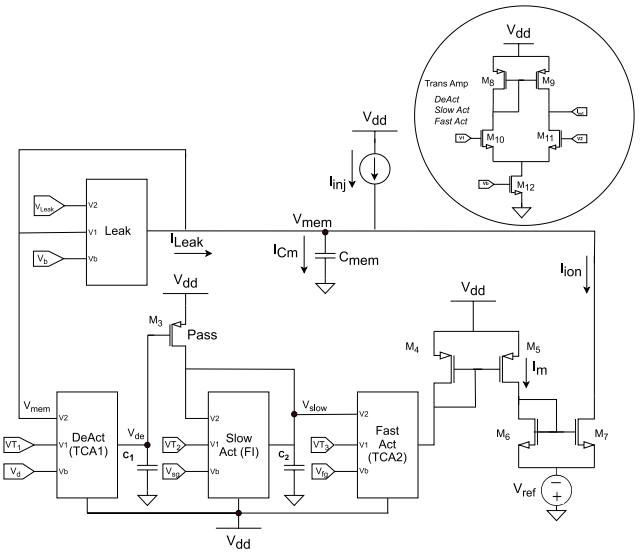
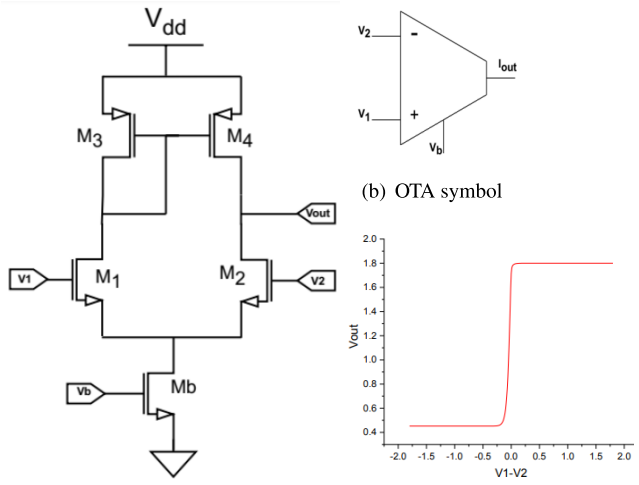


FIGURE 8. Proposed Neuron circuit includes Leak conductance, Deactivation block, Slow activation block and fast activation block.

can process a nonlinear arbitrary input signal. It can process spatially or temporally oriented input signals. Additionally, the threshold voltage, refractory time, and F-I curve are all dynamic. It has the ability to function as either an excitatory or inhibitory neuron. Like real biological neurons, it is capable of displaying rebound spikes, delayed spikes, and damped subthreshold oscillations of membrane voltage.

The proposed neuron shown in Figure 8 is made up of 25 transistors and 9 voltage sources. which is divided into four blocks named as Leaky conductance, Fast activation, Slow activation and Deactivation block. Each ionic channel in the proposed neuron design is built using a body biased



(a) Five Transistor OTA (b) OTA symbol (c) OTA response

FIGURE 9. Five transistor operational transconductance amplifier.

differential amplifier, transconductance amplifier (TCA) and Follower Integrator (FI). This neuron is able to process 10 kHz of input synaptic currents. These components, as well as the various channels currents, will be discussed below.

$$I_{Cm} = I_{Leak} + I_{inj} - I_{ion} \tag{1}$$

A. OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

The operational transconductance amplifier (OTA) has emerged as a fundamental component of many contemporary analog and mixed signal systems. Because of their ability to regulate voltage, OTAs are a crucial component in many different types of circuits. An operational transconductance amplifier (OTA) produces current (I_{out}) at its output terminal in response to a differential input voltage ($V_1 - V_2$). To describe this feature, we use the term ''voltage-controlled current source,'' or ''VCCS'' for short. Therefore, the OTA's transconductance and the differential input voltage determine the output current. The transconductance of the amplifier is typically adjusted via a third input (V_b). In many cases, a setup current can also be used to regulate an OTA's transconductance.

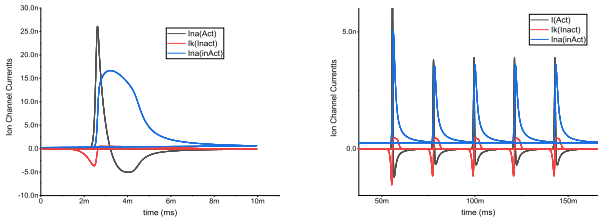
The schematic for the operational transconductance amplifier is depicted in Figure 9. The drain currents I_1 and $_2$ are subtracted using a differential pair (M_1, M_2) and a current mirror (M_3, M_4). Since the current drawn from M3 is mirrored at M4, the output current (I_{out}) is equal to the difference between the two currents ($I_1 - I_2$), and given by

$$I_{out} = I_1 - I_2 \tag{2}$$

$$I_{out} = I_b \tanh(V_1 - V_2) \tag{3}$$

$$G_m = \frac{\partial I_{out}}{\partial V_{in}} \tag{4}$$

where I_b is biasing current from M_b transistor, G_m is the transconductance and V_{in} is difference voltage ($V_1 - V_2$).



(a) (b)

FIGURE 10. Ion channel currents representing sodium activation current(I_{na}(Act)), sodium inactivation current (I_{na}(Inact)) and potassium inactivation current (I_k(InAct)).

The leaky conductance of a neuron can be reproduced with the help of transconductance amplifier depicted in Figure 9. Neuron resting potential is controlled by the V_{Leak}. The membrane voltage, denoted by V_{mem}, depends initially on leaky conductance and injected current [12] and is calculated as follows:

$$I_{\text{Leak}}\ (V_{mem}) = I_b \tanh((V_{Leak} - V_{mem})) \tag{5}$$

B. ION CHANNEL CURRENTS

The sodium and potassium currents of HH neuron model is generelized by ionic currents (I_{ion}) and deactivation current (I_{de}) as shown in Figure 10(a). These currents are produced by FastAct (TCA2), SlowAct (FI) and DeAct (TCA1) blocks respectively.

Where I_{Cm} is the membrane current stored in capacitor C_{mem}, I_{inj} is the post synaptic input current from another neuron, I_{Leak} is the Leakage current from body biased differential amplifier and I_{ion} is the ionic current. The ionic current is generated by TCA1, FI,TCA2 and current mirrors (PMOS,NMOS).

The deactivation current I_{de} is achieved by the negative feedback loop through Transconductance Amplifier (TCA1). As long as V_{mem} is below threshold (VT_1) the TCA1 output is low (Vde=11 mV and Ide=120 pA) and it turns ON the PMOS pass transistor and allows V_{dd} to flow to the next level. When V_{mem} is less than VT_1, The output of TCA1 is high (Vde=1.9 Volt and Ide=1.6 nA) which turns off the pass transistor.Therefore the chances of spike generation is reduced. The gain of TCA1 is controlled by the V_d.

The deactivation current can be given as

$$I_{\text{de}} = I_d \tanh(V_{mem} - VT_1) \tag{6}$$

where I_d is maximum gain current of TCA1. After the membrane voltage has increased to its maximum, the current responsible for deactivation acts to reduce it, causing the neuron to hyperpolarize. When V_{mem} exceeds VT_1, a deactivation current (I_{de}) is produced at the TCA1 output. It blocks the further increase of membrane voltage and delays the next spike generation. Hence, VT_1 is responsible for damped oscillations and frequency adaptation since it blocks further spikes. When VT_1 is higher than V_{mem}, no spikes are initiated.

When ΔV_{slow} is smaller than VT_3, the FastAct block (TCA2) does not emit any ionic current (I_{ion}). The output of TCA2 drops low when ΔV_{slow} is greater than VT_3, which turns ON the PMOS current mirror and produces the current I_m. The likelihood of a spike firing increases as VT_3 rises because the amplitude of I_{ion} rises with rising VT_3. The ionic current can be written as [12]

$$I_{\text{ion}} = I_m.\theta(\Delta V_{slow}(t, V_{mem})) \tag{7}$$

where θ is the Heaviside function and is 1 for $x > 0$ and 0 for $x \leq 0$. I_m is the current delivered by PMOS current mirror in response to ΔV_{slow} and can be given as

$$I_{\text{m}} = I_{fg} \tanh(\Delta V_{slow}(t, V_{mem})) \tag{8}$$

where I_{fg} is the maximmum gain current of TCA2. As V_{mem} rises, the voltage at node ΔV_{slow} rises linearly with time and fall linearly when V_{mem} is less than V_{slow}. The follower integrator (FI), constructed from a transconductance amplifier and an output driving capacitor, is responsible for producing the time varying signal ΔV_{slow} and can be given as,

$$C_2 \frac{dV_{\text{slow}}}{dt} = I_{sg} \tanh(VT_2 - V_{slow}) \tag{9}$$

where C_2 is the output driving capacitor of the follower integrator. I_{sg} is the maximum gain current of follower integrator (FI). The voltage V_{slow} at any given time for small signals can be calculated as

$$V_{\text{slow}}(t) = \int_0^{\infty} VT_2(t - \Delta) e^{-\Delta/\tau} d\Delta \tag{10}$$

where VT2 is the threshold voltage of follower integrator, t is the time of measurement (present value) and Δ is the time before measurement (previous value). Finally, I_{ion} current can be given from the eq 15, 16 and 18

$$I_{ion}(V_{mem}, t) = I_{fg} \tanh(\Delta V_{slow}(t, V_{mem})).\theta(\Delta V_{slow}(t, V_{mem})) \tag{11}$$

Since *tanh* behaviour causes the I_{ion} to decay after its maximum value, the ionic current gradually decreases over time as shown in Figure 10(b). The spike rate and width of the spikes are controlled by the capacitor (C_1) in the DeAct block (TCA1). The capacitor (C_2) in the fastAct block (TCA2) controls the time constant of I_{ion} current and V_{ref} controls the refractory period.

There is no mismatch between the layout in Figure 11 and the schematic in Figure 8. The post-layout simulation matches with the pre-layout simulation. This arrangement occupies a total area of 32 μm^2.

C. MONTE CARLO ANALYSIS OF PROPOSED NEURON

Since threshold voltage, capacitance, resistance, and other device attributes can vary from one semiconductor device to the next as a result of changes in manufacturing techniques, these parameters can have an impact on neuron function. Device performance is also susceptible to environmental factors like temperature and power supply voltage. To examine the effect of parameter modifications and uncertainties on the performance of a proposed neuron design, a statistical analysis approach known as Monte Carlo simulation is employed. To perform the Monte Carlo simulation, one thousand samples were ran with different set of parameters. Based on the data presented in the Figure 12, we can conclude that the proposed neuron has a maximum power consumption of between 20 pW and 80 pW (Mean: 58.98 p, Std Dev: 34.84 p).

D. AC RESPONCE AND NOISE ANALYSIS

Understanding how a circuit reacts to alternating current (AC) signals is crucial for designing circuits for applications such as amplifiers, oscillators, and filters. We can use this information to choose appropriate components and configurations to achieve the desired performance. The proposed neuron is also subjected to an AC response to determine the circuit's behavior at different frequencies. An AC signal of 100 pA with zero phase shift is applied as input to the neuron, and the circuit's frequency and phase response is monitored across a frequency spectrum of 10 Hz to 10 kHz. The proposed neuron spiking frequency is around 220 Hz, as seen in the Figure 13(a), which is comparable to the biological neuron spiking frequency of around 200 to 250 Hz.

Noise analysis of a neuron involves studying the impact of random electrical fluctuations on the performance of the circuit. Noise is an unwanted disturbance that can affect signal integrity, accuracy, and overall system behavior. Noise can arise from various sources, including thermal effects, semiconductor properties, and external electromagnetic interference. Noise analysis is essential for designing circuits that need to maintain a certain level of signal quality and reliability.

The Figure 13(b) shows input and output noise analysis of proposed neuron for the frequencies ranging from 10Hz to 10KHz. Input noise refers to the unwanted electrical fluctuations or disturbances that affect the input signal of a circuit or device. It can originate from various sources such as thermal noise, electromagnetic interference, and other external factors. Input noise can introduce errors or distortions in the signal being processed by the circuit. Output noise refers to the unwanted electrical fluctuations or disturbances present in the output signal of a circuit. It can result from the inherent noise sources within the circuit, as well as the amplification and processing of input noise. Output noise can degrade the quality of the signal being delivered to subsequent stages of a system.

As a result of the noise study, we were able to determine which parts of the system contributed the more noise. In an NMOS current mirror configuration, the M7 MOSFET is responsible for 14.45 percent of the drain current noise and 12.28 percent of the flicker noise. In the fast activation block, the NM1 MOSFET is responsible for 13.77 percent of the

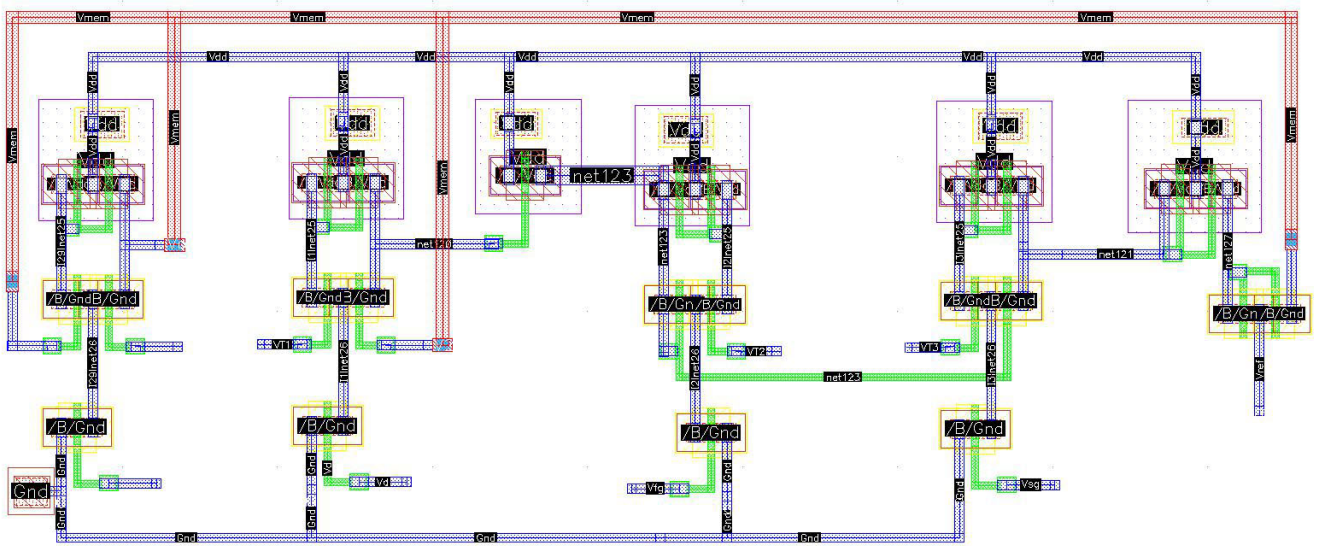


FIGURE 11. Layout of proposed neuron model using GPDK 45 nm technology occupying $32\mu m^2$.

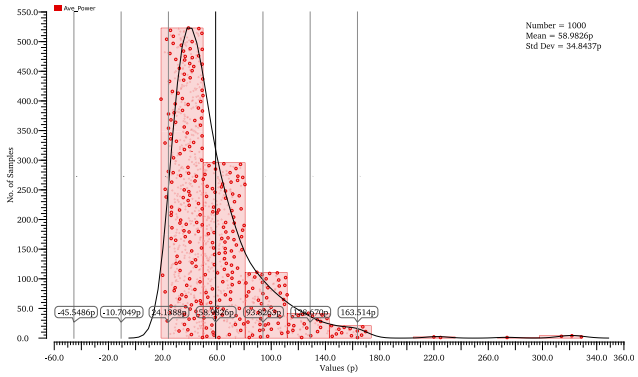
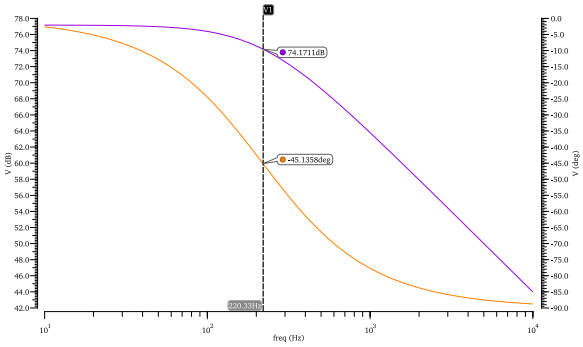


FIGURE 12. Monte carlo simulation of proposed neuron: maximum power consumption concentrated in the range of 20 pW to 80 pW.

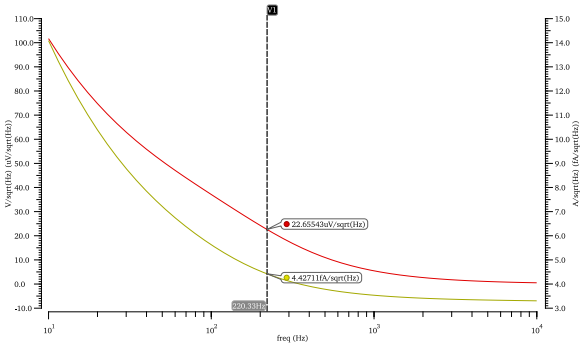
flickering noise. As can be seen in the Figure 13, both the input and output noises are high at low spiking frequencies and decrease as the frequency increases to that of a biological neuron (150-250 Hz). At a frequency of 220 Hz, the total input and output noise measured is 4.43fA/sqrt(Hz) and 22.65uV/sqrt(Hz) respectively.

E. PVT ANALYSIS OF PROPOSED NEURON

Semiconductor manufacturing processes are subject to inherent variability. PVT analysis allows designers to account for variations in transistor characteristics and other factors that can affect circuit performance. PVT analysis helps optimize the performance of integrated circuits by considering variations in the manufacturing process, supply voltage (VDD), and operating temperature. By simulating our neurons behavior under different PVT conditions, we ensure that our circuit meets the performance specifications across a range of real world scenarios.



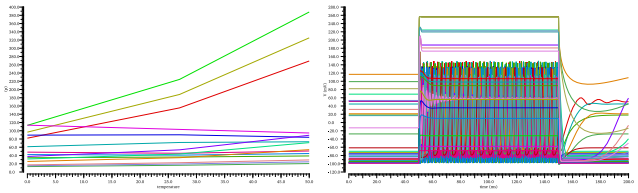
(a) AC Response



(b) Input and Output Noise

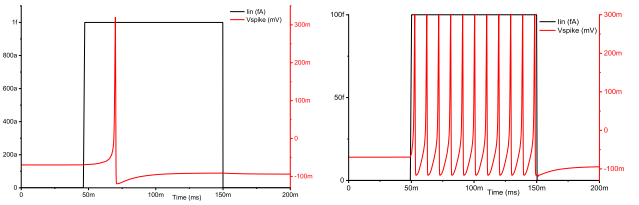
FIGURE 13. AC response and noise analysis of proposed neuron.

The PVT study is conducted to evaluate average power consumption and spiking nature of proposed neuron. The supply voltage exhibits variations of 270 mV, 300 mV, and 330 mV. The verification of process variation is conducted for all corners, namely ff, fs, mc, sf, and ss. Additionally, the variation in temperature is examined under three conditions:

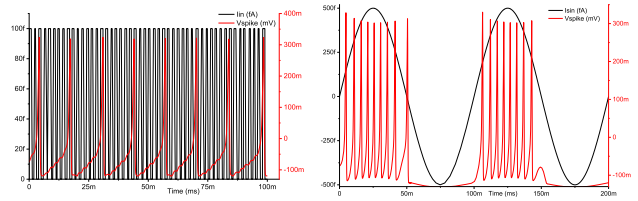


(a) Average Power (b) Membrane Potential

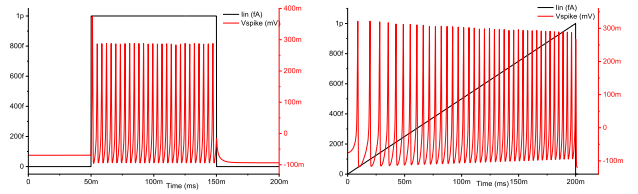
FIGURE 14. Process-voltage-temperature analysis of proposed neuron.



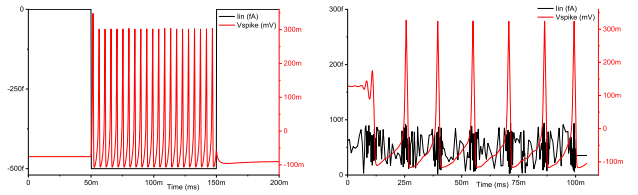
(a) Single spike (at Rheobase current(1fA)) (b) Bursting



(c) Integration (d) Sine wave input



(e) High input current(1pA) (f) Ramp input



(g) Inhibitory input (h) Arbitrary input

FIGURE 15. Simulation results of proposed neuron using nanosheet MOSFET.

0, 27, and 50 degrees Celsius. The response is depicted in the Figure 14. Based on the PVT results, we know that the proposed neuron can fire spikes in every corners but ff (fast, fast). For all of the aforementioned changes in process, voltage, and temperature, we find that the least power usage is 13 pW and the maximum is 388 pW, with a mean of 80.59 pW.

In summary, the Monte Carlo simulation results indicate that the proposed neuron maintains a maximum power consumption confined within the pW range. The AC response

TABLE 5. Power consumption comparison of the proposed neuron utilizing nanosheet transistors and GPDK 45 nm.

	GPDK 45 *nm*		nanosheet	
S.No	Iin	Power	Iin	Power
1	83 pA	172 pW	1 fA	715 fW
2	100 pA	200 pW	100 fA	1.16 pW
3	1 nA	2 nW	1 pA	1.90 pW
4	2 nA	4 nW	0-1 pA	2.43 pW
5	1.2 pA, 10Hz Sine wave	1.12 pW	200fA	16.7 fW

TABLE 6. Comparison of various neuron models with respect their power consumption.

S.No	Neuron Model	Technology	Power
1	HH [13]	-	60 uW
2	HH [14]	0.5 um CMOS	300 uW
3	HH [11]	0.13 um CMOS	43 nW
4	HH like [15]	0.35 µm CMOS	0.1-60 µW
5	HH [17]	FGMOS 0.18 um	119 uW
6	Morries Lecar [18]	65*nm* CMOS	105 pW
7	Simplified ML [10]	65 *nm* CMOS	30 pW
8	Mihalas Niebur [19]	0.5 um AMIS	70 uW
9	Hindmarsh and Rose [20]	0.25 um CMOS	163.4 uW
10	Izhikevich [21]	90*nm* MOSIS	7 nW
11	Proposed Neuron	GPDK 45*nm*	2 nW
12	Proposed Neuron	nanosheet 20 *nm*	1.9 *pW*

reveals that the spiking frequency of the proposed neuron closely mimics that of biological neurons. Noise analysis demonstrates a reduction in noise as the spiking frequency approaches the actual spiking frequency of neurons. PVT analysis further illustrates that the neuron consistently fires spikes across all corners except for ff (fast, fast). Considering the comprehensive analyses conducted, it is clear that the proposed neuron demonstrates robustness through various technical validation processes.

Figure 15 illustrates a range of spiking patterns generated by our proposed neuron model, employing nanosheet MOSFETs, under various input syna[tic currents. The voltage configurations are as follows: $V_{dd} = 250$ mV, $VT_1 = 120$ mV, $VT_2 = 38$ mV, $VT_3 = 40$ mV, $V_d = 202$ mV, $V_{Leak} = 30$ mV, $V_{sg} = 220$ mV, $V_{fg} = 200$ mV, $V_{bias} = 250$ mV, $V_{ref} = 50$ mV, and $I_{in} = 1$ pA. The capacitance values are $C_{mem} = 5$ fF, and $C_1 = C_2 = 10$ fF. By keeping the voltages fixed as specified above, various spike patterns can be obtained by solely adjusting the input current. The provided voltage set pertains to the nanosheet-based neuron, and for GPDK 45 nm, a different set of voltages will be employed to induce spikes.

Based on the data in Table 5, it is obvious that the suggested neuron requires a maximum of 4nW of power when utilising GPDK 45 *nm* technology and a pulse input current of 2 *nA*. For a 1 *pA* pulse input current, the same circuit with nanosheet transistors needs only 1.9 pW of power. As a result, our suggested neuron employing a nanosheet transistor can provide the lowest documented power consumption in neuromorphic engineering.

In Table 6, we contrast the power requirements of our suggested neuron model with those of previously known neuron models. Our statistics show that, whether built with a

TABLE 7. Comparative analysis of various type of transistors used to build analog neuron models.

Device	Reference	Technology	Type	Vdd	Iin	Energy/spike	Power	Freq	Area
FINFET	[22]	40 nm	LIF	1.8 V	-	5.4 fJ	-	Mhz	0.023 μm^2
	[23]	7 nm	LIF	800 mV	-	27 fJ	4.8 µW	5 Mhz-330 Mhz	42.4 μm^2
	[24]	20 nm	LIF	400 mV	0.05 mA	1.9 fJ	-	GHz	-
	[25]	-	LIF	3 V	0.35 µA	6.3 fJ	-	MHz	0.04 μm^2
FGMOS	[26]	0.18 µm	HH	900 mV	-	-	119 µW	50 Hz	-
	[27]	1.5 µm	HH	1.5 V	-	-	-	-	-
CNTFET	[28]	MTJ	LIF	-	-	-	8181 µW	-	26 μm^2
	[29]	MTJ	LIF	800 mV	-	3.7 fJ to 5.1 fJ	-	-	-
	[30]	MTJ	LIF	800 mV	-	121 fJ	-	-	-
	[31]	0.35 µm	LIF	-	150 µA	267 pJ	-	-	913 μm^2
SPINTRONICS	[32]	a-IGZO	AH	5 V	1 nA to 10 nA	700 pJ	nW	11.926 MHz	607.3 µm x 492.2 µm
CMOS	[33]	55 nm	LIF	300 mV	150 pA to 450 pA	639 fJ	-	145 Hz	400 μm^2
	[34]	65 nm	LIF	1 V	-	4 pJ	800 pW	230 Hz	127 μm^2
	[35]	180 nm	LIF	1.8v	1.2 µA	77.24 pJ	-	200 KHz	12975μm^2
NANOSHEET	**Proposed**	**20 nm**	**HH**	**250 mV**	**1 fA to 1 pA**	**1.23 fJ to 24.98 fJ**	**16.7 fW to 1.9 pW**	**250 Hz**	**32** μm^2.

regular transistor or a nanosheet transistor, our neuron model has lower power requirements than previous neuron models.

Transistors play a crucial role in neuromorphic computing by serving as the building blocks for the implementation of artificial neurons and synapses. There are several types of transistors that can be used in neuromorphic computing, each with its own characteristics. Here are some common types of transistors used to build analog neurons: FINFET, FGMOS, CNTFET, SPINTRONICS, and CMOS transistors. In this work, we are presenting a nanosheet transistor-based neuron model. The detailed comparisons of neuron models built with these transistors are listed in Table 7. From this analysis, it is clear that the neuron model built with nanosheet transistors provides better performance and power consumption with a minimal footprint. It is important to note that the field of neuromorphic computing is rapidly evolving, and researchers are continuously exploring new transistor technologies and architectures to improve the efficiency and performance of neuromorphic systems. The choice of transistor type depends on various factors, such as power efficiency, scalability, and the specific requirements of the neuromorphic application.

VI. POTENTIAL CHALLENGES AND LIMITATIONS

Nanosheet transistors represent an advanced semiconductor technology designed to address some of the limitations of traditional MOSFETs. However, like any emerging technology, nanosheet transistors come with their own set of challenges and limitations.

- One of the primary challenges is that the fabrication process involves precise control over multiple layers, and any deviations or defects in the manufacturing process can significantly impact device performance.
- As transistor dimensions shrink, tunneling effects can impact transistor behavior, leading to increased leakage currents that consequently increase power consumption. As transistor dimensions shrink, tunneling effects can impact transistor behavior, leading to increased leakage currents that consequently increase power consumption.
- The reduction in transistor dimensions also increases the proximity of neighboring devices, which can lead to increased crosstalk and interference. This can affect signal integrity and pose challenges for designing high-density integrated circuits.
- Integrating nanosheet transistors with other components, such as memory and interconnects, poses challenges in ensuring compatibility and optimal performance across the entire integrated circuit.

Addressing these challenges requires collaborative efforts from researchers, engineers, and the semiconductor industry.

VII. SUGGESTIONS FOR FUTURE RELATED RESEARCH

Research in the field of nanosheet transistor-based neurons holds promising avenues for advancing neuromorphic computing and artificial intelligence. Here are some suggestions for future research directions:

- Investigate strategies to incorporate more bio-inspired features [16] into nanosheet transistor-based neurons.
- Investigate the implementation of synaptic plasticity mechanisms in nanosheet transistor-based neurons to enhance learning capabilities.
- Promote collaboration between hardware and software researchers to develop efficient algorithms and programming models tailored to nanosheet transistor-based neuromorphic hardware.
- Establish standardized benchmarks for evaluating the performance of nanosheet transistor-based neuromorphic systems. This can facilitate fair comparisons

between different designs and implementations, fostering advancements in the field.

Collaborative efforts across interdisciplinary fields, including materials science, electrical engineering, computer science, and neuroscience, will be crucial for advancing research on nanosheet transistor-based neurons and unlocking their full potential in neuromorphic computing.

VIII. ANTICIPATED APPLICATIONS OF NANOSHEET BASED NEURONS

Neuromorphic engineering aims to design and develop circuits and systems that mimic the structure and function of the brain. Nanosheet transistors offer advantages such as improved performance, reduced power consumption, and enhanced scalability, making them potentially suitable for various neuromorphic applications, such as

- Nanosheet transistors can operate at lower voltages, enabling more energy-efficient neuromorphic computing. The reduced power consumption is crucial for applications like edge computing and wearable devices, where energy efficiency is a primary concern.
- The scalability of nanosheet transistors allows for higher integration densities on a chip. This is particularly beneficial for neuromorphic systems that require a large number of synapses and neurons for complex cognitive tasks.
- The three-dimensional structure of nanosheet transistors can be advantageous in creating complex synaptic and neuronal connectivity patterns.
- Nanosheet transistors offer improved switching speeds that can enhance the real-time processing capabilities of neuromorphic systems. This is critical for applications such as sensory processing, robotics, and autonomous systems.

Although these applications highlight the potential of nanosheet-based neurons, further research and development are needed to realize their full potential in real-world scenarios.

IX. CONCLUSION

Our research has demonstrated the promising potential of nanosheet transistors in the realm of neuromorphic engineering. Utilizing GPDK 45 *nm* and nanosheet 20 *nm* technology, we construct two distinct types of neurons: traditional Axon Hillock and our proposed neuron model. According to our research findings, nanosheet transistors prove to be a highly favorable option for neuromorphic engineering. It is capable of generating a variety of spike patterns while consuming a very small portion of power, and it might also overcome Moor's law bottleneck in the future. Our proposed neuron model, implemented with nanosheet transistors, showcases exceptional sensitivity to the femtoampere range of input synaptic currents, a crucial characteristic in mirroring the intricacies of real neural systems. In comparison to GPDK 45 *nm* transistors, the power consumption has been minimized to an ultra-low level. Nanosheet transistors may play a crucial role in advancing the development of energy-efficient and scalable neuromorphic architectures, offering advantages in terms of compactness and integration density. Nanosheet transistors can also be integrated into neuromorphic memory systems, providing benefits in terms of high-speed access, low power usage, and non-volatility. Through this work, we are strongly recommending nanosheet transistors for future neuromorphic engineering.

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