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RESEARCH ARTICLE

A Compact Model for Interface-Type Self-Rectifying Resistive Memory With Experiment Verification

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ABSTRACT Resistive random access memory (RRAM), a new non-volatile memory, enables hardware accelerators based on in-memory computing with improved throughput and energy efficiency, enabling machine learning on-the-fly inference at the edge. However, sneak-path currents in RRAM crossbar arrays (CBAs) can cause crosstalk, limiting high-density applications. The best choice for suppressing leakage current is self-rectifying RRAM (SRR). Interface-type RRAMs offer CMOS compatibility, better controllability, higher reliability, and lower power consumption compared to filament-type counterparts. However, while there is much research on the filament-type RRAMs, there is little research and no measurement validation on the interface-type RRAMs. In this paper, a compact model of the interface-type RRAM is developed for circuit and system exploration. The model includes Schottky barrier diode, effective layer resistance, nano-battery effect, parasitic resistance, and capacitance. It also has a dynamic behavior model, including device-to-device variation, retention, and endurance. Compared with measurements, it reproduces high accuracy of 98.97% in DC and 98.05% in AC. The proposed model is applied to a neuromorphic 64 × 64 SRR CBA with 32-bit fixed-point precision. A nano-battery bias scheme is also proposed to zero the current of RRAMs having non-zero I-V crossing points, reducing the sneak-pass current error to 0.02%. A vector matrix multiplication application demonstrates 3.44 TOPS/W with a 50:50 LRS to HRS ratio, and a deep neural network on a VGG-8 architecture using the CIFAR-10 dataset observes an accuracy degradation of 1.36%.

INDEX TERMS Compact model, crossbar array, interface-type RRAM, multiply and accumulate (MAC), nano-battery effect, parasitic capacitance, parasitic resistance, resistive random access memory (RRAM), self-rectifying RRAM (SRR), vector matrix multiplication (VMM).

I. INTRODUCTION

ARTIFICIAL intelligence (AI) edge devices use parallel computation and distributed systems to perform knowledge and reasoning processes that emulate human behavior, such as natural language processing, pattern recognition, knowledge modeling and representation, and intelligent data retrieval [1]. Parallel processing technology enables the processing of large-scale applications that are difficult to process on a single processor system [2]. However, most modern computing systems based on the von Neumann architecture need to move large amounts of data back and forth between processing and memory devices while executing various computational tasks, incurring significant

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costs in latency and energy [3]. Therefore, even with parallel processors, the von Neumann structure cannot completely overcome the data movement problem [4].

Memory-centric chip technologies of near-memory-computing (NMC) and in-memory-computing (IMC) have emerged to alleviate the bandwidth bottleneck issues. The NMC with advanced memory modules such as hybrid memory cube (HMC), high bandwidth memory (HBM), and three-dimensional (3D) monolithic integration places compute units closer to monolithic memory to minimize the expensive data movements, but there is still a physical separation between memory and the computing units. The IMC is an alternative approach to organizing compute memory devices by performing specific computational tasks on the memory itself, and it is implemented by utilizing array-level memory devices and computing units together in a monolithic fashion. The IMC has the potential to significantly improve the computational time complexity associated with certain computational tasks and mitigate the latency and energy costs associated with data movements [5].

State-of-the-art deep neural network (DNN)-based machine learning algorithms have demonstrated remarkable effectiveness in a variety of artificial intelligence applications, which requires the development of dedicated accelerators to improve energy efficiency and latency when running the DNN workloads on IMC systems. There are three major types of IMC computation: bitwise Boolean logic operations (AND, OR, XOR, etc.) using data stored in a given memory cell array, pattern-matching computation comparing the input data with the data stored in memory and then returning the matching data address, and multiply and accumulate (MAC) operation which are the primary calculations used in AI. Thus, the IMC requires high-speed, high-density, low-power, and scalable memory devices, which have been extensively studied in CMOS-based SRAMs [6]. While the SRAM is compatible with CMOS manufacturing and suitable for arithmetic operations, its volatility after power-off and density limitations due to its large cell area has led to the exploration of new non-volatile memory (NVM) technologies in in-memory computing, including resistive RAM (RRAM) [7], magnetic RAM (MRAM) [8], and phase change memory (PCM) [9], which can form two-dimensional crossbar arrays. Among these non-volatile memories, the RRAM is the most promising candidate for IMC architectures for deep learning acceleration due to its high-density integration, low read latency, and low power consumption compared to other candidates.

A passive crossbar array (CBA) architecture for high-density RRAM is shown in Fig. 1(a) where each cell with a unit area of $4F^2$ (where F represents the technology feature size) [10] is located at the intersection of a word-line from the top row electrodes and a bit-line from the bottom column electrodes. In analog MAC computing, the programming process is performed by updating the conductivity of the RRAM cells in the crossbar array, and the inference process is performed by reading the current

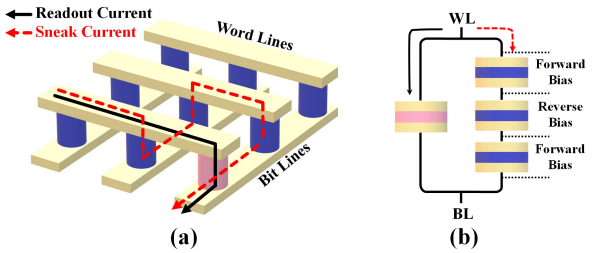

FIGURE 1. (a) RRAM-based passive crossbar array and (b) sneak-path current.

value of the cell conductivity value. A main challenge faced by RRAM-based CBA is the sneak-path leakage, an undesired current flowing through the RRAM cells parallel to the selected one [11]. The sneak-path leakage in the CBA is explained by describing a 3 × 3 CBA as shown in Fig. 1(b). It assumes that the cell between word-line WL0 and bit-line BL2 is selected and the cell resistance is labeled as Rs. Meanwhile, the sneak-path parallel to the selected cells consists of three unselected cells, whose resistances are represented by R_{P1}, R_{P2}, and R_{P3}. Hence, the resistance measured between word-line WL0 and bit-line BL2 is the parallel resistance of the selected resistance and the sneak-path resistance while reading the selected cell R_s, which can potentially lead to an inaccurate RRAM cell readout and resistance modulation. The larger the crossbar array, the more sneak-path currents there are, making it much harder to distinguish and program the stored values. Extensive research is being conducted on this urgent and important challenge to eliminate or suppress sneak-path current problems in RRAM crossbar arrays.

The 1T1R cell structure shown in Fig. 2(a), where a series transistor acts as a switch, is an effective solution to the sneak-path current problem. The unselected transistors are set to the OFF state to avoid crosstalk. However, the cell area is $8F^2$, the voltage drop across the transistor makes it less energy efficient during inference and set operations, and the threshold voltage drop during reset operation slows down programming time. A RRAM with a unit cell area of $4F^2$ and a stacked selector is shown in Fig. 2(b). The selector has bidirectional high nonlinear resistors to efficiently suppress sneak-path leakage by increasing the resistance at low read and write voltages, as shown in Fig. 2(d). However, it is difficult to operate each of the two series elements independently since a single terminal is used to read and program the RRAM cell through the selector unless the selector is specifically adapted for the RRAM cell or vice versa. Another approach to mitigate sneak currents is to utilize a self-rectifying RRAM (SRR) whose rectifying properties can inhibit current conduction through reverse-biased RRAM cells along the sneak-path, as shown in Fig. 2(c). A conventional structure for the SRR is metal-insulator-metal (MIM). The large work function difference between the top and bottom electrodes is essential for the asymmetric effective barrier that appears at the

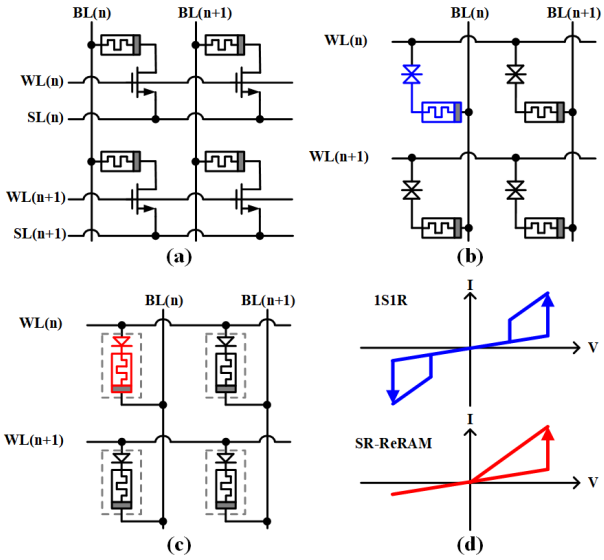

FIGURE 2. CBA with (a) 1T1R, (b) 1S1R, and (c) SRR and (d) I-V characteristics of 1S1R and SRR.

top and bottom electrodes to exhibit self-nonlinear I–V characteristics as shown in Fig. 2(d).

There are two types of switching mechanisms in RRAM: filament-type RRAM and interface-type RRAM. While the filament-type has large memory windows, fast switching speeds, and good retention characteristics, it inevitably has variability due to the stochastic nature of filament dynamics [12], which degrades system performance. The interfacial scheme exhibits much better device-to-device and cycle-to-cycle uniformity than the filament type due to the uniform variation through the oxide [13]. In addition, the highly nonlinear current-voltage characteristics allow the passive crossbar array to operate without transistors or selector devices. However, the low oxygen vacancy mobility inside the oxide switching layer and the high depolarization field after charge redistribution pose significant challenges to the operating speed and data retention of interfacial RRAMs [14]. Interface-type SRR with a Na-doped TiO_2 by using the highly dependable technique of atomic layer deposition (ALD) [15] exhibits an electroforming free bipolar self-rectifying resistive switching behavior and high mobility regardless of the underlying oxygen vacancy concentration and even under reverse-biased Schottky diode [16].

Quantitative circuit analysis is required to characterize the SRR CBA performance. Many integrated circuit engineers consider physics-based compact models the most accurate and simple enough for their circuit simulations as they can be used for the largest operating range. While there are many studies on compact models of the filament-type RRAMs [17], [18], [19], [20], there are few studies on those of the interface-type RRAMs [21] and, to the best of the author's knowledge, no measurement validation. The models implemented in Verilog-A are compatible with many industrial circuit simulators such as Spectre, HSPICE, Eldo, etc., making it a standardized behavioral language. Moreover,

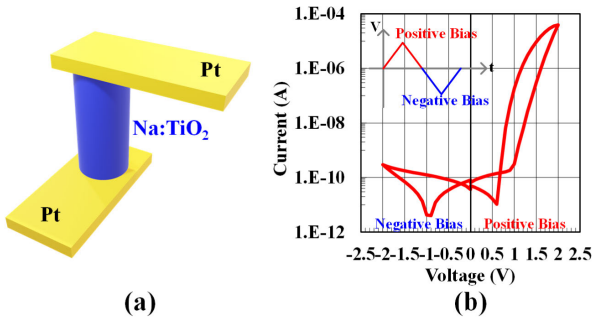

FIGURE 3. Pt/Na:TiO_2 structure and (b) measured I-V characteristics.

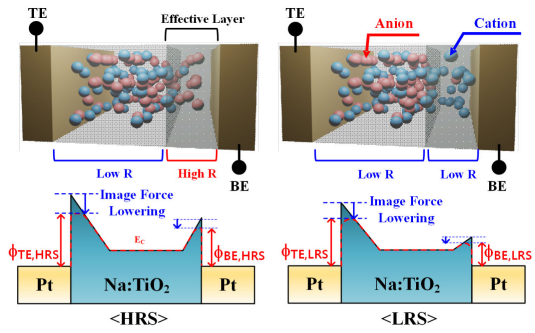

FIGURE 4. Conceptual operation and energy band diagram of HRS and LRS of Pt/Na:TiO_2/Pt SRR.

interconnect modeling of the nanometer scale of RRAM CBA becomes critical due to the dominant influence of parasitics in determining the overall system performance. The remainder of the article is organized as follows. Section II describes the behavior of Pt/Na:TiO2/Pt devices with self-rectifying I-V characteristics and the process of establishing the high/low Resistance state (HRS/LRS), and a physics-based model is proposed for the device. Section III presents the simulation results of the proposed model at the cell level with experimental validation. Section IV includes an assessment of the models at the circuit and system levels. Concluding remarks are in Section V.

II. SELF-RECTIFYING RRAM (SRR)

A. SRR STRUCTURE AND OPERATION

In this work, Na-doped TiO_2 SRRs (Na:TiO_2) with highly mobile sodium cations as the main component for resistive switching are measured and modeled. The structure of the proposed SRR is controllably grown via atomic layer deposition (ALD) by adopting TiO_2 as the matrix material. During fabricating the bottom electrode (BE), Ti ions diffuse from the adhesion layer below the BE and form an effective layer near the BE electrode. The effective layer is therefore represented by TiO_x stoichiometry, which is deficient in oxygen vacancies compared to TiO_2 on the TE side. This asymmetric distribution of oxygen vacancies causes the rectification behavior of the Pt/Na:TiO_2/Pt structure. Moreover, it can serve as an effective host for Na ion transport, as shown in Fig. 3(a) [16]. Unlike conventional

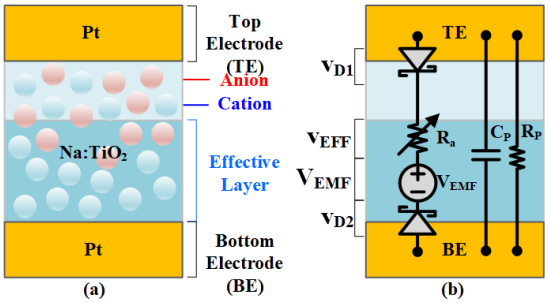

FIGURE 5. (a) Schematic diagram and (b) compact model of Pt/TiO_2 SRR.

RRAMs based on oxygen anions, the high mobility of Na ions provides RRAM behavior independent of the underlying oxygen vacancy concentration, even at low currents of reverse-biased Schottky diode operation. As a result, reversible switching is possible at negative-biased SRRs with rectification characteristics of currents lesser than those of positive-biased by more than 10^3 times, as shown in the measured data in Fig. 3(b). Fig. 4 shows the height of the Schottky barrier at the readout voltage for HRS and LRS. Based on the effective layer resistance value near the bottom electrode (BE) interface, a low resistance state (LRS) and a high resistance state (HRS) can be distinguished. In the case of HRS, the effective layer has a relatively high resistance compared to LRS because the BE interfacial voltage ($\phi_{BE,HRS}$) in HRS is much higher compared to LRS ($\phi_{BE,LRS}$). Instead, the top electrode (TE) interfacial voltage ($\phi_{TE,LRS}$) of the LRS is slightly smaller compared to the HRS ($\phi_{TE,HRS}$) since the oxide vacancy concentration between the TE and effective layer interfaces varies less with the resistance states. The SET operation from HRS to LRS is achieved by applying a positive program voltage between the anode and cathode to increase the concentration of Na+ cations in the effective layer, and the RESET operation from LRS to HRS is achieved by applying a negative program voltage to decrease the concentration of Na^+ cations in the effective layer. For stable readout current, the readout voltage is set to a voltage value sufficiently lower than the program voltage.

B. PHYSICS-BASED SRR COMPACT MODEL

Fig. 5(a) shows a simplified two-terminal SRR structure based on Pt/Na:TiO_2/Pt. According to the program voltage, the concentration of Na^+ ions in the active layer close to the BE is redistributed to change the resistance of the active layer and change the Schottky barrier at the Na:TiO_2/Pt interface. In the case of LRS, the concentration of Na^+ ions in the active layer increases, resulting in low resistance and lowering the Schottky barrier at the BE interface. In the case of HRS, the concentration of Na^+ ions in the active layer is reduced, resulting in a high-resistance state and increasing the Schottky barrier of the interface.

An equivalent circuit model is proposed for the LRS/HRS as shown in Fig. 5(b). Two Schottky barrier diodes (D_{SC}) at

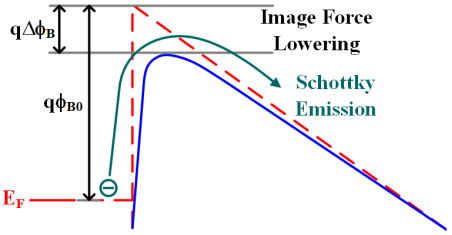

FIGURE 6. Schematic energy level diagrams showing thermionic–field emission, and field emission for a Schottky barrier under the reverse-bias voltage.

TE and BE are connected back-to-back, a forward-biased and a reverse-biased. An effective layer variable resistance (R_a) and electromotive force (EMF) due to the nano-battery effect (V_{EMF}) are connected in series between two D_{SC}s. Parasitic resistance (R_P) and capacitance (C_P) are added in parallel with the main current path. R_P represents the leakage current between the two electrodes, such as direct tunnel, FN tunnel, trap assisted hopping and so on. C_P represents the intrinsic capacitance of the MIM structure of SRR cell. The voltage across both terminals of the SRR can be expressed as the sum of the voltages across the three elements in series, as shown in equation (1)

$$v\,(TE, BE) = v_{DSC} + v_{EFF} + V_{EMF} \tag{1}$$

where v_{DSC} is summation between v_{DSC1} at TE interface and v_{DSC2} at BE interface and v_{EFF} is IR drop at effective layer.

1) SCHOTTKY BARRIER DIODE (D_{SC}, PT–TIO_2 CONTACT)

For a single D_{SC}, a forward-biased current is given as equation (2) with a thermionic emission model when the applied forward-bias voltage of $v_f \gg 3kT/q$ [22].

$$i_f = A_E A^* T^2 \exp\left(-\frac{q\phi_{Bf0}}{kT}\right) \exp\left(\frac{qv_f}{nkT} - 1\right) \tag{2}$$

where A_E represents the effective diode area, A^* is the effective Richardson constant for TiO_2 (6.71×10^6 A/m^{2}K^2), q is the electron charge, ϕ_{Bf0} is the effective Schottky barrier height, k is the Boltzmann constant, T is the absolute temperature, and n is the ideality factor defined as equation (3).

$$n = \frac{q}{kT}\frac{dv_f}{d\ln(i_f)} \tag{3}$$

Equation (1) shows rectifying behavior that varies exponentially with the applied forward-bias voltage and has a very small constant value for reverse-bias due to the fixed value of ϕ_{Bf0}. However, the image force lowering effect caused by Coulombic attraction due to the positive image charges induced inside the Pt by the conduction band electrons in the TiO_2 must be considered for reverse-bias condition. The positive image charges reduce the effective Schottky barrier height by $\Delta q\phi_B$ from $q\phi_{Br0}$ as shown in Fig. 6, and the reverse current can be described by equation (4) when the

applied reverse-bias voltage of $|v_r| \gg 3kT/q$ [22].

$$i_r = -A_E A^* T^2 \exp\left(-\frac{q\left(\phi_{Br0} - \gamma\sqrt{|v_r|}\right)}{kT}\right) \quad (4)$$

where γ is the barrier lowering factor.

For two Schottky diodes with different directions connected in series, as shown in Fig. 5(b), one is forward-biased, and the other is reverse-biased. It has $i_{DSC} = i_f = -i_r$ and $v_{DSC} = V_f - V_r$. Here V_{DSC} is the voltage applied on the two diodes, and i_{DSC} is the current. When a positive bias is applied to the TE, a forward-biased TE/TiO_2 contact and a reverse-biased TiO_2/BE contact are created. The voltage drop then comes mostly from the reverse-biased Schottky diode at TiO_2/BE. Therefore, the v_{DSC} can be approximated as $-V_r$, and the i_{DSC} can be approximated as the reverse-bias current in Equation (4). When a negative bias is applied to the TE, the situation is reversed: the TE/TiO_2 contact determines the current flow.

2) EFFECTIVE LAYER RESISTANCE (R_{EFF})

In SRR devices, the resistance of the effective layer depends on the density of the cations and anions. For HRS, the effective layer holds a high-density of anions and a low density of cations. For LRS, it has the opposite ion densities. In forward-bias, Ra has a different resistance value depending on the value of the state variable ω which is defined as a value between 0 and 1 depending on the ion density of the effective layer. For $\omega = 0$, the resistance is in the HRS state and corresponds to $R_{EFF} = R_{HRS}$. For $\omega = 1$, the resistance is in the LRS state and corresponds to $R_{EFF} = R_{LRS}$. In reverse-bias, the resistance is fixed at R_{HRS}. Therefore, the resistance of Ra is defined by equation (5).

$$R_{EFF} = \begin{cases} R_{HRS}\left(\frac{R_{LRS}}{R_{HRS}}\right)^w, & v_a \geq 0 \\ R_{HRS} & v_{EFF} \leq 0 \end{cases} \quad (5)$$

where v_{EFF} is the applied voltage across the effective layer.

LRS is programmed by applying a forward-bias voltage to the RRAM that is greater than the positive reference voltage, $V_{TH,L}$. Conversely, HRS is programmed with a value less than -$V_{TH,H}$, the negative reference voltage. For bias voltages between -$V_{TH,H}$ and $V_{TH,L}$, the resistance state remains unchanged. Thus, The dynamic behavior of the state variable ω is defined as equation (6) [23].

$$\frac{dw}{dt} = \begin{cases} \alpha\left(v_a - V_{TH,L}\right), & v_a \geq V_{TH,L} \\ \alpha\left(v_a + V_{TH,H}\right), & v_a \leq -V_{TH,H} \\ 0 & otherwise \end{cases} \quad (6)$$

where α is programming rates.

3) NANO-BATTERY EFFECT (V_N)

After the setup and reset process of SRR, ion accumulation can be detected at the electrode-solid electrolyte interface, which leads to a chemical potential gradient within the cell and the generation of electromotive force (emf), the nano-battery effect [24]. The accumulation effect is particularly pronounced in materials where the mobile ions are not initially present or cannot tolerate deviations in stoichiometry. The nano-battery effect affects the RRAM for ON/OFF steady-state and SET/RESET switching voltages; therefore, this effect must be considered in the CBA design. The emf voltage can be defined as equation (7) empirically.

$$V_{EMF} = V_0 + \frac{kT}{2q}\ln\frac{C_{ion}}{C_0} \quad (7)$$

where C_{ion} is ion concentration, and V_0 is defined as the condition where $\ln(C_{ion}/C_0) = 0$ on the V_{EMF} versus log-scaled C_{ion} curve.

4) VARIATION, ENDURANCE, AND RETENTION

Variations in resistive switching kinetics are an important factor affecting the adaptation of RRAM devices to high-density CBAs, so the compact models must predict the potential impact of the variability. The Schottky barrier inhomogeneities present at the TE and BE interfaces result in variations in the I-V characteristics of the SRR based on Schottky emission. The inhomogeneous Schottky barrier model, given by Equation (8), uses a Gaussian approximation of the Schottky barrier height distribution to account for the potential variability at the interface [25].

$$\phi_B^{app} = \overline{\phi_B} - \frac{\sigma^2}{2kT/q} \quad (8)$$

where ϕ_B^{app} is the apparent Schottky barrier height obtained as a result of the convolution of the Gaussian distributed Schottky barrier height with temperature in the thermionic emission model, $\overline{\phi_B}$ is the mean Schottky barrier height and σ is the standard deviation of the Gaussian distribution.

The stability including endurance and retention of the RRAM is an obstacle for the application of CBAs with the resistive switching devices. Interface-type RRAM devices have good endurance performance but poor retention performance. Retention time degradation of the interface-type RRAM occurs naturally, and it has been found that read voltage pulses can exacerbate the degradation process. The resistance of interface-type RRAMs tends to increase over time, which depends on the recombination process of oxygen vacancies and ions [26]. Most of the vacancies are clustered near the TiO_2/BE interface due to their thermodynamic stability [27], and the interface dominates this vacancy recombination process by trapping oxygen or Na ions. Therefore, the resistance stability and failure time depend on the recombination rate of vacancies and ions. This process follows a decay function of $e^{-\lambda t}$, and the Schottky barrier variation with the applied voltage in time can be expressed by equation (9).

$$i_{DSC}(t) = i_{DSC}(0)\,\beta\exp(-\lambda t) \quad (9)$$

where $i_{DSC}(0)$ is the initial current, λ is the decay constant, a parameter related to the average recombination time τ of

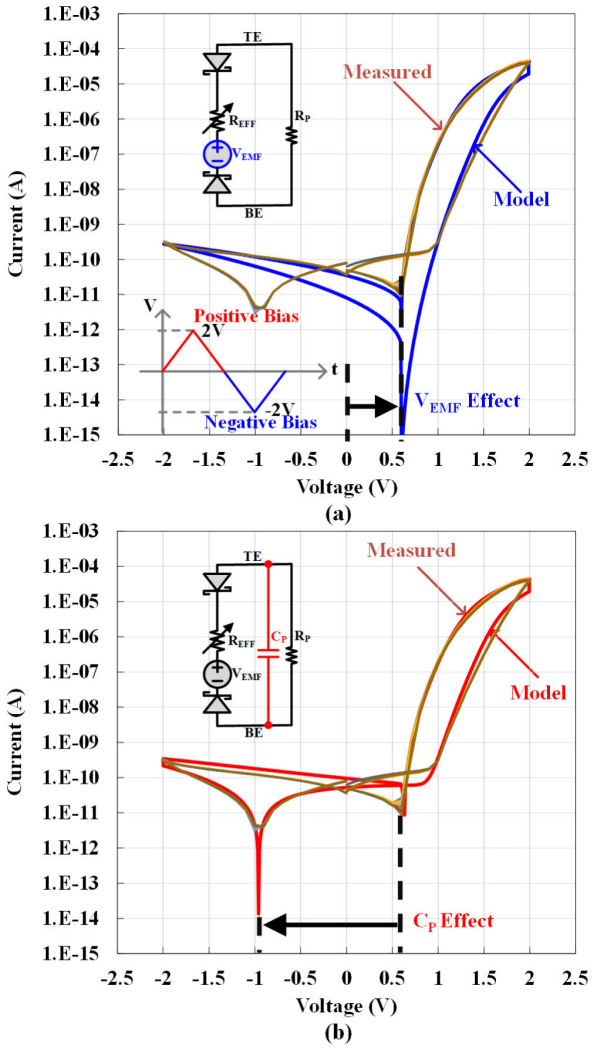

FIGURE 7. Consecutive I–V loops of the proposed Pt/Na:TiO_2/Pt SRR model (a) without and (b) with C_P effect under the applied voltage cycles shown in the bottom left inset.

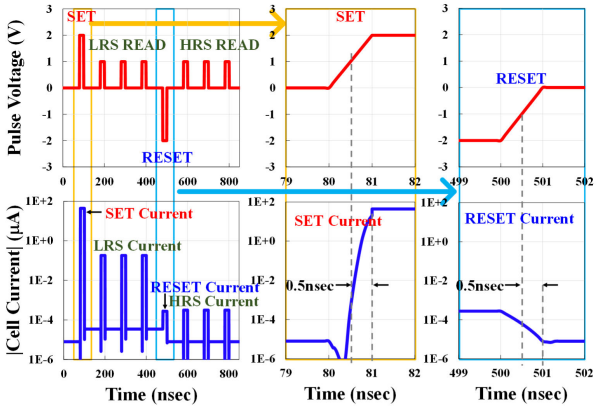

FIGURE 8. Successive SET, RESET, and read operations using the proposed Pt/Na:TiO_2/Pt SRR model.

the vacancies with $\lambda = 1/\tau$, and β is a correction factor ($0 \leq \beta \leq 1$) that reflects the strength of the recombination process.

III. MODEL VALIDATION WITH MEASUREMENTS

Fig. 7 shows the measured current-voltage (I-V) characteristics of the 10 samples and the simulation results for the Na-doped TiO_2 SRR at an external bias voltage that cyclically switches between -2 V and $+2$ V. The applied bias voltage has a sweeping sequence of $0 \rightarrow +2 \rightarrow 0 \rightarrow -2 \rightarrow 0V$ that is a cycle triangle wave over time, as shown in the bottom left inset of Fig. 7(a). When a positive bias is applied to the top electrode, that is, a reverse-bias to the bottom interface, Na cations migrate to the bottom interface. Therefore, the electron injection from the bottom electrode into the Na-doped TiO_2 layer increases due to the increased concentration of Na ions at the bottom interface, which is the SET operation. When a negative voltage is applied after the positive voltage sweep, the electron injection from the top electrode is suppressed due to the decreased concentration of Na at the top interface, resulting in HRS at the negative bias, which is the RESET behavior. Therefore, it exhibits a resistive switching characteristic within ± 2 V, and the switching occurs in the order of HRS $\rightarrow$ LRS $\rightarrow$ HRS. The progressive switching characteristic occurs without a forming process, unlike filamentary switching. For the 10 different SRR samples, an I-V characteristic is observed that is not a zero crossing. Non-equilibrium states are inherently induced during SRR device operation due to non-uniform cation distribution, and these non-equilibrium states can be modeled as a nano-battery (V_{EMF}) of 600 mV.

Fig. 7(a) also shows simulation results using the model described in Section II-B without parasitic capacitance to neglect the parasitic capacitance (C_P) effect (inset in the upper left corner of Fig. 7(a)). The proposed model is mainly coded in Verilog-A, a behavioral language standardized in the semiconductor industry because it can be run on various industrial circuit simulators (Spectre, HSPICE, Eldo, etc.) due to its ease of use and flexibility. The simulation results show well-matched behaviors with the experimental data for the SET/RESET operations and readout current at a readout voltage (V_R) of 1V. For the LRS and HRS conditions, the DC error between the measured and modeled readings is -1.04% and 1.03%, respectively, and the AC error is 0.195% and 1.38%, respectively. However, the simulation results show that the I-V zero crossings of LRS and HRS are the same at 600 mV without parasitic capacitance (C_P), which is different from the measurement of two different zero crossings at 600 mV for LRS and -900 mV for HRS.

Fig. 7(b) shows the simulation results using a model that includes the parasitic capacitance effect (inset in the upper left corner of Fig. 7(b)). During the sweep from $0 \rightarrow +2V$ in the HRS state, the current through the capacitor flows in the direction of increasing the overall current. During the sweep from $+2 \rightarrow -2V$ in the LRS state after a SET operation at 2 V, the current flowing through the capacitor flows in the direction of decreasing the overall current. This means that the zero crossing of the HRS is formed at a voltage lower than the V_{EMF} and the zero crossing of the LRS is

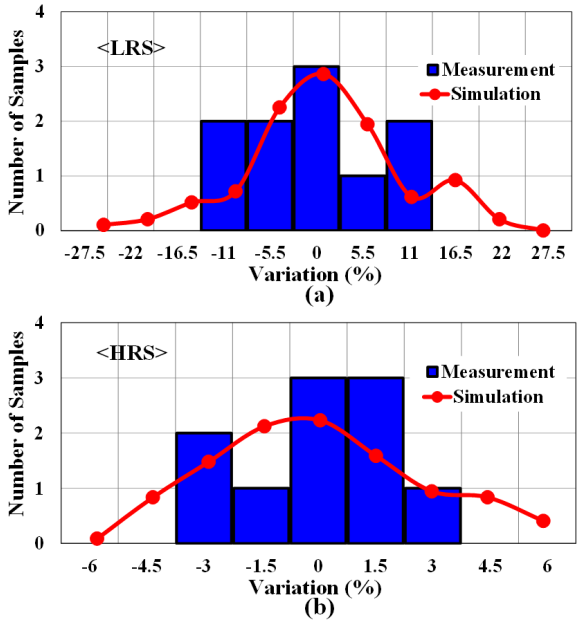

FIGURE 9. Cell current variation of Pt/Na:TiO_2/Pt SRR with 10 samples and normalized 100 simulations for (a) LRS and (b) HRS.

formed at a voltage higher than the V_{EMF}. Therefore, the model with the parasitic capacitor has two different I-V zero crossings as measured. However, since the amount of current flowing through the capacitor is insignificant compared to the amount of current in the LRS state and is compatible with the amount of current in the HRS state, the zero-crossing of the LRS varies little with V_{EMF}, but the zero-crossing of the HRS varies significantly so that only the zero-crossing of the HRS appears to deviate significantly from V_{EMF}. Therefore, the proposed model matches well with the measurements in the SET/RESET operations, the readout currents, and the low-current region where zero crossings occur.

A simulation of electrical pulses applied to successive SET, RESET, and read operations using the proposed model is shown in Fig. 8. The pulse widths were fixed to 20 nsec. The simulation shows that the SRR changes from the HRS state to the LRS state after a +2 V program pulse, and from the LRS state to the HRS state after a −2 V program pulse. The state changes occur in less than 0.5 nsec. After the SET/RESET operation, a steady LRS/HRS current value is delivered at a continuous +1 V readout voltage. The current values for LRS and HRS are 180 nA and 314 pA, respectively. Based on these results, the fabricated pt/Na:TiO_2/Pt structures are operated with programmable pulses commonly used in conventional electronics, demonstrating excellent applicability.

Device-to-device variations which is attributed to the nonuniformity of the patterned electrodes have created significant challenges for circuit design for SRR CBA integration. After applying the SET and RESET voltages to form the LRS and HRS, the experimental read-out currents of the 10 different samples are obtained. The current distributions are illustrated in Fig. 9 for LRS and HRS, and the average value and the percentage change from the average

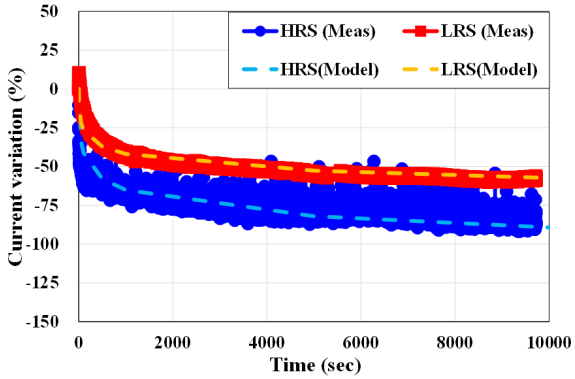

FIGURE 10. Measurements and simulation results for retention time of Pt/Na:TiO_2/Pt SRR.

value are calculated. The LRS distribution has a standard deviation of 9.06 % and the HRS has a standard deviation of 1.92 %. In Verilog-A, the Gaussian distribution of the apparent Schottky barrier height of ϕ_B^{app} is generated using the \$rdist_normal(seed, μ, σ) command, where the seed is an integer used to initialize the random number generation process, μ is set to 0, and σ is set to the corresponding values of the measured LRS and HRS current distributions. After performing simulations with 100 different devices with the proposed model, the standard deviations of the simulation results for LRS and HRS are found to be 9.50 % and 2.08 %, respectively. The histogram of the simulation results is normalized to 10 samples to match the measured data.

Fig. 10 shows the retention properties of the Pt/Na:TiO_2/Pt device with a repeated reading procedure for 10^4 sec at +1 V of the read voltage after +2 V for the SET or −2 V for the RESET operations as shown in the bottom left inset of Fig. 10. High temperature of 125°C accelerate the movement of ions and aggravate the degradation and instability. The LRS and HRS tend to drift toward the higher resistance after SET/RESET operations. This suggests that both the HRS and LRS decay spontaneously, and the HRS variation is more pronounced than the LRS variation. The current degradation rate of the HRS and LRS can be calculated by the slope of linear fitting in log(I)-log(time) scale respectively. The equation (9) is used to fit the current decay process, and the excellent agreement between simulation and measurement results confirms the retention validity of the proposed compact model.

Fig. 11 shows a 1000-cycle endurance test with SET and RESET voltages of +2 V and −2 V and a readout voltage of +1 V, respectively. The measurement voltage pulse sequence is shown in the inset of Fig. 11. The device shows excellent endurance performance, and the proposed compact model provides the same current for the first readout current immediately after SET and RESET operations.

IV. CBA APPLICATIONS WITH SRR

A distinctive feature of RRAM is that its conductivity depends on past electrical signals, allowing it to operate

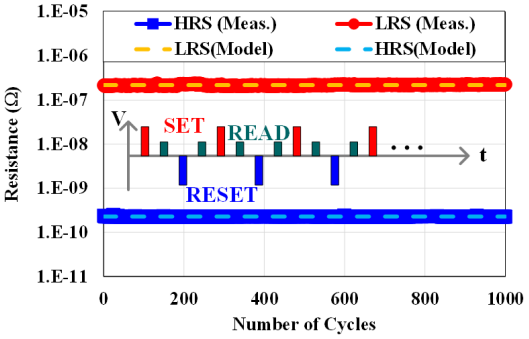

FIGURE 11. 1000 cycles of continuous switching in an Pt/Na:TiO_2/Pt SRR for endurance measurement and simulation analysis.

as a non-volatile memory. In addition, unlike the binary states of "0" and "1" in traditional digital storage systems, memristors can store multiple bits of information using continuously adjustable conductivity, enabling higher bit densities. Due to their non-volatility, fast programming, low programming energy, and small footprint, memristors are emerging as a promising solution for the next generation of embedded memory that can combine the advantages of SRAM and floating gate transistors. The simple two-terminal metal-insulator-metal (MIM) structure of RRAMs allows them to be integrated into high-density crossbar arrays. In the readout operations, the sneak-path mentioned in the introduction leads to additional energy consumption in unselected cells, which degrades the read margin and limits the array size. It is important to note that the average current issue, which is prominent in sequential read and write isolated memristors in crossbar arrays, has less of an impact on both machine learning and neuromorphic computing.

To mitigate the sneak-path problem, a bias scheme has been proposed for the write/read process by applying a fractional voltage to unselected cells. The floating bias scheme keeps all unselected words and bit-lines floating, as shown in Fig. 12(a). CBAs with the floating method can exhibit good energy efficiency with very high-density, but the sneak currents flow if the unselected three cells in series are not adequately suppressed. In the 1/2V bias scheme, the full voltage of V and 0 V are applied to the selected word-lines and the selected bit-lines, respectively, and 1/2V is applied to unselected word-lines and bit-lines, as shown in Fig. 12(b). This results in a V bias for selected cells, 1/2V for half-selected cells, and a 0V bias for unselected cells. The 1/3V bias scheme shown in Fig. 12(c) applies full voltage of V and 0 V to the selected word-line and the selected bit-line, respectively, the same as the 1/2V situation. 1/3V is applied to the unselected word-line and 2/3V is applied to the unselected bit-line. This puts the selected memory cells in a V bias, the semi-selected memory cells in a 1/3V bias, and the unselected memory cells in a 1/3 or −1/3V bias. A nano-battery bias scheme that utilizes the nano-battery effect is proposed. For SRR with Pt/Na:TiO_2/Pt structure, it has zero current at V_{EMF} bias rather than at 0V bias. A full voltage of V and 0 V is applied to the selected word-lines and selected bit-lines as

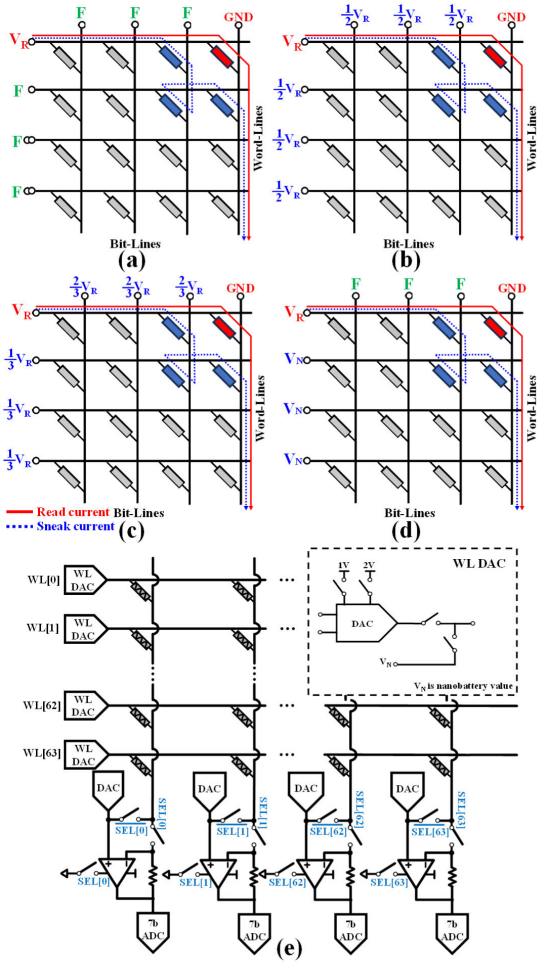

FIGURE 12. Conventioanl bias schems (a) with floating bias, (b) with 1/2V bias, and (c) with 1/3V bias. (d) Proposed nano-battery bias scheme and (e) schematic diagram of CBA architecture with the proposed bias scheme.

in the 1/2 V and 1/3 V bias schemes. The bit-lines of the unselected cells are floated and the word-lines are biased at V_{EMF}, as shown in Fig. 12(d).

The read current is measured with a 64 × 64 SRR CBA. The current error is calculated as $I_{ERR} = I_{BIT} / I_{CELL}$ based on the four bias methods mentioned earlier. I_{BIT} is the current flowing on one bit-line in a 64 × 64 CBA when applying the full voltage of V and 0 V to one cell and the other biases determined by each bias scheme to the remaining cells, while I_{CELL} is the current obtained by applying the maximum voltage V and 0V to only one cell without considering the 64 × 64 SRR cell arrangement. I_{BIT} is the sum of I_{CELL} and I_{SNK}, where I_{SNK} is the sneak-path current in the CBA. The current error of the floating bias method is 176.8 % since the sneak current cannot be suppressed even with the SRR cells when the three unselected cells are connected in series. The conventional 1/2V and 1/3V bias schemes apply partial bias voltages in series to the three unselected cells to reduce the current error to 0.45 % and 0.70 %, respectively. The 1/2V bias scheme has less error than the 1/3V bias scheme since the current at 0.33 V using the 1/3V scheme

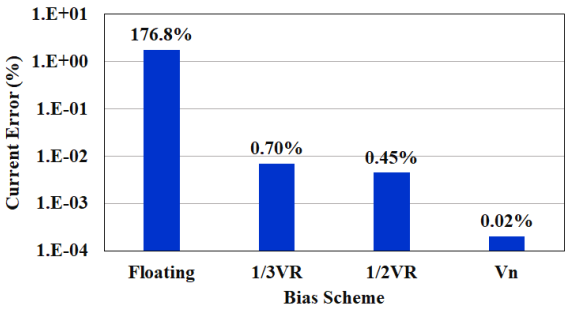

FIGURE 13. Comparison with various bias schemes for sneak-path current error.

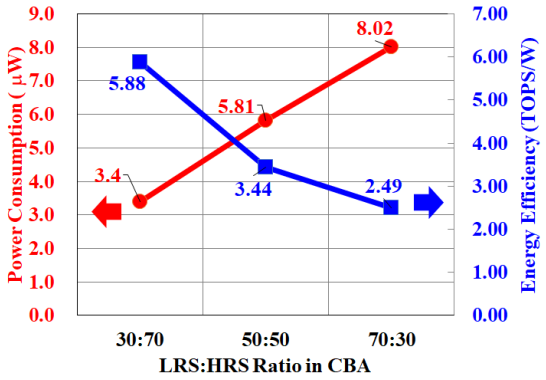

FIGURE 14. CBA power consumption and energy efficiency with different LRS:HRS ratios.

is higher than the current at 0.5 V using the 1/2V scheme, as shown in Fig. 13. The proposed V_{EMF} bias scheme can reduce the current error to 0.02 % because it provides zero current to unselected cells. It can also reduce the complexity of the readout circuit because it only requires a word-line bias circuit compared to the 1/2V and 1/3V bias schemes that use both word-line bias and bit-line bias, as shown in Fig. 12(e).

The non-volatile property of RRAM naturally lends itself to consolidating computations into memory and converting them into weighted sums. The MAC capabilities of memory arrays can greatly improve the computational efficiency of in-memory computing. The MAC, also known as vector matrix multiplication (VMM), is an important and expensive operation often used in neural network structures. The VMM performs the multiplication and accumulation process of computing the product of two numbers and adding that product to an accumulator. Many basic operations, such as dot multiplication, matrix multiplication, digital filter operations, and even polynomial evaluation operations, can be decomposed into VMM operations, as expressed in equation (10) [28].

$$\begin{bmatrix} G_{11} & G_{12} & \cdots & G_{1n} \\ G_{21} & G_{22} & \cdots & G_{2n} \\ \vdots & \vdots & \vdots & \vdots \\ G_{n1} & G_{n2} & \cdots & G_{nn} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_n \end{bmatrix} = \sum_{j=1}^{n} G_{ij} \cdot V_j = I_i \tag{10}$$

The total current on the i-th bit-line, I_i, is the sum of the currents through each RRAM cell in this column according to Kirchhoff's current law, where the current through each RRAM cell is the j-th word-line input voltage, V_j, and the conductance of the RRAM cell at the i-th and j-th indices, G_{ij}, according to Ohm's law. The ability to perform parallel VMM operations using RRAM thus enables general acceleration of all matrix operations, which naturally translates to the analog domain for low-power, high-speed operations. The scalability and flexibility of the array architecture also makes it very easy to reprogram, providing excellent hardware acceleration for a wide variety of VMM-based applications.

The proposed Pt/Na:TiO2/Pt SRR model is used to simulate the power consumption and energy efficiency of a 64 × 64 CBA in 180 nm CMOS technology for inference operation. In addition to the unit cell model, the parasitic resistance and capacitance of the CBA interconnects that affect the voltage drop, time delay, and power consumption are also included. Every cell in a 64 × 64 CBA performs a VMM operation with a 100 nsec period, and the cell read voltage is +1V. With an LRS to HRS ratio of 30:70, the power consumption of the CBA is $3.4\mu W$. As the LRS to HRS ratio increases, the power consumption increases linearly to $8.02\mu W$ for an LRS to HRS ratio of 70:30. TOPS/W (tera operations per second per watt) is used as a metric to estimate computational energy efficiency, where 1 OPS is defined as one analog multiplication or addition operation per second. The energy efficiency is estimated with 32-bit fixed-point precision. The energy efficiency of the CBA is 5.88 TOPS/W with an LRS to HRS ratio of 30:70, which decreases to 2.49 TOPS/W with a 70:30 ratio.

A deep neural network (DNN) is a type of machine learning algorithm, similar to an artificial neural network, that aims to mimic the brain's information processing. DNNs have one or more hidden layers between the input and output layers, as shown in Fig. 15(a). Each layer contains a given number of neurons that apply a specific functional transformation to the input. VMMs are the most common operation implemented in hardware for DNNs. However, DNNs are quite deep in layers and require an enormous amount of VMM operations, which require a large number of weights and a large input dataset.

The open-source simulator MNSIM [29] is used to evaluate the combined impact of all SRR non-idealities on DNN inference accuracy for the CIFAR-10 dataset. Simulations are performed using built-in DNN models including LeNet, AlexNet, VGG8, VGG16, and ResNet18. The accuracy is compared by applying the idealized RRAM model from the MNSIM package and the proposed SRR compact model to each DNN model. The accuracy depends on the number of convolution layers of the networks and the number of channels of each layer. Figure 12 shows the top-5 accuracy of each DNN model. VGG-16 and VGG-8 achieve higher accuracy than LeNet, AlexNet, and Resnet-18. The degradations of VGG-8 and VGG-16 are 1.36% and 4.46% respectively, which is much lesser than those of LeNet, AlexNet, and Resnet-18 since there is more redundancy in

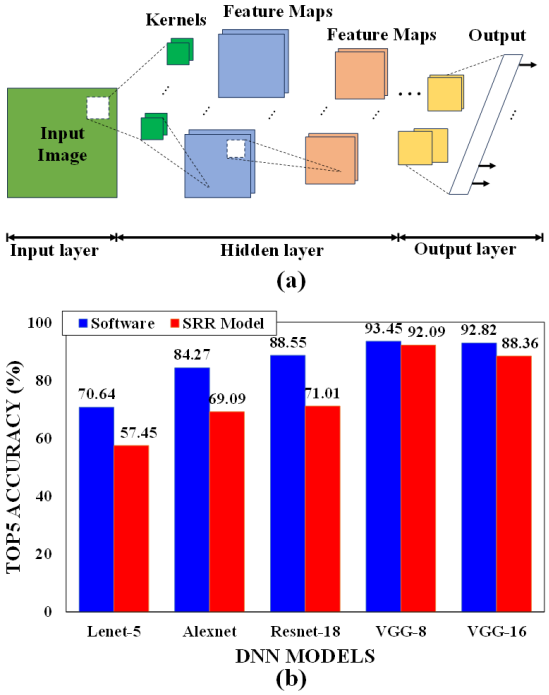

FIGURE 15. (a) Structure of the VGG-8 convolutional neural network for CIFAR-10 32 × 32 color image classification and (b) accuracy comparison with different neural network architectures.

VGG-8 and VGG-16. The Resnet-18 network has the worst accuracy degradation of 17.54% as it typically uses a much smaller number of fully connected layers than the other networks.

V. CONCLUSION

In this paper, a physics-based compact model for self-rectifying RRAM devices with bipolar switching characteristics is presented, and it is validated with the measured data from Pt/Na:TiO_2/Pt devices. The model simplifies the RRAM switching mechanism by using essential equations. The model considers the concentration of Na+ cations in the effective layer near the bottom electrode and the effect of Schottky barrier lowering under forward and reverse-bias. The developed compact cell model consists of Schottky barrier diodes, effective layer resistance, nano-battery effect, and parasitic resistance and capacitance. The I-V characteristics in HRS and LRS of with self-rectifying resistive switching behavior can be reproduced with high accuracy of 98.97% on DC and 98.05% on AC by the proposed model. Moreover, the proposed model also reproduces the behavior of different non-zero I-V crossings in HRS and LRS when the bias voltage is applied in a triangular waveform alternating between positive and negative with time. It also includes physics-based models of device-to-device variability, retention, and endurance, and is validated with measurement data.

The proposed model is applied to a neuromorphic 64 × 64 SRR CBA to simulate the sneak current. The proposed bias scheme utilizing the nano-battery voltage rather than the conventional 1/2V or 1/3V reduces the sneak current error to 0.02% in the interface-type SRR SRR array. Moreover, the SRR CBA also achieves 3.44 TOPS/W at a 50:50 LRS to HRS ratio in 32-bit fixed-point precision VMM operations. The computation of the DNN is significantly expedited by the resistive CBA since the RRAM devices can save weight factor, and the CBA provides multiplication and accumulation in one cycle in analog domain as explained in Section IV. From the proposed model, we can extract the degree of non-ideality of SRR cells as a function of the size of the crossbar array and use it to estimate the accuracy degradation of DNNs using SRR CBA. Several DNN benchmarks using MNSIM for CIFAR-10 datasets are observed that the accuracy degradation can be significant, ranging from 1.36 % to 17.54 %. The excellent agreement between model predictions and measured data shows promising prospects for future implementation of this compact model in circuit simulations and optimizing the design of SRR CBAs.

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(Jin-Wook Kim and Jun-Seok Beom are co-first author.)

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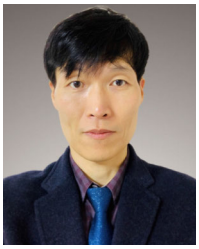

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