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RESEARCH ARTICLE

An Efficient Technique to Simulate the AC/DC Parameters of Trigate FinFETs

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ABSTRACT This paper discusses the alternating-current (AC) and direct-current (DC) characteristics of Trigate FinFETs. A modified non linear DC model is proposed to predict $I - V$ characteristics with effect of an efficient technique for the extraction of AC small signal parameters. The extraction of small signal parameters using S-measurements can be developed on advance design system (ADS) software which is based on the electrical behavior of the device. It examines the electrical response as it depends on bias voltages and the extrinsic and intrinsic parameters of Si FinFETs. The approaches discussed here are valid over a range of frequency starting from few Hz up to several tens of GHz. In this paper equivalent circuit procedure has been adopted to compute device AC parameters based on its measured AC response. The characteristics were then simulated by developing a Matlab code based on particle swam optimization (PSO) technique and compared with technology computer aided design (TCAD) data. The results shows that the good agreement are achieved between simulated and TCAD data.

INDEX TERMS FinFETs, DC characterization, FinFET AC parameters.

I. INTRODUCTION

Shrinkage of the devices carried out due to massive demand of the electronic industry and further reduction in size causes non ideal behavior of the devices known as short channel effects [1]. A three dimensional (3D) device Fin Field-Effect Transistor (FinFET) was introduced to cater these effects [2], [3]. FinFETs are enclosed by gates on three sides, forming 3D structures of the device, which results in additional control over the device [4] and reduces short-channel effects, consequently lowering leakage current. The structure of FinFETs, as illustrated in Fig. 1, with its reduced leakage current, makes them a highly valuable and relevant option [5].

The 3D structure of FinFETs overcome the limitations of planar Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) such as reduces channel length through the thickness of fin-shaped channel. FinFETs have gained significant attention in recent years because of their superior electrostatic control, low leakage, and high drive current [6].

Analytical modeling of FinFETs is important for optimizing their design and improving their performance. It can help to identify the key design parameters that affect the device performance, such as the gate length, fin width, and gate oxide thickness. It can also aid in the development of new FinFET structures and technologies, such as stacked or vertical FinFETs [7]. Overall, analytical modeling is a powerful tool for understanding and predicting the behavior of FinFETs, and it is essential for the continued advancement of semiconductor technology [8], [9], [10]. Analytical

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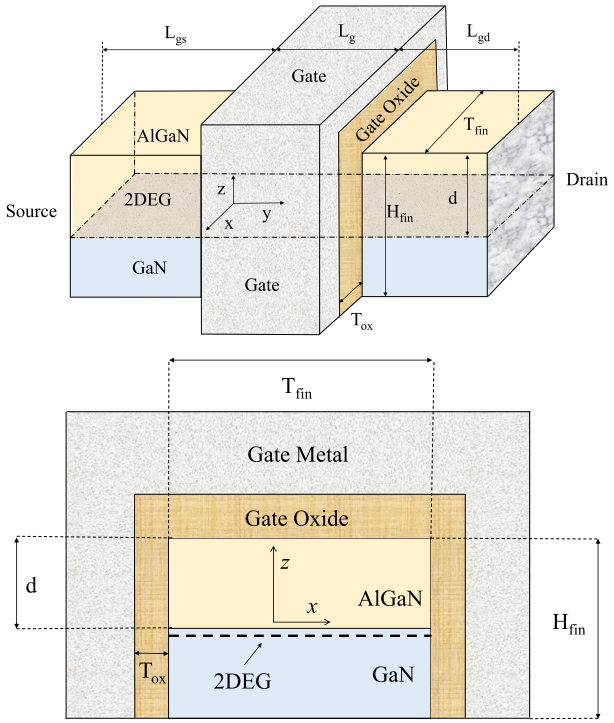

FIGURE 1. Cross sectional view of Tri-gate FinFET.

modeling of FinFETs has been extensively studied in the literature, researchers reported various models to accurately capture the electrical behavior of the devices. In recent years, researchers have continued to propose new analytical models for FinFETs that incorporate various physical effects, such as impact ionization, mobility degradation, and temperature dependence [11], [12]. These models have advanced our understanding of FinFETs and have contributed to the continued improvement of semiconductor technology. One of the earliest analytical models for FinFETs was proposed in 2002 by Pei et al. [3]. The model used analytical solution of 3-D Laplace's equation and by reducing fin thickness or fin height of silicon they controlled the Short-channel effects (SCE) of the FinFET reasonably. The model was validated against experimental data and showed good agreement of FinFETs DC characteristics.

Zhang et al. [13] proposed an improved surface potential-based analytical model for FinFETs that included the effects of drain-induced barrier lowering and channel length modulation. They showed that with the effect of hot carrier injection by the forward gated method, the extraction result of the interface state distribution in FinFET and validated against experimental data and showed good accuracy in predicting the device performance. Kim et al. [14] proposed a universal charge model by using the arbitrary potential technique. By using this charge model, they incorporated the effects of finite doping density in the channel and subthreshold inversion for undoped FETs. Further, they developed a novel analytical model for multiple-gate FinFETs that included the effects of quantum confinement and surface roughness on the device performance.

Srivastava et al. [15] designed a FinFET-based temperature sensor for high-temperature applications. They used a silicon-on-insulator (SOI) process to fabricate the FinFET sensor and demonstrated that the FinFET sensor has better sensitivity and linearity than the conventional MOSFET-based sensor. They also showed that the FinFET sensor can operate at temperatures up to 200°C.

Recently, Kang et al. [16] proposed a novel double-gate FinFET architecture with a vertical gate-all-around (VGAA) structure. They demonstrated that the VGAA FinFET exhibits better electrostatic control, gate control, and short-channel effects compared to the conventional single-gate FinFET. They also showed that the VGAA FinFET can be used for low-power and high-performance applications. Li et al. [17] proposed a FinFET-based floating-gate memory device. They demonstrated that the FinFET-based memory device has better performance in terms of write/erase speed, endurance, and retention compared to the conventional MOSFET-based memory device. They also showed that the FinFET-based memory device can be used for low-power and high-density memory applications.

The literature review shows that FinFETs have gained significant attention in recent years because of their superior electrostatic control, low leakage, and high drive current. Researchers have investigated various aspects of FinFET devices, including the impact of device parameters, temperature sensing, novel device architectures, crystal orientation, and memory applications. The results of these studies suggest that FinFETs have the potential to revolutionize the semiconductor industry by enabling low-power and high-performance electronic devices. Design of RF and analog circuits are much difficult in planar MOSFETs due to high leakage current, noise degradation and less matching performance. Therefore, certain novel device 3D structure are reported to address this issue. A 3D structure FinFET devices offer superior electrical properties, because fins are mostly left undoped. Thus, variability due to dopant fluctuations is eliminated, resulting in good matching behavior [18]. The fin shaped structure suppress the short channel effects, provide better electrostatics characteristics and gives higher current and power density then conventional FETs.

FinFET also called tri-gate FETs because the channel covers from three side with the gate. Fig. 1 shows a typical front view of a AlGaN/GaN FinFET device that have reassembles with HEMT structure. The only difference is channel envelops with all three side of the gate as seen from the figure and provide good control for device handling.

Miller capacitors, C_{gs} and C_{gd} play an important role in the device AC performance, as they relate the incoming changing signal to the device channel. As a result, they inhibit the maximum operating frequency, f_{max} of FET devices. Due to the tri-gate geometry, both C_{gs} and C_{gd} of FinFETs are relatively lower compared to conventional FETs thus, they offer high operating frequency.

FinFETs are getting great attraction in RF industry due to their relatively lower short channel effects and high operating frequency. The BSIM-CMG [19] is the first standard model of FinFET that is commercially available. Parasitic resistances and capacitances of the device have a significant impact on the FinFET's properties at high frequencies. As a result, the BSIM-CMG is incapable to predict device behaviour for wideÂ range of frequencies. Most of reported literature aims to develop accurate and higher efficient model which support to develop a device for fabrication. However, they provide a low range of frequency up to 110 GHz [20]. Katayama et al. [21] proposed the 65-nm low noise amplifier of CMOS up to 300 GHz. The authors did not provide detailed parameter extraction methods, however these models are suitable for 2-D planar MOSFETs. Wang et al. [22] reported the FinFET model for RF application, it provided a method for extracting model parameters for the range of 200 MHz to 50 GHz. Most of reported model describe the behavior of DC characteristics. Furthermore, current modeling approaches often fail to account for the rapid advancements in transistor technologies. An accurate and innovative model is required to develop the characteristics for 3D structure of the device. In addition for RF Operation, the small signal equivalent circuit can also be utilized for large signal, non quasi static model, junction less model and noise equivalent circuit model.

In this paper, AC and DC analysis of FinFET is performed considering equivalent circuit approach based on device electrical behavior. Initially an empirical DC model have been developed to optimize the DC characteristics. While, for AC behavior, a 3D FinFET equivalent circuit consists of resistors, capacitors and inductors. It is placed in such a way the device gives AC response over a range of frequencies starting from a few GHz to hundred of GHz.

II. DC PERFORMANCE

Due to small gate length, FinFETs has revolutionized the integrated circuits industry as it allows compact packing. FinFETs usage increased into ICs fabrication as it can operate under low voltage conditions with minimum battery consumption. It is a voltage controlled current device, in which current is controlled by the applied potential that produce potential difference which causes the non uniform depletion across the channel.

Under the applied voltages V_{ds}, drifting start in carriers with velocity v to produce a drain to source current I_{ds} which is proportional to the applied potential. Further increase in potential does not effect on current I_{ds} and this position is called saturation voltages $V_{ds(sat)}$ of the device. Also, with the change in V_{gs}, depletion height of 3D channel changes and when V_{gs} approaches to threshold value, V_{th} device act in pinch off condition.

A tri-gate FinFET has same structure and operation like conventional MOSFET devices. Rudenko et al. [23] proposed that, for $V_{gs} > V_{th}$, drain to source current I_{ds} can expressed

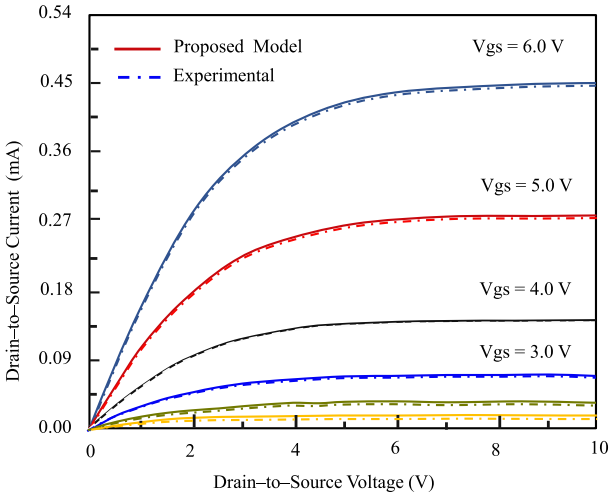

FIGURE 2. Modeled and experimental $I - V$ characteristics of n-type FinFETs.

as

$$I_{ds} = \frac{W}{L_g} C_{ox} \mu V_{ds} (V_{gs} - V_{th}) \tag{1}$$

In Eq. 1, L_g is the gate length, W is the gate width, μ is the mobility of the device and C_{ox} defines the capacitor oxide of the device respectively. μ also play a crucial rule as the electric field that is generated by applied voltages is effected and it attain its maximum value when V_{gs} increases. As V_{gs} increases, I_{ds} will also increase for V_{gs} just above V_{th}. Eq. 1 is further modified to accommodate short channel effects and shift in V_{th} [24].

$$I_{ds} = \frac{W}{L_g} C_{ox} \mu V_{ds} (V_{gs} - V_{th}) \left(1 + \lambda V_{ds} + \frac{\delta V_{gs}}{V_{ds(\text{sat})}}\right) \times \tanh(\alpha V_{ds}) \tag{2}$$

In Eq. 2, δ simulates the nonideality in Schottky barrier of a FinFET, α is fitting variable to adjust the slope of curve, λV_{ds} takes into account finite output conductance g_d and $V_{ds(\text{sat})}$ is the saturated value of V_{ds} at which the carriers attain the saturation velocity. In order to check the validity of Eq. 2, a submicron FinFET with L_g 1 μm and W 140 nm was selected [25] with the help of MATLAB code. For this purpose, particle swarm optimization (PSO) technique is used with an objective function given by Eq. 3

$$\varepsilon = \sqrt{\sum_{j=T_1}^{P} \left\{ \sum_{i=T_2}^{Q} \left(I_{ds(exp)}^{i,j} - I_{ds(sim)}^{i,j} \right)^2 \Big/ \sum_{i=T_2}^{Q} I_{ds(exp)}^{i,j} \right\}}. \tag{3}$$

In Eq. 3, for the termination of optimization technique (PSO), variable ε ensure a minimum error value where, P and Q represent the V_{ds} and V_{gs} biasing values having minimum values T_1 and T_2, respectively, whereas $I_{ds(exp)}$ and $I_{ds(sim)}$ represent experimental and simulated I_{ds} values, respectively.

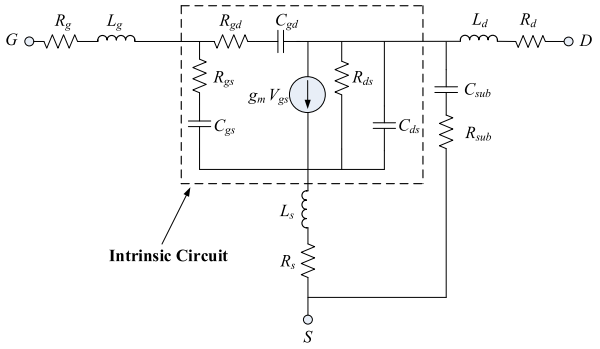

FIGURE 3. AC circuit of trigate FinFET.

III. AC PERFORMANCE

To study the AC capability of FinFET devices, knowledge of small signal parameters is a fundamental requirement. The most common AC equivalent circuit model used for FinFET AC parameters extraction is given by Fig. 3. This circuit can be further divided into two parts: the section enclosed by the dotted line represents the intrinsic parameter circuit model, while the remaining portion represents the extrinsic parameter circuit representation. The system is represented as a two port network and AC equivalent circuit can be developed by the following parameters. Gate-to-drain intrinsic capacitance C_{gd}, Gate-to-source intrinsic capacitance C_{gs}, Drain-to-source intrinsic capacitance C_{ds}, Transconductance g_m, Parasitic source, drain and substrate loss resistances, R_g, R_s, R_d and R_{sub}, Intrinsic resistances R_{gs} R_{ds} and R_{gd}, Unity gain frequency f_T, and maximum frequency f_{max}. To evaluate the effect of substrate on the AC performance of FinFET device, C_{sub} and R_{sub} elements are used in the model.

Extrinsic components are bias independent, while intrinsic are bias dependent [26]. The intrinsic capacitances, also known as Miller capacitances, such as C_{gs}, C_{gd} and C_{ds} play an important role in AC performance of the device. τ is the gate depletion charging and discharging time that directly effects the trans-conductance g_m of the device and for high speed and high gain it should be high for small value of τ. Output conductance g_{ds} and R_{ds} are generally reciprocal of each other and ideally g_{ds} should be small. It is well known fact that the device extrinsic parameters are material and technology dependent. To enhance the power handling capabilities of the device, R_s and R_g values should be small, whereas R_d controls the breakdown voltage of the device. While, pad capacitances has a small effect due to low magnitude as compared to other intrinsic capacitances and therefore omitted from the circuit.

A. ADMITTANCE OF EXTRINSIC CIRCUIT

Device operational capabilities are mostly dependent on intrinsic part of the device however, extrinsic part also important as signal would leave or reach the device through extrinsic part and that's why device S-parameters have strong impact on both intrinsic and extrinsic parameters. Dambrine et al. [27] proposed an appropriate de-embedding technique by involving S-parameters to approximate the AC parameters of the device. The two port network of extrinsic section of 3D FinFET equivalent circuit can be expressed in terms of Y-parameters as a function of terminal voltage relations:

$$I_1 = Y_{11}V_1 + Y_{12}V_2 \tag{4}$$

$$I_2 = Y_{21}V_1 + Y_{22}V_2 \tag{5}$$

Y parameters (Y_{ext}) of extrinsic part can be calculated and matrix of extrinsic circuit can be written as

$$Y_{ext} = \left(Z_{ext}\right)^{-1} = \begin{bmatrix} R_g + R_s + j\omega\left(L_g + L_s\right) & R_s + j\omega L_s \\ R_s + j\omega L_s & R_d + R_s + j\omega\left(L_d + L_s\right) \end{bmatrix} \tag{6}$$

B. ADMITTANCE OF INTRINSIC CIRCUIT

The two port network can be computed From Eq. (4)-(5) of intrinsic equivalent circuit

$$Y_{11} = \left.\frac{I_1}{V_1}\right|_{V_2=0} = \frac{j\omega C_{gs}}{j\omega C_{gs}R_{gs}+1} + \frac{j\omega C_{gd}}{j\omega C_{gd}R_{gd}+1} \tag{7}$$

$$Y_{12} = \left.\frac{I_1}{V_2}\right|_{V_1=0} = -\frac{j\omega C_{gd}}{j\omega C_{gd}R_{gd}+1} \tag{8}$$

$$Y_{21} = \left.\frac{I_2}{V_1}\right|_{V_2=0} = \frac{g_m e^{-j\omega t}R_{gs}}{1+j\omega R_{gs}C_{gs}} - \frac{j\omega C_{gd}}{j\omega C_{gd}R_{gd}+1} \tag{9}$$

$$Y_{22} = \left.\frac{I_2}{V_2}\right|_{V_1=0} = j\omega C_{ds} + \frac{1}{R_{ds}+j\omega L_{ds}} + \frac{j\omega C_{gd}}{j\omega C_{gd}R_{gd}+1} \tag{10}$$

Using Eq. (7) to (10), Intrinsic circuit matrix becomes (11), as shown at the bottom of the next page.

Above matrix can also be represented as

$$Y_{int} = \begin{bmatrix} \frac{j\omega\alpha}{j\omega\beta+1} + \frac{j\omega\gamma}{j\omega\lambda+1} & -\frac{j\omega\gamma}{j\omega\lambda+1} \\ \frac{\alpha_2 e^{-j\omega\alpha_3/\alpha_2}}{1+j\omega\beta} - \frac{j\omega\gamma}{j\omega\lambda+1} & j\omega\eta + \frac{1}{\frac{\zeta}{\zeta_2}+j\omega\zeta} + \frac{j\omega\gamma}{j\omega\lambda+1} \end{bmatrix} \tag{12}$$

Here, $C_{gs} = \alpha$, $R_{gs} = \beta/\alpha$, $C_{gd} = \gamma$, $C_{ds} = \eta$, $R_{gd} = \lambda/\gamma$, $L_{ds} = \zeta$, $R_{ds} = \zeta/\zeta_2$, $g_m = \alpha_2$, and $\tau_m = \alpha_3/\alpha_2$

$$Re(Y_{11}) = \frac{\omega^2\alpha\beta}{1+\omega^2\beta^2} + \frac{\omega^2\gamma\lambda}{1+\omega^2\lambda^2} \tag{13}$$

$$Im(Y_{11}) = \frac{\omega\alpha}{1+\omega^2\beta^2} + \frac{\omega\gamma}{1+\omega^2\lambda^2} \tag{14}$$

$$Re(Y_{12}) = -\frac{\omega^2\gamma\lambda}{1+\omega^2\lambda^2} \tag{15}$$

$$Im(Y_{12}) = \frac{\omega\gamma}{1+\omega^2\lambda^2} \tag{16}$$

$$Re(Y_{21}) = \frac{\alpha_3}{1+\omega^2\beta^2} + \frac{\omega^2\gamma\lambda}{1+\omega^2\lambda^2} \tag{17}$$

$$Im(Y_{21}) = -\frac{\alpha_3}{1+\omega^2\beta^2} + \frac{\omega^2\gamma\lambda}{1+\omega^2\lambda^2} \tag{18}$$

$$Re(Y_{22}) = \frac{\zeta/{\zeta_2}^2}{\zeta/{\zeta_2}^2+\omega^2\zeta^2} + \frac{\omega^2\gamma\lambda}{1+\omega^2\lambda^2} \tag{19}$$

$$Im(Y_{22}) = \omega\eta - \frac{\omega\zeta}{\zeta/{\zeta_2}^2+\omega^2\zeta^2} - \frac{\omega\gamma}{1+\omega^2\lambda^2} \tag{20}$$

$$Y = Y_{ext} + Y_{int} \tag{21}$$

Then Y components can be transform into S-parameters matrix can be defined as (22)–(26), shown at the bottom of the next page, where $Y_0 = 1/Z_0$ and Z_0 is the characteristic impedance, ΔY can be written as

$$\Delta Y = (Y_0 + Y_{11})(Y_0 + Y_{22}) - Y_{12}Y_{21} \tag{27}$$

Intrinsic parameters of the device at a given frequency, can be assessed by using the following equations.

$$C_{gd} = -\frac{Im(Y_{12})}{\omega} \tag{28}$$

$$C_{ds} = \frac{Im(Y_{22})}{\omega} - C_{gd} \tag{29}$$

$$C_{gs} = \frac{Im(Y_{11})}{\omega} - C_{gd} \tag{30}$$

$$g_{ds} = Re(Y_{22}) \tag{31}$$

$$g_m = Re(Y_{21}) \tag{32}$$

$$R_i = \frac{1-\left(1-\frac{4Re(Y_{11})}{\omega^2 C_{gs}^2}\right)}{Re(Y_{11})} \tag{33}$$

$$\tau_m = -\frac{1}{\omega}tan^{-1}\frac{Im(G)}{Re(G)} \tag{34}$$

where

$$Im(G) = g_m e^{-j\omega\tau_m} = Re(Y_{21}) - Im(Y_{21})R_i C_{gs} - \omega^2 C_{gd}C_{gs}R_i \tag{35}$$

and

$$Re(G) = Re(Y_{21})R_i C_{gs} - Im(Y_{21}) - \omega C_{gd} \tag{36}$$

Stability factor of a FinFET can be calculated with the help of device S-parameters. To achieve the expression for stability factor (S.F),

$$\text{S.F} = \frac{1+|S_{11}\times S_{22} - S_{12}\times S_{21}|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}|\times|S_{21}|} \tag{37}$$

Maximum stable gain (MSG) can be calculated as

$$\text{MSG/MAG} = \begin{cases} \dfrac{|S_{21}|}{|S_{12}|}, & \text{for S.F} < 1 \\ \dfrac{|S_{21}|}{|S_{12}|} \times \left(\text{S.F} - \sqrt{\text{S.F}^2 - 1}\right), & \text{for S.F} > 1 \end{cases} \tag{38}$$

Maximum unilateral transducer gain (MUG) of the FinFET can also written as

$$\text{MUG} = \frac{S_{21}^2}{(1-|S_{11}|^2)(1-|S_{22}|^2)} \tag{39}$$

For computing S-parameter the RMS error can be defines as

$$\text{RMSE} = \sqrt{\sum_{k=1}^{n}\sum_{i=1}^{2}\sum_{j=1}^{2}\left(S_{ij(\text{exp})}^k - S_{ij(\text{mod})}^k\right)^2 \Big/ S_{ij(\text{exp})}^k} \leq E_{r(min)} \tag{40}$$

The insertion loss (I_L) of the device can be calculated by using the following equation.

$$I_L = -20\log_{10}|S_{21}| \text{ (dB)} \tag{41}$$

IV. RESULT AND DISCUSSION

To validate the derived expression of DC and AC characteristics of 3D FinFETs, initially an empirical model expression has been developed for DC characteristics of the device. The parameters of this expression in Eq. (2) are optimized using the PSO technique, implemented through a MATLAB code. Subsequently, an error is generated by comparing experimental and measured data. When the minimum error is achieved, the device's results are plotted. Fig. 2 shows the plot of observed and simulated $I-V$ characteristics of n-type FinFET and the proposed model shows good agreement with experimental data and can, therefore, proposed model is be an appropriate choice to predict the output characteristics of a FinFET device. The extraction of small signal parameters using S-measurements can be accomplished by two procedures: a) systematic procedure and b) equivalent circuit procedure. In the systematic procedure, mathematical equations are formed that represent physical behavior such as carriers transfer, field distribution in the device current modulation etc. This approach requires a numerical solution and involves non-linear equations which increase the model complexity and makes it a less desirable one. On the other hand, an equivalent circuit approach is proposed that is directly link with its electrical behavior. The proposed circuit

$$Y_{int} = \begin{bmatrix} \dfrac{j\omega C_{gs}}{j\omega C_{gs}R_{gs}+1} + \dfrac{j\omega C_{gd}}{j\omega C_{gd}R_{gd}+1} & -\dfrac{j\omega C_{gd}}{j\omega C_{gd}R_{gd}+1} \\ \dfrac{g_m e^{-j\omega\tau_m}}{1+j\omega R_{gs}C_{gs}} - \dfrac{j\omega C_{gd}}{j\omega C_{gd}R_{gd}+1} & j\omega C_{ds} + \dfrac{1}{R_{ds}+j\omega L_{ds}} + \dfrac{j\omega C_{gd}}{j\omega C_{gd}R_{gd}+1} \end{bmatrix} \tag{11}$$

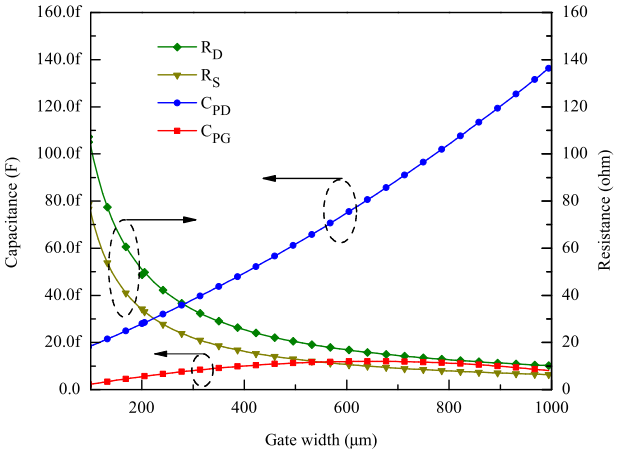

FIGURE 4. Pad capacitances and resistances as a function of gate width of FinFET.

consists of lumped elements i.e., resistors, capacitors, and inductors [28] placed in such a manner that gives complete device AC response. Both the approaches discussed hitherto are valid over a range of frequency starting from few Hz up to several tens of GHz. Fig. 4 shows the behavior of pad capacitance and resistance as a function of gate width. R_s and R_d has no impact as the gate width increases. Similarly, pad capacitance of the gate side C_{pg} has also negligible effect but pad capacitance of drain side C_{pd} increases with the increase in gate width and play a minute effect on AC performance. In this paper equivalent circuit procedure has been adopted to compute device physical parameters based on its measured AC response.

To achieve maximum reliability of the proposed technique a MATLAB code developed by involving particle swarm optimization (PSO) with the following steps.

1) In first step, initialize the position, velocity and swarm size;
2) By initializing the extrinsic parameters of the device along with experimental S-parameters data;
3) Convert these S-parameters into Y-parameters using Eq. 6;

TABLE 1. Extrinsic parameters used for optimization process.

Parameters	Value
$R_g(\Omega)$	17
$R_s(\Omega)$	18
$R_d(\Omega)$	15
$L_g(pH)$	0.1
$L_s(pH)$	1
$L_d(pH)$	1

TABLE 2. Physical parameters of the devices used in this study.

Parameters	T_1 [22]
$L_g\ (\mu m)$	16
$T_{fin}\ (nm)$	8
$H_{fin}\ (nm)$	42
$T_{ox}\ (nm)$	1
$N_a\ (m^{-3})$	1.0 x 10^{24}

4) Now update the position and velocity of all swarm particle;
5) Find the local and global best position of each particle;
6) Now convert again Y-parameters into S-parameters using Eq. 26;
7) By using your defined objective function, evaluate the error analysis;
8) Again update the position and velocity of local and global best position;
9) If minimum error is achieved stop the process, If not then repeat the process until you get desire results;

Initially, calculate Y_{ext} and Y_{int} using Eq. (6) and (11); both equation are added and found scattering parameter through (26), During optimization process, the fitness

$$S_{11} = \frac{(Y_0 - Y_{11})(Y_0 + Y_{22}) + Y_{12}Y_{21}}{\Delta Y} \tag{22}$$

$$S_{12} = \frac{-2Y_0Y_{12}}{\Delta Y} \tag{23}$$

$$S_{21} = \frac{-2Y_0Y_{21}}{\Delta Y} \tag{24}$$

$$S_{22} = \frac{(Y_0 + Y_{11})(Y_0 - Y_{22}) + Y_{12}Y_{21}}{\Delta Y} \tag{25}$$

$$S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} = \begin{bmatrix} \frac{(Y_0 - Y_{11})(Y_0 + Y_{22}) + Y_{12}Y_{21}}{\Delta Y} & \frac{-2Y_0Y_{12}}{\Delta Y} \\ \frac{-2Y_0Y_{21}}{\Delta Y} & \frac{(Y_0 + Y_{11})(Y_0 - Y_{22}) + Y_{12}Y_{21}}{\Delta Y} \end{bmatrix} \tag{26}$$

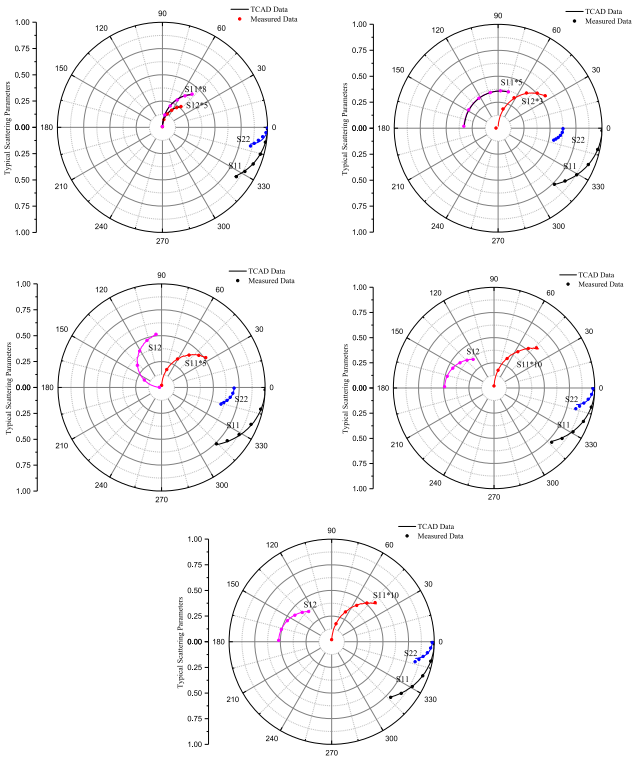

FIGURE 5. Typical Scattering Parameters of trigate FinFET at Table 2: a) $V_{ds} = 0$ and $V_{gs} = 0$, b) $V_{ds} = 0.15$ and $V_{gs} = 0.18$, c) $V_{ds} = 0.3$ and $V_{gs} = 0.9$ d) $V_{ds} = 0.6$ and $V_{gs} = 0.7$ e) $V_{ds} = 0.9$ and $V_{gs} = 0.9$.

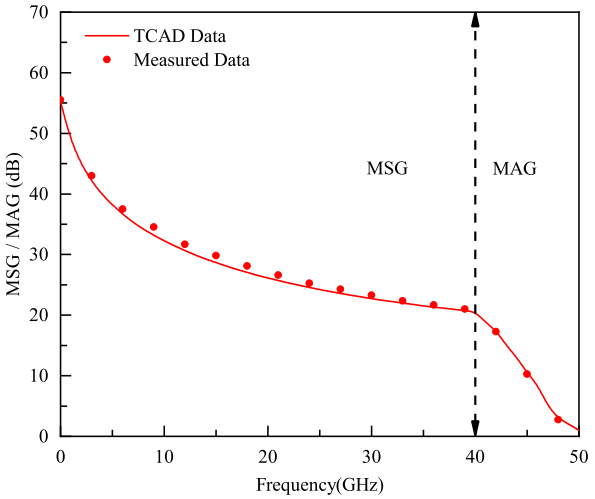

FIGURE 6. Experimental and simulated MSG/MAG of trigate FinFET.

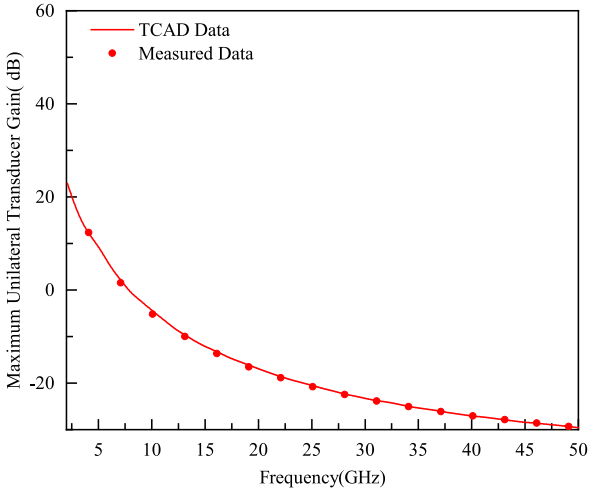

FIGURE 7. Experimental and simulated MUG of trigate FinFET.

function defined in Eq. (40) is used as a convergence condition, which is used to calculate the error between simulated and TCAD data; If minimum criteria is met the process is terminated, otherwise parameter values are updated and procedure is repeated. To ensure the rapid and repeated convergence a search space for each variable has been defined at the start of the process.

Fig. 5 show the simulated and TCAD S-parameters of the device having the physical parameter are given in Table-2, respectively. A good match between the simulated and TCAD data shows that the optimization process for the evaluation of intrinsic AC parameters of Si FinFETs is valid.

This research is relating to a technique in which evolutionary optimization process is used to evaluate Si FinFETs intrinsic and extrinsic circuit parameters. The extrinsic parameters are taken from the simulated data which has been simulated through ADS Software are given in Table-1. Extrinsic components and S-parameters are simulated through ADS software to check its validity.

Further, the maximum stable gain (MSG), maximum available gain (MAG) and unilateral gain are shown in the linear scale in Figs. 6 and 7 for the devices under consideration. In Fig. 6, stability factor (S.F) known as Rollet's stability factor is a threshold between MSG and MAG. When S.F less then one, it is MSG and for greater then one it shows the MAG of the device can be seen from Eq. 38. Its values as a function of frequency show that these devices are low noise and can perform good in mm-wavelength regime. Figs. 8 and 9 are the graph of Rollet's stability factor and insertion loss of the device as a function of frequency. Eq. 41 refers that the substrate losses increases by increasing the frequency and the same behavior is exhibited for stability factor as reported in plot of Figs. 8 and 9.

The accuracy of S-parameters were achieved by using Eq. 40 alone, the difference in accuracy of simulated and TCAD data at different bias voltages is shown in Table-4 for the devices under consideration. It is noted that the highest inaccuracy is observed in S_{12} parameter the devices and this can be overcome by defining the objective function based on both phase and magnitude of S-parameters. By using combined objective function the phase error of S_{12} reduced drastically and the overall S-parameter error, i.e., combined error of all the four parameters is well within acceptable range. If there is negative phase it is converted into positive

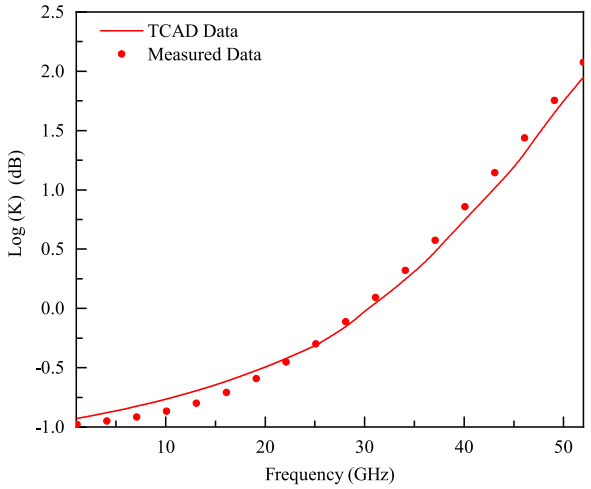

FIGURE 8. Stability factor, as function of frequency for a trigate FinFET.

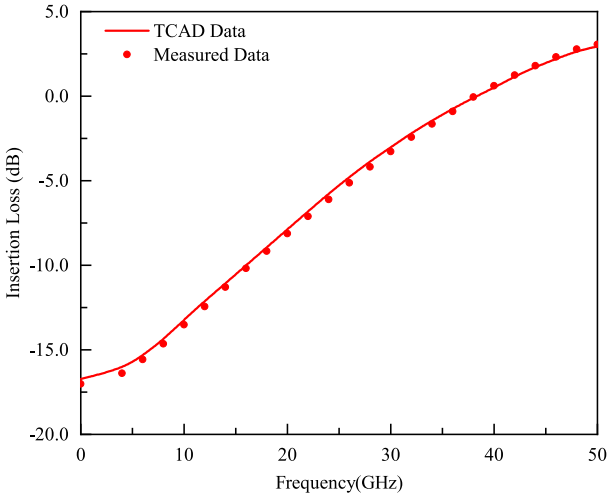

FIGURE 9. Experimental and simulated insertion loss of trigate FinFET.

TABLE 3. Comparison of simulated and TCAD intrinsic parameters.

Parameter	$\{V_{ds}, V_{gs}\}=\{0,0\}$		$V_{ds}=0.15, V_{gs}=0.18$		$V_{ds}=0.3, V_{gs}=0.9$		$V_{ds}=0.6, V_{gs}=0.7$		$V_{ds}=0.9, V_{gs}=0.9$	
	TCAD	Sim	TCAD	Sim	TCAD	Sim	TCAD	Sim	TCAD	Sim
$R_{gs}(\Omega)$	11.89	8.97	0.19	0.29	0.1	0.02	5.3	2.95	2.9	1.65
$R_{gd}(\Omega)$	855	751	450	434.89	486	458	806	690	876	737
$R_{ds}(k\Omega)$	0	0	180	174.54	0.24	0.22	5.69	1.68	4.65	1.59
$C_{gs}(fF)$	18.83	1.8	25.19	25.14	26.16	26.25	25.58	26.47	25.81	26.6
$C_{gd}(fF)$	2.13	2.21	5.27	5.39	4.99	26.22	2.56	2.7	2.6	2.7
$C_{ds}(fF)$	0.5	5.05	1.28	4.82	2.72	7.24	0.76	6.22	0.62	5.91
$g_m(mS)$	0	0	1.627	1.6	2.886	2.9	5.44	5.5	5.746	5.8
$Tau(mS)$	0	0	0.08	0.07	0.08	0.058	0.08	0.09	0.08	0.05

by subtracting it from 360Â° and a radian value is then used in further evaluation.

DC characteristic of the proposed Eq. (2) are calculated by optimizing the variables through PSO and for this purpose a Matlab code is developed to perform the validity of the model. Fig. 2 shows simulated and experimental $I-V$ characteristics for device under consideration whereas, It is evident from these figure that the proposed model simulates the DC characteristics with reasonable accuracy. Also, for

TABLE 4. Accuracy of modeled S-parameters.

Parameter	$\{V_{ds}, V_{gs}\}=\{0,0\}$		$V_{ds}=0.15, V_{gs}=0.18$		$V_{ds}=0.3, V_{gs}=0.9$		$V_{ds}=0.6, V_{gs}=0.7$		$V_{ds}=0.9, V_{gs}=0.9$	
	r	ϕ	r	ϕ	r	ϕ	r	ϕ	r	ϕ
S_{11}	0.0052	0.00067	0.001	0.028	0.016	0.0014	0.0026	0.0074	0.0031	0.0053
S_{12}	0.0060	0.0065	0.0037	0.087	0.0054	0.0015	0.0014	0.0094	0.0105	0.0069
S_{21}	0.0060	0.0063	0.0023	0.022	0.0053	0.002	0.0569	0.0076	0.0013	0.0059
S_{22}	0.0364	0.017	0.0089	0.0013	0.0015	0.0034	0.029	0.028	0.025	0.0064
Avg. MSE	0.0134	0.0076	0.0039	0.0345	0.0034	0.052	0.0024	0.0131	0.0131	0.0062

AC analysis of the device, RMS error values calculated for the proposed model at different V_{gs} and V_{ds} are given in Table-4, respectively. Table - 3 shows the evaluation of all intrinsic parameters through Eqs. 28-36 at different bias voltages. Its comparison are also taken between TCAD and simulated data, it is observed a reasonable accuracy was achieve between TCAD and simulated data. A small variation in data at some values could be the result of impact ionization and self heating effects of the device as the number of electron and hole pairs generation by impact ionization is proportional to the maximum electric field and carrier concentrations. The data of these tables clearly demonstrate the validity of the proposed model and it is capable to simulate the DC and AC characteristics of the device with reasonable accuracy.

V. CONCLUSION

To achieve the desired electrical behavior, simulation and modeling of the device play a vital role in its optimization, design, and deployment. This process is closely associated with experiments, the development of mathematical theories, and their subsequent validation. For this purpose, the AC/DC performance of FinFETs primarily relies on both intrinsic and extrinsic device parameters, which are crucial for predicting the device's accuracy. In modern electronics technology, devices for energy-efficient and low-power applications place a significant emphasis on accurately generating device characteristics, particularly for Trigate FinFETs. Therefore, future research should focus on optimizing AC/DC parameters meticulously in both analog and digital circuit design to achieve the desired results.

In this paper, a model has been developed to simulate its DC and AC characteristics of Si FinFET. The characteristics were then simulated by developing a Matlab code based on particle swam optimization (PSO) technique. The results of the proposed model are compared with TCAD data and it is observed that the proposed model is efficient in accuracy. It has been demonstrated that the proposed model having ability to simulate DC and AC characteristics of Si FinFET with reasonable accuracy in nanometer regime and could be a useful tool for designing integrated circuits.

An objective function based on both the magnitude and phase information of S-parameters is proposed to achieve high accuracy. Trapping in local minimum and to avoid exploding of the process, a search space is defined and it has been noted that PSO optimizer is a good choice that provides a perfect convergence for the evaluation of AC/DC characteristics of FinFETs.

CONFLICTS OF INTEREST

The authors declare no conflict of interest.

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