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RESEARCH ARTICLE

Lower Output Voltage Harmonics With Optimum Switching Angles of Single PV-Source Based Reduced Switch Multilevel Inverter Using BWO Algorithm

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ABSTRACT This paper presents a technique of harmonic minimization from output voltage waveform of a reduced switch Multilevel Inverter (MLI) through an efficient bio inspired metaheuristic algorithm called Black widow optimization (BWO). The proposed reduced switch 13- level MLI scheme uses a single Photovoltaic (PV) source which can be suitable for grid integration. The proposed BWO algorithm minimizes the Total Harmonic Distortion (THD) of output voltage with low operational time compared to other existing nature based algorithms considering large searching area. The weighted THD (WTHD) of the output voltage is also minimized in order to reduce the effect of lower order harmonics from the output voltage in a greater extent. The convergence rate and level of accuracy of BWO algorithm is compared with two different bio inspired algorithms for justification. The MLI operation is carried out with fundamental frequency, minimizing the switching stress while lowering the power loss compared to PWM or Sinusoidal PWM switching schemes. A single PV panel with multi winding flyback converter is used for medium voltage application through reduced switch MLI, serving the purpose of both isolation and reduction of energy sources. Simulation and experimental analysis are carried out with online control technique using a three phase 13-level reduced MLI to validate the proposed concept on a practical system.

INDEX TERMS BWO algorithm, flyback converter, modulation index, reduced multilevel inverter, total harmonic distortion.

I. INTRODUCTION

The demand for electricity has seen a rise for the past few years. Therefore, fulfilling this rise in demand from alternating sources and its effect on environment is a major challenge. Most of the research has been carried out to extract maximum power from solar energy which can be synchronized to AC as well DC grid. Conversion of lower rating DC power from renewable sources to higher rating AC power for AC grids or different loads with better power quality is a major concern. The use of Multilevel Inverters (MLI) for AC power conversion has become a significant field of research that has replaced the usage of filter circuits for improving power quality. For PV energy utilization in the remote area, a utility scale PV plant with modular DC-DC converter is proposed in [1]. Different control schemes and algorithms are developed for

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Maximum Power Point Tracking from solar PV panel [2], [3]. Due to the modular design and enhanced output voltage of Cascade H-bridge MLI (CHBMLI), this topology and its modified design are connected to grid without transformer as mentioned in [4] and [5]. This topology does not require clamping diodes and capacitors as discussed in [6] and [7] for its operation, but CHBMLI requires larger number of switching devices to increase the output voltage level which leads to more switching loss. Due to this deficit, modular form of CHB multilevel inverter has been used for integrating PV with grid as discussed in [7]. But the design of multilevel inverter with optimum number of switching devices has dragged the attention towards its compact and lossless characteristics. A review on different proposed topologies of reduced switch MLIs with their operation, efficiency and comparison with classical MLIs are discussed in [8]. In order to obtain magnified output voltage waveform with lesser number of switching devices, minimum switching loss and low standing voltage, reduced switch MLIs are proposed in different literatures [9], [10], and [11]. A cross switched multilevel inverter with reduced number of power switches is proposed in [12]. The topology of MLI is influenced from a cross connected voltage source inverter discussed in [13]. The efficiency and performance of the proposed MLI in the above literature has been discussed and compared with the existing topologies too. In order to achieve higher output voltage level with lesser number of switching devices the MLI topologies with unequal DC sources are designed and implemented for grid integration [4] and high power application [14].When synchronization of PV with grid is considered the primary objective, which is necessary to achieve is power quality improvement that deals with less harmonic content in grid side and less THD. Some control schemes have been implemented like PWM and modified SPWM for selective harmonic elimination (SHE) to get the appropriate triggering angles, which have achieved the minimum THD as per IEEE standard stated in [15] and [16]. As PWM switching frequency is very high, these techniques lead to the increase of switching stress. The above complications are avoided by adopting several search-based optimization algorithms which have reduced the output voltage THD using MLI up to desired level. A selective harmonics elimination problem in a single phase 11-level CHBMLI is solved using Particle Swarm Optimization (PSO) algorithm [17]. In order to increase the convergence of PSO, Modified PSO algorithm for solving SHE problem in a three phase 11-level reduced MLI has been proposed in [18], that can be able to reduce the output voltage THD to 7.45%. To eliminate the undesired lower order harmonics from the output voltage of a 7,13 and 9 level cascade H-bridge MLI, the colonial competitive algorithm has been proposed in [19]. Also, a modified Grey Wolf Optimization (GWO) algorithm for SHE-PWM has been proposed in [20], which has reduced the line voltage THD up to 5.53%, but the higher order harmonics voltages are not reduced properly as viewed in the FFT analysis.

This paper presents a 13-level cross switched MLI (CSMLI) with unequal DC voltage sources generated from single PV module for medium voltage range application. In literature [12], the efficiency and working principle of an 11-level CSMLI operated with equal voltage sources has been discussed, but the harmonic reduction using this MLI has not been highlighted. Here the following contributions are carried out:

1- In this article, the performance of the above MLI with reduced number of switches and DC voltage sources for THD minimization has been examined thoroughly and results are shown in section IV.
2- Instead of using multiple solar panels in each phase for different voltage level, a single solar panel has been used in this scheme with multi output through flyback converter to provide unequal DC sources to the CSMLI, which has been discussed in section II.
3- To obtain the desired switching angles that would trigger the CSMLI with minimum voltage THD and WTHD, Black Widow Optimization (BWO) algorithm has been adopted and to justify the productivity of this algorithm the objective function of the system is calculated in MATLAB program environment using GWO and PSO algorithms of same population size. The comparative analysis of the above discussed algorithms has been carried out and presented in section IV-A.
4- These algorithms have successfully minimized the WTHD and THD for the line voltage of the system output.
5- Piecewise mixed model equation [21] has been utilized to store the nonlinear variation of triggering angles with modulation indices, which is calculated offline for BWO algorithm to obtain minimum voltage THD. The details are explained thoroughly in section II-E.

To affirm the above concept, programming and simulation has been carried out using 13-level CSMLI for grid interconnection. The experimental set up has been done to verify the result and performance of the reduced MLI with modulation index 0.92 and 0.6. The rest of the paper is organized as follows. Section II introduces the proposed scheme and section III discusses the Black Widow Optimization method. The simulation results and discussions are given in section IV. While section V concludes the paper.

II. PROPOSED SCHEME

The main objective of this proposed scheme is to implement a newly available metaheuristic search based algorithm for THD minimization of a reduced switch Multilevel Inverter to interface PV energy with medium or high voltage grid. The novelty behind this design is the use of a single PV panel to obtain multiple isolated DC sources for inputs to the MLI, hence making this scheme modular. Multiple PV panels can also be used for this purpose [4], [6] but without the advantages mentioned for the proposed scheme as above. Moreover, application of the new optimization

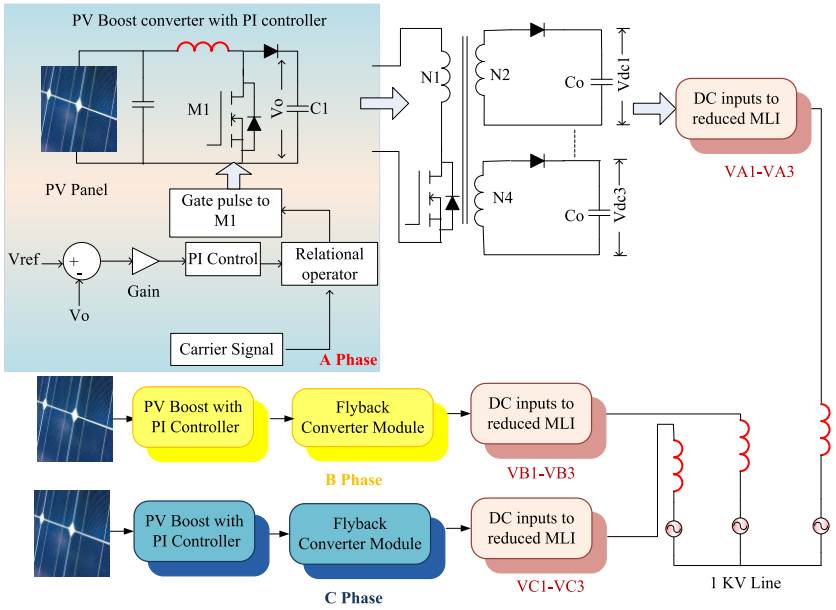

FIGURE 1. PV based CSMLI through proper isolation for grid application.

algorithm helps to reach lower THD and thereby reducing the interfacing reactor values compared to existing schemes.

A. PV BOOST CONVERTER CONTROL

In this model, three 260-Watt PV panels are used for three phase system as shown in Fig.1. In order to step up the PV voltage, a DC-DC boost converter with PI controller is implemented in each phase. PI controller is used to maintain a constant output voltage by varying the duty ratio (D) with change in input voltage. The controller generates a reference signal that is compared with a carrier signal of 20KHzfrequency to induce a triggering pulse for boost converter as explained in Fig.1. The relation of boost output voltage (V_o) with input voltage from PV (V_i) is given below.

$$V_o = \frac{V_i}{1-D} \tag{1}$$

B. ISOLATION THROUGH FLYBACK CONVERTER

In this paper, a 13-level reduced MLI is considered with three unequal DC inputs per phase for its operation. Furthermore, these sources require isolation to avoid possible short circuit during abnormal operation. To achieve this, an isolated multi output flyback converter operating from PV-boost converter output is considered in the proposed scheme. Thus, the proposed scheme reduces the number of input PV sources compared to the existing schemes which usually require 's' number of solar panels for 's' inputs per phase for the MLI [4], [6]. Therefore, the overall system cost can be reduced considerably. The proposed scheme is shown in Fig. 1. The flyback converter has been energized from the boost converter output voltage for all the three phases separately. The output of this converter V_{dc1} to V_{dc3} are fed to each phase of the reduced MLI for generating 13-level output voltage. The output of the flyback converter (V_{out} i.e V_{dc1} of secondary winding N_2) can be expressed as:

$$V_{out} = K1 * \left(\frac{D}{1-D}\right) V_{c1} \tag{2}$$

V_{c1} = Input voltage to flyback converter shown in Fig.1. D=Duty cycle or duty ratio. Here, duty ratio 'D' and transformation ratio 'K1' are set to 0.6 and 2 respectively. Transformation ratios K1, K2 and K3 for the secondary windings bear a ratio of 1:3:2 to generate unequal DC voltages for the MLI inputs.

C. REDUCED SWITCH MULTILEVEL INVERTER

This topology of MLI is implemented for unequal voltage sources with a ratio of 1:3:2 to develop 13 level output voltage. Presented reduced MLI requires less power semiconductor devices in comparison to symmetrical CSMLI and conventional CHBMLI. For developing 13-level output voltage, CHBMLI needs 24 numbers of switching devices and symmetrical CSMLI needs 14 switching devices whereas CSMLI with unequal sources needs 8 switches and three DC sources only. The relation between number of switches (S_n) and number of DC voltage sources (S) for both the topologies are:

$$\text{In case of CHB MLI}: \; S_n = 4 * S \tag{3}$$

$$\text{In case of CSMLI}: \; S_n = 2 * (S+1) \tag{4}$$

The presented asymmetrical CSMLI exhibits a relation of output voltage level (V_{level}) with number of DC sources as given by equation (5):

$$V_{level} = 2S(S-2) + 7 \tag{5}$$

The optimum switching angles are determined by the help of BWO algorithm using MATLAB program. To obtain the desired staircase output voltage waveform, triggering patterns for the 13-level reduced MLI are designed using Table 1. Here, asymmetrical DC sources are applied to develop the above-mentioned output voltage level. The input voltages to reduced MLI are determined using a relationship shown in equation (6).

$$V1 : V2 : V3 = 1 : 3 : 2 \tag{6}$$

TABLE 1. Switching table of single phase 13-level reduced switch MLI.

Switching combinations for each voltage level												
switches	V1	V3	V2	V1+V2	V2+V3	V1+V2+V3	-(V1)	-(V3)	-(V2)	-(V1+V2)	-(V2+V3)	-(V1+V2+V3)
S1	1	1	0	1	0	1	0	0	1	0	1	0
S2	1	0	1	1	1	1	0	1	0	0	0	0
S3	0	1	1	1	1	1	1	0	0	0	0	0
S4	0	0	1	1	0	0	1	1	0	0	1	1
S5	0	0	1	0	1	0	1	1	0	1	0	1
S6	0	1	0	0	0	0	1	0	1	1	1	1
S7	1	0	0	0	0	0	0	1	1	1	1	1
S8	1	1	0	0	1	1	0	0	1	1	0	0

The MLI is operating with unequal DC voltages but results equal step voltage at each level that is illustrated in Fig. 2 As per the switching scheme explained in Table 1, the six modes of operation for the MLI are demonstrated in Fig.3. The output voltage can vary from V_{max} to $-V_{max}$, which will be accelerated by the triggering angles $\alpha_1, \alpha_2, \ldots .\alpha_6$ and V_{max} is expressed in equation (7) as:

$$V_{max} = V1 + V2 + V3 \tag{7}$$

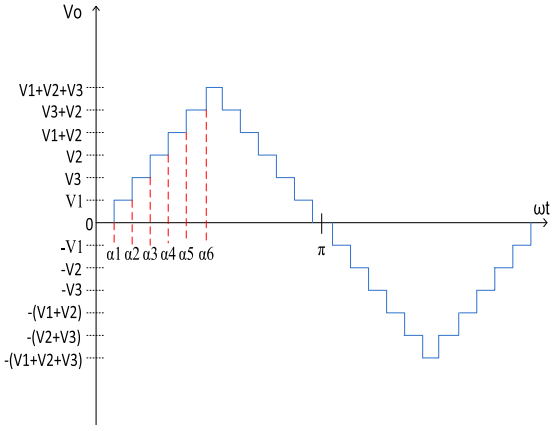

FIGURE 2. Output voltage waveform of a 13- level reduced inverter.

For generating different output voltage levels, the requirement of power switches for asymmetrical CSMLI and symmetrical CSMLI [12] is presented in Fig. 4.

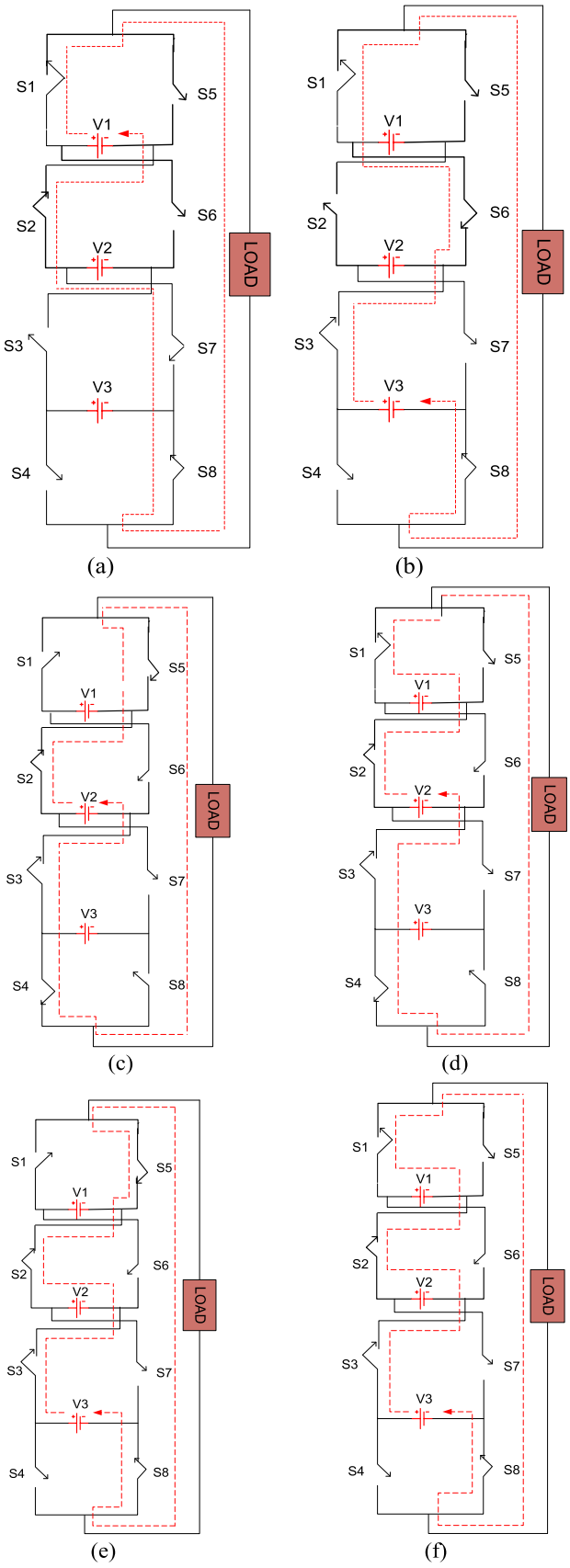

FIGURE 3. Operational diagram of 13- level CSMLI. (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4, (e) Mode 5 and (f) Mode 6.

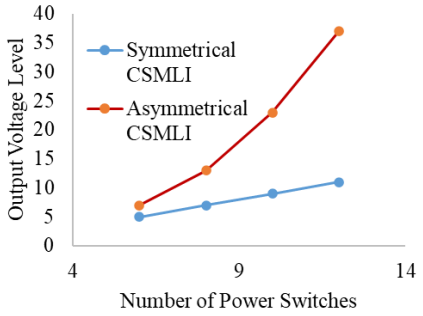

FIGURE 4. Number of power switches vs output voltage level.

D. MATHEMATICAL DERIVATION FOR OUTPUT VOLTAGE AND HARMONIC DISTORTION

The nonlinear equation for MLI output voltage waveform shown in Fig.2 can be represented as:

$$V(\omega t) = \sum_{\alpha=1}^{ai} \frac{4V_D}{n\pi} (\cos(n\alpha_1) + \cos(n\alpha_2) + \ldots + \cos(n\alpha_{ai})) \sin(\omega t) \quad (8)$$

V_D is the DC input voltage to the MLI for each level and $\alpha_1, \alpha_2 \ldots\ldots \alpha_{ai}$ are the triggering angles which must need to gratify the following condition:

$$\alpha_1 < \alpha_2 < \ldots \alpha_{ai} < \frac{\pi}{2} \quad (9)$$

The nonlinear equation representing the fundamental voltage and harmonic voltages is shown below.

$$\left.\begin{array}{c} \cos(\alpha_1) + \cos(\alpha_2) + \ldots + \cos(\alpha_6) = KV_1 \\ \cos(5\alpha_1) + \cos(5\alpha_2) + \ldots + \cos(5\alpha_6) = 0 \\ \cos(7\alpha_1) + \cos(7\alpha_2) + \ldots + \cos(7\alpha_6) = 0 \\ \cos(11\alpha_1) + \cos(11\alpha_2) + \ldots + \cos(11\alpha_6) = 0 \end{array}\right] \quad (10)$$

Here, $K = \pi/4V_D$. The Modulation index (MI) can be represented as:

$$MI = \frac{V_1}{V_{max}} \quad (11)$$

Here, $V_{max} = (V_{level} - 1)^* V_D/2$. In this paper, THD of output voltage is minimized through BWO, PSO and GWO algorithms. To prune the lower order harmonics from the system, the weighted THD (WTHD) of the output voltage is also considered and minimized through the above algorithms. The minimization of WTHD ensures the lowest value of voltage THD with negligible lower order harmonics and the optimum switching angles are obtained for the MLI operation. The output voltage THD and WTHD are expressed by,

$$THD\% = \frac{\sqrt{\sum_{n=3,5\ldots}^{39} V_n^2}}{V_1} * 100 \quad (12)$$

$$WTHD\% = \frac{\sqrt{\sum_{n=3,5\ldots}^{17} \left(\frac{V_n^2}{n^2}\right)}}{V_1} * 100 \quad (13)$$

In this case, V_1 is the fundamental output voltage and 'n' is the number of harmonics. Here, the WTHD is minimized up to 17th order and the THD of output voltage is minimized considering up to 39th order and which is explained through FFT analysis.

E. ONLINE CONTROL SCHEME

In the proposed work, an online control scheme is developed for reduced MLI to provide low harmonic injection when connected to main grid. The same is verified through simulation model. To initiate the control action, the grid voltages are measured through voltage sensors and through PLL corresponding angle is measured.

The current is controlled using the inner loop and frequency is compared with the fundamental. The current error is processed through PI controller and the modulation index is obtained as shown in Fig.5. The desired switching angles for minimum THD are calculated offline with different modulation indices (MI) using BWO algorithm as depicted in Fig.6. The linear and nonlinear equations at each section of the curve are derived through the mixed model equation proposed in [21]. The same have been presented in equations (14) and (15).

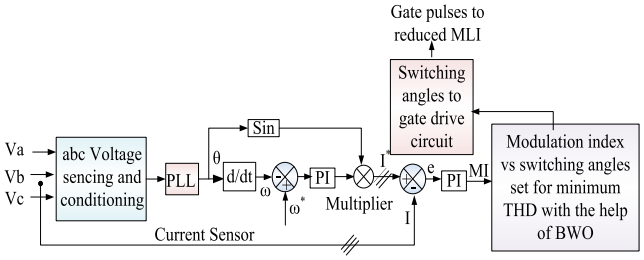

FIGURE 5. Developed control scheme.

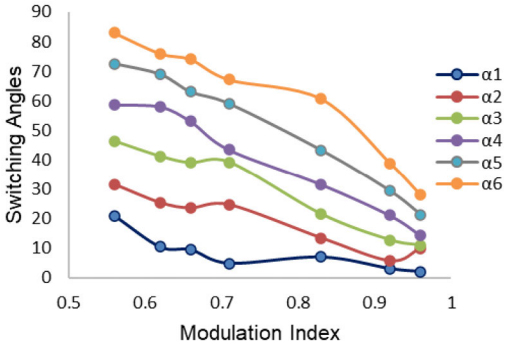

FIGURE 6. Switching angles vs modulation index graph for 13-level CSMLI.

For 0.55≤ MI ≤0.71, the switching angles are:

$$\left.\begin{array}{l} \alpha 1 = -103.4MI + 77.311 \\ \alpha 2 = -47.644MI + 56.633 \\ \alpha 3 = -49.282MI + 72.88 \\ \alpha 4 = -101.16MI + 117.76 \\ \alpha 5 = -94.147MI + 125.93 \\ \alpha 6 = -101.97MI + 139.93 \end{array}\right] \quad (14)$$

and for 0.72≤MI≤0.96, the switching angles are:

$$\left.\begin{array}{l}\alpha 1 = -343.83MI^2 + 577.56MI - 236.22\\ \alpha 2 = 284.02MI^2 - 534.73MI + 259.95\\ \alpha 3 = 269.1MI^2 - 611.46MI + 324.84\\ \alpha 4 = -87.243MI^2 + 22.843MI + 73.156\\ \alpha 5 = -214.51MI^2 + 214.64MI + 13.112\\ \alpha 6 = -621.02MI^2 + 859.8MI - 225.69\end{array}\right] \quad (15)$$

The modulation indices are varied from 0.55 to 0.96 as this is usually the working range for the converter. For the modulation index below 0.55, the overall THD can become out of the permissible range. These equations are set aside in the processor memory. The gate pulses for MLI are originated as per the stored data in processor memory to attain minimum voltage THD.

F. LOSS CALCULATION OF ASYMMETRICAL CSMLI

The inverter loss depends on conduction loss and switching loss of the power devices. In this paper, a 13-level asymmetrical CSMLI is implemented for PV-grid synchronization. The loss is calculated by considering a single phase 250 watt CSMLI with RL load and unequal voltage sources. To determine the MLI loss, following formulation is employed as per [12]:

$$MLI_{loss} = P_{conduction} + P_{switching} \quad (16)$$

$P_{conduction}$ and $P_{switching}$ are the conduction loss and switching loss of the power switches respectively. Conduction loss of the power device can be determined by the overall conduction loss of the transistor and antiparallel diode which can by derived as,

$$P_{conduction} = \frac{1}{T}\left[\int_{t1}^{t2} (V_{tr} + R_{tr}\beta I(t)) + (V_d + R_d\beta I\,(t))\, I\,(t)\, dt\right] \quad (17)$$

Here, T is the total conduction period of the switch. Conduction of the switch occurs between $t1$ and $t2$. V_{tr} and V_d are the on-state voltage drop across transistor and reverse conducting diode respectively. R_{tr} and R_d are the resistance of transistor and reverse diode respectively. Gain constant is represented by β and I(t) is symbolized for instantaneous current which is 0.5A in the above mentioned MLI. From equation (17), the total conduction loss is calculated to be 4.25 W.

Switching loss of the power device occurs during its turning on and turning off period which is determined by,

$$P_{switching} = \frac{1}{T}\left[EN_{ON}n_{ON} + EN_{OFF}n_{OFF}\right] \quad (18)$$

Energy loss during switching on and switching off are denoted by EN_{ON} and EN_{OFF} respectively and the number of times a power switch getting on and off are denoted by n_{ON} and n_{OFF} respectively. These energy losses can be calculated by,

$$En_{ON} = \frac{1}{6}\left[V_{pD}I_pT_{ON}\right] \quad (19)$$

$$En_{OFF} = \frac{1}{6}\left[V_{pD}I_pT_{OFF}\right] \quad (20)$$

V_{pD} is the voltage across each power switch before getting on or after getting off. I_p represents the current across the power switch during the above periods. The time taken by a power device to get on and off are represented by T_{ON} and T_{OFF} respectively. After putting the voltage and current values and times, the switching loss is calculated to be 0.012 W. From equation (16), the overall power loss of the presented MLI is calculated to be 4.262 W.

III. BLACK WIDOW OPTIMIZATION

A new metaheuristic algorithm known as Black Widow Optimization (BWO) has been proposed by V. Hayyolalam and A.P Kazem in the year 2020 to solve the real-world problem. The mating process of Black Widow spiders and reproduction of their offspring is the main motivation to develop this algorithm. This algorithm has set a benchmark for solving real engineering problem with a greater accuracy as discussed in [22]. In order to find out the global optima, BWO algorithm has proved its efficiency in comparison to other existing population based algorithm. This algorithm has been initialized by randomly assigning the population known as widow. The assigned population is divided into two groups of parents based on procreating rate. The reproduction is started by the mating process in between the group of parents and as per the biological nature of Black widow spider, the male spider is consumed by the female spider during mating or after mating. The spider babies are reproduced, where stronger babies are survived and rest are consumed by the stronger group which is decided by the cannibalism rate. The following equations are developed for generating new offspring:

$$off_1 = a * par_1 + (1 - a) * par_2 \quad (21)$$

$$off_2 = a * par_2 + (1 - a) * par_1 \quad (22)$$

where par_1 and par_2 are treated as two group of parents and 'a' is the randomly generated array with same length of parents. In this algorithm, the fitness function value decides the stronger population group. After determining the stronger group, mutation is carried out randomly to generate a new solution. The entire process is formulated and an algorithm has been developed to solve the optimization problem.

A. DESCRIPTION OF BWO ALGORITHM FOR CSMLI

For the design of three phase 13-level CSMLI, suitable triggering angles are evaluated using BWO algorithm that provides minimum THD and WTHD across output voltage. Here, the set of angles are acknowledged as the population size of the spider. The position vector of the spider is provided as $\alpha_i = [\alpha_{i1}, \alpha_{i1}, \ldots\ldots \alpha_{im}]$. The best population group

which provides the optimum result is found out using the following steps:

1) Initialize the maximum iteration count, procreating rate, cannibalism rate and mutation rate.
2) The population or triggering angle matrix denoted by 'Trig' of size [k X i] is generated randomly between 0 to $\pi/2$ and vector 'a' is initialized randomly of size 'i'.
3) In this step the fitness function is calculated for each set of population (triggering angles) using the following equations:

$$f1 = min\frac{\sqrt{\sum_{n=3,5...}^{49} V_n^2}}{V_1} \tag{23}$$

$$f2 = min\frac{\sqrt{\sum_{n=3,5...}^{17} \frac{V_n^2}{n^2}}}{V_1} \tag{24}$$

4) Based on the fitness function values select the stronger population and stored in another matrix say 'Trig1'
5) The reproduction is started in this step. Two parents' matrices are selected from matrix 'Trig1' and the offspring are generated using equations (21) and (22). From the new population, the stronger population are obtained based on the minimum fitness functions (eq.(23) and eq.(24)) value and rest are destroyed. The best population is now stored in matrix say 'Trig2'.
6) Mutation is started in this step. From the population matrix 'Trig1', positions of two randomly selected population vectors are exchanged and the new population is stored in 'Trig3'.
7) Now the population is updated by using the following equation:

$$Trig = Trig2 + Trig3 \tag{25}$$

8) The best solutions are obtained from the updated population matrix 'Trig' and displayed.
9) Termination condition: If maximum iteration is occurred then the entire process is stopped or returned to step 3.

IV. SIMULATION RESULTS AND COMPARITIVE STUDY

The simulation is carried out using grid connected reduced switch 13-level MLI. To get the desired triggering angles, MATLAB based program is used for BWO, GWO and PSO algorithms to achieve the lowest weighted THD and overall output voltage THD. The performance and results of these optimization algorithms are compared to verify the usefulness of the proposed BWO technique. Each phase of this inverter is energized from PV cell with proper isolation. The PV voltage is boosted up from 32.63 volts to 62.87 volts through boost converter. To provide multiple unequal DC sources across MLI, flyback converter develops voltages of ratings 122, 245 and 368 volts for MLI operation. The optimum switching angles are calculated for the modulation index (MI) range of 0.55 - 0.96 using all the above algorithms. For a typical modulation index of 0.92, the calculated angles, WTHD and corresponding THD values are shown in Table 2.

TABLE 2. Triggering angles obtained from BWO, GWO and PSO.

Algorithm	WTHD	Output Voltage THD	Optimum triggering angles (Degrees)					
			α_1	α_2	α_3	α_4	α_5	α_6
BWO	0.42%	2.12%	2	8.32	13.71	21.55	31.5	39.8
GWO	0.54%	2.58%	4.65	6.16	13.50	22.87	33.1	41.4
PSO	0.71%	3.63%	2.02	10.5	14.81	19.50	30.8	44.2

Total Standing Voltage per unit (TSV_{PU}) of the presented MLI is calculated by,

$$\frac{\boldsymbol{Totalstandingvoltage of MLI}}{\boldsymbol{maximum output voltage}} \tag{26}$$

$$\frac{\boldsymbol{2V1 + 2\,(V1 + V2) + 2\,(V2 + V3) + 2V3}}{\boldsymbol{6V_D}} = \frac{\boldsymbol{24V_D}}{\boldsymbol{6V_D}} \tag{27}$$

From the above calculation, TSV_{PU} of the 13 level CSMLI is computed to be 4. The cost factor and component level factor are also calculated by considering the number of components and TSV of the presented MLI according to the equation described in [23].

$$\boldsymbol{CF = S + S_n + S_D + S_c + S_{driv} + \alpha c * TSV_{PU}} \tag{28}$$

Here, S_c, S_D, S_{driv} are the number of capacitors, diodes and driver circuits respectively used for the MLI and αc is the weight factor of the components which is taken as 0.5 and 1 according to [23] for optimal calculation. The component level count depends on the output voltage level and it can be described by,

$$\boldsymbol{CF_{level} = \frac{CF}{V_{level}}} \tag{29}$$

The comparison study of the presented MLI in different aspects with existing MLI topologies is done and presented in Table 4. The boost converter output voltage and the flyback converter output voltages are shown in Figs. 7 (a) and 7 (b) respectively. The system is connected to a medium voltage grid of 1KV and 50Hz for verification. The grid connected MLI output voltage, converter current waveforms and synchronised voltage waveforms of MLI and grid output are

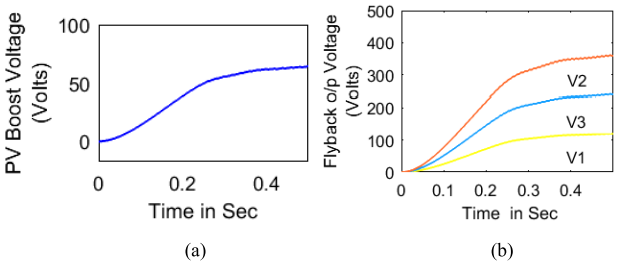

FIGURE 7. a) PV output voltage waveform with respect to time, (b) Output DC voltage waveform of Flyback converter.

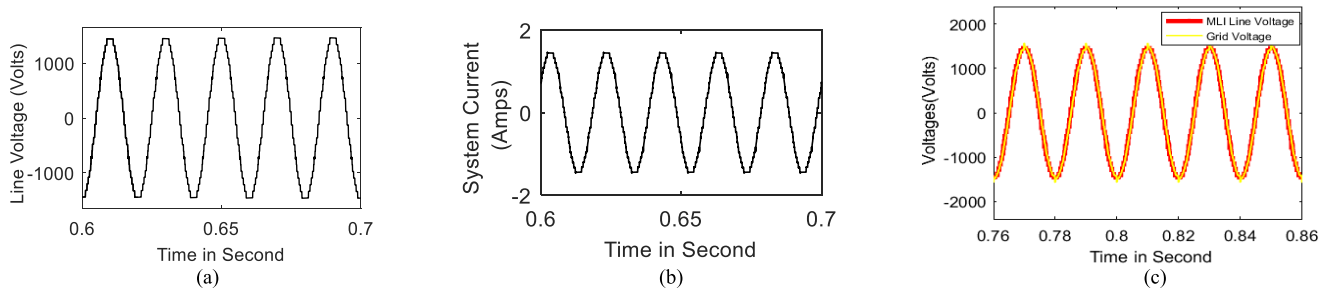

FIGURE 8. (a) Grid connected line voltage waveform with respect to time. (b) Converter current waveform with respect to time (c) Synchronized voltages of MLI and grid.

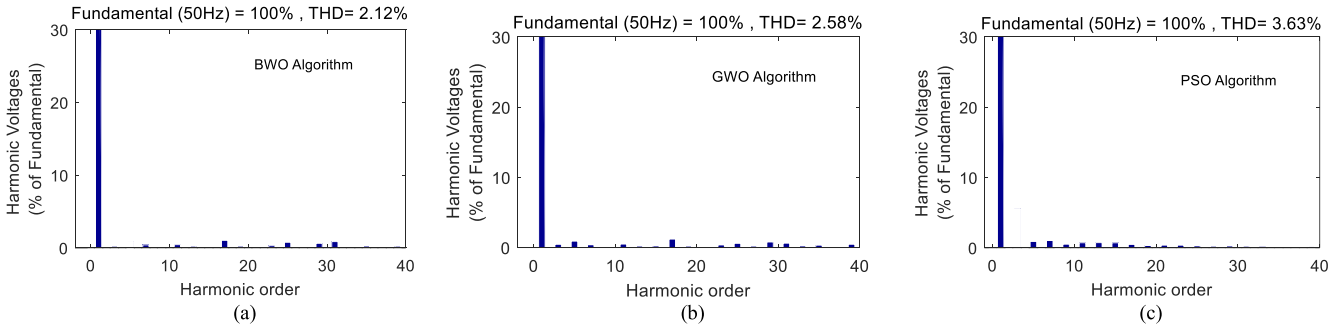

FIGURE 9. Harmonic spectra for output line voltage waveform for modulation index 0.92 using (a) BWO, (b) GWO and (c) PSO algorithm.

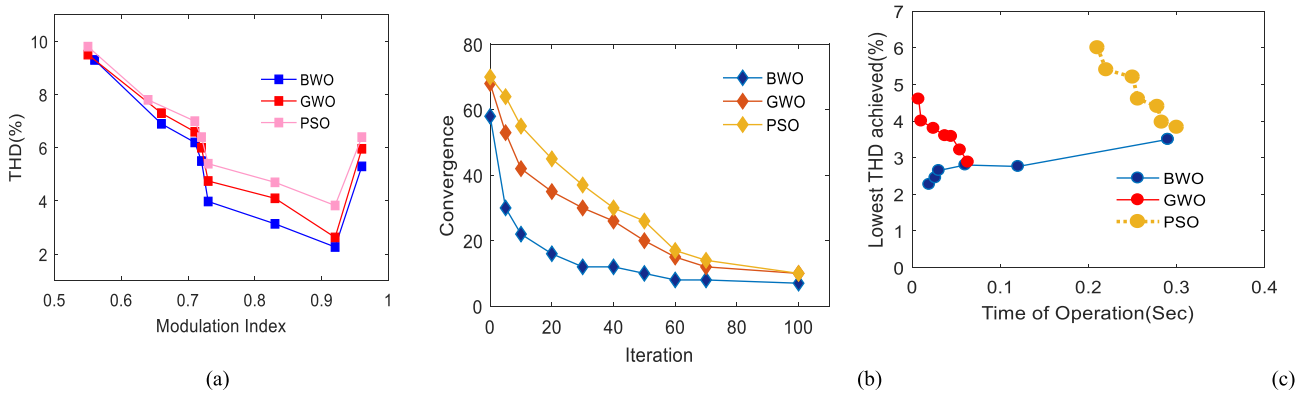

FIGURE 10. (a) Comparative study of output voltage THD with respect to modulation index for BWO, GWO and PSO algorithm, (b) convergence vs iteration graph of BWO in comparison with GWO AND PSO algorithm, (c) Lowest THD VS time of operation for BWO, GWO and PSO algorithm.

displayed in Fig. 8. FFT analysis is performed for the above three Algorithms to perceive nth harmonic order voltages and the overall THD. The results are illustrated in Fig.9.

A. COMPARISON STUDY BETWEEN BWO WITH GWO AND PSO ALGORITHMS FOR THE PROPOSED APPLICATION

The simulated output voltage THD is measured for different values of modulation indices, which is shown in Fig.10 (a). It shows a gradual decrease with increasing modulation index for all the three methods. However, the THD obtained through BWO is lowest compared to the other two methods. The typical convergence characteristics for the objective function with modulation index 0.92 are shown in Fig. 10(b). In this case, too, the proposed BWO technique shows better performance compared to the other two methods. In Fig. 10(c), the time taken to achieve the minimum voltage THD for all the three methods with same modulation index of 0.92 is shown, which also reflects the superiority of BWO technique over the others. In Table 3, different parameters along with lower order harmonic content computed through all the above three methods for typical two modulation indices of 0.6 and 0.92 are shown. From Table 3, it is also evident that the proposed BWO technique is more effective compared to GWO and PSO methods

TABLE 3. Comparison table for BWO, GWO and PSO algorithm.

Sl NO	BWO Algorithm	PSO Algorithm	GWO Algorithm	Sl NO	BWO Algorithm	PSO Algorithm	GWO Algorithm
At Modulation Index 0.92				At Modulation Index 0.6			
Convergence Time	0.02Sec	0.28Sec	0.063sec	Convergence Time	0.02Sec	0.28Sec	0.063sec
Line voltage THD	2.12%	3.63%	2.58%	Line voltage THD	5.60%	6.8%	6.32%
5^{th} order	0.04%	0.7%	0.22%	5^{th} order	0.8%	2.6%	1.8%
7^{rth} order	0.06%	0.64%	0.08%	7^{rth} order	1.18%	1.45%	1.09%
11^{th} order	0.12%	0.7%	0.48%	11^{th} order	1.1%	1.3%	1.20%
Grid current THD	2.42%	3.54%	3.86%	Grid current THD	6.3%	7.845%	7.06%

TABLE 4. Comparison study of proposed MLI topology with existing MLI topologies.

Existing Topology	voltage level	No of Switches	No of diodes	No of capacitors	Input DC voltage sources	No of Driver circuit	Total standing Voltage	Cost Factor (CF)		CF_{level}		Output Voltage THD	Triggering scheme
								αc =0.5	αc =1	αc =0.5	αc =1		
[4]	5	8	0	0	2 (Symmetrical)	8	4	20	22	4	4.4	4.3%	Phase shifted PWM
[6]	19	24	0	6	6 (Asymmetrical)	21	6.33	60.165	63.33	3.16	3.33	3.81%	NLC
[9]	31	12	0	0	4 (Asymmetrical)	12	6.93	31.466	34.93	1.01	1.126	4.25%	Unipolar PWM
[14]	13	10	0	0	3 (Asymmetrical)	8	5	23.5	26	1.87	2	6.6%	Fundamental frequency technique
[18]	11	12	0	1	2 (Asymmetrical)	12	3	28.5	30	2.59	2.72	7.45%	Modified PSO
[20]	11	12	0	1	2 (Asymmetrical)	12	3	28.5	30	2.59	2.72	5.51%	Modified GWO
[24]	23	12	0	0	3 (Asymmetrical)	12	4.27	29.21	33.35	1.27	1.45	3.23%	PWM
[25]	13	15	0	3	1 (Asymmetrical)	15	4.3	36.15	38.3	2.78	2.94	9.73%	LS-PWM
proposed	13	8	0	0	3 (Asymmetrical)	8	4	21	23	1.61	1.76	2.12%	BWO

(a) (b)

FIGURE 11. (a) Pulse voltage of switch S1, (b) Pulse voltage of switch S2. (Scale: -Channel1: Y axis=5V/DIV.)

TABLE 5. Component list.

SI NO	Components	
1	PV panels	260W
Boost Converter		
2	Series inductor	1.371mH
3	Input capacitance	10μF
4	output capacitance	83.583μF
5	Switching Frequency	25KHz
Isolated Converter		
6	Core	Ferrite E-48, 24AWG
7	Power MOSFET, Power diode	IRF740, BYV26E
8	Switching Frequency	10KHz
Driver Circuit for MLI Switches		
9	Optocoupler	TLP250H
10	Microcontroller	PIC18f452
CSMLI		
11	Power switches (IGBT)	FGA25N120
12	Load	R=100Ω, L=20mH
13	Switching Frequency	50Hz

for the proposed application. The presented scheme with BWO algorithm is compared with other available switching schemes used for MLI operation and the results are tabulated in Table 4.

From TABLE.4 it can be observed that the presented topology exhibits lowest voltage THD in comparison to the existing schemes. This topology also exhibits minimum cost factor than the equivalent level of MLI topologies which make this topology suitable for industrial application and grid integration.

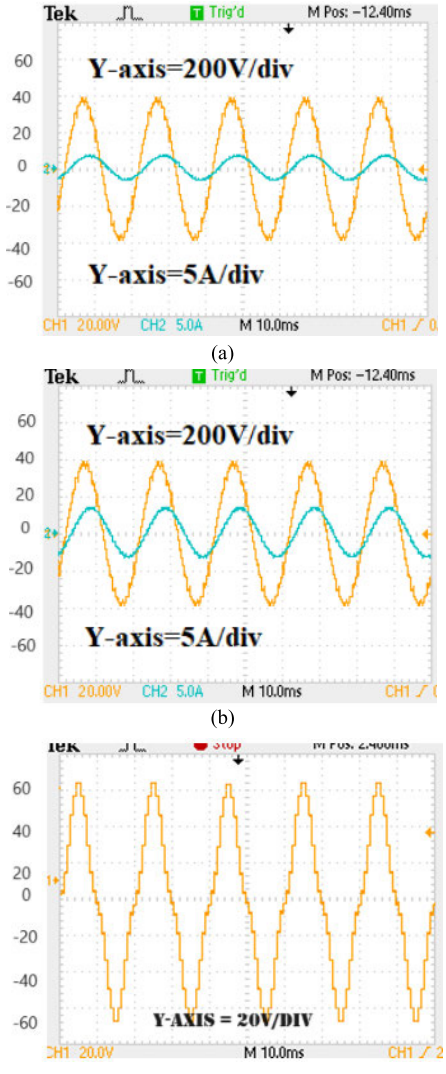

FIGURE 12. (a) Line voltage and load current at normal loading, (b) Line voltage and load current at 50% increase of loading, (c) Phase voltage waveform.

V. EXPERIMENTAL RESULTS

To verify the proposed scheme experimentally, a 260-watt solar panel is used as a DC voltage source for a 13-level CSMLI as per configuration shown in Fig.1. The inverter is designed with eight semiconductor switches. The performance of the reduced MLI is experimented with RL load. For recording the gate pulses, load voltage and current waveforms, and voltage harmonic spectrum, a DSO model no-TDS 2022B is used. The component list is provided in Table 5. The typical pulses of s1 and s2 are recorded and shown in Fig.11.

The output line voltage output current with dynamic loading and phase voltage are recorded and shown in Fig.12 (a),(b) and Fig.12(c) respectively. The harmonics spectrum of the output voltage waveform at two different MIs of 0.92 and 0.6 are shown in Fig. 13 (a) and (b) respectively.

From the FFT analysis graph of Fig. 13, it is observed that almost all the lower order harmonics up to 39th is removed

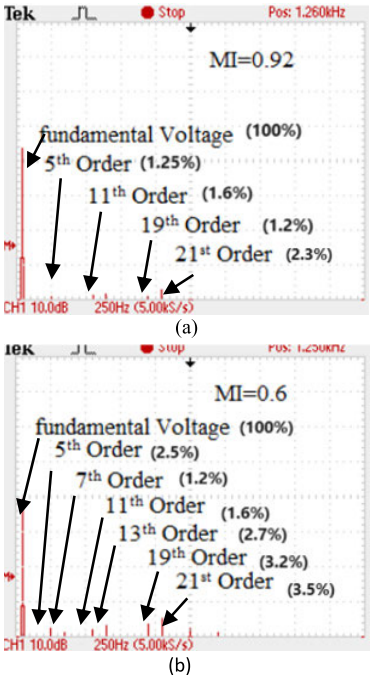

FIGURE 13. Output voltage harmonic spectrum (a) at modulation index 0.92 (b) at modulation index 0.6.

from the line voltage waveform for MI of 0.92 with the help of the proposed algorithm however for the MI of 0.6 some of the higher order harmonics are having larger magnitude which increases the THD. The laboratory setup is shown in Fig.14.

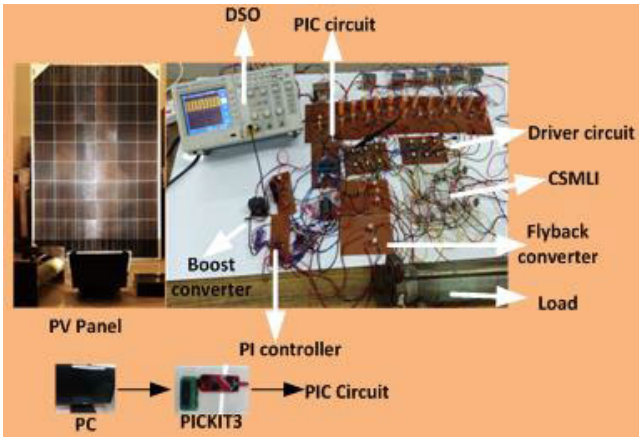

FIGURE 14. Developed prototype in the laboratory.

VI. CONCLUSION

In this paper, a PV based scheme with cross switched multilevel inverter suitable for grid interconnection has been studied. The proposed scheme reduces the number of sources for developing desired output voltage level with low output voltage THD in comparison to other existing techniques. Three different metaheuristic algorithms have been tried for

the proposed application, out of which BWO algorithm has been proved to be more accurate compared to the others. Thus, the BWO algorithm has been used to obtain optimum switching angles for lowest output voltage THD and lowest weighted THD at different modulation indices. In this application, the output voltage THD and WTHD of the MLI has been reduced to 2.12% and 0.42% respectively at 0.92 modulation index. The resulted voltage THD is well below the limits specified in IEEE standard-519.The calculated angles have been stored in micro controller memory in the form of mixed model equations for online application. To verify the capability of this MLI, a 13-level CSMLI has been simulated for three phase system and an experimental set up has been developed. It has been observed that both simulation and experimental results corroborate with theoretical model developed. The proposed technique is simple and can be easily implemented for a practical system.

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