IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 28 November 2023, accepted 24 December 2023, date of publication 2 January 2024,
date of current version 10 January 2024.

Digital Object Identifier 10.1109/ACCESS.2023.3349186

RESEARCH ARTICLE

SPICE Model of a Passive Battery Management System

IONUŢ-CONSTANTIN GURAN, ADRIANA FLORESCU, (Senior Member, IEEE), AND LUCIAN ANDREI PERIŞOARĂ

Department of Applied Electronics and Information Engineering, Faculty of Electronics, Telecommunications and Information Technology, University Politehnica of Bucharest, 060042 Bucharest, Romania

Corresponding author: Ionuţ-Constantin Guran (ionut.guran32@gmail.com)

ABSTRACT The migration towards green energy has seen a big increase in the number of electric vehicles and energy storage systems existing on the market, where the battery is a fundamental part. In order to provide the necessary voltage and current for the power supply of the system, the battery cells are connected in series and/or in parallel. These types of connections lead to an imbalance in the cells' state-of-charge over time and drastically decrease the battery life. In order to prevent this imbalance, a battery management system must be used. At the moment, the simulation is used before the physical implementation in order to verify the system design, with SPICE being the preferred mixed-signal simulator. However, the literature focuses on the physical design and implementation of BMS without treating the SPICE simulation. For this reason, this article proposes for the first time the implementation and verification of a passive battery management system simulation model in the most used SPICE-based environment, OrCAD Capture. The BMS model consists of a modular approach, with the following blocks used in the implementation: cell voltage sensing, battery pack current sensing, cell balancing, power supply, microcontroller. Each block is simulated and verified separately and then integrated into the final BMS model. The simulation results of the final BMS model show that the system performs the balancing of the cells correctly according to the balancing algorithm, while the maximum error in the measurement of the cell voltages and battery pack current is 1.5%. Based on these results, the proposed methodology can be used in the design of real-world battery management systems to reach the best possible architecture before the physical implementation, leading to cost and time optimization.

INDEX TERMS Battery, battery management system, state-of-charge, SPICE simulation model, cost optimization, time optimization.

LIST OF ACRONYMS

BMS (Battery Management System), SPICE (Simulation Program with Integrated Circuit Emphasis), EV (Electric Vehicle), ESS (Energy Storage Systems), SOC (State-of-Charge), SOH (State-of-Health), isoSPI (isolated Serial Peripheral Interface), EMU (Electric Multiple Unit), Li-ion (Lithium ion), MOSFET (Metal Oxide Semiconductor Field Effect Transistor), NTC (Negative Temperature Coefficient) DC (Direct Current), AC (Alternating Current), IoT (Internet of Things), PV (Photovoltaic), OCV (Open Circuit Voltage), LiFePO4 (Lithium Iron Phosphate), CALB (China Aviation Battery Limited), IC (Integrated Circuit), UVLO (Undervoltage Lockout), LDO (Low Drop-Out)

LIST OF SYMBOLS

I_{IN} (current sensor input current), CS_OUT (current sensor output voltage), RDS_{ON} (On-State Drain-Source Resistance), V_{GSth}(Gate-to-Source Threshold Voltage), V_{GS} (Gate-to-Source Voltage), V_{DS} (Drain-to-Source Voltage), I_{DS} (Drain-to-Source Current), V_{OUT} (Boost converter's output voltage), Rvref2 (lower resistor of Boost converter's target voltage resistive divider), Rvref1 (upper resistor of Boost converter's target voltage resistive divider), $I_{L,max}$

The associate editor coordinating the review of this manuscript and approving it for publication was Gian Domenico Licciardo.

(Boost converter's inductor L1 maximum current), ΔI_L(Boost converter's inductor L1 ripple current), $I_{OUT,max}$(desired maximum output current needed for the Boost converter application), $V_{IN,typ}$ (Boost converter's typical input voltage), L1 (Boost converter's inductance), f_s (Boost converter's switching frequency), $C_{OUT,min}$ (Boost converter's minimum output capacitor value), D (Boost converter's duty cycle), ΔV_{OUT} (Boost converter's output voltage desired ripple), $V_{IN,min}$ (Boost converter's minimum input voltage), η (Boost converter's efficiency)

I. INTRODUCTION

A. MOTIVATION

The battery is one of the most important components in electric vehicles (EV), energy storage systems (ESS), laptops, smartphones and other electronic equipment, being the main energy source in these applications [1], [2].

The battery management system (BMS) is another fundament component of systems powered by batteries [3]. A BMS is an electronic circuit which prevents the battery from operating outside its safety range. When any unexpected conditions in the functioning of a battery arise, the BMS must be able to take corrective actions [1], [4], [5].

One of the BMS primary roles is to keep the battery cells running at the same SOC. In order to do this, the BMS measures the battery cells' current and voltages, and then computes the battery SOC and SOH. Moreover, the BMS must stop the charging if an overvoltage condition on a battery cell is detected or disconnect the load if an undervoltage condition occurs. The BMS also performs the battery thermal management such that the battery temperature stays within the optimal operating range. The acquired data can be sent to a server for remote monitoring of the battery parameters [6], [7], [8], [9], [10]. All these characteristics of the BMS are briefly presented in Figure 1.

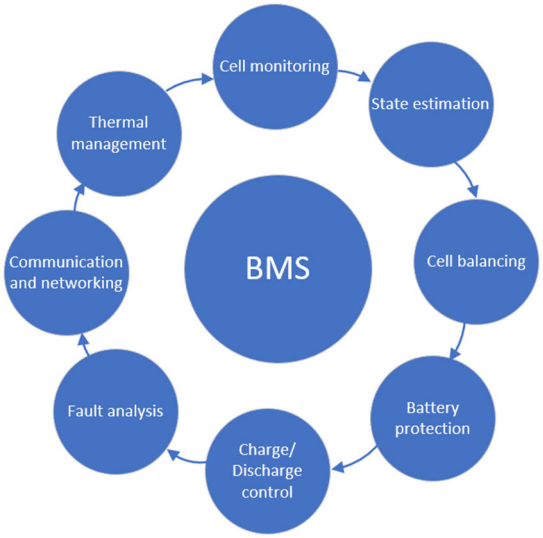

FIGURE 1. BMS general characteristics [2], [11].

Since the batteries have become widely used in applications from diverse domains, the battery management system has also become a topic of critical interest for researchers. Moreover, the simulation is the preferred method of choice for the system design verification nowadays, because it implies the testing of the design without physically implementing it, thus reducing the cost and the time. The most used simulator for analog-mixed signal circuits is SPICE, because there are many simulation environments using it, such as: OrCAD Capture, TINA, SIMetrix, LTSpice, and some of them do not require a paid license. However, a full-functionality BMS simulation model in SPICE has not been proposed until now. Having a SPICE simulation model before the physical implementation of a circuit is critical because this assures a fault-free design, optimizing both the development cost and time, as expressed previously. More details about existing work in the BMS domain is presented in the next section I-B.

B. LITERATURE SURVEY

Section I-B briefly presents the development directions in battery management systems in recent years.

In 2021, Wu et al. [12] proposed a battery management system designed for electric vehicles. The BMS monitors the battery status, improves its efficiency and prevents the over-discharging and over-charging of the battery cells. The designed BMS is based on the LTC6811 multi-cell battery stack monitor which communicates with the NuMicro M487 microcontroller through the LTC6820 isoSPI communications interface. The results present the practical implementation of the BMS, which displays the battery voltage and temperature using a user interface, without performing any simulation of the BMS before its physical implementation. The battery is composed of only one cell; hence the balancing process can not be performed.

In 2022, Liu et al. [13] presented the development of a BMS for the storage system of the auxiliary power unit, which is part of EMUs. The BMS is designed based on a master-slave approach, where the master module uses the S32K144 microcontroller, and the slave module uses the MC33771 Li-ion battery cell controller. The work presents the detailed hardware design schematics for both master and slave modules. Moreover, a cell SOC estimation model is built in MATLAB, in order to verify the SOC estimation method proposed by this paper. The conclusions show that the BMS can perform the real-time monitoring of the cell voltage, battery pack voltage and current, battery pack temperature, a ambient temperature, as well as the cells' SOC estimation. However, only a simulation model for the SOC estimation method is built in MATLAB, while the other functionalities of the BMS were not simulated prior to the physical implementation.

In 2022, Prakasha et al. [14] suggested a BMS for electric vehicles, which is able to determine the battery SOH, temperature, discharge rate, voltage, and current. The design

also uses a master-slave approach. The master controller is the Raspberry Pi microprocessor, and the slave controller is the Arduino Nano development board. The cell balancing is performed using a constant current load circuit based on the LM358 amplifier and the IRFZ44N MOSFET. The cell voltage measurement uses the Arduino analog pins, while the temperature measurement is performed using a 10k NTC thermistor. The results show that the BMS can detect automatically the most discharged cell in the battery and provides additional charge to it in order to keep its SOC in a safe area. However, no simulations were performed before the physical system implementation.

In 2022, Ding et al. [15] designed a BMS based on an active flyback DC/AC balancing circuit. There is one balancing DC/AC module for each cell of the pack. The DC side is connected to the cell's positive and negative terminals; one terminal of the AC side will be connected to the common AC side ground, and the other terminal is connected to the common voltage rail through the balancing resistor. The active balancing topology of the bidirectional DC/AC circuit is the zero-voltage switch resonance. The results show that the BMS can reach balancing currents of 1A, but there is no indication on the number of cells that the BMS was designed for, and also there were no simulations performed throughout the BMS design.

In 2022, Rehman et al. [16] proposed a cost-effective IoT based BMS for electric vehicles. The BMS is able to determine the cell voltage, the current flowing through the cells, the battery temperature, the power rating, as well as the cell SOC. In order to determine the cell voltage, a resistive voltage sensor was used, while the ACS712 current sensor module was used for the current measurement. For temperature measurement, the LM-35 temperature sensor was proposed. Arduino UNO development board was used for data acquisition, and the ESP8266 Wi-Fi module was interfaced with the microcontroller in order to send the acquired data to IoT channels. However, the designed BMS was only tested for one Li-ion cell and does not perform the cell balancing. Moreover, the design was not simulated before the physical implementation.

In 2022, Gullu et al. [17] presented a high voltage BMS design for PV energy systems. The proposed work focuses on describing the SOC estimation methods: OCV technique and Coulomb Counting technique, the modelling of a battery cell using the Thevenin model, including its thermal model, and the design of the three-level flying capacitor DC-DC converter used for the 5V power supply. The DC-DC converter was simulated using the MATLAB Simulink environment, but the design of the entire BMS circuit was not finalized.

In 2021, Guran et al. [18] proposed a four-cell passive BMS for Automotive Applications. The work presents the detailed design of the cell balancing circuit, the cell voltage monitoring circuit, the power supply circuits, and the processing and communication circuit. Moreover, the cell balancing and the cell voltage monitoring circuits were simulated using the LTSpice environment, but the creation of the simulation model for the entire BMS was not approached.

C. MAIN CONTRIBUTIONS OF THIS PAPER

The literature survey presented in section I-B shows that the BMS is a subject of a high importance for researchers, but mainly the physical design and verification have been extensively studied until now. The SPICE simulation has been approached in limited cases, but only for a part of the BMS circuitry. As a consequence, no full-functionality BMS model for SPICE or any other type of simulators has been proposed in the literature until now. The importance of creating a full-functionality BMS SPICE model is critical, because a physical BMS can be implemented afterwards using the SPICE model, reducing the development time and cost, simultaneously assuring a fault-free design.

For this reason, this paper proposes for the first time the SPICE model of a passive battery management system designed for four LiFePO4 cells connected in series. The SPICE-based simulator used in the BMS model development is OrCAD Capture.

The main contributions of this paper are:

- Development of the cell voltage sensing circuit model;
- Development of the battery pack current sensing model;
- Development of the passive cell balancing model;
- Development of the power supply circuit model;
- SPICE emulation of the microcontroller and the cell balancing algorithm;
- Integration of all the above-mentioned blocks into the final BMS model and simulation of the BMS model with the four-cell LiFePO4 battery pack;

D. PAPER STRUCTURE

The rest of this paper is organized as it follows: Section II presents the development of the internal BMS circuits' SPICE models, Section III represents the integration of the models developed in Section II into the final BMS model, which is then followed by the simulation of the BMS model together with the four-cell LiFePO4 pack model, Section IV presents the results and discussions based on the proposed BMS model, while the final Section V synthesizes the conclusions of this paper, highlighting the importance of this work in the electronics domain.

II. MODEL DESIGN OF THE BATTERY MANAGEMENT SYSTEM INTERNAL CIRCUITS

The proposed BMS model has the scope of assuring the balancing process of four series-connected LiFePO4 cells.

This section presents the LiFePO4 cell model that the proposed BMS model is connected to, along with the design of the BMS main internal circuits: the cell voltage sensing circuit, the battery current sensing circuit, the passive cell

balancing circuit, the power supply circuit, and the microcontroller.

A. LIFEPO4 CELL MODEL

The LiFePO4 cell model used in this paper is based on the implementation from [19]. The model implements the CA180FA cell specifications from CALB, which has a nominal capacity of 180Ah, the nominal operating voltage is 3.20V, the minimum discharging voltage is 2.5V, and the maximum charging voltage is 3.65V. The recommended discharging/charging current is 54A, the discharging current limit is 1800A, and the maximum internal resistance is 0.6mΩ.

The simulated open circuit voltage (OCV) vs. SOC characteristic for the LiFePO4 cell in [19] is presented in Figure 2. It can be noted that the OCV for a SOC of 0 is 2.5V and for a SOC of 1 is 3.5V.

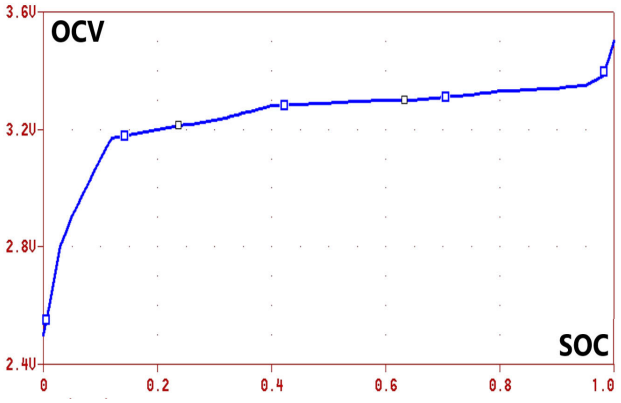

FIGURE 2. Simulated OCV vs. SOC characteristic of CA180FA cell [19].

B. CELL VOLTAGE SENSING CIRCUIT MODEL

The schematic view of the cell voltage sensing circuit model is presented in Figure 3. The input pins VIN+ and VIN− represent the battery cell positive and negative terminals connections, VS is the power supply pin, GND represents the ground point connection, while the pin OUT performs the difference between VIN+ and VIN−, and represents the cell voltage sensing model output pin.

U1 represents an instance of the INA148 chip model, which is a low-power, precision difference amplifier from Texas Instruments with a set gain of 1, having a high common mode input voltage range.

The INA148 difference amplifier supports both single and dual supply. The supported single supply range is 2.7V to 36V, while the supported dual supply range is ±1.35V to ±18V [20]. In the proposed BMS model, a 5V single supply will be used for INA148. The resulting maximum common-mode voltage for a 5V supply voltage is +75V. The resistor Rfilter and the capacitor Cfilter form a low-pass filter which eliminates the output pin (OUT) noise, while Cvs is the supply voltage capacitor, also having the role of rejecting the

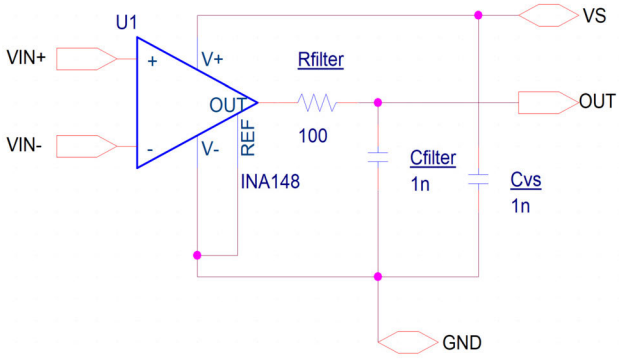

FIGURE 3. Schematic view of the cell voltage sensing circuit model.

supply noise. The simulation model of INA148 is available on Texas Instruments' website [21].

The internal schematic of INA148 is presented in Figure 4. $V_{IN}+$ and $V_{IN}-$ create the differential input, V_O is the output pin, V+ and V− represent the dual supply pins, and Ref is the reference voltage pin. A1 is a monolithic precision bipolar operational amplifier.

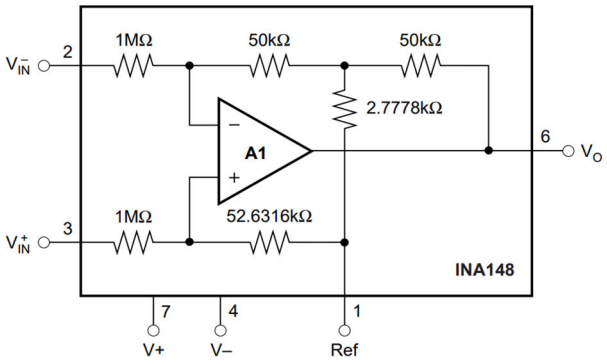

FIGURE 4. Internal schematic of INA148 [20].

The simulation testbench of the cell voltage sensing model is presented in Figure 5. The cell voltage sensing circuit model is C1, Vcm is the common-mode voltage source, Vdiff is the differential voltage source, and Vvs is the power supply source.

The simulation waveforms of the cell voltage sensing circuit model are shown in Figure 6. The supply voltage is 5V, and the common-mode voltage is set at 12V. The differential voltage (VIN+) - (VIN−) is increased linearly from 0V up to 5V. The output voltage OUT shows that the cell voltage sensing circuit output tracks the input difference accurately until 4.77V when the difference between input and output increases due to saturation.

C. BATTERY PACK CURRENT SENSING CIRCUIT MODEL

The schematic view of the battery pack sensing circuit model is shown in Figure 7. The CIN+ pin is the input current positive pin, CIN- is the input current negative pin, VS is

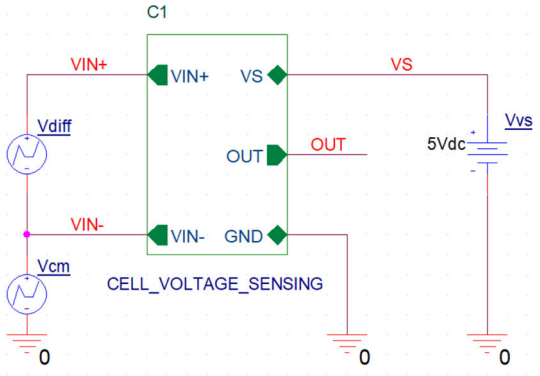

FIGURE 5. Simulation testbench of the cell voltage sensing circuit model.

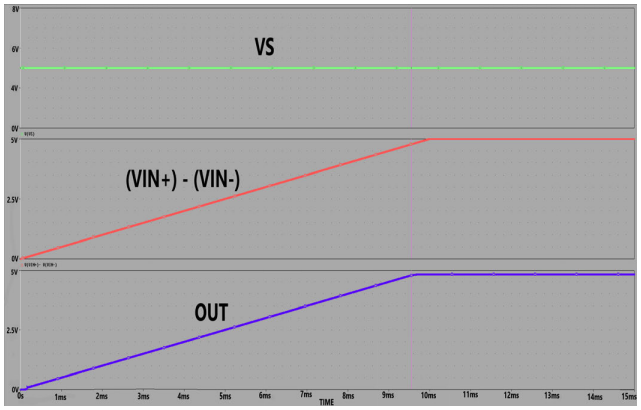

FIGURE 6. Simulation waveforms of the cell voltage sensing circuit model.

the positive supply voltage pin, CS_OUT is the current sensor output voltage, an GND is the ground connection pin. The capacitor C1 is the supply voltage filter capacitor and has a value of 100nF. The resistor R1 (1kΩ) and the capacitor C2 (1nF) form a 1μs time constant low-pass filter between the output (OUT) of the Hall-effect current sensor TMCS1107A1B and the current sensing circuit model output (CS_OUT).

The TMCS1107A1B IC is a galvanically isolated Hall-effect current sensor, which is able to measure AC or DC current with high accuracy and linearity. The input current between the IC pins IN+ and IN− flows through an internal conductor of 1.8mΩ internal resistance, which generates a magnetic field. The IC output voltage (OUT) is proportional to the input current, having a sensitivity of 50mV/A. The current sensor is supplied with 5V, and the zero current output voltage is 2.5V. The input current linear measurement range is ±46A [22].

The input current value I_{IN} is computed as it follows:

$$I_{IN} = \frac{CS\_OUT - 2.5V}{50mV/A} \quad (1)$$

The simulation testbench of the battery pack current sensing circuit model is presented in Figure 8. The Vcm voltage source represents the input common mode voltage, Iin is the input current piecewise linear (PWL) current source, and Vvs is the supply voltage source.

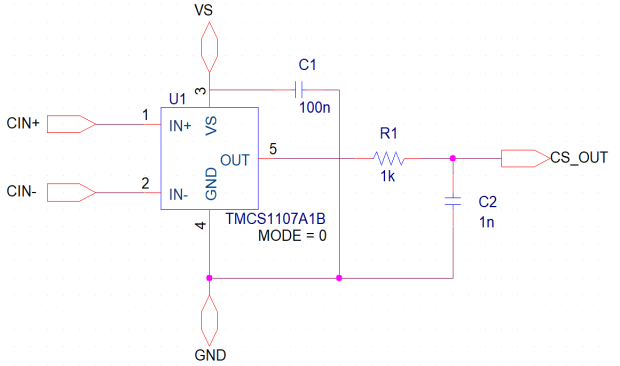

FIGURE 7. Schematic view of the battery pack current sensing circuit model.

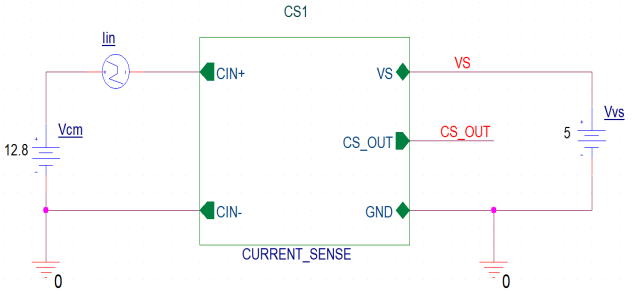

FIGURE 8. Simulation testbench of the battery pack current sensing circuit model.

The simulation waveforms of the battery pack current sensing circuit model are shown in Figure 9. The supply voltage VS is 5V and the common mode voltage Vcm is 12.8V, which is the nominal voltage of four-series connected LiFePO4 cells. When the input current Iin is 0A, the output voltage CS_OUT is 2.5V. When Iin is 46A, CS_OUT becomes 4.79V, and when Iin −46A, CS_OUT becomes 0.208V, which results in a simulated sensitivity of 49.8mV/A.

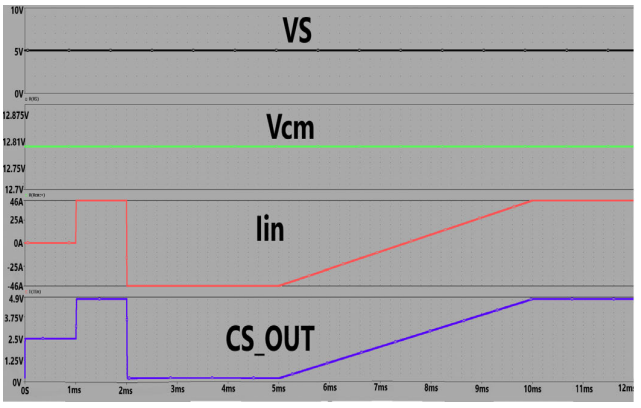

FIGURE 9. Simulation waveforms of the battery pack current sensing circuit model.

D. CELL BALANCING CIRCUIT MODEL

The schematic view of a single battery cell balancing circuit model is presented in Figure 10. CTRL is the control pin (active high) which turns-on the balancing circuit, VDD is the supply voltage pin, CEL+ is the battery cell positive terminal, and CEL- is the battery cell negative terminal.

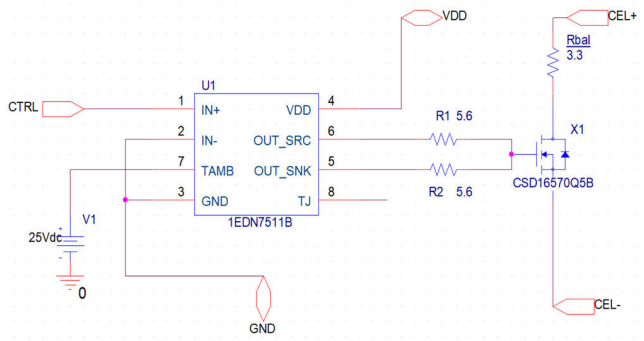

FIGURE 10. Schematic view of the cell balancing circuit model.

U1 represents an instance of the 1EDN7511B low-side gate driver from Infineon used here to drive into conduction the CSD16570Q5B transistor from Texas Instruments.

The simplified block diagram of 1EDN7511B is presented in Figure 11. IN+ is the non-inverting input pin, IN- is the inverting input pin, TAMB is the ambient temperature pin, GND is the ground pin, VDD is the positive supply voltage pin, OUT_SRC is the driver output sourcing pin, and OUT_SNK is the driver output sinking pin. The pins TAMB and TJ in Figure 10 are only used in the simulation model and do not appear in the real product.

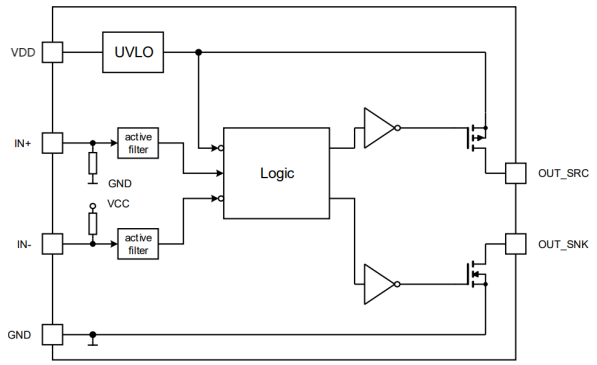

FIGURE 11. Simplified block diagram of 1EDN7511B gate driver.

The gate driver chip has a 4A sourcing and 8A sinking driving capability with a 19ns typical propagation delay between the input and output. Moreover, the IC presents undervoltage lockout (UVLO) protection functionality, having the UVLO turn-on threshold of 4.2V, and the UVLO turn-off threshold of 3.9V. The operating range for the VDD supply pin is 4.5V to 20V [23]. Pin TAMB is connected internally to 25V (which emulates the 25°C ambient temperature), while TJ is left open because the self-heating effect is not an object of this paper.

X1 represents an instance of the CSD16570Q5B N-Channel NexFET power MOSFET. NexFET is a new generation of power MOSFETs introduced with the aim to reduce the inherent parasitic capacitance, keeping similar RDS_{ON} values with the trench-gate power MOSFETs [24].

The transistor has a typical threshold voltage (V_{GSth}) of 1.5V, while the RDS_{ON} has typical values of 0.68mΩ at V_{GS} = 4.5V and of 0.48mΩ at V_{GS} = 10V. The maximum V_{DS} is 25V, the maximum V_{GS} is 20V, and the I_{DS} limit is 100A [25]. Figure 12 shows the I_{DS} vs. V_{GS} at V_{DS} = 5V for three distinct temperatures: −55°C, 25°C, 125°C. It can be noted that for V_{GS} voltages above 2V, I_{DS} become higher than 10A.

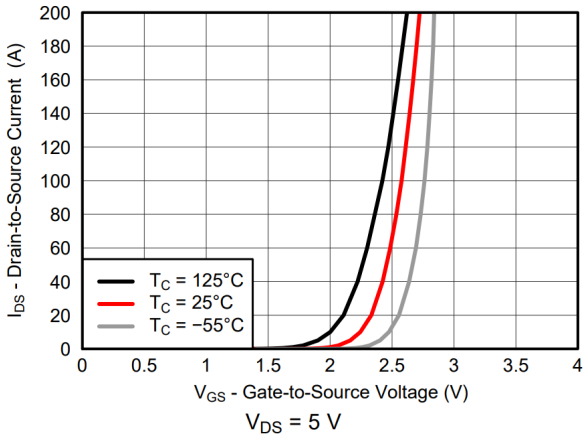

FIGURE 12. I_{DS} vs. V_{GS} characteristic of CSD16570Q5B.

The simulation models of 1EDN7511B [26] and CSD16570Q5B [27] are available online.

R1 and R2 have the role of preventing the ringing of OUT_SRC and OUT_SNK respectively. As the LiFePO4 cell voltage varies between 2.5V and 3.65V, and considering that the RDS_{ON} of CSD16570Q5B is neglectable, for a Rbal resistance value of 3.3Ω, the balancing current varies between 757mA and 1.1A.

The simulation testbench of the cell balancing circuit model is presented in Figure 13. Vvdd is the power supply source, Vctrl is the balancing process control source, Vcel- is the cell negative terminal potential, and Vcell is the actual cell voltage source.

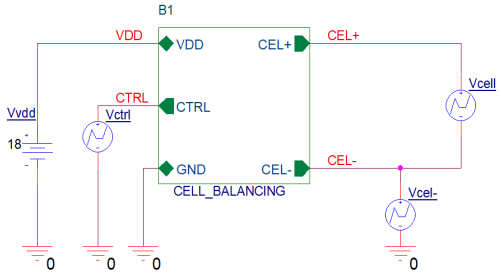

FIGURE 13. Simulation testbench of the cell balancing circuit model.

The cell balancing circuit is tested for two cases: the first one is considering that the cell under test is the fourth cell of the battery pack and all the previous three cells are fully charged, hence (Vcel-) = 3 · 3.65V = 10.95V; the second one is considering that the cell under test is the first cell of the battery pack, hence (Vcel-) = 0V.

The simulation waveforms of the cell balancing circuit model for (Vcel-) = 10.95V are presented in Figure 14. The VDD voltage is set at 18V, such that the balancing process can be performed for each cell of battery pack, keeping a minimum V_{GS} of 7.05V even for the fourth cell of the pack, and subsequently a low RDS_{ON}. When CTRL switches from 0V to 5V, the balancing process is turned on and the balancing current becomes 757.45mA for a cell voltage of 2.5V. If the cell voltage increases to 3.65V, the balancing current becomes 1.1059A. When CTRL switches from 5V to 0V, the balancing process is stopped.

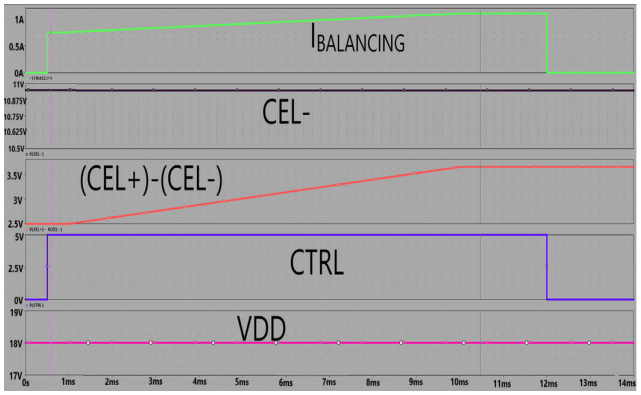

FIGURE 14. Simulation waveforms of the cell balancing circuit model for a common mode voltage of 10.95V.

The simulation waveforms of the cell balancing circuit model for (Vcel-) = 0V are presented in Figure 15. In this case the balancing current varies between 757.464mA for a cell voltage of 2.5V and 1.1059A for a cell voltage of 3.65V. The simulated behavior of the cell balancing circuit model is the expected one.

E. POWER SUPPLY CIRCUIT MODEL

The BMS circuit model needs two single-ended supply voltages: 18V for the supply of the cell balancing circuits, and 5V for the supply of the battery pack current sensing circuit, cell voltage sensing circuits and the microcontroller.

The schematic view of the power supply circuit model is shown in Figure 16. The power supply uses a Boost DC-DC converter to produce the 18V output voltage. VIN is the input voltage pin coming from the four-cell battery pack, GND is the ground pin, VOUT_18V is the 18V output pin and VOUT_5V is the 5V output pin of the TPS7B8850-Q1 LDO regulator.

The Boost converter uses the LM51231-Q1 synchronous Boost controller from Texas Instruments. The BIAS pin is the supply voltage of the VCC regulator which must be connected

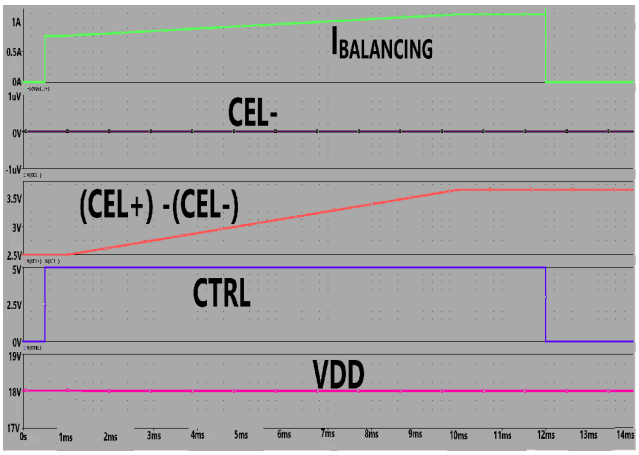

FIGURE 15. Simulation waveforms of the cell balancing circuit model for a common mode voltage of 0V.

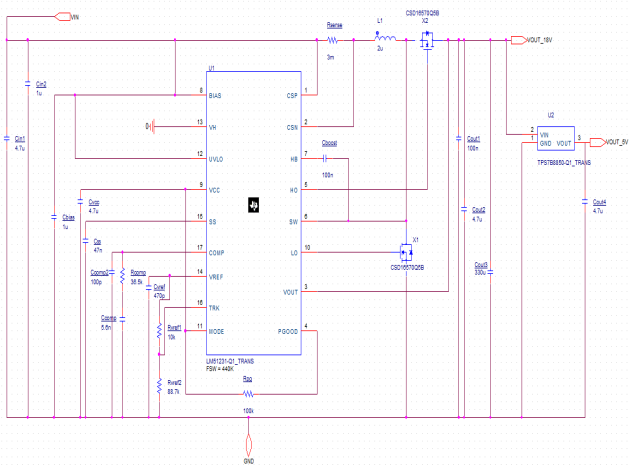

FIGURE 16. Schematic view of the power supply circuit model.

to GND through a 1μF capacitor (Cbias). VH is the spread spectrum frequency programming pin, but as this function is not needed, it is deactivated by connecting the pin to GND [28].

The UVLO pin is the undervoltage lockout programming pin, and connecting it to BIAS deactivates the functionality. The VCC pin is the output of the internal 5V VCC regulator. The maxim output current is 100mA, and it must be connected to GND through a 4.7μF capacitor (Cvcc). The SS pin is the soft-start programming pin: the ramp-up rate of the internal error amplifier (EA) reference is set through an internal current source of 20μA and an external capacitor. The suggested minimum soft start capacitor is 25nF, hence a 47nF capacitor (Css) will be used to reduce the soft start time. The COMP pin is the output of the internal EA, which must be connected to the loop compensation components, Rcomp, Ccomp and Ccomp2, which create a type-2 compensation loop [28], [29], [30].

The VREF pin is the 1.0V internal reference voltage output which must have a 470pF capacitor connected to GND. TRK

is the output regulation target programming pin. If the lower resistor Rvref2 is in the range 75kΩ -100kΩ, then the 5V-20V output voltage range is selected. If the TRK pin is connected directly to VREF then the output voltage is 20V [28]. The output voltage is computed as it follows:

$$V_{OUT} = 20V \cdot \frac{Rvref2}{Rvref2 + Rvref1} \tag{2}$$

Based on relation (2), a value of 88.7kΩ is chosen for Rvref2 and 10kΩ is chosen for Rvref1.

The MODE pin is the device switching mode selection pin: FPWM or diode emulation. Connecting the pin to VCC chooses the FPWM mode. The PGOOD pin is the power-good indicator pin, with open-drain output stage. It is connected to the VCC output through an 100kΩ pull-up resistor (Rpg). The VOUT pin is the output voltage sensing pin and must have an 100nF capacitor connected to GND (Cout1). The LO pin is the low-side gate driver output, which is connected to the gate of the X1 N-channel CSD16570Q5B transistor. The SW pin is the high-side MOSFET source voltage sensing pin. It is connected to the source of the X2 N-channel CSD16570Q5B transistor. The HO pin is the high-side gate driver output and it is connected directly to the gate of X2. The HB pin is the high-side driver supply and must have a 100nF capacitor Cboost connected to SW. The CSP and CSN pins represent the current sense amplifier positive and negative inputs. The voltage difference between CSP and CSN is amplified by a factor of 10 [28]. If this difference reaches 60mV, the Boost controller terminates the LO output. The inductor L1 maximum current ($I_{L,max}$) is computed as it follows:

$$I_{L,max} = \frac{60mV}{3m\Omega} = 20A \tag{3}$$

The inductor L1 ripple current (ΔI_L) is calculated as it follows [31], [32], [33]:

$$\Delta I_L = 0.3 \cdot I_{OUT,max} \cdot \frac{V_{OUT}}{V_{IN,typ}} \tag{4}$$

where $I_{OUT,max}$ is the desired maximum output current needed for the application (10A in this case), V_{OUT} is the converter output voltage of 18V, $V_{IN,typ}$ is the converter typical input voltage ($4 \cdot 3.2V = 12.8V$).

Based on equation (4), the inductor ripple current value becomes 4.21A. Moreover, the L1 inductance value is computed as [31], [32], and [33]:

$$L1 = \frac{V_{IN,typ} \cdot (V_{OUT} - V_{IN,typ})}{\Delta I_L \cdot f_s \cdot V_{OUT}} \tag{5}$$

where f_s is the converter switching frequency of 440kHz.

Based on equation (5) the calculated inductance value of L1 is 1.996μH, hence a 2μH inductor will be chosen.

The minimum output capacitor value ($C_{OUT,min}$) is calculated based on [31], [32], and [33]:

$$C_{OUT,min} = \frac{I_{OUT,max} \cdot D}{f_s \cdot \Delta V_{OUT}} \tag{6}$$

where D is the converter duty cycle, and ΔV_{OUT} is the output voltage desired ripple of 50mV.

D is calculated as it follows [31], [32], [33]:

$$D = 1 - \frac{V_{IN,min} \cdot \eta}{V_{OUT}} \tag{7}$$

where $V_{IN,min}$ is the minimum input voltage ($4 \cdot 2.5V = 10V$) and η is the converter efficiency (96% at loads higher than 4A).

Based on (7), D value results of 46.66% and based on (6), $C_{OUT,min}$ results of 212μF, hence Cout2 = 4.7μF and Cout3 = 330 μF are chosen.

U2 is an instance of the TPS7B8850-Q1 LDO regulator. It has three pins, VIN - the input voltage, VOUT - the output voltage, and GND - the ground pin. The input of U2 is connected at the output of the Boost converter (VOUT_18V) and it produces a 5V output VOUT_5V with a maximum current of 500mA. Since the internal VCC regulator of the Boost converter is limited at 100mA, TPS7B8850-Q1 is needed in order to increase the maximum generated load [34].

The simulation models of the LM51231-Q1 Boost controller [35] and TPS7B8850-Q1 [36] LDO regulator are available online.

The simulation testbench of the power supply circuit model is shown in Figure 17. Vvin is the input voltage source, IBOOST is the PWL current source connected to the VOUT_18V pin, and ILDO is the PWL current source drawing current from the VOUT_5V pin.

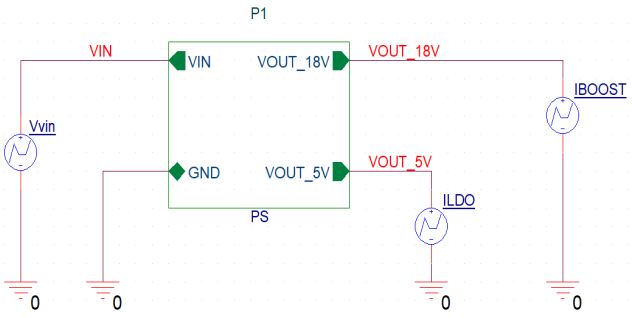

FIGURE 17. Simulation testbench of the power supply circuit model.

The simulation waveforms of the power supply circuit model are presented in Figure 18. At the beginning of the simulation, the input voltage VIN is set at 12.8V, which is the nominal voltage of four LiFePO4 cells connected in series.

The Boost converter's output voltage reaches its stationary value of 18V after around 845μs, which represents the soft-start time. The LDO output voltage (VOUT_5V) reaches the 5V stationary values after approximately 450μs. After 2ms, the LDO output current (ILDO) increases abruptly to 500mA, and after 200μs decreases abruptly down to 0A, causing an 0.5V amplitude undershoot and overshoot voltages with a duration of 40μs. Afterwards, IDLO increases slowly from 0A to 500mA without affecting VOUT_5V. At 4ms, the Boost converter output current (IBOOST) increases suddenly from 0A to 10A, causing the output voltage to drop from 18V to

17.75V for 200μs. At 4.2ms, IBOOST decreases suddenly from 10A to 0A, causing VOUT_18V to increase to 18.17V, dropping back at 18V after 270μs. IBOOST is then swept softly from 0A up to 10A without affecting VOUT_18V.

At 12ms, VIN increases abruptly from 12.8V up to 15V, which is approximately the maximum voltage of four LiFePO4 cells, without affecting significantly VOUT_18V or VOUT_5V. At 13ms, VIN drops abruptly from 15V to 10V, which is the minimum voltage of four LiFePO4 cells. This causes VOUT_18V to drop down to 16.57V, recovering in 3.6ms. At 15ms. VIN starts increasing softly from 10V up to 15V, without affecting VOUT_18V this time.

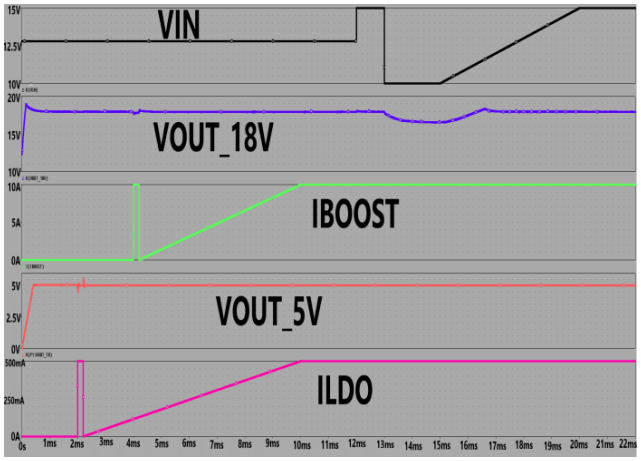

FIGURE 18. Simulation waveforms of the power supply circuit model.

F. MICROCONTROLLER MODEL

The BMS model uses an emulated microcontroller model which performs the following tasks: readout of each cell's voltage in the battery pack, readout of the battery pack current, and control of each cell's balancing circuit based on a specific algorithm.

The microcontroller model interface is presented in Figure 19. The VS is the power supply pin, RESET is the microcontroller's operation reset pin (active high), ADC0-ADC4 represent the analog-to-digital (ADC) converter input channels, OUT0-OUT3 represent the microcontroller's digital output channels, and GND is the ground connection pin. ADC4 will be used for the current measurement, while ADC0-ADC3 will be used for the cells' voltage measurement.

The SPICE code implementation for the microcontroller model is presented in Figure 20.

The four input ADC channels are sampled once a second with a frequency of 1Hz. Each time the sampling process begins, the order is ADC4 towards ADC0.

Each ADC channel will be sampled six times with a frequency of 1kHz, and the final ADC channel's sampled value is the average of the six acquired samples. Hence, two clock signals of 1Hz (VCLOCK_1Hz) and 1kHz

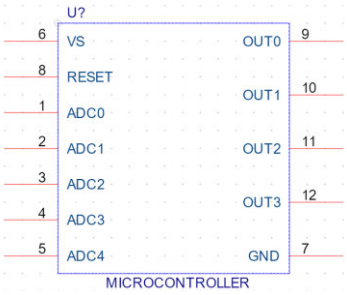

FIGURE 19. Microcontroller model interface.

```
.SUBCKT MICROCONTROLLER  ADC0 ADC1 ADC2 ADC3 ADC4 VS GND RESET  OUT0 OUT1 OUT2 OUT3
E1 CLRB 0 VALUE={IF(TIME<200n,0,1)}
E2 FREQUENCY_1Hz 0 VALUE={1}
E3 DUTY_CYCLE 0 VALUE={0.5}
XCLOCK_GENERATOR2   VCLOCK_1Hz_a 0  FREQUENCY_1Hz  DUTY_CYCLE CLRB  CLOCK_GENERATOR
E4 VCLOCK_1Hz GND VALUE={V(VCLOCK_1Hz_a)* V(VS,GND)}
X0  VCLOCK_1Hz_a  VCLOCK_1Hz_a_DEL DELAY_CELL PARAMS: DELAY_TIME=100u
E5  FREQUENCY_1KHZ  0 VALUE={1K}
E5A CLRB_1KHZ 0 VALUE={IF(TIME<200n | V(OUT_DW)<0.5,0,1)}
XCLOCK_GENERATOR1k   VCLOCK_1KHZ_A 0  FREQUENCY_1KHZ  DUTY_CYCLE CLRB_1KHZ  CLOCK_GENERATOR
E5B VCLOCK_1kHz GND VALUE={V(VCLOCK_1KHZ_A)* V(VS,GND)}
E6 CLK_UP 0 VALUE={V(VCLOCK_1KHZ_A)}
E7 RESET_UP 0 VALUE={IF(V(OUT_UP)>6.5,1,0)}
X1 RESET_UP RESET_UP_DEL DELAY_CELL PARAMS: DELAY_TIME=70u
E8 RESET_UP2 0 VALUE={IF(TIME<100n | V(RESET_UP_DEL) > 0.5,1,0)}
XUP_COUNTER   CLK_UP RESET_UP2 OUT_UP  UP_COUNTER PARAMS: DELAY_TIME=50u
E9 STARTING_VALUE 0 VALUE={5}
E10 CLK_DW 0 VALUE={IF(V(OUT_UP) > 6.5,1,0)}
E11 RESET_DW 0 VALUE={IF(TIME<200n | (V(VCLOCK_1Hz_a)>0.5 & V(VCLOCK_1Hz_a_DEL)<0.5),1,0)}
XDW_COUNTER   CLK_DW RESET_DW OUT_DW  STARTING_VALUE   DW_COUNTER    PARAMS:
+DELAY_TIME=100n
E12 IN 0 VALUE={TABLE(V(OUT_DW),0,0,1,V(ADC0),2,V(ADC1),3,V(ADC2),4,V(ADC3),5,V(ADC4))}
E13 CTRL 0 VALUE={V(VCLOCK_1KHZ_A)}
E14 RST 0 VALUE={IF( TIME <100n | V(OUT_UP)>6.5 | V(OUT_UP)<0.5,1,0)}
XSUM RST  CTRL IN OUT_SUM   SUMMING_CIRCUIT  PARAMS: DELAY_TIME=100n
E15 IN_REGISTER 0 VALUE={V(OUT_SUM)/6}
E16 CTRL_ADC4   0 VALUE={IF(V(OUT_DW) >4.5 & V(OUT_UP) > 5.5 & V(OUT_UP) < 6.5 &
+V(VCLOCK_1KHZ_A)<0.5 & V(VCLOCK_1KHZ_A_DEL)>0.5,1,0)}
E17 CTRL_ADC3   0 VALUE={IF(V(OUT_DW) >3.5 & V(OUT_DW)<4.5 & V(OUT_UP) > 5.5 & V(OUT_UP) <
+6.5 & V(VCLOCK_1KHZ_A)<0.5 & V(VCLOCK_1KHZ_A_DEL)>0.5,1,0)}
E18 CTRL_ADC2   0 VALUE={IF(V(OUT_DW) >2.5 & V(OUT_DW)<3.5 & V(OUT_UP) > 5.5 & V(OUT_UP) <
+6.5 & V(VCLOCK_1KHZ_A)<0.5 & V(VCLOCK_1KHZ_A_DEL)>0.5,1,0)}
E19 CTRL_ADC1   0 VALUE={IF(V(OUT_DW) >1.5 & V(OUT_DW)<2.5 & V(OUT_UP) > 5.5 & V(OUT_UP) <
+6.5 & V(VCLOCK_1KHZ_A)<0.5 & V(VCLOCK_1KHZ_A_DEL)>0.5,1,0)}
E20 CTRL_ADC0   0 VALUE={IF(V(OUT_DW) >0.5 & V(OUT_DW)<1.5 & V(OUT_UP) > 5.5 & V(OUT_UP) <
+6.5 & V(VCLOCK_1KHZ_A)<0.5 & V(VCLOCK_1KHZ_A_DEL)>0.5,1,0)}
X2 VCLOCK_1KHZ_A  VCLOCK_1KHZ_A_DEL DELAY_CELL PARAMS: DELAY_TIME=3u
XADC4  RESET CTRL_ADC4 IN_REGISTER ADC4_SAMPLE   REGISTER
XADC3  RESET CTRL_ADC3 IN_REGISTER ADC3_SAMPLE   REGISTER
XADC2  RESET CTRL_ADC2 IN_REGISTER ADC2_SAMPLE   REGISTER
XADC1  RESET CTRL_ADC1 IN_REGISTER ADC1_SAMPLE   REGISTER
XADC0  RESET CTRL_ADC0 IN_REGISTER ADC0_SAMPLE   REGISTER
EMIN MINIMUM_VOLTAGE 0 VALUE={MIN(MIN(MIN(V(ADC3_SAMPLE),V(ADC2_SAMPLE)),V(ADC1_SAMPLE)),
+V(ADC0_SAMPLE))}
EOUT0 OUT0 GND VALUE={IF(V(OUT_DW)<0.5 & V(ADC0_SAMPLE,MINIMUM_VOLTAGE) > 25m,5,0)}
EOUT1 OUT1 GND VALUE={IF(V(OUT_DW)<0.5 & V(ADC1_SAMPLE,MINIMUM_VOLTAGE) > 25m,5,0)}
EOUT2 OUT2 GND VALUE={IF(V(OUT_DW)<0.5 & V(ADC2_SAMPLE,MINIMUM_VOLTAGE) > 25m,5,0)}
EOUT3 OUT3 GND VALUE={IF(V(OUT_DW)<0.5 & V(ADC3_SAMPLE,MINIMUM_VOLTAGE) > 25m,5,0)}
.ENDS MICROCONTROLLER
```

FIGURE 20. SPICE code implementation of the microcontroller model.

(VCLOCK_1kHz) are implemented inside the microcontroller model, using the technique presented in [37].

In order to set the sampled ADC channel, a down counter (XDW_COUNTER) is implemented using the methodology shown in [38]. When the down-counter's output (OUT_DW) is 5, ADC4 input is sampled, and when the down-counter's output OUT_DW is 1, ADC0 input is sampled.

In order to count the number of samples acquired for each channel, an up-counter (XUP_COUNTER) is implemented using the technique proposed in [39]. At each rising edge of the 1kHz clock signal, the up-counter's output (OUT_UP) is incremented. When OUT_UP reaches the value of 7V, that means the six samples have been acquired, OUT_UP is reset to 0V and the down-counter's output (OUT_DW) is decremented if the current sampled channel is ADC4-ADC1, or the sampling process ends if the current sampled channel is ADC0. OUT_DW is reset to 5V when a new

sampling interval begins on the rising edge of the 1Hz clock (VCLOCK_1Hz).

In order to not interfere with the cell voltages and current measurement processes, the balancing algorithm is stopped during the sampling period and is turned on when the sampling of all five channels has ended. The balancing algorithm, computes the minimum value of the 4 four sampled cell voltage values (ADC3-ADC0). If a sampled cell voltage is larger than the minimum cell voltage by at least 25mV, the corresponding output is turned on. The OUTx output corresponds to the ADCx input channel, where x takes values from 0 to 3. Whenever the RESET pin is high (5V), the microcontroller operation is reset and the operation is restored again when the RESET becomes low (0V). Also, if the supply voltage VDD is lower than 4.3V, the microcontroller is reset.

The simulation testbench of the proposed microcontroller model is presented in Figure 21. Vvs is the 5V power supply source, Vreset is the reset signal source, Vadcx is the input signal source on the ADCx channel. In this simulation, Vadc0 is set at 2.567V, Vadc1 at 3.005V, Vadc2 at 3.31V, Vadc3 at 3.65V, and Vadc4 at 4.87V.

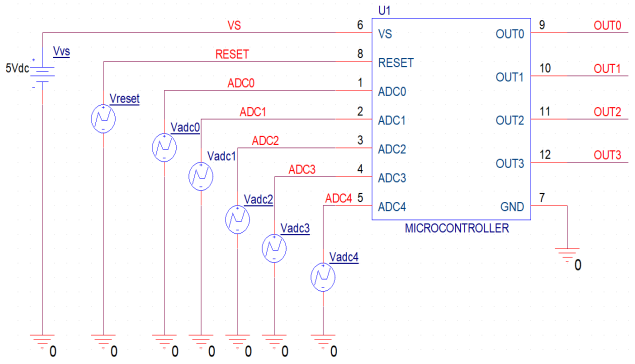

FIGURE 21. Simulation testbench of the microcontroller model.

The simulation waveforms of the proposed microcontroller model for multiple sampling periods are shown in Figure 22.

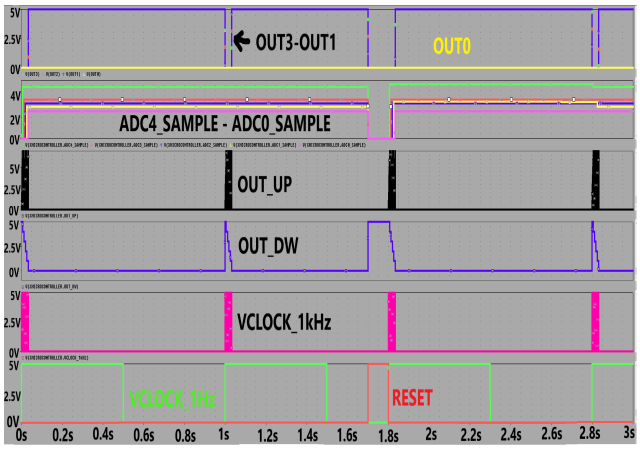

FIGURE 22. Simulation waveforms of the microcontroller model for multiple sampling periods.

It can be noticed that the sampling period always begins on the rising edge of the 1Hz clock signal (VCLOCK_1Hz), when the 1kHz clock signal (VCLOCK_1kHz) starts switching. The up-counter output (OUT_UP) increases on every rising edge of VCLOCK_1kHz. The first sampled channel is ADC4 when the down-counter output (OUT_DW) is 5V. When the sampling process of one input channel ends, meaning that OUT_UP has reached the value of 7V, OUT_DW is decreased, OUT_UP is reset to 0V and the process is repeated. Whenever the sampling of one input channel ADCx is done, the corresponding sample ADCx_SAMPLE is obtained. The sampling period stops when OUT_DW becomes 0V.

It can also be noticed that the cell balancing is performed only outside the sampling intervals, when VCLOCK_1kHz is not switching and OUT_DW and OUT_UP are 0V. As the minimum cell voltage is connected to ADC0, OUT0 is 0 and the balancing is performed only for OUT3-OUT1, corresponding to input signals ADC3-ADC1.

When reset becomes high (5V) the microcontroller stops operation and all the signals become 0V, apart from OUT_DW which is reset to the initial value of 5V.

In order to better visualize one sampling period, the simulation waveforms of the proposed microcontroller model for one sampling period are presented in Figure 23. The transition from one input channel to another can be seen by looking at the OUT_DW signal, whereas the number of samples acquired for each channel can be visualized by looking at the OUT_UP signal. The input ADC channels measured sampled values are: ADC0_SAMPLE = 2.566V, ADC1_SAMPLE = 3.0045, ADC2_SAMPLE = 3.3095V, ADC3_SAMPLE = 3.6494V, ADC4_SAMPLE = 4.8692V.

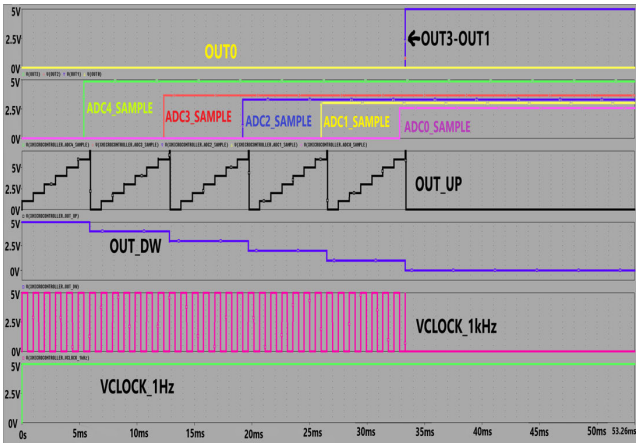

FIGURE 23. Simulation waveforms of the microcontroller model for one sampling period.

III. FINAL BATTERY MANAGEMENT SYSTEM MODEL

The final battery management system model is obtained by connecting together in one circuit all the models presented in Section II. The schematic view of the final BMS model

internal schematic is presented in Figure 24. It can be noted that there are four cell voltage sensing circuits and four cell balancing circuits, one for each cell in the four-cell LiFePO4 battery. The pins SENSE_CELx+ are connected to the positive terminal of the corresponding cell, while the pins SENSE_CELx- are connected to the negative terminal of the corresponding cell. For example, the fourth cell in the battery is connected between pins SENSE_CEL4+ and SENSE_CEL4−.

The pins BLC_CELx+ and BLC_CELx− are connected to the positive terminal and negative terminals respectively of the corresponding cell, and perform the balancing when they are activated by the microcontroller digital output.

The pin VIN represents the input voltage pin for the power supply circuit P1, and connects to the fourth cell positive terminal typically, while the pin GND represents the BMS circuit ground and connects to the first cell negative terminal. The pin VOUT_18V is the 18V voltage produced by the internal Boost converter referenced to the BMS ground, while VOUT_5V is the 5V voltage produced by the internal LDO, also referenced to the BMS ground.

In order to sense the charging or discharging currents flowing in or out of the battery pack, the charger/load must be connected to the CURRENT_SENSE+ pin, while the fourth cell positive terminal is connected to the CURRENT_SENSE− pin.

The cell balancing circuits B1-B4 are supplied by the 18V voltage produced by P1 and are controlled by the microcontroller digital outputs OUT0-OUT3 based on the implemented algorithm presented in Section II-F. The cell voltage sensing circuits C1-C4 are supplied by the 5V voltage produced by P1 and their outputs are connected to the microcontroller's input ADC channels, ADC0-ADC3. The microcontroller U1 and the current sensing circuit CS1 are also supplied by the 5V voltage produced by P1, and the output of CS1 is connected to the microcontroller U1 input ADC4.

The simulation testbench of the final BMS model is shown in Figure 25. The BMS performs the balancing of the four LiFePO4 cells U1-U4 presented in Section II-A, which are connected in series. The LiFePO4 cell model used is presented in detail in [19] and has three pins: CEL+ is the positive terminal voltage, CEL- is the negative terminal voltage, and SOC is the current SOC of the cell. The initial cell SOC at the beginning of the simulation can be set using the parameter INITIAL_SOC.

The battery pack positive voltage (CEL4+ net) is connected to the input of the power supply circuit, namely the VIN pin. The battery pack load represented through the current source ILOAD is connected to the CURRENT_SENSE+ pin, while the battery pack positive terminal is connected to the CURRENT_SENSE- pin. In this way, the current sensor is placed in series with the battery pack and the load.

The simulation waveforms of the final BMS model are presented in Figure 26. The voltage VOUT_5V reaches its

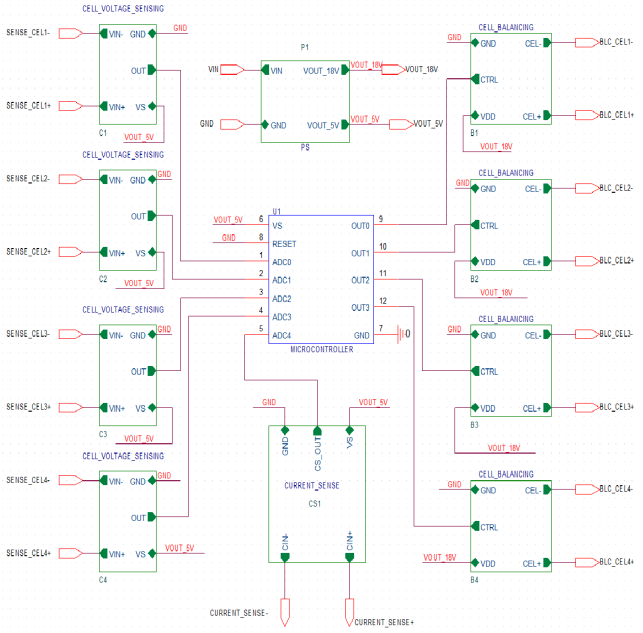

FIGURE 24. Schematic view of the final BMS model.

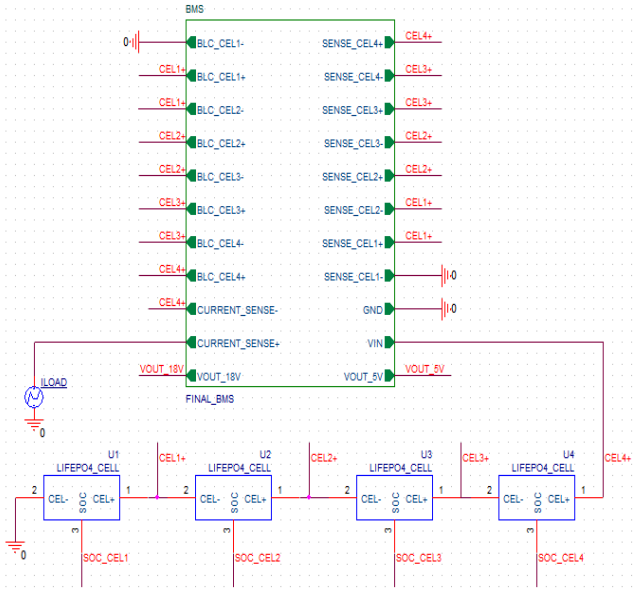

FIGURE 25. Simulation testbench of the final BMS model.

stationary value of 5.023V after 870μs, and VOUT_18V reaches the stationary value of 17.996V after 845μs. The cells' SOC is set at the beginning of the simulation through the parameter INITIAL_SOC: cell 1 SOC is set at 1, cell 2 SOC is set at 0.65, cell 3 SOC is set at 0.1, and cell 4 SOC is set at 0.3 (signals SOC_CELx in Figure 26). Based on the cells' SOC, the cell voltages become: $V_{CEL1} = 3.4874$V, $V_{CEL2} = 3.288$V, $V_{CEL3} = 3.088$V, $V_{CEL4} = 3.218$V. Once the VOUT_5V voltage reaches 4.3V at 715μs, the microcontroller enters the normal operation mode and the sampling of the ADC channels begins.

The first sampled channel is ADC4 and corresponds to the battery pack current. There is a 20A external load connected to the battery and the acquired ADC4_SAMPLE is 1.5149V. Using equation (1) the sampled battery current value is -19.7A and the relative error is 1.5%. The next sample is ADC3_SAMPLE which corresponds to the cell 4 voltage and has a value of 3.2167V, which results in a relative error of 0.04% to the $V_{CEL4} = 3.218$V real value. Afterwards, ADC2 channel, corresponding to cell 3 voltage, is sampled and the resulting ADC2_SAMPLE is 3.087V. Compared to $V_{CEL3} = 3.088$V, the relative error is 0.03%. The ADC1_SAMPLE value of 3.2872V corresponds to the cell 2 voltage ($V_{CEL2} = 3.288$V) and the relative error is 0.02%, while the ADC0_SAMPLE value of 3.4871V corresponds to the cell 1 voltage ($V_{CEL1} = 3.4874$V) and the relative error is 0.008%.

Knowing that cell 3 has the minimum voltage, it can be noted that once the sampling process ends, only cells 1, 2, and 4 have the balancing circuits activated. I_{BLCx} is the balancing current of cell x. The balancing currents are: $I_{BLC1} = 1.0566$A for cell 1, $I_{BLC2} = 0.996$A for cell 2, $I_{BLC4} = 0.974$A and their value can be computed as the cell voltage divided to the balancing resistor value of 3.3Ω. The simulation waveforms file size resulted in 126GB for a simulation time of 240ms, hence multiple sampling periods couldn't be displayed.

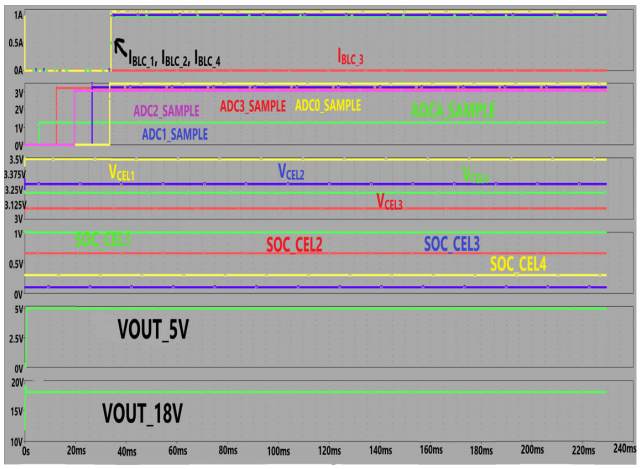

FIGURE 26. Simulation waveforms of the final BMS model.

IV. RESULTS AND DISCUSSION

The BMS model design starts with the LiFePO4 battery cell model in SPICE, described in section III-A, which uses the implementation from [19]. From the simulated characteristics, the cell voltage varies between 2.5V and 3.5V for a cell SOC varying between 0% and 100%.

The next step is establishing the main blocks of the passive BMS: cell voltage sensing circuit, battery pack current sensing circuit, cell balancing circuit, power supply circuit, and microcontroller.

The cell voltage sensing circuit, described in section II-B, is supplied with a voltage of 5V and supports an input common-mode voltage range between −75V and +75V. The simulation results show that the output voltage varies at the fourth decimal for differential input voltages between 200mV and 4.77V, which translates into a neglectable error (<0.001%). For input voltages below 200mV and 4.77V, the cell voltage sensing circuit saturates and the output voltage can not be considered in order to accurately read the input voltage. However, as the LiFePO4 cell produces voltages varying between 2.5V and 3.5V, the proposed cell voltage sensing circuit can be used successfully in the BMS model design.

The battery pack current sensing circuit, described in section II-C is able to measure both charging and discharging currents flowing through the LiFePO4 battery pack. The circuit is supplied by a single polarity voltage of 5V, has a zero current output voltage of 2.5V and a theoretical sensitivity of 50mV/A. Moreover, the input current linear measurement range is ±46A, making it a good choice considering that the recommended current range for the LiFePO4 cell is ±54A. The simulation results show that when the input current is 0A, the output voltage of the circuit is exactly 2.5V. By varying the current between -46A and 46A, the output of the current sensing circuit varies between 0.208V and 4.79V, which results in a simulated sensitivity of 49.8mV/A. The relative error to the theoretical sensitivity of 50mV/A is 0.4%, which shows that the proposed implementation of the battery pack current sensing circuit is suitable to be used in the BMS model design.

The cell balancing circuit model, described in section II-D, uses the 1EDN7511B low-side gate driver circuit from Infineon, which drives into conduction the CSD16570Q5B transistor from Texas Instruments, allowing the balancing process to be performed. The cell balancing circuit is supplied with a VDD voltage of 18V and performs the cell balancing when the control signal CTRL is 5V. A 3.3Ω resistor is placed in series with the power transistor CSD16570Q5B. As the RDS_{ON} of the transistor into conduction is around 0.5mΩ, it can be neglected. As the LiFePO4cell voltages vary between 2.5V and 3.65 (maximum allowed voltage at any time), the theoretical balancing currents vary between 757mA and 1.1A. The simulation results show that the balancing currents vary between 757.45mA and 1.1059A when the cell voltage varies between 2.5V and 3.65V, leading to a relative error varying between 0.059% and 0.53%, proving that the proposed cell balancing circuit model provides reliable results.

The power supply circuit model, described in II-E produces an 18V output voltage for the supply of the cell balancing circuits and a 5V output voltage for the supply of the battery pack current sensing circuit, cell voltage sensing circuits and the microcontroller. This power supply circuit model uses the

LM51231-Q1 synchronous Boost controller from Texas Instruments to produce the 18V voltage and the TPS7B8850-Q1 LDO regulator to produce the 5V output. The simulation results show that the Boost converter's output voltage reaches its stationary value of 18V after around 845μs, and the LDO output voltage reaches the 5V stationary values after

approximately 450μs, which represent the startup times. During simulation, both line jumps and load jumps are performed, showing that the Boost converter and the LDO recover successfully from these events. Considering this, the proposed power supply circuit model can be used successfully in the BMS model design.

The microcontroller model, described in section II-F, emulates the basic functions of a real microcontroller and performs the following tasks: readout of each cell's voltage in the battery pack, readout of the battery pack current, and control of each cell's balancing circuit based on a specific algorithm. The four ADC channels are sampled once a second with a frequency of 1Hz and each ADC channel will be sampled six times with a frequency of 1kHz, while the final ADC channel's sampled value is the average of the six acquired samples. The balancing algorithm, computes the minimum value of the four sampled cell voltage values. If a sampled cell voltage is larger than the minimum cell voltage by at least 25mV, the corresponding output is turned on. In order not to interfere with the cell voltages and current measurement process, the balancing algorithm is stopped during the sampling period and is turned on when the sampling of all five channels has ended. The simulation results show that the microcontroller model behaves as expected, performing successfully all the required tasks. Although the microcontroller model could be replaced by voltage sources connected to each balancing circuit and controlled by the user, the BMS model could not be considered complete and could not perform its task successfully without the help of an external user.

The final BMS model is obtained by bringing together in one circuit all the models described in section II. In the final BMS model there are four cell voltage sensing circuits, four cell balancing circuits, one battery pack current sensing circuit, one power supply circuit and one microcontroller. The relative errors of the sampled voltages and battery current vary between 0.008% and 1.5% which lead to a high overall performance of the BMS model with regards to the sampling aspect. Moreover, it can be noticed that the balancing algorithm works as expected, by activating all the balancing circuits corresponding to the cell voltages which are at least 25mV higher than the minimum value.

Based on the simulation results mentioned above, the proposed BMS model represents a breakthrough in the simulation domain, being the first implemented BMS model which has all the required functionalities of a modern BMS, including the microcontroller. The accuracy of this proposed BMS model is a high one, where all the measurement errors do no exceed 1.5%; it can be concluded that the modeled BMS can be successfully translated into a real-world BMS. There is no comparison that can be made with other BMS models in terms of accuracy, efficiency, or practicality, because this is the first work of this kind in the simulation domain.

The practical implications of this work in developing a real world BMS are very important, because the BMS can now be fully simulated before the physical design and reach the best implementation only by simulation, leading to a cost, time and functionally efficient design.

The potential challenges and limitations that the engineers might face when implementing the BMS simulation model in practice are given by the microcontroller model, which emulates only the basic functionality of a real microcontroller. Hence, a real microcontroller is more advanced than the proposed microcontroller model, but depending on the necessity, the microcontroller model can be enhanced with the new desired functionality.

V. CONCLUSION

In this paper, a SPICE model of a battery management system designed for four series-connected LiFePO4 cells was proposed for the first time. The BMS model measures the voltage of each cell in the battery pack, along with the charging/discharging currents, and performs the passive balancing of the cells. The passive balancing implies the discharging of the most charged cells through a shunting resistor, hence resulting into energy dissipation. This allows the most charged cells to reach the same state-of-charge as the most discharged cell over a long period of time.

The BMS model development and testing is performed in OrCAD Capture, which is the most used SPICE-based simulator at the moment. The verification shows that the BMS model works as expected, performing correctly all the implemented tasks. The relative errors for the sampled cell voltages vary between 0.008% and 0.04%, while the sampled current relative error is 1.5%.

The results of the study presented in this paper can be described from a multidimensional perspective as it follows: (1) the relative errors of the BMS model measurements are less than 1.5% which prove its high overall performance; (2) at this moment it is impossible to create a comparison with other BMS models as this is the first work which proposed a BMS model having all the functionalities of a modern BMS, including the a microcontroller; (3) the practical implications of this work are very important, because the proposed model opens a way of creating real-world battery management systems starting from the simulation model, reducing the development time, cost and flaws; (4) the proposed BMS model also has limitations, because it uses a microcontroller model that emulates just the basic functionality of a real one; however, the existing microcontroller model can be tailored with new functionalities and specifications based on the user's needs.

Considering that the BMS is a topic of high importance for researchers nowadays, when the migration towards green energy has seen the number of battery powered systems increase drastically, the proposed SPICE model of a passive battery management system fills a big gap in the electronics simulation domain, given the fact that only the BMS physical design and verification have been approached until now, while the simulation only focused on part of the BMS internal circuits. This work proposes for the first time a SPICE model

of a battery management system which emphasizes all the functionalities of a modern BMS.

REFERENCES

[1] B. Devi and V. S. Kumar, "Lithium-ion battery management system: A review," in *Proc. Int. Conf. Power, Energy, Control Transmiss. Syst. (ICPECTS)*, Chennai, India, Dec. 2022, pp. 1–6, doi: 10.1109/ICPECTS56089.2022.10047494.

[2] R. Pakdel, M. Yavarinasab, M. R. Zibad, and M. R. Almohaddesn, "Design and implementation of lithium battery management system for electric vehicles," in *Proc. 9th Iranian Conf. Renew. Energy Distrib. Gener. (ICREDG)*, Mashhad, Iran, Feb. 2022, pp. 1–6, doi: 10.1109/ICREDG54199.2022.9804549.

[3] P. Maithili, R. Kavitha, R. Nithishkumar, T. Ganeshbharathi, S. V. Kannan, and R. M. Kumar, "Intelligent battery management system," in *Proc. Int. Conf. Advancements Electr., Electron., Commun., Comput. Autom. (ICAECA)*, Puducherry, India, Oct. 2021, pp. 1–5, doi: 10.1109/ICAECA52838.2021.9675596.

[4] M. Kamel, V. Sankaranarayanan, R. Zane, and D. Maksimovic, "State-of-charge balancing with parallel and series output connected battery power modules," *IEEE Trans. Power Electron.*, vol. 37, no. 6, pp. 6669–6677, Jun. 2022, doi: 10.1109/TPEL.2022.3143835.

[5] R. Zhang, J. Wu, R. Wang, R. Yan, Y. Zhu, and X. He, "A novel battery management system architecture based on an isolated power/data multiplexing transmission bus," *IEEE Trans. Ind. Electron.*, vol. 66, no. 8, pp. 5979–5991, Aug. 2019, doi: 10.1109/TIE.2018.2873143.

[6] Y.-D. Yang, K.-Y. Hu, and C.-H. Tsai, "Digital battery management design for point-of-load applications with cell balancing," *IEEE Trans. Ind. Electron.*, vol. 67, no. 8, pp. 6365–6375, Aug. 2020, doi: 10.1109/TIE.2019.2940001.

[7] Y. Shang, C. Zhang, N. Cui, and C. Mi, "A delta-structured switched-capacitor equalizer for series-connected battery strings," *IEEE Trans. Power Electron.*, vol. 34, no. 1, pp. 452–461, Jan. 2018, doi: 10.1109/TPEL.2018.2826010.

[8] Y. Shang, S. Zhao, Y. Fu, B. Han, P. Hu, and C. C. Mi, "A lithium-ion battery balancing circuit based on synchronous rectification," *IEEE Trans. Power Electron.*, vol. 35, no. 2, pp. 1637–1648, Feb. 2020, doi: 10.1109/TPEL.2019.2917390.

[9] M. K. Al-Smadi and J. A. A. Qahouq, "Evaluation of current-mode controller for active battery cells balancing with peak efficiency operation," *IEEE Trans. Power Electron.*, vol. 38, no. 2, pp. 1610–1621, Feb. 2023, doi: 10.1109/TPEL.2022.3211905.

[10] Z. Gong, A. Kachura, S. A. Assadi, N. Cusimano, J. Piruzza, J. Xu, and O. Trescases, "An EV-scale demonstration of in-situ battery electrochemical impedance spectroscopy and BMS-limited pack performance analysis," *IEEE Trans. Ind. Electron.*, vol. 70, no. 9, pp. 9112–9122, Sep. 2023, doi: 10.1109/TIE.2022.3215833.

[11] K. Lin, Y. Chen, Y. Liu, and B. Zhang, "Reliability prediction of battery management system for electric vehicles based on accelerated degradation test: A semi-parametric approach," *IEEE Trans. Veh. Technol.*, vol. 69, no. 11, pp. 12694–12704, Nov. 2020, doi: 10.1109/TVT.2020.3012197.

[12] T.-H. Wu, T.-Y. Pai, C.-H. Liu, and P.-Y. Chen, "Design of battery management system for electric vehicles," in *Proc. Int. Symp. Intell. Signal Process. Commun. Syst. (ISPACS)*, Hualien City, Taiwan, Nov. 2021, pp. 1–2, doi: 10.1109/ISPACS51563.2021.9650999.

[13] H. Liu, Y. Li, B. Duan, and L. Li, "Development and application of battery management system for storage system of the auxiliary power unit of EMUs," in *Proc. 4th Int. Conf. Smart Power Internet Energy Syst. (SPIES)*, Beijing, China, Dec. 2022, pp. 1911–1915, doi: 10.1109/SPIES55999.2022.10082066.

[14] G. Prakasha, S. S. Kumar, K. N. S. Kumar, A. B. Darshan, and G. Venkatesha, "Electric vehicle battery power management system analysis," in *Proc. Int. Interdiscipl. Humanitarian Conf. Sustainability (IIHC)*, Bengaluru, India, Nov. 2022, pp. 1179–1183, doi: 10.1109/IIHC55949.2022.10060304.

[15] S. Ding, S. Liu, H. Chen, Y. Yang, and J. Huang, "Research on battery management system based on flyback DC-AC converter," in *Proc. IEEE 6th Inf. Technol. Mechtron. Eng. Conf. (ITOEC)*, Chongqing, China, Mar. 2022, pp. 802–806, doi: 10.1109/ITOEC53115.2022.9734330.

[16] M. H. Rehman, A. Alam, and A. Q. Ansari, "Design of a cost-effective IoT based battery management system for electric vehicles," in *Proc. Int. Conf. Power, Instrum., Energy Control (PIECON)*, Aligarh, India, Feb. 2023, pp. 1–5, doi: 10.1109/PIECON56912.2023.10085853.

[17] S. Gullu, M. T. Elrais, I. Batarseh, M. Salameh, and S. Al-Hallaj, "High voltage battery management system hardware and software design for photovoltaic energy systems," in *Proc. IEEE 7th Southern Power Electron. Conf. (SPEC)*, Nadi, Fiji, Dec. 2022, pp. 1–5, doi: 10.1109/SPEC55080.2022.10058391.

[18] I. C. Guran, L. A. Perişoară, A. Florescu, and D. I. Sacaleanu, "4-cell passive battery management system for automotive applications," in *Proc. IEEE 27th Int. Symp. Design Technol. Electron. Packag. (SIITME)*, Timisoara, Romania, Oct. 2021, pp. 338–341, doi: 10.1109/SIITME53254.2021.9663604.

[19] I. C. Guran, L. A. Perişoară, and A. Florescu, "SPICE model implementation for $LiFePO_4$ cell," in *Proc. Int. Symp. Fundam. Electr. Eng. (ISFEE)*, Bucharest, Romania, Nov. 2020, pp. 1–4, doi: 10.1109/ISFEE51261.2020.9756177.

[20] "±200 V common-mode voltage difference amplifier," Datasheet INA148.

[21] INA148. *±200V Common-Mode Voltage Difference Amplifier*. Accessed: May 4, 2023. [Online]. Available: https://www.ti.com/product/INA148?keyMatch=INA148&tisearch=search-everything&usecase=GPN-ALT#design-development

[22] "TMCS1107-Q1 AEC-Q100, 3% basic isolation Hall-effect current sensor with ±420-V working voltage, SBOSA71," Datasheet TMCS1107-Q1, Jul. 2021.

[23] "Single-channel low-side gate driver IC with 4 A source/8 A sink output stage," Datasheet EiceDRIVERTM 1EDN751x/1EDN851x, Rev. 2.3, 21, Jan. 2022.

[24] B. Yang, J. Wang, S. Xu, J. Korec, and Z. J. Shen, "Advanced low-voltage power MOSFET technology for power supply in package applications," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4202–4215, Sep. 2013, doi: 10.1109/TPEL.2012.2230407.

[25] "CSD16570Q5B 25-V N-channel NexFETTM power MOSFET, SLPS496A," Datasheet CSD16570Q5B, Jul. 2014, May 2017.

[26] *1EDN7511B, Rugged, Cool and Fast, 1-Channel Low-Side A/8A Gate Driver ICs*. Accessed: May 5, 2023. [Online]. Available: https://www.infineon.com/cms/en/product/power/gate-driver-ics/1edn7511b/?tab=~%27simulation_models#!designsupport

[27] *CSD16570Q5B, 25-V, N Channel NexFET Power MOSFET Single SON 5 mm x 6 mm, 0.82 mOhm*. Accessed: May 5, 2023. [Online]. Available: https://www.ti.com/product/CSD16570Q5B#design-tools-simulation

[28] "2.2 MHz wide VIN synchronous boost controller with VOUT tracking, SLVSGN5," Datasheet LM515231-Q1, LM51231-Q1, Oct. 2022.

[29] W. Lu, J. Han, S. Li, and H. H. Iu, "Mitigating line frequency instability of boost PFC converter under proportional outer-voltage loop with additional third current-harmonic feedforward compensation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 11, pp. 4528–4541, Nov. 2019, doi: 10.1109/TCSI.2019.2925663.

[30] A. E. Aroudi, K. Mandal, M. S. Al-Numay, D. Giaouris, and S. Banerjee, "Piecewise quadratic slope compensation technique for DC–DC switching converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 12, pp. 5574–5585, Dec. 2020, doi: 10.1109/TCSI.2020.2993793.

[31] L. Schmitz, D. C. Martins, and R. F. Coelho, "Generalized high step-up DC–DC boost-based converter with gain cell," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 2, pp. 480–493, Feb. 2017, doi: 10.1109/TCSI.2016.2603782.

[32] L. Cong, J. Liu, and H. Lee, "A high-efficiency low-profile zero-voltage transition synchronous non-inverting buck-boost converter with auxiliary-component sharing," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 1, pp. 438–449, Jan. 2019, doi: 10.1109/TCSI.2018.2858544.

[33] B. Hauke, "Basic calculation of a boost converter's power stage," Texas Instrum., Dallas, TX, USA, SLVA372D, November 2022.

[34] "Low-dropout regulator, SBVS377," Datasheet TPS7B88-Q1, TPS7B88-Q1 500-mA,40-V, Jan. 2021.

[35] *2.2-MHz Wide-VIN, Synchronous Boost Controller With Output Voltage Tracking*. Accessed: May 7, 2023. [Online]. Available: https://www.ti.com/product/LM51231-Q1#design-tools-simulation

[36] *TPS7B88-Q1, Automotive 500-mA, 40-V, Low-Dropout (LDO) Linear Regulator With Fast Transient Response*. Accessed: May 7, 2023. [Online]. Available: https://www.ti.com/product/TPS7B88-Q1#design-tools-simulation

[37] I.-C. Guran, A. Florescu, L.-A. Perisoara, A. Vasile, and C.-D. Oancea, "Fully analog clock signal generator for SPICE based simulators," in *Proc. 14th Int. Conf. Electron., Comput. Artif. Intell. (ECAI)*, Ploiesti, Romania, Jun. 2022, pp. 1–4, doi: 10.1109/ECAI54874.2022.9847455.

[38] I.-C. Guran, A. Florescu, L. A. Perişoară, M. Ş. Teodorescu, I. B. Bacîş, and A. Vasile, "Advanced down-counting operation in SPICE," in *Proc. 13th Int. Symp. Adv. Topics Electr. Eng. (ATEE)*, Bucharest, Romania, Mar. 2023, pp. 1–4, doi: 10.1109/ATEE58038.2023.10108172.

[39] I.-C. Guran, A. Florescu, L.-A. Perisoara, M. S. Teodorescu, and I. B. Bacîş, "SPICE implementation of digital counters for battery management systems used in energy storage systems," in *Proc. 14th Int. Conf. Electron., Comput. Artif. Intell. (ECAI)*, Ploiesti, Romania, Jun. 2022, pp. 1–4, doi: 10.1109/ECAI54874.2022.9847485.

IONUŢ-CONSTANTIN GURAN received the B.S. degree in applied electronics and the M.S. degree in advanced microelectronics from the Faculty of Electronics, Telecommunications, and Information Technology, University Politehnica of Bucharest, Romania, in 2017 and 2019, respectively, where he is currently pursuing the Ph.D. degree in advanced battery management for electric vehicles. His research interests include the SPICE modeling domain, advanced battery management, and power electronics.

ADRIANA FLORESCU (Senior Member, IEEE) received the B.S. and Ph.D. degrees in electronics from the University Politehnica of Bucharest, Romania, in 1988 and 2001, respectively. She joined as an Assistant Professor with the Department of Applied Electronics and Information Engineering, Faculty of Electronics, Telecommunications and Information Technology, University Politehnica of Bucharest, in 1993, where she was a Lecturer, in 2000, an Associate Professor, in 2003, a Professor, in 2015, and has been a Ph.D. Coordinator, since 2016. Her current research interests include power converters, computer-aided design, renewable energy systems, and artificial intelligence.

She has been a member of the IEEE Power Electronics Society, since 1995, and the IEEE Romania Section Executive Committee, since 2014.

LUCIAN ANDREI PERIȘOARĂ received the Ph.D. degree in electronics and telecommunications, University Politehnica of Bucharest, in 2012. He is currently an Associate Professor with the Faculty of Electronics, Telecommunications and Information Technology, University Politehnica of Bucharest, Romania. His current research interests include information theory and coding, wireless communications, wireless sensor networks, embedded systems, and automotive electronics.