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RESEARCH ARTICLE

Novel MMC Sub-Module Topology With DC Fault Clearing Capability

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ABSTRACT The traditional half bridge sub-module (HBSM) cannot clear the DC side fault by itself. On the other hand, the clamp double sub-module (CDSM) has the ability to self-clear the fault current, but it can only output the negative level of the single capacitive voltage during reverse locking, which will affect the speed of fault removal. To address this issue, a three-level bidirectional switch sub-module (TLBSSM) based on the bidirectional switch and CDSM is proposed in this paper. The sub-module can output 3 levels when working normally and twice the negative level of the capacitive voltage when reverse locking, which greatly accelerates the fault current removal. In addition, compared with other common sub-module, TLBSSM has certain economic advantages and stronger DC fault clearing capability. Simulation results based on MATLAB/Simulink show that TLBSSM can quickly remove DC faults, and the sub-module capacitance voltage is stably near the rated voltage after the fault, which is conducive to the rapid restart of MMC. Finally, the effectiveness of TLBSSM and its DC fault clearing capability are validated by the experiment results.

INDEX TERMS Flexible DC transmission, modular multilevel converter (MMC), sub-module topology, DC fault clearance, blocking capability.

I. INTRODUCTION

Flexible DC transmission technology has developed rapidly driven by the current world energy landscape. Compared with traditional DC transmission, flexible DC transmission has many advantages, including flexible control, low output harmonic content of the AC and DC sides, absence of commutation failure issues, dynamic reactive power support for the AC side, and the ability to supply power to passive networks [1], [2], [3]. As one of the research directions of flexible DC transmission, the modular multilevel converter (MMC) has become the future development trend because of its high transmission efficiency, high modularity and scalability [4].

At present, MMC based on the traditional half-bridge sub-module (HBSM) are mostly used in flexible DC transmission engineering. Owing to the influence of the HBSM topology, the half-bridge MMC does not have the capability to clear the DC fault [5], which seriously limits the development of MMC-HVDC. Therefore, how to quickly clear DC faults has become one of the research hotspots in the field of MMC-HVDC. There are two methods commonly used in engineering to remove DC faults, the first one is to isolate the fault using DC circuit breakers, and the second one is to use a sub-module with DC fault clearing capability in the MMC to cut off the fault current [6].

DC side fault current characteristics are different from the AC side fault current, so the DC circuit breaker interrupting principle needs to be studied additionally. Furthermore, the development of fault currents in the DC network is much faster than in the AC network, which requires high breaking speed of DC circuit breakers. Therefore, the research cost and cost of DC circuit breakers are high and cannot be used as widely as AC circuit breakers, which have greater limitations [7], [8], [9]. Currently, there are few research results on high-voltage and high-power DC circuit breakers, and the engineering application is still immature. In 2016, China's Zhoushan Soft Straight Project officially put into use the world's first DC circuit breaker, realizing the world's

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first commercial application of HVDC circuit breakers [10], filling the gaps at home and abroad in this field and providing reference for the future engineering applications of DC circuit breakers.

Using the sub-module's own topology for DC fault clearance is another more efficient and feasible method, which is also a hot research topic in the field of MMC DC fault clearance in the future. R. Marquardt, the founder of the half-bridge sub-module, first proposed the clamp double sub-module (CDSM) and the full bridge sub-module (FBSM) with DC fault current blocking capability. These two sub-modules have different working states and output characteristics, and both have certain DC fault clearing capabilities [11], [12], which provides a theoretical basis for the subsequent research of other sub-modules. The literature [13] introduced a diode clamp bidirectional switch sub-module (DCBSSM) that presents a bidirectional switch configuration capable of blocking fault current when latching and utilizing a clamp diode to establish a pathway for the fault current. However, this sub-module requires more power devices to output the unit level and has fewer types of output levels. In literature [14], two HBSMs are connected in series, and an IGBT and clamp diode are connected in the middle, the capacitor of the sub-module is introduced into the bridge arm to block the fault current. The sub-module proposed in the literature has certain economic advantages and application value. In the pursuit of achieving higher-level numbers, literature [15] developed a novel four-capacitor half-bridge sub-module (FCC-HBSM) based on HBSM. Compared to traditional MMC sub-modules, the FCC-HBSM is capable of producing multiple levels and offers greater control flexibility while reducing operating losses and the footprint area of the converter station. However, the sub-module requires higher voltage withstand for certain devices. A new T-shaped half-bridge sub-module (T^2 HBSM) based on HBSM was designed in the literature [16], which saves one diode compared to CDSM, is more economical, and can restart faster after fault removal. In addition, scholars at home and abroad have also studied hybrid MMC, which combines the sub-module with DC fault removal capability and the traditional half-bridge sub-module to access the bridge arm in a certain proportion, so as to further reduce the investment cost of MMC while ensuring that the converter station can clear DC faults by itself. Literature [17], [18], [19] respectively proposed hybrid MMC with different topologies and control strategies. Theoretical analysis and simulation results show that all the proposed schemes can effectively block DC fault current, which has certain guiding significance for practical engineering.

Based on CDSM, a new three-level bidirectional switch sub-module (TLBSSM) that utilizes a bidirectional switch is proposed in this paper, which can address the limitations of CDSM. Firstly, section II introduces the topology structure and working state of TLBSSM. Secondly, the mechanism of DC fault current blocking of TLBSSM is analyzed in section III. Thirdly, in section IV, its fault current blocking ability and device cost are compared with common sub-modules. Then the validity of the proposed sub-module is verified by MATLAB/Simulink platform simulation in section V and experiments in section VI. Finally, section VII summarizes whole this paper and gives the conclusions.

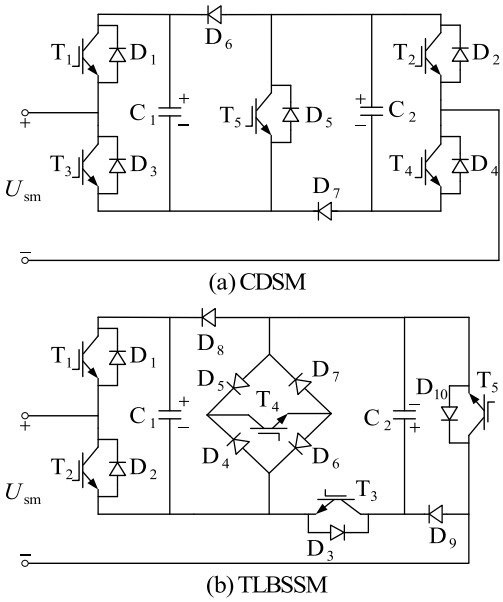


FIGURE 1. Topology of CDSM and TLBSSM.

II. TLBSSM TOPOLOGY AND ITS WORKING STATUS

A. TLBSSM TOPOLOGY

The CDSM topology is shown in Figure 1(a). In normal operation, the IGBT (T_5) is always on, and two diodes (D_6, D_7) are reversed off, the two sub-module capacitors of CDSM can be operated independently or in series. Compared with HBSM, the control of CDSM is more flexible and it can output three levels. All IGBTs should be blocked immediately when the DC faults occur. When CDSM flows through forward fault current, the output voltage of the sub-module is $2U_c$, while when CDSM flows through reverse fault current, the output voltage is $-U_c$, which will affect the removal rate of the reverse fault current.

Figure 1(b) shows the new three-level bidirectional switch sub-module (TLBSSM) proposed in this paper, the bridge bidirectional switch is composed of the diodes (D_4, D_5, D_6, D_7) and an IGBT (T_4). The bidirectional switch can flow through the bidirectional current when T_4 is on, and can block the bidirectional current when T_4 is off. The diode (D_7) in the CDSM is replaced by the diode (D_3), which is connected in reverse parallel to the IGBT (T_3). The purpose of this configuration is to regulate the charging and discharging of capacitor (C_2). TLBSSM inversely connects the capacitor (C_2) and replaces the IGBT (T_2, T_4) with a structure consisting of (D_9, D_{10}, T_5), this structure can introduce the capacitors (C_1, C_2) into the arm without affecting the forward fault current. Therefore, TLBSSM can output two units of negative level when the direction of the arm current is in the negative direction, which accelerates the cutting speed

of fault current and simplifies the balanced control of two capacitor voltages in the sub-module.

B. WORKING STATUS OF TLBSSM

There are two operating states of TLBSSM, normal operating state and blocking state.

In normal operating state, the control strategy of TLBSSM is consistent with that of CDSM, the IGBT (T_5) remains on and the diodes (D_8, D_9) are in reverse cutoff state. Regardless of redundant operation, TLBSSM has four operating states in normal operation and can output three levels, namely, $U_{c1}+U_{c2}$, $U_{c1}(U_{c2})$ and 0, the corresponding current path is shown in Figure 2 and the relationship between the output voltage and the on-state of the power switch can be expressed as

$$U_{sm} = S_{T1}U_{c1} + S_{T3}U_{c2} \tag{1}$$

where S_{T1} and S_{T3} are the trigger signals of the power switch T_1 and T_3 respectively, 1 is taken when the switch is on, 0 is taken when the switch is off, U_{c1} and U_{c2} are the capacitor voltages of the sub-module.

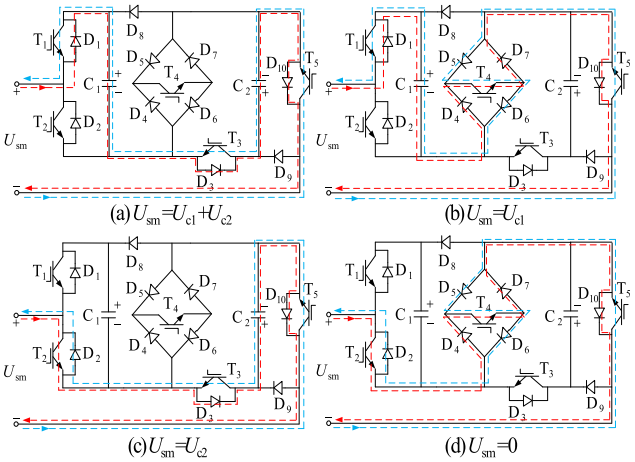


FIGURE 2. Current path of TLBSSM during normal states.

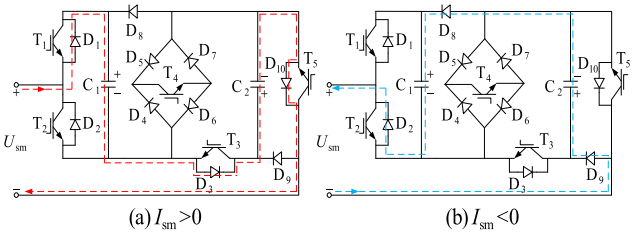


FIGURE 3. Fault current path of TLBSSM after blocking.

After blocking, the fault current path of TLBSSM can be divided into two cases. When the current of the sub-module $I_{sm}>0$, the forward fault current passes through the diodes (D_1, D_3, D_{10}) and the capacitors (C_1, C_2), at this time, the output voltage (U_{sm}) is equal to $2U_c$, the current path is shown in Figure 3(a). When $I_{sm}<0$, the reverse fault current passes through the diode (D_9, D_8, D_2) and the capacitors (C_1, C_2), the output voltage (U_{sm}) is equal to $-2U_c$ and the current path is shown in Figure 3(b). Therefore, the working state of TLBSSM can be summarized as Table 1.

TABLE 1. Switching states of TLBSSM.

Working state	T_1	T_2	T_3	T_4	T_5	I_{sm}	U_{sm}
Normal Operation	1	0	1	0	1	~	$U_{c1}+U_{c2}$
	1	0	0	1	1	~	U_{c1}
	0	1	1	0	1	~	U_{c2}
	0	1	0	1	1	~	0
Fault blocking	0	0	0	0	0	>0	$U_{c1}+U_{c2}$
	0	0	0	0	0	<0	$-(U_{c1}+U_{c2})$

According to Table 1, during the normal operation of TLBSSM, the switch transistor T_5 remain conductive. T_1 and T_2 have opposite switch states and together control the operating states of capacitor C_1. Similarly, T_3 and T_4 also have opposite switch states and jointly control the operating states of capacitor C_2. The TLBSSM can be considered as two HBSMs, where T_1 and T_3 are equivalent to T_1 in the HBSM, while T_2 and T_4 are equivalent to T_2 in the HBSM. Therefore, the control methods and voltage balance control strategy of the HBSM are equally applicable to the TLBSSM.

III. DC-SIDE FAULT CURRENT BLOCKING ANALYSIS

A. FAULT CURRENT BLOCKING THEORY OF TLBSSM

The pole-to-pole short-circuit fault is the most serious fault in DC side, so this paper takes it as an example to study the fault current blocking mechanism of TLBSSM.

Since the fault detection system has a certain delay from detecting the fault to issuing the blocking signal, the clearance of the fault current can be divided into two stages: before blocking and after blocking. Stage 1: before blocking. The DC side pole-to-pole short-circuit fault is equivalent to a three-phase short-circuit fault for the AC-side, and the sum of the three-phase currents flowing into the short-circuit point is zero, so the fault current at this stage mainly comes from the discharge of the sub-module capacitors.

It is assumed that the MMC has $2N$ TLBSSMs per phase unit, with N in each of the upper and lower bridge arms. The number of sub-module capacitors in operation and bypassed at any moment are both $2N$, and the upper and lower bridge arm sub-module capacitors can be considered in parallel. Therefore, the MMC three-phase sub-module capacitor discharge loop can be equated to the RLC second-order discharge loop shown in Figure 4 [20]. Where R_0 and L_0 are the resistance and inductance of the bridge arm respectively; C is the capacitance of the sub-module; R_{dc} and L_{dc} are the resistance and inductance of the DC line respectively.

According to Kirchhoff's voltage law, the differential equation and initial conditions of this circuit can be listed as

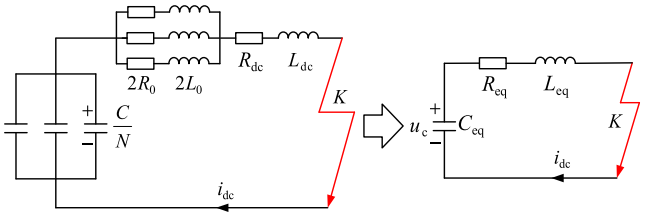


FIGURE 4. RLC equivalent circuit of capacitor discharge stage.

the formula (2)

$$\begin{cases} L_{eq}C_{eq}\dfrac{d^2u_c(t)}{dt^2} + R_{eq}C_{eq}\dfrac{du_c(t)}{dt} + u_c(t) = 0 \\ u_c(0_+) = u_c(0_-) = 2NU_c \\ i_{dc}(0_+) = i_{dc}(0_-) = I_{dc} \end{cases} \tag{2}$$

$$\begin{cases} C_{eq} = \dfrac{3C}{N} \\ R_{eq} = \dfrac{2}{3}R_0 + R_{dc} \\ L_{eq} = \dfrac{2}{3}L_0 + L_{dc} \end{cases} \tag{3}$$

where C_{eq}, R_{eq} and L_{eq} are the equivalent capacitance, resistance and inductance of the RLC discharge circuit respectively, which can be calculated by the formula (3). $u_c(t)$ is the voltage of C_{eq} and I_{dc} is the steady-state current of the DC side. Combining formula (2) and (3), the voltage across the equivalent capacitor and the DC side current can be expressed as the formula (4).

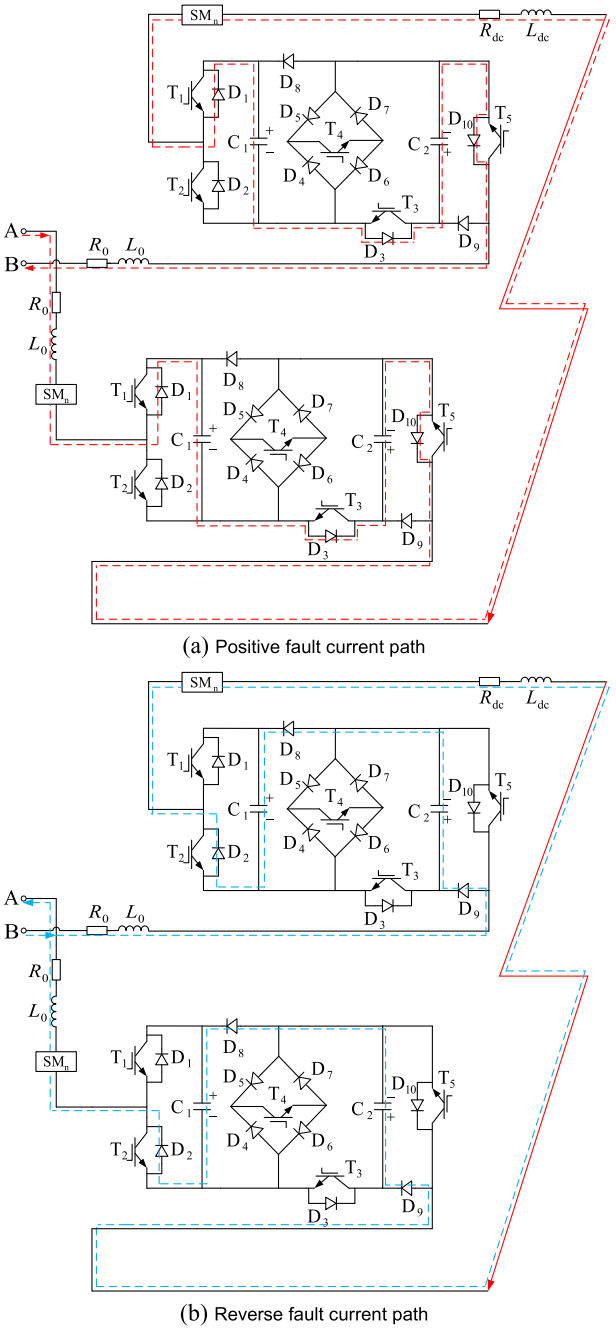
$$\begin{cases} u_c(t) = e^{-\frac{t}{\tau}}[\dfrac{U_{dc}\omega_0}{\omega}\sin(\omega t + \alpha) - \dfrac{I_{dc}}{\omega C_{eq}}\sin(\omega t)] \\ i_{dc}(t) = e^{-\frac{t}{\tau}}[I_{peak}\sin(\omega t + \beta)] \end{cases} \tag{4}$$

where τ is the discharge time constant of RLC. ω_0 is the resonant angular frequency and ω is the angular frequency of oscillation. α is the initial phase angle. The above parameters can be calculated by equation (5).

$$\begin{cases} \tau = \dfrac{2L_{eq}}{R_{eq}}, \omega_0 = \sqrt{\dfrac{1}{L_{eq}C_{eq}}}, \omega = \sqrt{\omega_0^2 - \tau^2} \\ I_{peak} = \sqrt{4\dfrac{C_{eq}}{L_{eq}}N^2U_c^2 + I_{dc}^2} \\ \beta = \arctan(\dfrac{I_{dc}}{2NU_c}\sqrt{\dfrac{L_{eq}}{C_{eq}}}) \end{cases} \tag{5}$$

From Formula (4), it can be seen that the fault current undergoes oscillation attenuation before the sub-module is blocked. The oscillation period and current change rate are influenced by the inductance of the bridge arm, capacitance of the sub-module, and inductance of the line.

Stage 2: after blocking. The energy in the AC side and the inductance of the bridge arm is fed into the short circuit point through the continuous current diode. At this time, the fault current will form a loop with the sub-module capacitor through the freewheeling diode and charge the sub-module capacitor until the freewheeling diode is turned off under the reverse voltage, then the fault current will be blocked. This paper takes AB phase fault current path as an example to analyze the clearing mechanism of sub-module fault current, and Figure 5 shows the fault current path of MMC after blocking. When the current of sub-module $I_{sm} > 0$, the MMC forward fault current path is shown in Figure 5(a). When $I_{sm} < 0$, the MMC reverse fault current path is shown in Figure 5(b).



(a) Positive fault current path

(b) Reverse fault current path

FIGURE 5. Fault current path of MMC after blocking.

Due to the fault current only flows through the diodes and capacitors when the sub-module is blocked, Figure 5 can be

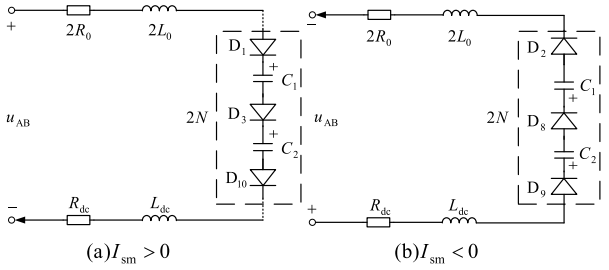


FIGURE 6. Simplified fault current circuit of MMC.

further simplified to obtain the simplified fault current circuit of MMC as shown in Figure 6.

As shown in Figure 6(a), when the fault current of the sub-module is positive, the current passes through several components in the circuit. These components include the resistance and inductance of the bridge arm, $2N$ sub-modules, and the resistance and inductance of the DC line. So the AB phase short-circuit current flows through $6N$ diodes and $4N$ sub-module capacitors. According to the KVL law, voltages of the circuit can be obtained as

$$u_{\mathrm{AB}} = 2(u_{R_0} + u_{L_0}) + 6Nu_{\mathrm{d}} + 4Nu_{\mathrm{c}} + u_{R_{\mathrm{dc}}} + u_{L_{\mathrm{dc}}} \tag{6}$$

where u_{AB} is the AB phase to phase voltage of AC side. u_{R_0} and u_{L_0} are the resistance and inductance voltage of the bridge arm respectively. u_{d} is the voltage of a single diode. u_{c} is the sub-module capacitor voltage, it is assumed that it is constant and equal to the rated voltage during this period because the blocking time is very short. $u_{R_{\mathrm{dc}}}$ and $u_{L_{\mathrm{dc}}}$ are the voltage shared by the resistance and inductor on the DC line, respectively.

When the MMC is in normal operation, the AC side voltage, DC side voltage and sub-module capacitor voltage meet the following relation

$$\begin{cases} U_{\mathrm{dc}} = 2NU_{\mathrm{c}} = 2Nu_{\mathrm{c}} \\ u_{\mathrm{p}} = \dfrac{1}{2} m U_{\mathrm{dc}} \\ u_{\mathrm{L}} = \sqrt{3}\, u_{\mathrm{p}} \end{cases} \tag{7}$$

where U_{dc} is the DC side voltage and it is assumed that U_{dc} remain unchanged at the blocking moment. m is the modulation degree. u_{L} and u_{p} are the line voltage and phase voltage of AC side, respectively.

By connecting the formula (6) and (7), the voltage at both ends of a single diode is

$$u_{\mathrm{d}} = \frac{\left(\frac{\sqrt{3}}{2} m - 2\right) U_{\mathrm{dc}} - \left(2\left(u_{R_0} + u_{L_0}\right) + u_{R_{\mathrm{dc}}} + u_{L_{\mathrm{dc}}}\right)}{6N} \tag{8}$$

Generally, for the modulation degree $0 < m \leq 1$, it can be observed from Formula (8) that the voltage on both sides of the diode (u_{d}) is less than zero. Therefore, the diode is subjected to reverse voltage when the sub-module is blocked, preventing the fault current from flowing.

Similarly, when the fault current flows into the sub-module from the opposite direction, as shown in Figure 6(b), the reverse fault current path is symmetrical to the forward fault current path. Therefore, $u_{\mathrm{d}} < 0$ is also true, and the reverse fault current cannot flow either.

Based on the above study, it is known that when the TLBSSM is blocked, the sub-module freewheeling diodes are subjected to reverse voltage, and both forward and reverse fault currents cannot flow continuously, so it can be concluded that the TLBSSM has DC fault clearing capability.

In addition, by observing the MMC fault current path, it can be seen that as long as the total reverse clamping voltage provided by the capacitors is greater than the AC side line voltage after TLBSSM is blocked, the freewheeling diodes will be turned off by the reverse voltage, and the fault current can be effectively blocked, it can be expressed as

$$4N_{\mathrm{sm}}u_{\mathrm{c}} > u_{\mathrm{L}} \tag{9}$$

where N_{sm} is the number of TLBSSMs required for each bridge arm. Combined with the formula (7), it can be obtained that

$$N_{\mathrm{sm}} > \frac{\sqrt{3}\, mN}{4} \tag{10}$$

To preserve certain design fault tolerance and N_{sm} must be an integer, N_{sm} can be calculated by the formula (11).

$$N_{\mathrm{sm}} = \left\lceil \frac{\sqrt{3}\, mN}{4} \right\rceil \tag{11}$$

where $\lceil x \rceil$ is the symbol of ceiling function, based on the equation (11), it is evident that the MMC composed solely of TLBSSMs possesses an excessive fault current blocking capability. To further reduce the construction costs of the converter station while ensuring fault blocking capability, a hybrid MMC can be formed by combining TLBSSMs with HBSMs. Taking a 9-level TLBSSM-MMC as an example, only 2 TLBSSMs per bridge arm are required to achieve DC fault clearing capability, while the remaining sub-modules can be replaced with equivalent HBSMs to save investment cost for the MMC.

B. DC-SIDE FAULT HANDLING PROCESS

The fault handling process flowchart of TLBSSM-MMC is illustrated in the Figure 7.

During normal operation, the fault detection system continuously monitors the DC side current. In the event that the DC side current exceeds the specified limit, the fault detection system promptly issues a blocking signal to all IGBTs, effectively blocking all sub-modules. Subsequently, with the assistance of TLBSSM, the fault current rapidly decays to zero. T represents the number of times the DC side current exceeds the limit, if T is less than the preset threshold value T_{set}, the control system will issue a trigger signal to all IGBTs, attempting to restart the TLBSSM-MMC. If the DC current does not exceed the limit at this time, the fault is a transient fault, and the entire MMC system will return to the normal working state. Otherwise, the fault detection system will send a blocking signal again, and the fault current

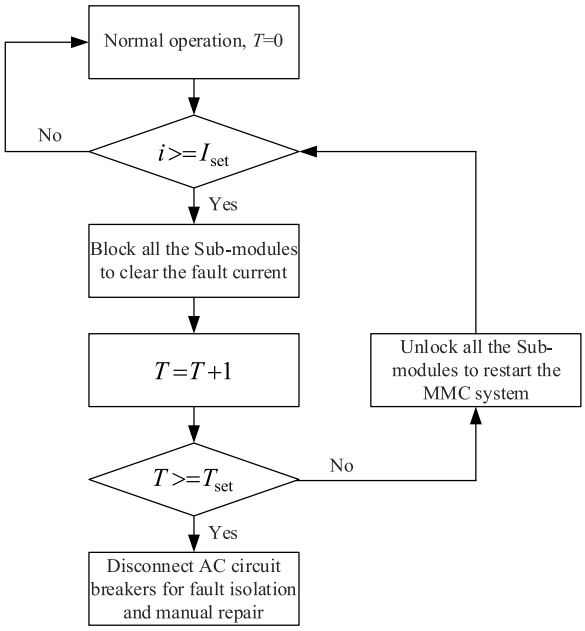


FIGURE 7. Flow chart of fault clearing process.

clearing process will be repeated. Each time the fault current exceeds the limit, the value of T increases by 1. After multiple cycles, if T reaches or exceeds the preset threshold value T_{set}, it indicates that the fault is the permanent fault. In such cases, it is necessary to disconnect the AC side circuit breaker for fault isolation and manual repair.

IV. STUDY ON THE CHARACTERISTICS OF TLBSSM

In this section, the relevant characteristics of TLBSSM will be investigated from four aspects: DC fault blocking capability, sub-module device withstand voltage, sub-module investment cost, and sub-module operating loss.

A. ANALYSIS OF BLOCKING CAPABILITY

The sub-module critical capacitance voltage (U_{ct}) is defined to measure the fault current blocking capability of different sub-modules, which represents the minimum capacitance voltage required for the sub-module to completely block the fault current after a DC fault occurs in the MMC and the sub-module is blocked.

$$u_d = \frac{\left(\sqrt{3}\, mNU_c - 4NU_c\right) - U_Z}{6N} \tag{12}$$

Formula (8) is written in the form shown in Formula (12), where U_Z is the voltage shared by the DC line and the bridge arm when a fault occurs, and when the fault is cleared, this part of voltage is zero. Therefore, the voltage at both ends of the diode is only determined by the left part of the molecule in equation (12). It is easy to know that when $\sqrt{3}\, mNU_c$ is less than $4NU_c$, the diode is turned off by reverse voltage, it can be obtained as

$$U_c > \frac{\sqrt{3}\, mU_c}{4} \tag{13}$$

In order to completely block the fault current, the capacitor voltage of the sub-module must satisfy the inequality shown in equation (13). The right side of the inequality is defined as the critical capacitor voltage of the sub-module, U_{ct} can be expressed as

$$U_{ct} = \frac{\sqrt{3}\, mU_c}{4} \tag{14}$$

Based on this definition, the critical capacitance voltage of some sub-modules can be obtained as (15)

$$\begin{cases} FBSM : U_{ct} = \dfrac{\sqrt{3}\, mU_c}{4} \\ \text{CDSM} : U_{ct} = \dfrac{\sqrt{3}\, mU_c}{2} \\ DCBSSM : U_{ct} = \dfrac{\sqrt{3}\, mU_c}{4} \\ TLBSSM : U_{ct} = \dfrac{\sqrt{3}\, mU_c}{4} \end{cases} \tag{15}$$

where, the critical capacitor voltage of CDSM is twice that of FBSM, because when CDSM is in forward lock, the capacitors of the sub-module are connected to the fault loop in series and the output voltage is $2U_c$, while when CDSM is reversely locked, the capacitors are connected to the fault loop in parallel and the output voltage is $-U_c$. The asymmetry of CDSM's forward and reverse locking output voltage affects the cutting speed of the fault current and limits the critical capacitance voltage of CDSM. According to the definition of the critical capacitor voltage, in order to possess the fault current blocking capability at the same voltage modulation ratio, the CDSM's capacitor voltage must be maintained above $0.866U_c$, while the TLBSSM's capacitor voltage only needs to be maintained above $0.433U_c$. Therefore, the TLBSSM has a stronger blocking capability because the sub-module capacitance voltage required to cut off the DC fault current is lower. Theoretically, TLBSSM has the same strong DC fault blocking capability as FBSM.

B. ANALYSIS OF DEVICE WITHSTAND VOLTAGE

When the MMC works normally or blocks, it is assumed that the capacitor voltage difference of each sub-module is small and its rated voltage is U_c. Suppose the conduction voltage drop is ΔU_D for single diode, and the conduction voltage drop for single IGBT is ΔU_T.

When the sub-module is working normally, it can be seen from Figure 2 that the IGBT T_5 is always in the on-state and its voltage is ΔU_T. When the current path of the sub-module is shown in Figure 2(a) and 2(c), the diode D_8 is connected between the sub-module capacitor (C_1, C_2) and the diode D_3. At this time, it will bear the sum of twice the capacitor voltage $2U_c$ and the conduction voltage drop of a single diode ΔU_D, which is the maximum reverse voltage borne by the diode D_8. While the diode D_9 will bear the sum of the U_c and ΔU_D regardless of the on-off state of the power switch.

As for the T_1, T_2, T_3 and the paralleled diodes D_1, D_2, D_3, it is known that the trigger signals of the T_1 and T_2 are

opposite and the trigger signals of the T_3 and T_4 are also opposite. When T_1 or T_2 is off, the voltage withstood by (T_1 & D_1) and (T_2 & D_2) is the sum of U_c and ΔU_D or ΔU_T. When T_3 is off, the bidirectional switch is on, it can be seen from Figure 2(b) and (d) that the maximum reverse voltage withstood by the T_3 and D_3 is the sum of U_c and ΔU_D. As for the power devices in the bidirectional switch, due to the symmetry of their operation, it can be inferred that the maximum reverse voltage they can withstand is the sum of the single capacitor voltage (U_c) and a single IGBT conduction voltage drop (ΔU_T).

After the sub-module is blocked, when the fault current is positive, the fault current path is consistent with the positive current in Figure 2(a), so the voltage resistance of the power device is consistent with that in normal operation. When the fault current is negative, as shown in Figure 3(b), the diode D_8 and D_9 are on, at this time, the reverse voltage borne by the T_5 and D_{10} are the sum of U_c and ΔU_D. It should be noted that the T_3 and D_3 are connected to the two sub-module capacitors because the diode D_8 is on. At this time, the voltage withstood by T_3 and D_3 is the sum of twice the sub-module capacitor voltage and the single diode conduction voltage drop.

To sum up, if the conduction voltage drop of the diodes and IGBT are ignored, it can be known that the voltage borne by the T_3, D_3 and D_8 are $2U_c$, the remaining power devices bear the voltage U_c.

C. NALYSIS OF DEVICE COST

In addition to the resistance and inductance of the bridge arms and lines, the converter station is primarily composed of the IGBTs, diodes and capacitors. Since the device cost of the sub-module is evaluated based on the number of power devices needed to output a unit level, and the number of capacitors required to output a unit level is the same for different sub-modules, the capacitor cost index is not taken into account in this paper. Instead, it only takes into account the impact of the number of IGBTs and diodes on the sub-module cost.

Regarding the IGBT (T_3), as mentioned earlier, it needs to withstand double the capacitor voltage during sub-module fault blocking, which requires a higher withstand voltage level. However, in practical engineering, sub-module fault blocking is rare and of extremely short duration. Additionally, the MMC provides a certain safety margin for the working voltage of the sub-module IGBTs. The rated voltage of the sub-module capacitors are set to be no more than half of the selected IGBT's withstand voltage level. Therefore, it is possible to reduce the withstand voltage level for T_3 to the single capacitor voltage. This approach helps to mitigate the withstand voltage requirements for the sub-module power devices and reduces the cost of the sub-modules.

The specific type of IGBT selected in this paper is FZ600R65KE3 kind and its parameter is 6.5 kV/1.2 kA. It is assumed that N_T and N_D are the number of IGBTs and diodes required by sub-module to output a unit level respectively. Equation (16) can be constructed to calculate the cost evaluation factor of each sub-module device.

$$M = pN_T + qN_D \tag{16}$$

where p is the price weight coefficient of IGBT, which is 1 in this paper. q the price weight coefficient of diode and it is 0.2 in this paper. M is the cost evaluation coefficient of sub-module devices.

Compared with HBSM, FBSM, CDSM and hybrid sub-module (HB-FBSM), etc. which are widely used in engineering at present, the device cost index of each sub-module is calculated by using Formula (16), as shown in Table 2.

TABLE 2. Investment cost of common SM.

SM	N_T	N_D	M	Reverse blocking output voltage
HBSM	2	2	2.4	0
FBSM	4	4	4.8	$-U_c$
CDSM	2.5	3.5	3.2	$-U_c$
HB-FBSM	3	3	3.6	$-U_c$
DCBSSM	3	8	4.6	$-U_c$
TLBSSM	2.5	5	3.5	$-2U_c$

Table 2 shows that TLBSSM proposed in this paper has certain economic advantages compared with FBSM, HB-FBSM and DCBSSM. Compared with CDSM, although the cost of TLBSSM is relatively high, the output negative voltage of TLBSSM in reverse locking is twice that of CDSM, and its ability to cut off fault current is stronger than that of CDSM, and the design of the control system is simpler. In practical engineering, appropriate sub-modules should be selected according to the needs of MMC construction.

D. ANALYSIS OF OPERATING LOSS

According to existing research findings, the operating losses of MMC are mainly generated by power devices such as IGBTs and diodes. These losses can be divided into three parts: static-state losses, switching losses, and driver losses.

The driver losses refer to the power losses caused by the IGBT gate driver, because the driver losses are very small compared with the static-state losses and switching losses, so they can be ignored.

The static-state losses mainly include the conducting losses of IGBTs and diodes and the off-state blocking losses when they are turned off. The off-state losses are generated by the tiny leakage current when IGBTs and diodes are turned off, which can be neglected due to their small proportion. Therefore, the static-state losses are mainly composed of conducting losses, and can be calculated by the following formula

$$\begin{cases} P_{\text{Tcon}} = i_{\text{CE}} V_{\text{CE0}} + i_{\text{CE}}^2 r_{\text{CE}} \\ P_{\text{Dcon}} = i_{\text{f}} V_{f0} + i_f^2 r_f \end{cases} \tag{17}$$

where P_{Tcon}, P_{Dcon} are the conducting losses of IGBT and diode respectively; $V_{\text{CE0}}(V_{f0})$ is the voltage offset of an

IGBT(diode); r_{CE}, r_f are the on-state resistance; i_{CE}, i_f represent the current of IGBT and diode, respectively.

As for IGBTs, the switching losses contain the turn-on loss and the turn-off loss. However, for diodes, the turn-on loss is much less than the reverse recovery loss, so only the reverse recovery loss of the diode is considered. The paper [21] provides the calculation formulas and relevant coefficients for the turn-on loss E_{on}, the turn-off loss E_{off} of IGBTs, and the recovery loss E_{rec} of diodes, as follows

$$\begin{cases} E_{off} = (a_1 + b_1 i_{CE} + c_1 i_{CE}^2)k_1 \\ E_{on} = (a_2 + b_2 i_{CE} + c_2 i_{CE}^2)k_2 \\ E_{rec} = (a_3 + b_3 i_f + c_3 i_f^2)k_3 \end{cases} \tag{18}$$

where a_i, b_i and c_i(i=1, 2, 3) are the fitting coefficients; $k_i(i = 1, 2, 3)$ are the adjustment coefficients.

In order to obtain the operating loss of TLBSSM and compare it with common sub-modules, this paper selected the sub-modules composed of IGBTs and diodes with the same parameters, and let them run under the same working conditions. By using the method in literature [21], simulation was built in MATLAB/Simulink environment to calculate the operating loss as a percentage of total output power of each sub-module. The results are shown in the Table 3.

TABLE 3. Operating loss of sub-modules.

SM	N_T	Conducting loss /%	Switching Loss /%	Operating Loss /%
HBSM	2	1.107	0.182	1.289
FBSM	4	2.613	0.219	2.832
CDSM	2.5	2.036	0.250	2.286
DCBSSM	3	2.768	0.417	3.185
TLBSSM	3	2.213	0.296	2.509

According to the analysis of Table 3, it can be observed that the conducting loss and switching loss of TLBSSM are second only to HBSM and CDSM. The total operating loss of the TLBSSM are also second only to HBSM and CDSM, accounting for 2.509% of the system's output power. In comparison to FBSM and DCBSSM, which also have fault clearing capability, the TLBSSM exhibits higher output efficiency. This higher efficiency can further extend the lifespan of the converter station and reduce its operating and maintenance costs.

V. SIMULATION AND ANALYSIS

A. MODEL ESTABLISHMENT

In order to verify the DC fault current blocking capability of TLBSSM and the voltage resistance characteristics of the device, the 11-level MMC single-ended rectifier system [22] as shown in Figure 8 is built on the MATLAB/Simulink simulation platform. Each bridge arm of the converter is composed of 5 TLBSSMs, and MMC adopts the nearest level approximation modulation mode (NLM). Simulation parameters are shown in Table 4.

In this paper, the most serious DC side pole-to-pole short-circuit fault of MMC is selected for simulation research. The simulation results and analysis conclusions obtained from this model can be extended to TLBSSM-MMC with higher capacity and any level number.

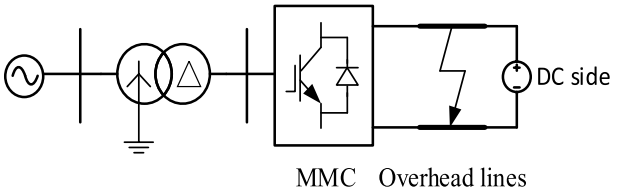


FIGURE 8. Simulation model of single ended MMC.

TABLE 4. Simulation parameters.

Parameters	Value
Rated active power /MW	1.2
Ac side line voltage RMS /kV	12.25
DC voltage /kV	20
Number of bridge arm sub-modules	5
Sub-module capacitance value /mF	3
Capacitor rated voltage /kV	2
Bridge arm inductance /mH	40
Bridge arm resistance /Ω	0.04
Length of transmission line /km	10
Transmission line resistance /(Ω/km)	0.4
Transmission line inductance /(mH/km)	1

B. POLE-TO-POLE SHORT-CIRCUIT FAULT

If a permanent pole-to-pole short-circuit fault occurs at 1.0 s at 5 km from the MMC DC side outlet, the fault detection system issues a blocking signal after 2 ms and all IGBTs are blocked at 1.002 s. Figure 9 shows the TLBSSM-MMC permanent pole-to-pole short circuit fault simulation waveforms.

Among them, Figure 9(a) shows the AC side phase voltage waveform, U_{ac} is a step waveform with 11 levels during normal operation of MMC, which is consistent with the theoretical analysis, and if more TLBSSMs are put into each bridge arm in the actual project, the AC side phase voltage will be approximately sinusoidal. After the fault current is cleared, the converter operates in uncontrolled rectification mode because all sub-modules are blocked. The capacitor voltage sequencing algorithm and the nearest level approximation modulation lose their efficacy, so U_{ac} is not an 11-level step wave, but a non-standard sine wave with harmonics.

Figure 9(b) shows the DC side voltage waveform, and during normal operation, the DC voltage is stable at about 20 kV. After the fault occurs, the bridge arm inductor voltage reverses instantaneously to suppress the rapid increase of the bridge arm current, so U_{dc} drops rapidly at 1.0 s, and then rises due to the gradual reduction of the bridge arm inductor voltage. At 1.002 s, the sub-module is blocked, and the capacitors are connected to the fault circuit. The short-circuit

current decreases rapidly. As a result, the voltage across the bridge arm inductor reverses again. The instantaneous DC voltage drops below 0 V when the sub-module is blocked and reaches 0 V once the energy from the bridge arm inductor is fully released.

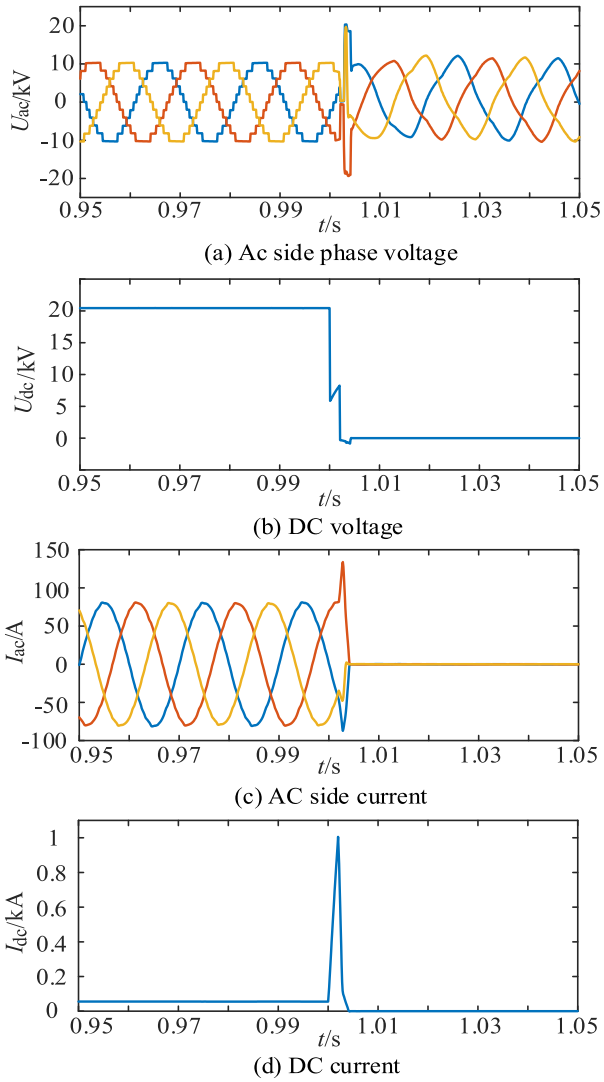


FIGURE 9. Simulation waveform diagrams of the permanent pole to pole fault.

Figure 9(c) and 9(d) show the AC and DC side current waveforms respectively, which are in steady state during normal operation, and the DC current remains stable at approximately 55 A. The AC side current and DC current increase rapidly after the fault occurs at 1.0 s, and the maximum DC current increases to 18.2 times of that in the normal operation. In 1.002 s, all IGBTs enter the blocked state. The freewheeling diodes are turned off under reverse voltage, blocking both the AC and DC currents quickly. The whole fault clearing process takes about 4 ms, which verifies that the sub-module discussed in this paper has the capability to rapidly interrupt the fault current.

The balanced waveform of the capacitor voltage of the lower bridge arm of phase A is shown in Figure 10(a). Before the occurrence of the fault, the ten capacitor voltages of the lower bridge arm of phase A are maintained at about 2.04 kV, with fluctuations of about ±0.8%. After 1.0 s, when the fault occurs, the sub-module capacitor discharges rapidly and the capacitor voltage drops to a minimum of 1.96 kV. After 2 ms, the sub-modules are blocked, and the bridge arm inductor starts to recharge the capacitors. As a result, the sub-module capacitor voltage recovers and remains at about 2 kV, which is conducive to the rapid restart of the MMC after the fault is cleared. The current of the sub-module capacitor is shown in Figure 10(b). During normal operation of the MMC, the sub-module capacitors are sequentially switched on or off based on the voltage sorting algorithm. When a sub-module capacitor is switched on to the bridge arm, its current is equal to the bridge arm current. When a sub-module capacitor is bypassed and switched off, its current becomes zero.

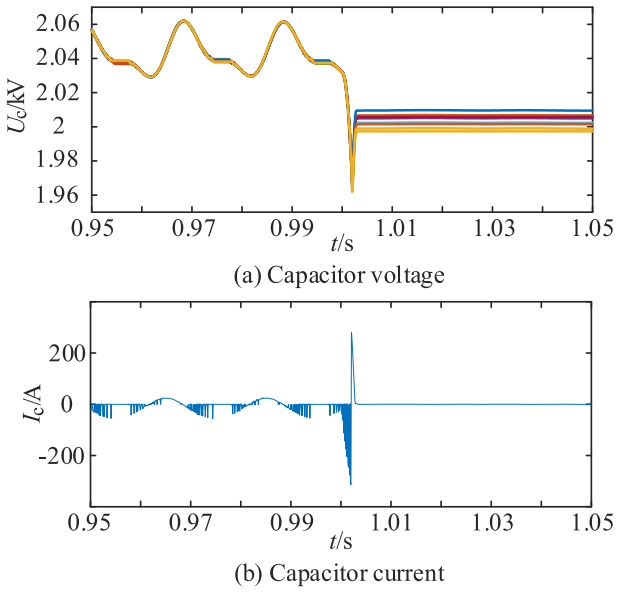


FIGURE 10. Waveform diagrams of capacitor voltage and current of the phase-A lower arm.

If the pole-to-pole short-circuit fault time lasts only 0.05 s for transient faults, the AC-side current and DC voltage fault traversal simulation waveforms can be obtained as shown in Figure 11. As can be seen from the figure, the AC side current is rapidly blocked after the fault occurs, and the fault disappears at 1.05 s. The AC current returns to normal after a brief fluctuation. The DC voltage is restored to about 20 kV about 0.05 s after the fault is cleared, which verifies that the TLBSSM-MMC has a fast self-restarting capability.

C. DEVICE VOLTAGE WITHSTAND

When the pole-to-pole short-circuit fault occurs on the DC side, the voltage withstand simulation waveforms of typical power devices of sub-modules are shown in Figure 12.

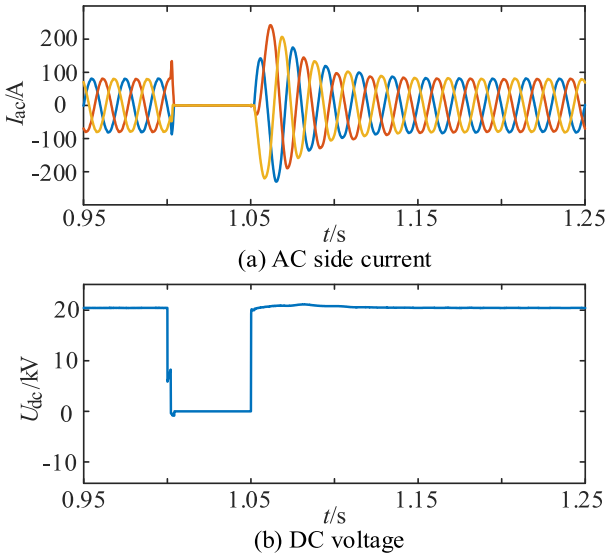


FIGURE 11. Simulation waveform diagrams of the transient pole to pole fault.

As can be seen from the Figure 12, before the fault occurs, the T_1 and T_2 take turns to bear the capacitor voltage U_{c1} while the T_3 and T_4 take turns to bear the capacitor voltage U_{c2}. The IGBT T_5 is always on during the normal operating state, so the voltage across the two ends of it is 0. Under different working states, the diode D_8 bears double capacitor voltage $U_{c1} + U_{c2}$ or single capacitor voltage U_{c1}. At 1.0 s, after the fault occurs, the sub-module capacitor feeds energy into the bridge arm inductor and short circuit point. The sub-module capacitor voltage drops slightly, and the voltage borne by the power switch and diode decreases. 2 ms later, all IGBTs are locked, the sub-module capacitor enters into the charging stage, the voltages of the five IGBTs increase, where the maximum voltage withstand of T_3 in the fault state is $U_{c1} + U_{c2}$, which is twice of that in normal operation, and the maximum voltage withstand of T_5 after blocking is a single capacitor voltage U_{c2}. It can be seen that the voltage withstand simulation results of the device are consistent with the theoretical analysis in both the normal working state and the fault blocking state of the sub-module.

D. BLOCKING CAPABILITY SIMULATION

Under the same system parameters and working conditions, the DC-side fault current blocking simulation results of the TLBSSM, CDSM, FBSM and HB-FBSM are compared in Figure 13. According to the Figure 13, it can be observed that after the sub-modules are blocked, the fault current clearing speed of TLBSSM is similar to FBSM. Both of them are capable of interrupting the fault current at approximately 1.004 s, which indicates that TLBSSM and FBSM have the same fault current blocking capability, this is consistent with the theoretical analysis. CDSM and HB-FBSM exhibit slower fault current blocking speeds compared to TLBSSM. Both completely interrupt the fault current at about 1.009 s, the entire fault current clearing process taking approximately

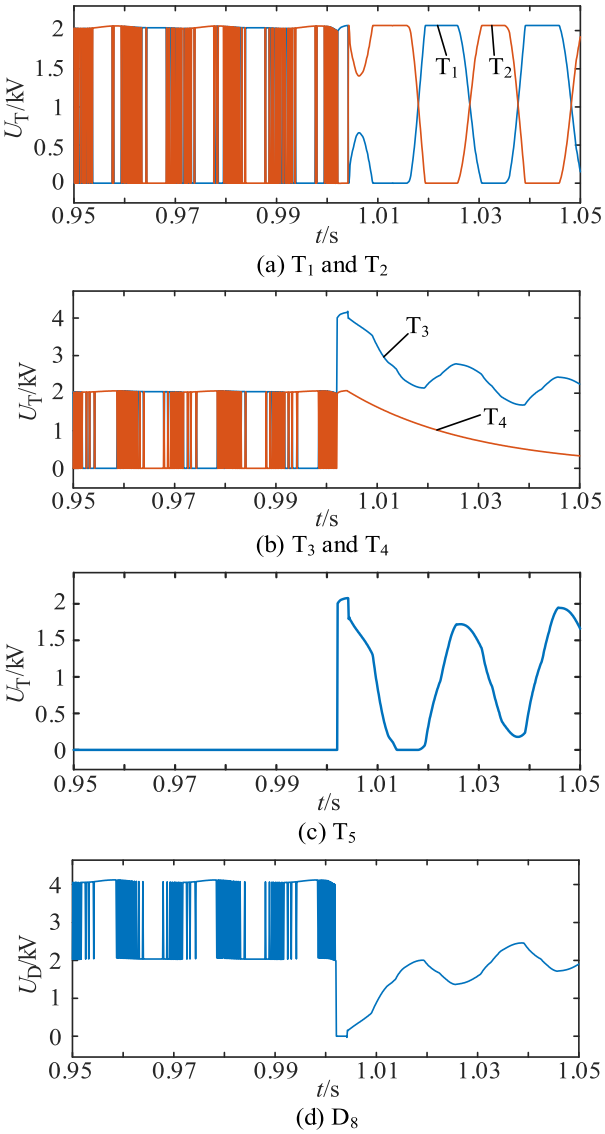


FIGURE 12. Waveform diagrams of device withstand voltage.

9 ms. The simulation results indicate that TLBSSM possesses a stronger fault current interruption capability.

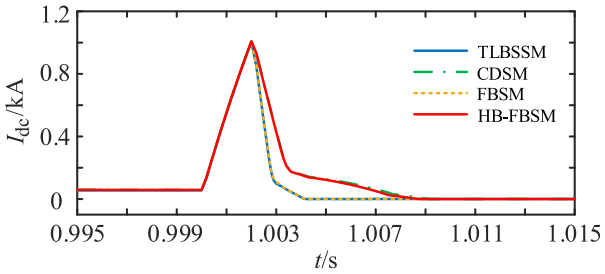


FIGURE 13. Comparison of fault current blocking.

VI. EXPERIMENTS

To validate the effectiveness of TLBSSM in practical engineering, an experimental platform of 11-level low power TLBSSM-MMC was constructed as shown in Figure 14.

FIGURE 14. TLBSSM-MMC experimental platform.

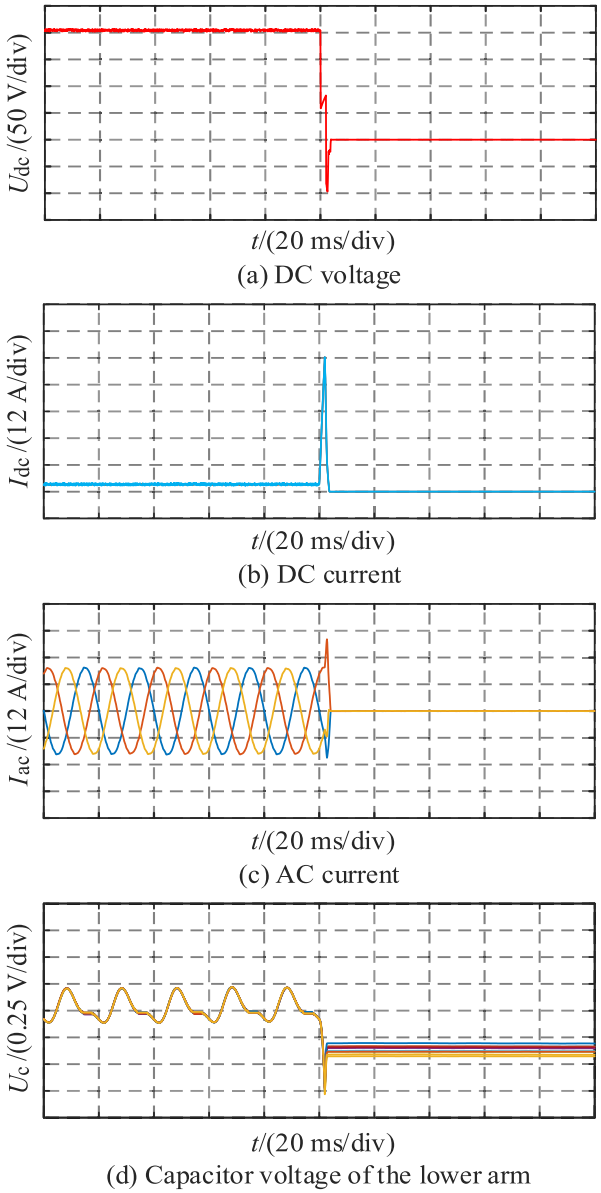


FIGURE 15. Experiment results.

Considering the limited experimental conditions, some experimental parameters are set as: AC side power supply voltage is 120 V (50 Hz), DC voltage is 200 V, Sub-module capacitor voltage is 20 V, Sub-module switching frequency is 2 kHz, Bridge arm inductance is 4 mH. Other parameters remain unchanged. At 1.0 s, a permanent pole-to-pole short-circuit fault occurs on the DC side, and all sub-modules are blocked 2 ms later.

The experiment results for the DC fault current blocking capability performance of TLBSSM are shown in Figure 15. Figures 15(a), (b), (c), and (d) represent the experimental results for DC voltage, DC current, AC current, and sub-module capacitor voltage on the lower bridge arm, respectively. Based on Figures 15(a), (b), and (c), it can be observed that before the occurrence of the DC short circuit fault, the entire experimental system maintains a stable operating state. However, after the fault occurs, the DC voltage, DC current, and AC current rapidly decay to zero under the action of TLBSSM. In addition, Figure 15(d) demonstrates that the sub-module capacitor voltages remain steady at approximately 20 V after the occurrence of the fault. The experiment results show that TLBSSM has the ability to quickly remove the DC short circuit fault, and can restart the MMC quickly after the fault is cleared.

VII. CONCLUSION

In this paper, a three-level bidirectional switch sub-module (TLBSSM) is improved based on the shortcomings of CDSM, and its working state, DC fault current blocking mechanism and some characteristics are theoretically analyzed. Finally, simulation and experiment are constructed for verification. The conclusions are as follows:

1) Compared with common sub-modules, TLBSSM requires fewer IGBTs and diodes to output unit level, so it has certain economic advantages.

2) Compared with CDSM, TLBSSM connects the sub-module capacitors C_1 and C_2 in series to the fault loop during reverse blocking, which not only improves the blocking speed of the fault current, but also optimizes the equalization control of the voltage between the sub-module capacitors, which is conducive to the fast restart of the MMC after the fault is cleared.

3) Subsequent studies on TLBSSM will tend to be mixed with HBSM, which can further reduce the cost of converter station construction while ensuring that hybrid MMC can safely clear the fault current.

REFERENCES

[1] J. Wu, Z. Wang, H. Rao, Y. Chen, and W. Huang, "A review of control strategies for inertia support in VSC-HVDC system," in *Proc. 4th IEEE Workshop Electron. Grid (eGRID)*, Xiamen, China, Nov. 2019, pp. 1–6.

[2] J. Zhang, Z. Hu, D. Cui, X. Tian, and X. Yin, "MMC new type sub module topology and control," *IEEE Innov. Smart Grid Technol. Asia*, Chengdu, China, May 2019, pp. 2228–2233.

[3] S. Wu, X. Zhang, W. Jia, Y. Zhu, L. Qi, X. Guo, and X. Pan, "A modular multilevel converter with integrated energy dissipation equipment for offshore wind VSC-HVDC system," *IEEE Trans. Sustain. Energy*, vol. 13, no. 1, pp. 353–362, Jan. 2022.

[4] Z. Liu, H. Hu, Y. Liang, Y. Wang, C. Liu, S. Shi, and X. Dong, "Overview of modeling schemes for MMC converter in flexible DC distribution network," in *Proc. Int. Conf. Mach. Learn. Intell. Syst. Eng. (MLISE)*, Chongqing, China, Jul. 2021, pp. 131–134.

[5] C. Zhao, S. Li, and J. Zhang, "An augmented modular multilevel converter for clearing fault in DC grid," (in Chinese), *Autom. Electr. Power Syst.*, vol. 44, no. 5, pp. 60–67, Oct. 2020.
[6] S. Cui and S.-K. Sul, "A comprehensive DC short-circuit fault ride through strategy of hybrid modular multilevel converters (MMCs) for overhead line transmission," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7780–7796, Nov. 2016.
[7] Z. Xu, H. Xiao, and Y. Xu, "Study on basic principle and its realization methods for DC circuit breakers," (in Chinese), *High Voltage Eng.*, vol. 44, no. 2, pp. 347–357, Feb. 2018.
[8] X. Diao, R. Li, and J. Cai, "A DC circuit breaker with automatic and controllable shutoff function for flexible DC distribution system," (in Chinese), *Proc. CSEE*, vol. 43, no. 2, pp. 703–714, Oct. 2023.
[9] K. Tahata, S. E. Oukaili, K. Kamei, D. Yoshida, Y. Kono, R. Yamamoto, and H. Ito, "HVDC circuit breakers for HVDC grid applications," in *Proc. 11th IET Int. Conf. AC DC Power Transmiss.*, Birmingham, U.K., Feb. 2015, pp. 1–9.
[10] P. Qiu, X. Huang, and Y. Wang, "Application of high voltage DC circuit breaker in Zhoushan VSC-HVDC transmission project," (in Chinese), *High Voltage Eng.*, vol. 44, no. 2, pp. 403–408, Feb. 2018.
[11] R. Marquardt, "Modular multilevel converter: An universal concept for HVDC-networks and extended DC-bus-applications," in *Proc. IEEE Int. Power Electron. Conf. (IPEC)*, Jun. 2010, pp. 502–507.
[12] R. Marquardt, "Modular multilevel converter topologies with DC-short circuit current limitation," in *Proc. IEEE Int. Conf. Power Electron. (ECCE Asia)*, May/Jun. 2011, pp. 1425–1431.
[13] R. Wang, Z. Li, X. Wen, N. Liu, and X. Wang, "A novel MMC sub-module topology with DC fault clearance capability," *IEEE Access*, vol. 7, pp. 96085–96093, 2019.
[14] Y. Sun, X. Yang, and J. Ren, "Research on MMC novel dual sub-module topology with fault self-clearance capability," (in Chinese), *High Voltage Appar.*, vol. 57, no. 8, pp. 115–119, Aug. 2021.
[15] R. Jiang, C. Wang, and Y. Wang, "A novel half bridge MMC sub-module topology with four capacitors," (in Chinese), *High Voltage Eng.*, vol. 48, no. 9, pp. 3744–3754, Jul. 2022.
[16] F. Zhao, G. Xiao, D. Yang, M. Liu, X. Han, and B. Liu, "A novel T-type half-bridge cell for modular multilevel converter with DC fault blocking capability," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2016, pp. 1–6.
[17] Q. Fan, X. Zhao, and C. Zhao, "A parallel hybrid MMC for clearing fault in DC grid," (in Chinese), *Proc. CSEE*, vol. 41, no. 14, pp. 4965–4974, Dec. 2021.
[18] R. Zeng, L. Xu, L. Yao, and B. W. Williams, "Design and operation of a hybrid modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1137–1146, Mar. 2015.
[19] X. Zhao, J. Ding, J. Xu, and J. Yuan, "Hybrid MMC with low voltage operations and DC fault ride-through capabilities based on auxiliary full-bridge converter," *CSEE J. Power Energy Syst.*, vol. 8, no. 3, pp. 864–871, May 2022.
[20] S. Wang, X. Zhou, and G. Tang, "Analysis of sub-module overcurrent caused by DC pole-to-pole fault in modular multilevel converter HVDC system," (in Chinese), *Proc. CSEE*, vol. 31, no. 1, pp. 1–7, Jan. 2011.
[21] Z. Zhang, Z. Xu, and Y. Xue, "Valve losses evaluation based on piecewise analytical method for MMC–HVDC links," *IEEE Trans. Power Del.*, vol. 29, no. 3, pp. 1354–1362, Jun. 2014.
[22] C. Wang, T. Xu, Y. Wang, J. Tao, X. Wei, and X. Wang, "A clamp dual capacitor sub-module of MMC with DC fault current blocking capability," *High Voltage Eng.*, vol. 47, no. 5, pp. 1729–1739, May 2021.

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