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RESEARCH ARTICLE

Non-Isolated Zeta PWM DC-DC Power Converter Analysis for CCM Including Parasitics

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ABSTRACT This paper presents a theoretical circuit analysis for the non-isolated PWM DC-DC Zeta converter, operated at CCM (Continuous Conduction Mode) in steady-state conditions. The analysis derives the voltage and current waveforms for both current and voltages in the converter, and determines the DC voltage conversion ratio. The boundary between CCM and DCM modes is derived, as well as the expressions to determine the values of the four reactive components of the converter. The expression resulting in the maximum voltages across the mosfet and diode are determined. The expressions giving the maximum, average and *rms* values of the currents associated to all the converter devices were also derived as well as the expressions of power losses due to parasitic elements in the converter circuit, and, therefore, the converter efficiency, which also included the switching losses. To validate the proposed theoretical analysis, the converter is studied both using a time-domain circuit simulation software, and building an experimental circuit utilized for practical measurements. Theoretical results were in good agreement with simulation and experimental results.

INDEX TERMS Zeta DC-DC converter, dual SEPIC converter, PWM converter, step-down converter, step-up converter, non-inverting and non-isolated converter, power losses, efficiency, continuous conduction mode.

I. INTRODUCTION

The non-isolated Zeta DC-DC PWM converter is a non-inverting step-down and step-up converter, which has been introduced for the first time in [1]. This circuit is also referred in the literature as ''dual SEPIC'' [2] and [3]. One of its properties is the continuous output current, which makes this converter an attractive circuit in many energy-conversion applications, such as battery or supercapacitors charging applications. Parasitic parameters of converter components limit the voltage step-up capability of basic dc-dc converters at high duty cycles, preventing traditional dc-dc converters to be applied in certain applications, like renewable energy generation systems.

An insulated version of the Zeta converter is proposed in [4].

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Several applications of this circuit, also combined with other power converters, are shown in the literature, but these papers neglect the analysis of the single Zeta converter circuit. Paper [5] deals with a transformerless buck-boost converter based on a ZETA converter and, there, the analysis is focused on the introduced buck-boost converter rather than the Zeta one. In [6], the adaptive sliding-mode control is applied to the circuit introduced in [5]. The basic Zeta topology analyzed in this paper is combined with a coated circuit in [7] to achieve a high output voltage gain. Also, this paper neglects the analysis of the Zeta converter and focuses the investigations on the reduction of voltage stress on the semiconductor devices. One more high gain circuit, the Zeta converter is shown in [8], which proposes a new topology obtained from the combination of an Isolated Zeta Converter and a Quadratic-Boost Converter, whose results are suitable for application in PV plants. One more application of the Zeta converter to PV plants, where high gains are required,

is given in [9]. Other papers, [10] and [11], apply the Zeta converter for PFC applications, even if these papers deal with the so-called SEPIC topology rather than the Zeta converter as proposed in [1]. Note that the SEPIC converter is largely investigated in [12], [13], [14], and [15]. Some dynamical modeling of the Zeta converter, based on a state-space averaging technique, is given in [16] and [17]. A small-signal modeling of the dc-dc Zeta converter power stage, operating in continuous-conduction mode, is addressed in [3] by using the circuit averaging technique. Finally, reliability of the Zeta converter has been investigated in [18].

However, a detailed analysis of this converter for steady-state operation and design equations are still missing in the literature. Some efforts have been spent in [19], where the circuit analysis is addressed, but with some limitations, such as the design of the output filter, which is not as accurate as that provided in [20]. An accurate loss analysis is missing as well as, the efficiency effect on the DC voltage transfer function and, then, on the duty cycle. As a result, the design equations provided in [19] are largely approximated.

The purpose of this paper is to overcome the above-mentioned limitations and provide the readers and designers with an accurate understanding of the converter operation and its limitations. The design equations are analytically derived, including the circuit device parasitic components. The effect of both conduction losses and power mosfet switching losses on the converter operation are investigated and accurately described. Theoretical derivations are utilized in a design example, which has been used to size a circuit. The designed converter was simulated, built, and experimentally tested. The results of the derivations were confirmed by the measurements made in the operating experimental circuits.

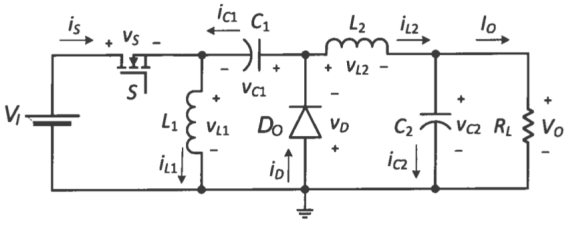

FIGURE 1. Circuit of the non-isolated Zeta dc-dc PWM power converter.

II. WAVEFORMS

The waveform of the Zeta converter operated in CCM are derived under the following assumptions:

1) All the components are ideal, i.e. all the parasitic resistances ($r_{DS} = r_F = r_{L1} = r_{L2} = r_{C1} = r_{C2} = 0$, and diode offset voltage $V_F = 0$). Also, the switching times of the mosfet and the diode are zero.
2) The ripple voltage of capacitors C_1 and C_2 are low enough so that the voltages across these capacitors can be regarded as constant, i.e., $v_{C1} = V_O$ and $v_{C2} = V_O$.

For $0 < t \leq DT$, the mosfetis on and the diode is off. Hence, $v_{DS} = 0$ and $i_D = 0$. The voltage drop across

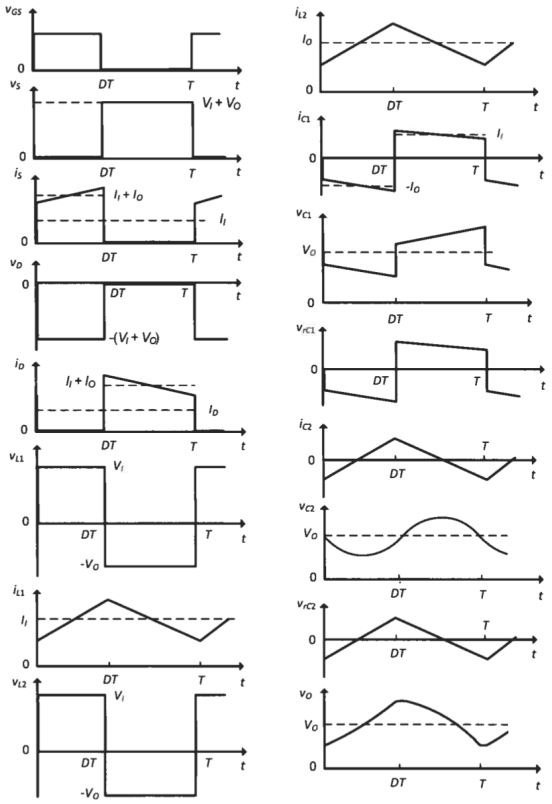

FIGURE 2. Idealized current and voltage waveforms of a non-isolated Zeta converter.

inductor L_1 is

$$v_{L1} = V_I = L_1 \frac{di_{L1}}{dt} \tag{1}$$

and the current waveform through the inductor L_1 is

$$i_{L1} = \frac{1}{L_1}\int_0^t v_{L1}dt + i_{L1}(0) = \frac{1}{L_1}\int_0^t V_I dt + i_{L1}(0)$$
$$= \frac{V_I}{L_1}t + i_{L1}(0). \tag{2}$$

At $t = DT$,

$$i_{L1}(DT) = \frac{V_I}{L_1}DT + i_{L1}(0) \tag{3}$$

and the ripple current through inductor L_1 is

$$\Delta i_{L1} = i_{L1}(DT) - i_{L1}(0) = \frac{DV_I}{f_s L_1} = \frac{(1-D)V_O}{f_s L_1}. \tag{4}$$

The energy stored in the magnetic field in inductor L_1 increases with the time like a parabola

$$w_{L1} = \frac{1}{2}L_1 i_{L1}^2(t) = \frac{1}{2}L_1\left[\frac{V_I}{L_1}t + i_{L1}(0)\right]^2. \tag{5}$$

The voltage across the coupling capacitor C_1 for the entire cycle is $v_{C1} \approx V_{C1} \approx V_O$ if the ripple of this voltage is very low as compared with V_O. From KVL,

$$v_{L2} = v_{C2} + V_I - V_O \approx V_O + V_I - V_O = V_I = L_2\frac{di_{L2}}{dt}, \tag{6}$$

yielding the current waveform through the inductor L_2

$$i_{L2} = \frac{1}{L_2}\int_0^t v_{L2}dt + i_{L2}(0) = \frac{1}{L_2}\int_0^t V_I dt + i_{L2}(0). = \frac{V_I}{L_2}t + i_{L2}(0). \quad (7)$$

At $t = DT$,

$$i_{L2}(DT) = \frac{V_I}{L_2}DT + i_{L2}(0), \quad (8)$$

resulting in the current ripple of L_2

$$\Delta i_{L2} = \frac{V_I}{L_2}DT = \frac{DV_I}{f_s L_2}. \quad (9)$$

This gives the maximum ripple current in inductor L_2

$$\Delta i_{L2max} = \frac{D_{min}V_{Imax}}{f_s L_2}. \quad (10)$$

The energy stored in the magnetic field in inductor L_2 increases with the time as a second-order function

$$w_{L2} = \frac{1}{2}L_2 i_{L2}^2(t) = \frac{1}{2}L_2\left[\frac{V_I}{L_2}t + i_{L2}(0)\right]^2. \quad (11)$$

The switch current waveform is

$$\begin{aligned} i_S &= i_{L1} - i_{C1} = i_{L1} + i_{L2} \\ &= \frac{V_I}{L_1} + i_{L1}(0) + \frac{V_I}{L_2} + i_{L2}(0) \\ &= V_I\left(\frac{1}{L_1} + \frac{1}{L_2}\right) + i_{L1}(0) + i_{L2}(0) \\ &= \frac{V_I}{L_p} + i_{L1}(0) + i_{L2}(0), \end{aligned} \quad (12)$$

where

$$\frac{1}{L_p} = \frac{1}{L_1} + \frac{1}{L_2} = \frac{L_1 + L_2}{L_1 L_2}. \quad (13)$$

The switch current ripple is

$$\Delta i_S = \Delta i_{L1} + \Delta i_{L2} = \frac{V_I}{L_1}DT + \frac{V_I}{L_2}DT = \frac{DV_I}{f_s L_P}. \quad (14)$$

The inverse diode voltage is

$$v_{KA} = -v_D = v_{L2} + V_O \approx V_I + V_O. \quad (15)$$

Fig. 2 shows the idealized current and voltage waveform of a non-isolated Zeta converter.

A. TIME INTERVAL $DT < T \leq T$

For $DT < t \leq T$, the mosfet is off and the diode is on. Hence, $i_S = 0$ and $v_D = 0$. The voltage drop across inductor L_1 is

$$v_{L1} = -v_{C1} \approx V_O = L_1\frac{di_{L1}}{dt}, \quad (16)$$

which gives the current waveform through inductor L_1

$$\begin{aligned} i_{L1} = i_{C1} &= \frac{1}{L_1}\int_{DT}^t v_{L1}dt + i_{L1}(DT) \\ &= \frac{1}{L_1}\int_{DT}^t -(V_O)dt + i_{L1}(DT) \\ &= -\frac{V_O}{L_1}(t - DT) + i_{L1}(DT) \\ &= -\frac{V_O}{L_1}(t - DT) - \frac{DTV_O}{L_1} + i_{L1}(0). \end{aligned} \quad (17)$$

The magnetic energy stored in the magnetic field in inductor L_1 decreases with the time as a second-order function

$$\begin{aligned} w_{L1} &= \frac{1}{2}L_1 i_{L1}^2(t) \\ &= \frac{1}{2}L_1\left[-\frac{V_O}{L_1}(t - DT) - \frac{DTV_O}{L_1} + i_{L1}\right]^2. \end{aligned} \quad (18)$$

The drain-to-source voltage is

$$v_{DS} = V_I - v_{L1} \approx V_I - (-V_O) = V_I + V_O. \quad (19)$$

The voltage across inductor L_2 is

$$v_{L2} \approx -V_O = L_2\frac{di_{L2}}{dt}, \quad (20)$$

producing the current through this inductor is given by

$$\begin{aligned} i_{L2} &= \frac{1}{L_2}\int_{DT}^t v_{L2}dt + i_{L2}(DT) \\ &= \frac{1}{L_2}\int_{DT}^t -(V_O)dt + i_{L2}(DT) \\ &= -\frac{V_O}{L_2}(t - DT) + i_{L2}(DT) \\ &= -\frac{V_O}{L_2}(t - DT) - \frac{DTV_O}{L_2} + i_{L2}(0). \end{aligned} \quad (21)$$

The magnetic energy stored in the magnetic field in inductor L_2 decreases with time

$$\begin{aligned} w_{L2} &= \frac{1}{2}L_2 i_{L2}^2(t) \\ &= \frac{1}{2}L_1\left[-\frac{V_O}{L_2}(t - DT) - \frac{DTV_O}{L_1} + i_{L2}(0)\right]^2. \end{aligned} \quad (22)$$

The diode current is expressed as

$$\begin{aligned} i_D &= i_{L1} + i_{C1} = i_{L1} + i_{L2} \\ &= -\frac{V_O}{L_1}(t - DT) + i_{L1}(DT) - \frac{V_O}{L_2}(t - DT) + i_{L2}(DT) \\ &= -\frac{V_O}{L_p}(t - DT) + i_{L1}(DT) + i_{L2}(DT). \end{aligned} \quad (23)$$

The diode and switch ripple currents are the same and expressed as follows:

$$\Delta i_D = \Delta i_S = \Delta i_{L1} + \Delta i_{L2}(DT) = \frac{DV_I}{f_s L_p} = \frac{(1 - D)V_O}{f_s L_p}. \quad (24)$$

III. DC VOLTAGE CONVERSION RATIO

In a DC-DC PWM converter operating in steady state, the balance of the magnetic linkage of inductor L_1 is $|\Delta\lambda_{L1}^{+}| = |\Delta\lambda_{L1}^{-}|$. Hence, using the volt-second balance for the voltage across inductor L_1 or L_2, one obtains

$$DTV_I = (1-D)TV_O, \tag{25}$$

which results in the dc conversion voltage ratio of the lossless Zeta converter

$$M_{VDC} \equiv \frac{V_O}{V_I} = \frac{V_{KA}}{V_{DS}} = \frac{I_I}{I_O} = \frac{I_{DS}}{I_D} = \frac{I_{DS}}{I_{L2}} = \frac{D}{D'} = \frac{D}{1-D}. \tag{26}$$

Hence, duty cycle of the lossless Zeta converter required for achieving a desired M_{VDC} is

$$D = \frac{M_{VDC}}{M_{VDC}+1}. \tag{27}$$

Fig. 3 shows the dc voltage transfer function as a function of the duty cycle D for lossless converter ($\eta = 100\%$).

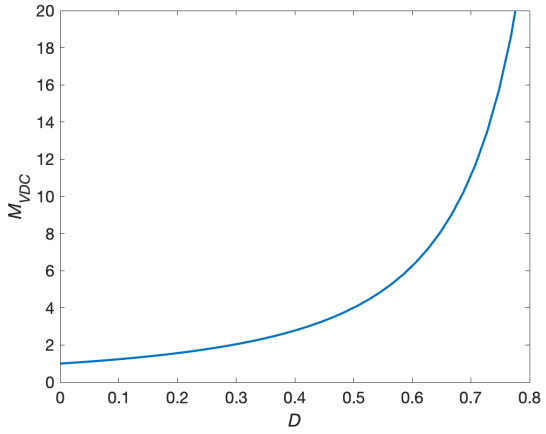

FIGURE 3. DC voltage transfer function $M_{VDC} = D/(1-D)$ as a function of the duty cycle D for non-isolated Zeta converter at efficiency $\eta = 100\%$.

The converter efficiency is

$$\eta \equiv \frac{P_O}{P_I} = \frac{I_O V_O}{I_I V_I} = M_{IDC} M_{VDC} = \frac{M_{VDC(lossy)}}{M_{VDC(lossless)}}. \tag{28}$$

Therefore, the dc voltage transfer function of the real lossy Zeta converter is reduced by the converter efficiency

$$M_{VDC(lossy)} = \frac{V_O}{V_I} = \eta M_{VDC(lossless)} = \eta \frac{D}{(1-D)} \tag{29}$$

and the required duty cycle for the lossy Zeta converter is

$$D = \frac{M_{VDC}}{M_{VDC}+\eta}. \tag{30}$$

IV. BOUNDARY BETWEEN CCM AND DCM

The peak-to-peak inductor ripple currents at the boundary between CCM and DCM modes are

$$\Delta i_{L1} = \frac{(1-D)V_O}{f_s L_1} \tag{31}$$

and

$$\Delta i_{L2} = \frac{(1-D)V_O}{f_s L_2}. \tag{32}$$

At the CCM/DCM boundary, the diode current at the end of the cycle is $i_D(T) = 0$. The peak diode current occures at $t = DT$ and is given by

$$\Delta i_D = i_D(DT) = \Delta i_{L1} + \Delta i_{L2} = \frac{(1-D)V_O}{f_s L_1} + \frac{(1-D)V_O}{f_s L_2} = \frac{(1-D)V_O}{f_s L_p}. \tag{33}$$

The average diode current over the cycle is equal to the dc load current. The load current at the boundary CCM/DCM is

$$I_{OB} = \frac{1}{T}\frac{(1-D)T\Delta i_D}{2} = \frac{V_O(1-D)^2}{2f_s L_p}, \tag{34}$$

where it is assumed that the converter is operated at a constant output voltage. Fig. 4 shows the normalized load current $I_O/(V_O/2f_s L_p)$ as a function of the duty cycle D for the loss-less non-isolated Zeta converter at $\eta = 100\%$.

The load resistance at the boundary between CCM and DCM is

$$R_{LB} = \frac{V_O}{I_{OB}} = \frac{2f_s L_p}{(1-D)^2}. \tag{35}$$

Fig. 4 shows the normalized load resistance $R_{LB}/2f_s L_p$ as a function of the duty cycle D for loss-less non-isolated Zeta converter at $\eta = 100\%$.

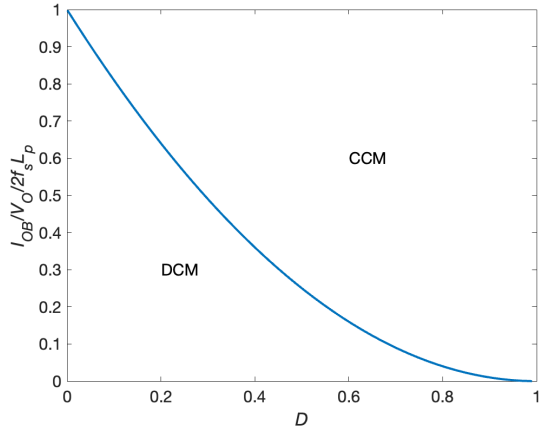

FIGURE 4. Normalized load current $I_O/(V_O/2f_s L_p)$ as a function of the duty cycle D for lossless non-isolated Zeta converter at efficiency $\eta = 100\%$.

From (35), the Zeta converter operates in the continuous-conduction mode for the total inductance given by

$$L_p > L_{pmin} = \frac{L_1 L_2}{L_1 + L_2} = \frac{V_O(1-D)^2}{2f_s I_{Omin}}, \tag{36}$$

which, for at $D = 0.5$, results in

$$L_{pmin} = 0.125\frac{V_O}{f_s I_{Omin}}. \tag{37}$$

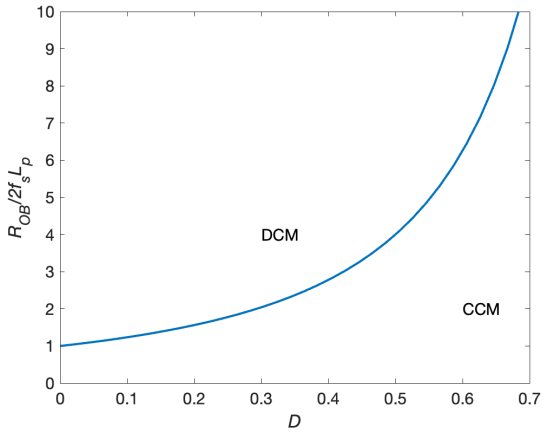

FIGURE 5. Normalized load resistance $R_L/2f_sL_p$ as a function of the duty cycle D for loss-less non-isolated Zeta converter at efficiency $\eta = 100\%$.

Let $L_2 = aL_1$. Then

$$L_p = \frac{L_1L_2}{L_1+L_2} = \frac{L_1(aL_1)}{L_1+aL_2} = \frac{a}{a+1}L_1, \tag{38}$$

yielding the inductances

$$L_1 = \left(\frac{1}{a}+1\right)L_p \tag{39}$$

and

$$L_2 = (a+1)L_p. \tag{40}$$

For a converter operated a constant dc input voltage V_I, the combination of (34) and (27)

$$I_{OB} = \frac{V_O(1-D)^2}{2f_sL_p} = \frac{V_ID(1-D)}{2f_sL_p}, \tag{41}$$

which produces the minimum inductance for CCM at a constant input voltage V_I

$$L_{pmin} = \frac{V_ID(1-D)}{2f_sI_{Omin}}. \tag{42}$$

For $D = 0.5$,

$$L_{pmin} = 0.125\frac{V_I}{f_sI_{Omin}}. \tag{43}$$

V. MAXIMUM VOLTAGES AND CURRENTS

The maximum voltage of the drain-to-source voltage and the maximum reverse diode voltage are

$$V_{DSmax} = V_{Dmax} = V_{Imax} + V_O = \frac{V_O}{D_{min}}. \tag{44}$$

It is assumed above that the dc output voltage V_O is fixed, like in many applications of DC-DC converters. If the output voltage V_O varies, the maximum dc output voltage V_{Omax} should be used, like in battery and super-capacitor chargers.

The maximum voltages across capacitors C_1 and C_2 are

$$V_{C1max} = V_{C2max} = V_O. \tag{45}$$

The maximum current through inductor L_1 is

$$\begin{aligned} I_{L1max} &= \frac{D\,I_{Omax}}{1-D_{min}} + \frac{\Delta i_{L1max}}{2} \\ &= \frac{D\,I_{Omax}}{1-D_{min}} + \frac{(1-D_{min})\,V_O}{2f_sL_1} \end{aligned} \tag{46}$$

and the maximum current through inductor L_2 is

$$\begin{aligned} I_{L2max} &= I_{Omax} + \frac{\Delta I_{L2max}}{2} \\ &= I_{omax} + \frac{(1-D_{min})\,V_O}{2f_sL_2}. \end{aligned} \tag{47}$$

The maximum drain current and the maximum diode current are

$$\begin{aligned} I_{DSmax} &= I_{DMmax} = I_{L1max} + I_{L2max} \\ &\approx I_{Imax} + I_{Omax} = \frac{D_{min}}{1-D_{min}}I_{omax} + I_{omax} \\ &= \frac{1}{1-D_{min}}I_{omax}. \end{aligned} \tag{48}$$

VI. CAPACITORS OF ZETA CONVERTER

The equivalent circuit of the coupling capacitor is the combination of capacitance C_1 and its series equivalent resistance (ESR) r_{C1}, related waveforms are shown in Fig. 6.

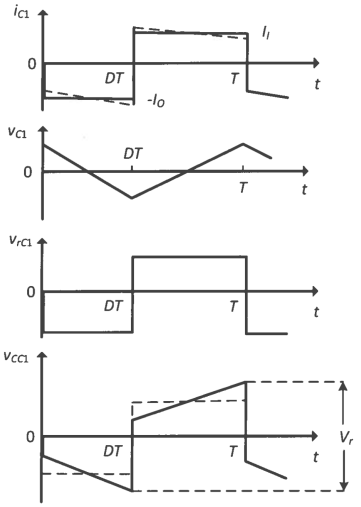

FIGURE 6. Waveforms across equivalent components of the coupling capacitor C_1.

For $0 < t \le DT$, the current through coupling capacitor C_1 is

$$i_{C1} \approx -I_O, \tag{49}$$

yielding the voltage waveform across capacitance C_1

$$\begin{aligned} v_{C1} &= \frac{1}{C_1}\int_0^t i_{C1}dt + v_{C1}(0) \\ &= \frac{1}{C_1}\int_0^t (-I_O)dt + v_{C1}(0) = -\frac{I_O}{C_1}t + v_{C1}(0). \end{aligned} \tag{50}$$

Hence,

$$v_{C1}(DT) = -\frac{I_O}{C_1}DT + v_{C1}(0) = -\frac{DI_O}{f_sC_1} + v_{C1}(0) \tag{51}$$

and the peak-to-peak voltage across coupling capacitance C_1 is

$$\Delta v_{C1} = v_{C1}(0) - v_{C1}(DT) = v_{C1}(0) - \left[-\frac{DI_O}{f_s C_1} + v_{C1}(0)\right] = \frac{DI_O}{f_s C_1}. \quad (52)$$

This gives the maximum peak-to-peak voltage change across C_1

$$V_{C1pp} = \frac{D_{max} I_{Omax}}{f_s C_1}, \quad (53)$$

resulting in the maximum coupling capacitance

$$C_1 > C_{1min} = \frac{D_{max} I_{Omax}}{f_s V_{c1pp}}. \quad (54)$$

The minimum coupling capacitor current is

$$I_{C1min} \approx I_{Omax}. \quad (55)$$

During time interval $DT < t \leq T$, the coupling capacitor current is

$$I_{C1} \approx I_I = I_O \frac{D}{1-D} \quad (56)$$

and the voltage waveform across the coupling capacitance C_1 is

$$v_{C1} = \frac{1}{C_1}\int_{DT}^{t} i_{C1} dt + v_{C1}(DT) = \frac{1}{C_1}\int_{DT}^{t} \frac{DI_O}{1-D} dt + v_{C1}(0) = \frac{DI_O}{1-D}(t - DT) + v_{C1}(DT). \quad (57)$$

The maximum current through the coupling capacitance C_1 is

$$I_{C1max} \approx I_I = I_{Omax} \frac{D_{min}}{1-D_{min}}. \quad (58)$$

The maximum peak-to-peak current through the coupling capacitance C_1 is

$$I_{C1ppmax} = I_{C1max} - I_{C1min} = I_{Imax} - (-I_{Omax}) = I_{Imax} + I_{Omax} = \frac{D_{min} I_{Omax}}{1-D_{min}} - I_{Omax} = \frac{I_{Omax}}{1-D_{min}}. \quad (59)$$

Hence, the maximum peak-to-peak voltage across resistance r_{C1} is

$$V_{rC1ppmax} = r_{C1} I_{rC1ppmax} \frac{r_{C1} I_{Omax}}{1-D}, \quad (60)$$

producing the the maximum allowed ESR of C_1 is

$$r_{C1max} = V_{rC1ppmax} \frac{1-D_{min}}{I_{Omax}}. \quad (61)$$

The total peak-to-peak voltage ripple of physical capacitor C_1 is

$$V_r = V_{C1pp} + V_{rC1pp} = \frac{D_{max} I_{Omax}}{f_s C_1} + \frac{r_{C1} I_{Omax}}{1-D_{min}} = I_{Omax}\left(\frac{D_{max}}{f_s C_1} + \frac{r_{C1}}{1-D_{min}}\right). \quad (62)$$

VII. LOSSES IN THE ZETA CONVERTER

Fig. 7 shows the equivalent circuit of a non-isolated Zeta converter with parasitic resistances and diode offset voltage V_F.

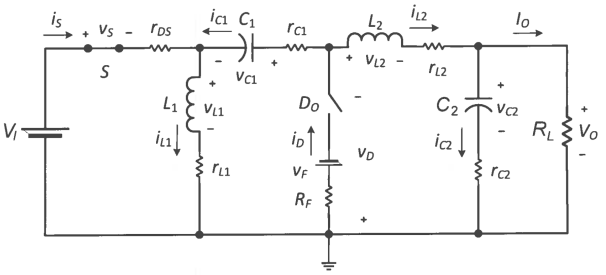

FIGURE 7. Equivalent circuit of non-isolated Zeta converter with parasitic resistances and diode offset voltage.

Neglecting the current ripple, the switch current is

$$i_S \approx \begin{cases} I_I + I_O = \dfrac{I_O}{1-D} & \text{for } 0 < t \leq DT; \\ 0 & \text{for } DT < t \leq T. \end{cases} \quad (63)$$

Hence, the rms switch current is

$$I_{Srms} = \sqrt{\frac{1}{T}\int_0^{DT} i_S^2 dt} = \sqrt{\frac{1}{T}\int_0^{DT} \left(\frac{I_O}{1-D}\right)^2 dt} = \frac{I_O}{1-D}\sqrt{\frac{1}{T}\int_0^{DT} dt} = \frac{I_O\sqrt{D}}{1-D}, \quad (64)$$

yielding the mosfet conduction power loss

$$P_{rDS} = r_{DS} I_{Srms}^2 = \frac{D r_{DS} I_O^2}{(1-D)^2} = \frac{D r_{DS}}{(1-D)^2 R_L} P_O. \quad (65)$$

The mosfet turn-on time is $t_{Ton} = t_{ir} + t_{vf}$, where t_{ir} is the drain current rise time and t_{vf} is the drain-to-source voltage fall time during the mosfet turn-on. Assume that the mosfet turn-off time is $t_{Toff} = t_{Ton}$. The drain current is $i_D \approx I_{DSon} = I_I + I_O = I_O/(1-D)$ during the mosfet on time. The drain-to-source voltage is $v_{DS} = V_{DSoff} = V_I + V_O = V_O/D$ during the mosfet off time. Hence, the switching power loss during the turn-on and turn-off mosfet transitions caused by overlapping the drain current waveform i_{DS} and the drain-to-source waveform v_{DS} is

$$P_{sw} = \frac{1}{2} f_s (t_{Ton} + t_{Toff}) V_{DSoff} I_{DSon} = \frac{1}{2} f_s (t_{Ton} + t_{Toff})(V_i + V_O)(I_I + I_O) = \frac{f_s (t_{Ton} + t_{Toff}) V_O I_O}{2D(1-D)} = \frac{f_s (t_{Ton} + t_{Toff})}{2D(1-D)} P_O = \frac{f_s (t_{Ton} + t_{Toff}) V_O^2}{2D(1-D) R_L}. \quad (66)$$

The minimum switching power loss occurs at $D = 0.5$. The total mosfet power loss is

$$P_{FET} = \frac{D r_{DS}}{(1-D)^2 R_L} P_O + f_s \frac{(t_{Ton} + t_{Toff})}{2D(1-D)} P_O. \quad (67)$$

The current through inductor L_1 is

$$i_{L1} \approx I_{L1} = I_I = I_{L1rms} = \frac{I_O D}{1-D}, \tag{68}$$

producing the power loss in inductor L_2 ESR r_{L2} given as

$$P_{rL1} = r_{L1} I_{L1rms}^2 = \frac{D^2 r_{L1} I_O^2}{(1-D)^2} = \frac{D^2 r_{L1}}{(1-D)^2 R_L} P_O. \tag{69}$$

The current through the coupling capacitor C_1 can be approximated as

$$i_{C1} \approx \begin{cases} -I_O & \text{for } 0 < t \le DT; \\ I_I & \text{for } DT < t \le T. \end{cases} \tag{70}$$

The rms value of the coupling capacitor current C_1 is

$$\begin{aligned} I_{C1rms} &= \sqrt{\frac{1}{T}\int_0^T i_{C1}^2 dt} \\ &= \sqrt{\frac{1}{T}\int_0^{DT} I_O^2 dt + \frac{1}{T}\int_{DT}^T I_I^2 dt} \\ &= \sqrt{DI_O^2 + (1-D)I_I^2} = I_O\sqrt{\frac{D}{1-D}}. \end{aligned} \tag{71}$$

Thus, the conduction power loss in the coupling capacitor C_1 is

$$P_{rC1} = r_{C1} D I_{C1rms}^2 = \frac{D I_O^2 r_{C1}}{(1-D)} = \frac{D r_{C1}}{(1-D) R_L} P_O. \tag{72}$$

The current through the filter capacitor C_2 is

$$i_{C2} = \begin{cases} \dfrac{\Delta i_{L2} t}{DT} - \dfrac{\Delta i_{L2}}{2} & \text{for } 0 < t \le DT; \\ \dfrac{\Delta i_{L2}(t-DT)}{(1-D)T} + \dfrac{\Delta i_{L2}}{2} & \text{for } DT < t \le T. \end{cases} \tag{73}$$

The rms current through the filter capacitor C_2 is

$$I_{C2rms} = \sqrt{\frac{1}{T}\int_0^T i_{C2}^2 dt} = \frac{\Delta i_{L2}}{\sqrt{12}} = \frac{(1-D)V_O}{\sqrt{12} f_s L_2}. \tag{74}$$

The power loss in the ESR of the filter capacitor C_2 is given by

$$\begin{aligned} P_{rC2} &= r_{C2} I_{C2rms}^2 = \frac{\Delta i_{L2}^2 r_{C2}}{12} = \frac{(1-D)^2 V_O^2 r_{C2}}{12 f_s^2 L_2^2} \\ &= \frac{(1-D)^2 r_{C2} R_L}{12 f_s^2 L_2^2} P_O. \end{aligned} \tag{75}$$

This power is usually very low and can be neglected.

The current through the inductor L_2 is

$$i_{L2} \approx I_O = I_{L2rms}, \tag{76}$$

which gives the power loss in the ESR r_{L2} of inductor L_2

$$P_{rL2} = r_{L2} I_{L2rms}^2 = r_{L2} I_O^2 = \frac{r_{L2}}{R_L} P_O. \tag{77}$$

The diode current is

$$i_D \approx \begin{cases} 0 & \text{for } 0 < t \le DT; \\ I_I + I_O = \dfrac{I_O}{1-D} & \text{for } DT < t \le T. \end{cases} \tag{78}$$

The average diode current is approximated by

$$I_D = \frac{1}{T}\int_{DT}^T i_D dt = \frac{1}{T}\int_{DT}^T \frac{I_O}{1-D} dt = I_O, \tag{79}$$

yielding the power loss in the diode offset voltage source V_F

$$P_{VF} = V_F I_O = \frac{V_F}{V_O} P_O. \tag{80}$$

The diode rms current is

$$\begin{aligned} I_{Drms} &= \sqrt{\frac{1}{T}\int_0^T i_D^2 dt} = \sqrt{\frac{1}{T}\int_0^T \left(\frac{I_O}{1-D}\right)^2 dt} \\ &= \frac{I_O}{\sqrt{1-D}}. \end{aligned} \tag{81}$$

Hence, the power loss in the diode forward resistance is

$$P_{RF} = R_F I_{Drms}^2 = \frac{r_F I_O^2}{1-D} = \frac{R_F}{R_L(1-D)} P_O. \tag{82}$$

The overall power loss in the diode is

$$\begin{aligned} P_D &= P_{RF} + P_{VF} = \frac{R_F I_O^2}{1-D} + V_F I_O \\ &= \frac{R_F}{R_L(1-D)} P_O + \frac{V_F}{V_O} P_O. \end{aligned} \tag{83}$$

The total power loss in Zeta converter is

$$\begin{aligned} P_{LS} &= P_{rDS} + P_{sw} + P_D + P_{rL1} + P_{rL2} + P_{rC1} + P_{rC2} \\ &= \left[\frac{D r_{DS}}{(1-D)^2 R_L} + \frac{f_s(t_{Ton} + t_{Toff})}{2D(1-D)} + \frac{R_F}{R_L(1-D)} + \frac{V_F}{V_O} \right. \\ &\quad \left. + \frac{D^2 r_{L1}}{(1-D)^2 R_L} + \frac{r_{L2}}{R_L} + \frac{D r_{C1}}{(1-D) R_L} + \frac{(1-D)^2 r_{C2} R_L}{12 f_s^2 L_2^2}\right] P_O. \end{aligned} \tag{84}$$

VIII. DESIGN AND EFFICIENCY OF ZETA CONVERTER

A. CONVERTER DESIGN PROCEDURE

The efficiency of the Zeta converter is

$$\eta = \frac{P_O}{P_I} = \frac{P_O}{P_I + P_{LS}} = \frac{1}{1 + \frac{P_{LS}}{P_O}}, \tag{85}$$

where

$$\begin{aligned} \frac{P_{LS}}{P_O} &= \frac{V_F}{V_O} + \frac{D r_{DS}}{(1-D)^2 R_L} + \frac{R_F}{(1-D) R_L} + \frac{D^2 r_{L1}}{(1-D)^2 R_L} + \frac{r_{L2}}{R_L} \\ &\quad + \frac{D r_{C1}}{(1-D) R_L} + \frac{r_{C2} R_L (1-D)^2}{12 f_s^2 L_2^2} + \frac{f_s(t_{Ton} + t_{Toff})}{2D(1-D)}. \end{aligned} \tag{86}$$

Taking into account the converter efficiency η, the dc voltage transfer function of the Zeta converter is

$$M_{VDC} = \frac{V_O}{V_I} = \eta \frac{D}{1-D} = \frac{1}{1 + \frac{P_{LS}}{P_O}} \frac{D}{1-D}. \tag{87}$$

A Zeta converter was designed and simulated for the following specifications: $V_I = 12 \pm 3$ V, $V_O = 12$ V, $I_O = 0.1$-1 A, and $P_O = 1.2$-12 W. This corresponds to $R_L = 120$-12 Ω and $P_O = 1.2$-12 W, respectively. The values of the DC voltage transfer function are derived as

$$M_{VDCmin} = \frac{V_O}{V_I max} = 0.81. \tag{88}$$

$$M_{VDCmax} = \frac{V_O}{V_I min} = 0.67. \tag{89}$$

According to (87) the nominal duty cycle is $D_{nom} = 0.526$ at $V_I = 12$ V, assuming $\eta = 90\%$, wile the minimum and the maximum values duty cycle are determined as

$$D_{min} = \frac{M_{VDCmin}}{M_{VDCmin} + \eta} = 0.44 \tag{90}$$

and

$$D_{max} = \frac{M_{VDCmax}}{M_{VDCmax} + \eta} = 0.57, \tag{91}$$

respectively.

The maximum drain-to-source voltage of the MOSFET and the maximum reverse diode voltage are

$$V_{DSmax} = V_{Imax} + V_O = 27 \text{ V}. \tag{92}$$

The maximum currents of the MOSFET and the diode are

$$I_{DSmax} = I_{Dmax} = \frac{I_{Omax}}{1 - D_{min}} = 1.9 \text{ A}. \tag{93}$$

This allows for a proper MOSFET and diode selection. Assume the switching frequency $f_s = 2$ MHz. According to 42, the equivalent inductance is calculated as $L_p = 8.42$ μH. Let us assume L_p=11 μH, hence $L_1 = L_2 = 2L_p = 22$ μH.

The peak-to-peak ripple current of capacitor C_1 is

$$\Delta I_{C1max} = \frac{I_{Omax}}{1 - D_{min}} = 1.9 \text{ A}. \tag{94}$$

and this allows for a maximum capacitor C_1 equivalent series resistance

$$r_{C1max} = \frac{V_{rC1}}{\Delta IC1max} = 16.1 \text{ mΩ}. \tag{95}$$

while the resulting capacitance is

$$C_1 > C_{1min} = \frac{I_{Omax} D_{max}}{f_s V C1pp} = 10.14 \text{ μF}. \tag{96}$$

The maximum voltage across capacitor C_1 is $V_{C1max} = 12$ V. The peak-to-peak ripple current of capacitor C_2 and inductor L_2 is

$$\Delta I_{C2max} = \frac{V_O(1 - D_{min})}{f_s L_2} = 0.14 \text{ A}. \tag{97}$$

The resulting allowed capacitor C_2 ESR is

$$r_{C2max} = \frac{V_{rC2}}{\Delta I_{C2max}} = 107 \text{ mΩ}. \tag{98}$$

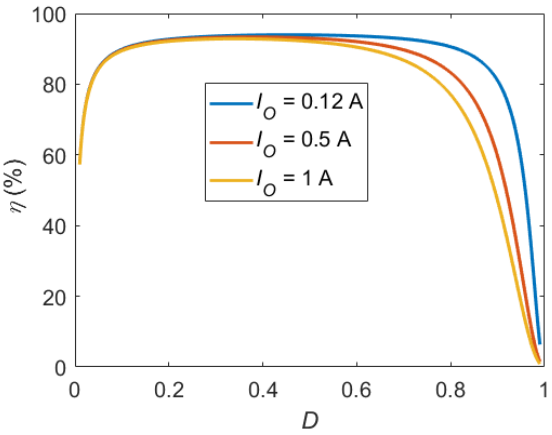

FIGURE 8. Converter efficiency η as a function of duty cycle D at $V_O = 12$ V and load currents $I_O = 0.12$, 0.5, and 1 A for the non-isolated Zeta converter.

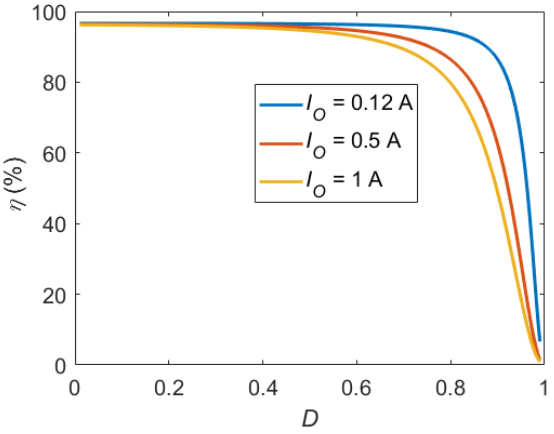

FIGURE 9. Converter efficiency η as a function of duty cycle D at $V_O = 12$ V and load currents $I_O = 0.12$, 0.5, and 1 A, when switching losses are neglected.

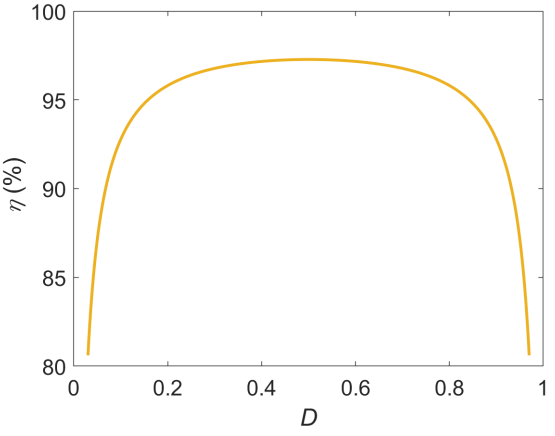

FIGURE 10. Converter efficiency η as a function of duty cycle D at $V_O = 12$ V and load currents $I_O = 0.12$, 0.5, and 1 A, when only switching losses are considered.

Capacitor C_2 value is determined by

$$C_2 > C_{2min} = \frac{max(D_{max}, 1 - D_{min})}{2 f_s r_{C2}} = 1.38 \text{ μF}. \tag{99}$$

The maximum voltage across capacitor C_2 is $V_{C2max} = 12$ V.

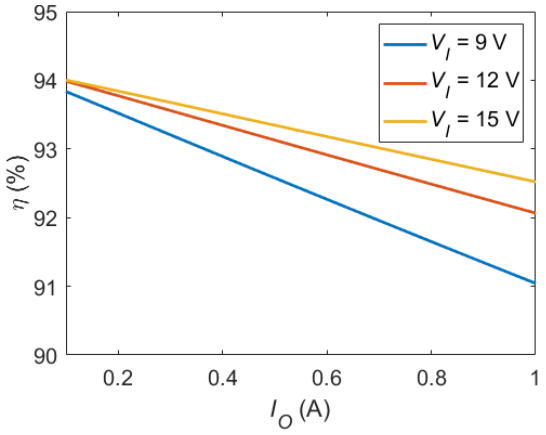

FIGURE 11. Converter efficiency η as a function of I_O at $V_O = 12$ V and dc input voltages $V_I = 9$, 12, and 15 V.

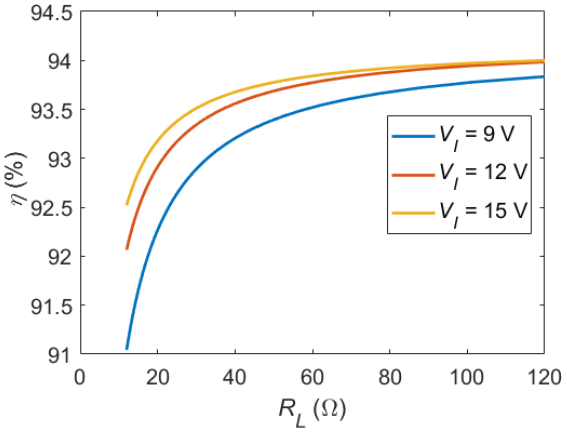

FIGURE 12. Converter efficiency η as a function of R_L at $V_O = 12$ V and at input voltages $V_I = 9$, 12, and 15 V.

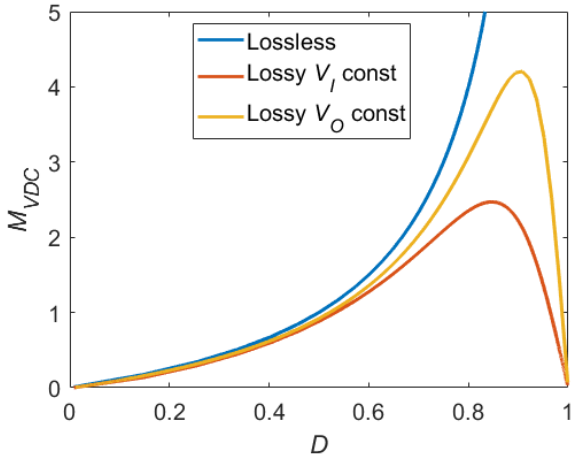

FIGURE 13. DC voltage transfer functions M_{VDC} as a function of the duty cycle D at $I_O = 1$ A (1) for a loss-less converter $V_O = 12$ V, (2) a lossy converter at $V_O = 12$ V, (3) for lossy converter at $V_I = 12$ V.

The parasitic components values utilized in the simulations are as follows: $r_{DS} = 182$ mΩ, $t_{ri} = 4$ ns, $t_{fv} = 3$ ns, $V_F = 0.4$ V, $R_F = 17$ mΩ, $r_{L1} = 132$ mΩ, $r_{L2} = 52$ mΩ, $r_{C1} = 6$ mΩ, and $r_{C2} = 140$ mΩ.

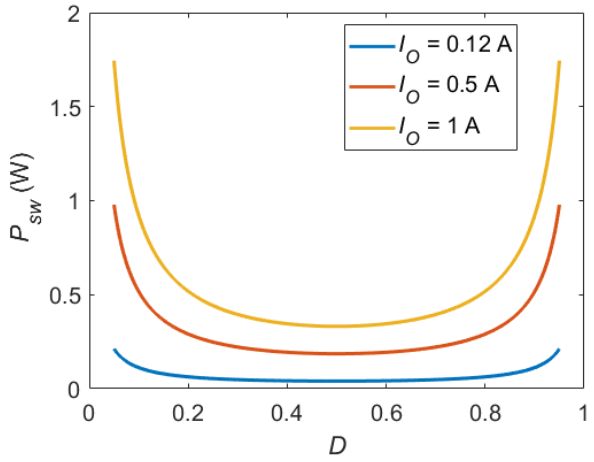

FIGURE 14. Power mosfet switching losses P_{loss} as a function of the duty cycle D at $V_O = 12$ V.

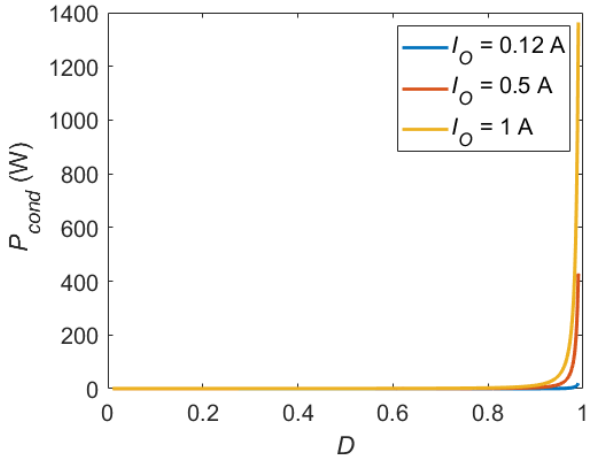

FIGURE 15. Conduction power losses P_{cond} as a function of duty cycle D (with D ranging from 0.01 to 0.99) at $V_O = 12$ V.

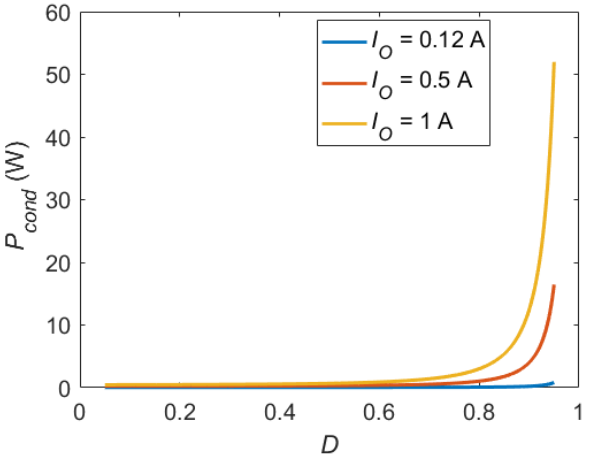

FIGURE 16. Conduction power losses P_{cond} as a function of duty cycle D (with D ranging from 0.05 to 0.95) at $V_O = 12$ V.

B. EFFICIENCY ANALYSIS

Fig. 8 shows the converter efficiency η as a function of duty cycle D at $V_O = 12$ V for at three values of the load current

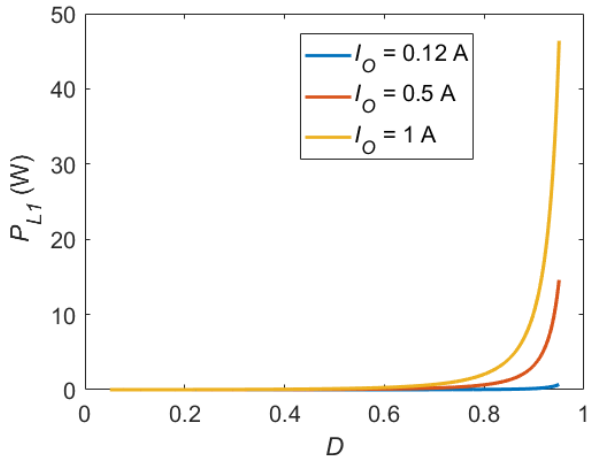

FIGURE 17. Inductor L_1 ESR power loss P_{L1} as a function of duty cycle D (with D ranging from 0.05 to 0.95) at V_O = 12 V.

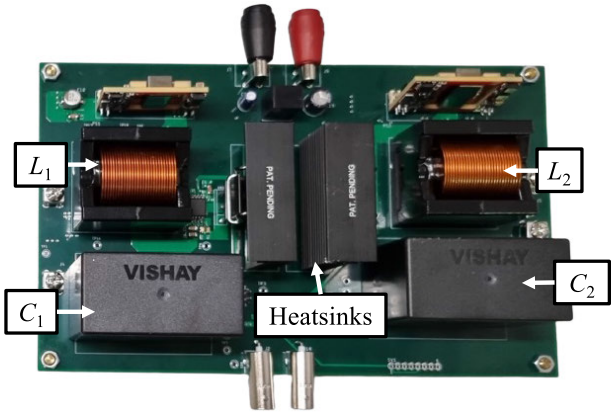

FIGURE 18. Designed, assembled, and experimentally tested circuit.

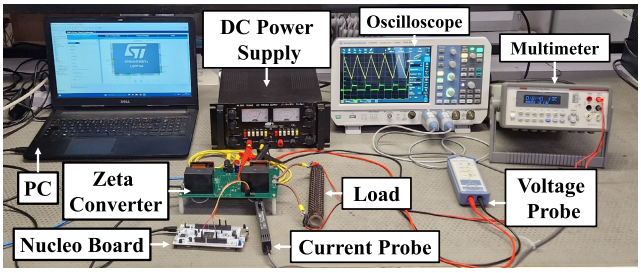

FIGURE 19. Experimental test setup.

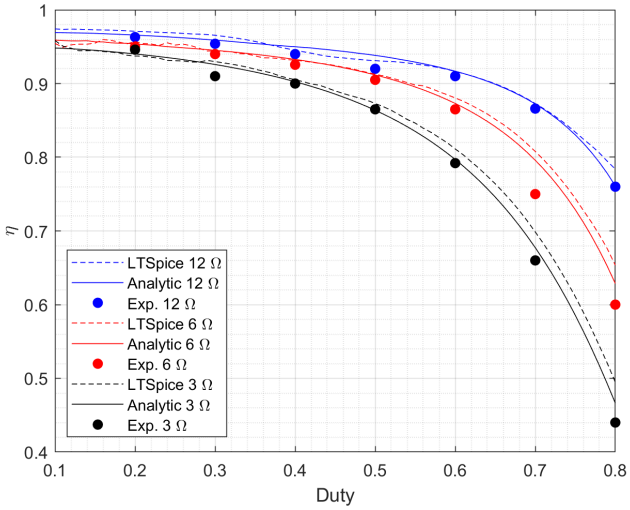

FIGURE 20. Converter efficiency at R_L = 12 Ω (Blue plots), R_L = 6 Ω (Red plots), and R_L = 3 Ω (Black plots). C Continuous line: analytical, dashed line: simulations, dots: experimental.

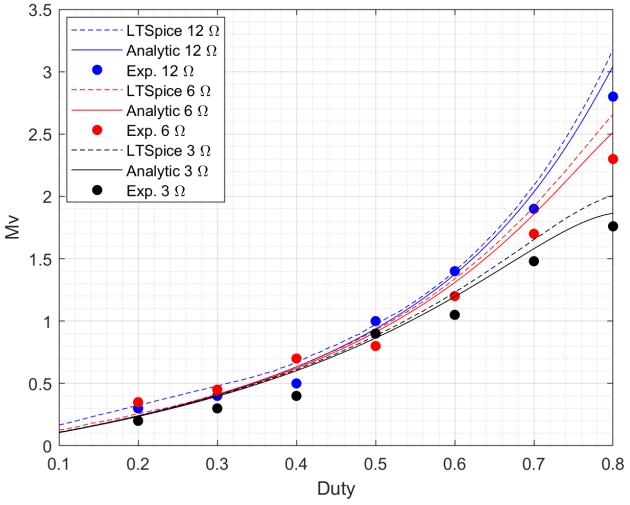

FIGURE 21. Converter dc voltage transfer function at R_L = 12 Ω (Blue plots), R_L = 6 Ω (Red plots), and R_L = 3 Ω (Black plots). Continuous line: analytical, dashed line: simulations, dots: experimental.

I_O = 0.12, 0.5, and 1 A, i.e., at R_L = 10, 24, and 12 Ω and P_O = 1.44, 6, and 12 W, respectively.

The switching frequency is f_s = 2 MHz Assuming that the converter efficiency is η = 90%, the duty cycle calculated from (30) is D_{min} = 0.473 at V_{Imax} = 15 V, and D_{max} = 0.599 at V_{Imin} = 9 V. It can be observed that the converter efficiency η is high for D in the range from 0.1 to 0.8, and it is low for D = 0-0.1 and D = 0.8-1. As D become close to 0 or 1, the term $1/D(1-D)$ present in P_{sw} approaches infinity and, therefore, the efficiency decreases to 0. Fig. 9 shows the converter efficiency, when the switching losses P_{sw} are neglected. In this case, the efficiency does not decrease at D = 0, but it still does at D = 1. Fig. 10 shows the converter efficiency when only stitching losses are considered, demonstrating that switching losses contribute to the efficiency reduction both at D = 0 and D = 1.

The converter efficiency η is depicted in Fig. 11 as a function of the load current I_O at V_O = 12 V and at three values of the dc input voltage V_I = 9, 12, and 15 V. As seen, the converter efficiency η linearly decreases when load current I_O is increased. It also decreases as the dc input voltage V_I decreases.

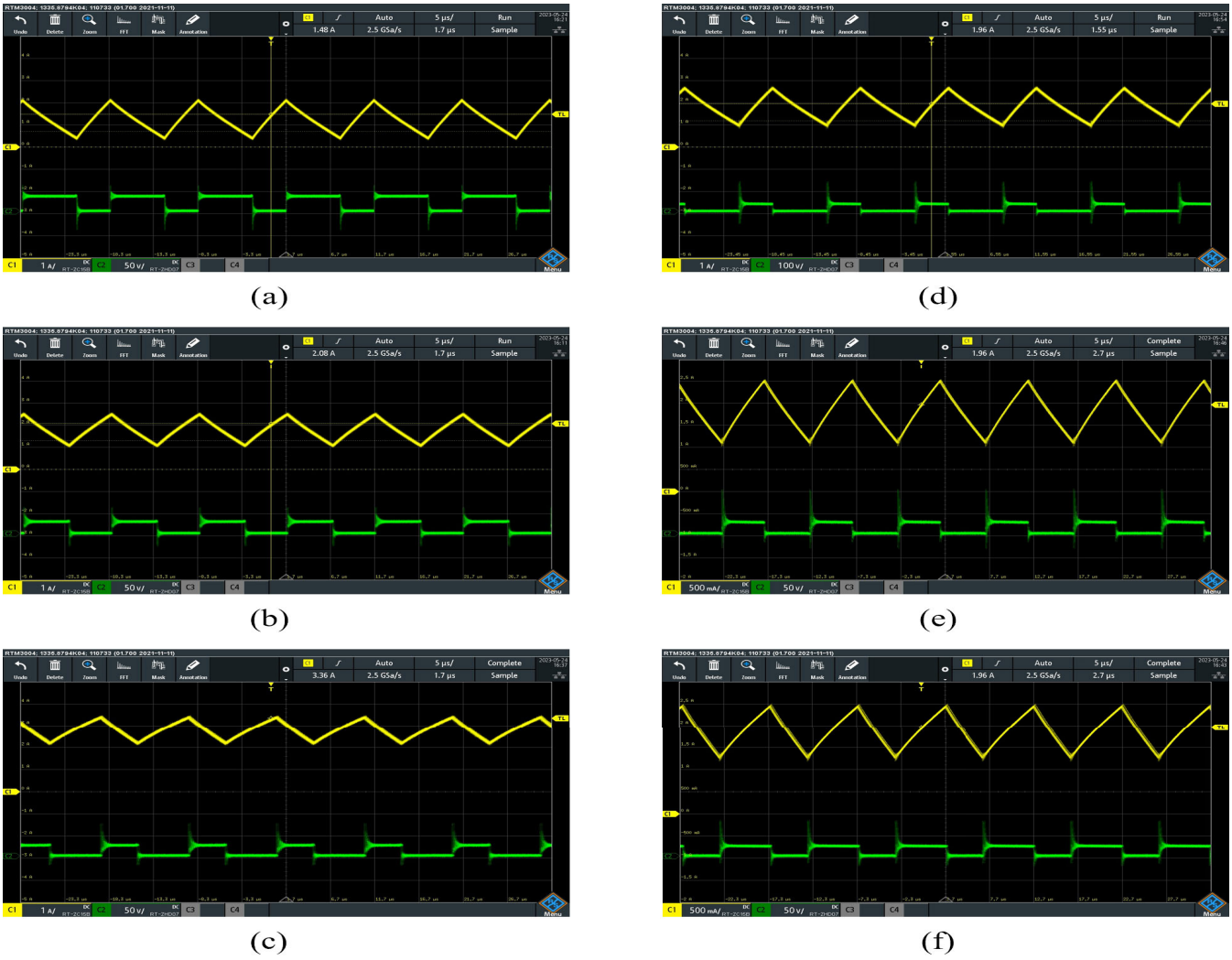

FIGURE 22. Experimental waveforms at $V_O = 12$ V, and $R_L = 6\ \Omega$. Horizontal axis, time, 10 μs/div. a) $D = 0.4$. Vertical axis: inductor i_{L1} current (1 A/div), upper trace; voltage across the mosfet v_S, lower trace. (b) $D = 0.4$. Vertical axis: inductor i_{L2} current (1 A/div), upper trace; voltage across the diode v_D (50 V/div). (c) $D = 0.5$. Vertical axis: inductor i_{L1} current (1 A/div), lower trace; voltage across the mosfet v_S (100 V/div), lower trace. (d) $D = 0.5$. Vertical axis: inductor i_{L2} current (1 A/div), upper trace, voltage across the diode v_D (50 V/div), lower trace. (e) $D = 0.6$. Vertical axis: inductor i_{L1} current (0.5 A/div), upper trace, voltage across the mosfet v_S (50 V/div), lower trace. (f) $D = 0.6$. Vertical axis: inductor i_{L2} current (0.5 A/div), lower trace; voltage across the diode v_D (50 V/div), lower trace.

Fig. 12 shows the converter efficiency η as a function of the load resistance R_L at $V_O = 12$ V and at three values of the dc input voltage $V_I = 9$, 12, and 15 V. The efficiency η increases as the load resistance R_L was increased and it is higher at higher voltages V_I.

Fig. 13 shows a comparison of the dc voltage transfer function M_{VDC} as a function of duty cycle D for three cases:

1) the loss-less converter with $V_O = 12$ V, $I_O = 1$ A ($R_L = 12\ \Omega$), and variable dc input voltage V_I,
2) the lossy converter with $V_O = 12$ V, $I_O = 1$ A ($R_L = 12\ \Omega$), and variable dc input voltage V_I,
3) for the lossy converter with $V_I = 12$ V, $I_O = 1$ A, and variable dc output voltage V_O.

For the lossy converter, the dc transfer function M_{VDC} is low for the duty cycle D close to 1. This is because the efficiency is low at high values of the duty cycle D.

IX. CASE STUDY, SIMULATION, AND EXPERIMENTAL RESULTS

A. EXPERIMENTAL CONVERTER DESIGN

To validate the theoretical derivations, a Zeta converter was designed according to the following design specifications and, then, simulated and experimentally tested. The converter was designed to operate at a minimum output power $P_{Omin} = 12$ W, a maximum output power $P_{Omax} = 48$ W, at a constant output voltage $V_O = 12$ V, for an input voltage ranging from $V_{Imin} = 10$ V to $V_{Imax} = 22.5$ V. Assuming the converter efficiency $\eta = 0.8$, according to (30), the duty cycle is in a range determined as follows:

$$D_{min} = \frac{M_{VDCmin}}{M_{VDCmin}+\eta} = \frac{12/22.5}{12/22.5+0.8} = 0.4 \tag{100}$$

and

$$D_{max} = \frac{M_{VDCmax}}{M_{VDCmax}+\eta} = \frac{12/10}{12/10+0.8} = 0.6. \tag{101}$$

The switching frequency $f_s = 100$ kHz was chosen and from (37), one can derive

$$L_{pmin} = \frac{0.125 \times 12}{100 \times 10^3 \times 12} = 1.25\ \mu\text{H}. \quad (102)$$

According to (39) and (40) assuming $a = 1$, the minimum value of the converter inductance is $L_{1min} = L_{2min} = 2.5\ \mu$H. According to (59), the voltage ripple $V_{C1pp} = 150$ mV was achieved if $C_1 = 47\ \mu$F. Similarly, according to [20] a capacitance $C_2 = 50\ \mu$F allows the output voltage ripple $V_{C2pp} = V_{Opp} = 100$ mV to be achieved.

B. SIMULATIONS AND EXPERIMENTAL RESULTS

The designed and tested circuit, is shown in Fig. 18, here, two inductors $L_1 = L_2 = 47\ \mu$H were utilized to achieve the CCM operation over the entire load range. Both the inductors were 7443763540470 devices with a rated current $I_L = 32$ A, a maximum inductor dc resistance $r_{DC(max)} = 6.38$ mΩ, and a self-resonance frequency $f_{self} = 6$ MHz. The capacitors utilized in the experimental circuit were two MKP1848S65050JYF ceramic devices with a capacitance $C_1 = C_2 = 50\ \mu$F each. The experimental circuit was built and the breadboard is shown in Fig. 18, which shows the inductors and te capacitors,,as well as the heat sink of the TP65H023WS power mosfet, which is an N-channel device, TO-247 package, GaN device with $V_{DS} = 650$ V, $I_D = 46.5$ A, and $r_{DS(on)} = 41$ mΩ, and that of the IDW40G65C5 device, which is a SiC Schottky diode, PG-TO247 package, with $V_{DC} = 650$ V, $I_F = 40$ A, and $R_F = 12.5$ mΩ. The circuit was both simulated with LT Spice and experimentally tested at $V_I = 22.5$ V, 15 V, and 10 V, which resulted in $V_O = 12$ V at $D = 0.4$, 0.5, and 0.6, respectively. The experimental set-up is shown in Fig. 19.

Fig. 20 shows the plots of the converter efficiency and Fig. 21 shows the plots of the dc voltage transfer function, according to the values resulting from the analytical derivation introduced in this paper, the LT Spice simulations and the measurements of the experimental circuit. The simulations and the experimental tests were performed at a constant output voltage $V_O = 12$ V, several values of input voltage, and a variable load, with $I_O = 1$ A, 2 A, and 4 A.

The theoretical derivation results were in agreement with those of simulations and experimental tests. According to theoretical derivations, the power losses increase at high values of D and, therefore, the efficiency become low when $D > 0.6$. The dc voltage transfer function is affected by losses only at higher values of the output current.

The waveforms of i_{L1}, v_S, i_{L2}, and v_D are plotted in Figs. 22 (a) and (b) at $D = 0.4$, in Figs. 22 (c) and (d), and in Figs. 22 (e) and (f) at $D = 0.6$.

X. CONCLUSION

The analysis of the non-isolated DC-DC PWM Zeta DC-DC PWM or steady-state CCM operation has been presented. The analysis gave insight on the electrical behaviour of the converter, expecially referring to the DC transfer function, losses due to parasitics and converter efficiency. A design procedure has been derived by using the equations to size the reactive elements, which have been derived and used to design a prototype of the converter. The theoretical results have been verified by simulations with LTSpice and experimental tests. The analysis on the losses and the efficiency highlighted that efficiency the power losses are high and the converter efficiency is low at the duty cycle D close to 0 and 1. At duty cycle D close to 0, switching losses are high, reducing the efficiency η while conduction losses are low. At duty cycle D close to 1, both the conduction and switching losses are high, reducing the efficiency η and the voltage conversion ratio M_{VDC}. The Zeta converter topology can be used in place of buck and boost cascaded converters to achieve a dc output voltage lower and higher than the dc input voltage. Moreover this converter is extremely useful due to its ripple distribution in PV and SC related applications. Therefore, the derived equations and dependencies are a key asset for the correct sizing of an energy conversion system when high efficiencies are mandatory as in energy harvesting scenarios.

Finally, the complete circuit analysis of this converter represent the base for the development, as a future work, of the converter small-signal models, applicable in the design of the converter control circuit and also for the development of specific applications such as maximum power point tracking for photovoltaic sources or dynamic current adjustment for supercapacitors DC links.

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