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RESEARCH ARTICLE

Multi-Channel Step FinFET With Spacer Engineering

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ABSTRACT Multi-channel FinFET (M_{ch}-FinFET) is an emerging device having promising use due to its excellent driving capability. In this paper, we have investigated the significance of multiple channels of FinFET configuration. We have examined the performance of the multi-channel-based step FinFET (M_{ch}- step FinFET) structure with spacer engineering. The results obtained from this simulation work indicate that M_{ch}-step FinFET is a good competitor for future improvisation of CMOS technology. The proposed device has improved drain conductivity, transconductance (G_m), intrinsic gain (A_v), and drain conductance (G_d) performance by introducing high-K dielectric spacer material by 38.2%, 46.12%, 88.57%, and 22.55%, respectively. The proposed device with a spacer is preferable to obtain better performance regarding ON current and device efficiency.

INDEX TERMS Semiconductor device, short channel effect (SCE), subthreshold swing (SS), bipolar junction transistor (BJT).

I. INTRODUCTION

The The prime member of today's semiconductor industry, MOSFET (metal oxide semiconductor field effect transistor) failed to maintain its immunity against the industry's primary objective: down-scaling electronic devices. Therefore, the semiconductor industry is searching for an alternative to the MOSFET, which overcomes the problems of MOSFET and withstands the negative impacts of down-scaling [1]. With down-scaling of device attributes, various undesired side effects are experienced, called non-deal effects or short channel effects (SCEs) [2]. A few non-ideal effects in MOSFET are subthreshold swing (SS), drain-induced barrier lowering (DIBL), variation of threshold voltage (V_{th}), leakage current, tunneling current, and channel length modulation, mobility variation, velocity saturation, etc. Such effects have led to serious concerns for MOSFETs as the industry proceeds for smaller dimensions. To optimize these SCE problems, researchers developed various kinds of modified MOSFET architectures mainly operated in high-frequency applications. Many researchers have proposed various novel devices that fulfill the semiconductor industry's current requirements in the last many years. Various updated MOS structures have been suggested to enhance efficiency, including dual gate (DG), surrounding gate (SG), and independent-gate (IG) MOSFET designs [3].

Fin-shaped Field Effect Transistor (FinFET) is a 3D [4], a multi-gate-based device where the channel is covered by a thin layer called 'Fin'. The gate overlaps the 'Fin', forming three self-aligned channels along the top and vertical sides of the Fin. Compared to planar transistors, FinFET operates at a lower voltage and offers a higher drive current. FinFET is a new technology that allows further channel length scaling, which was impossible by the single gate-based MOSFET device.

It was also noticed that the complexity, cost, and power consumption of these single channel-based FinFET (conventional FinFET) increase rapidly with lesser dimensions, reducing their reliability. However, various modified FinFET devices have been proposed by researchers to overcome the issues in conventional FinFET. The scaling of Fin width helps to recover the degradation of short channel parameters due to high-k integration. Das et al. [5] proposed a triple material gate (TMG) step FinFET to analyze the stress effect on device

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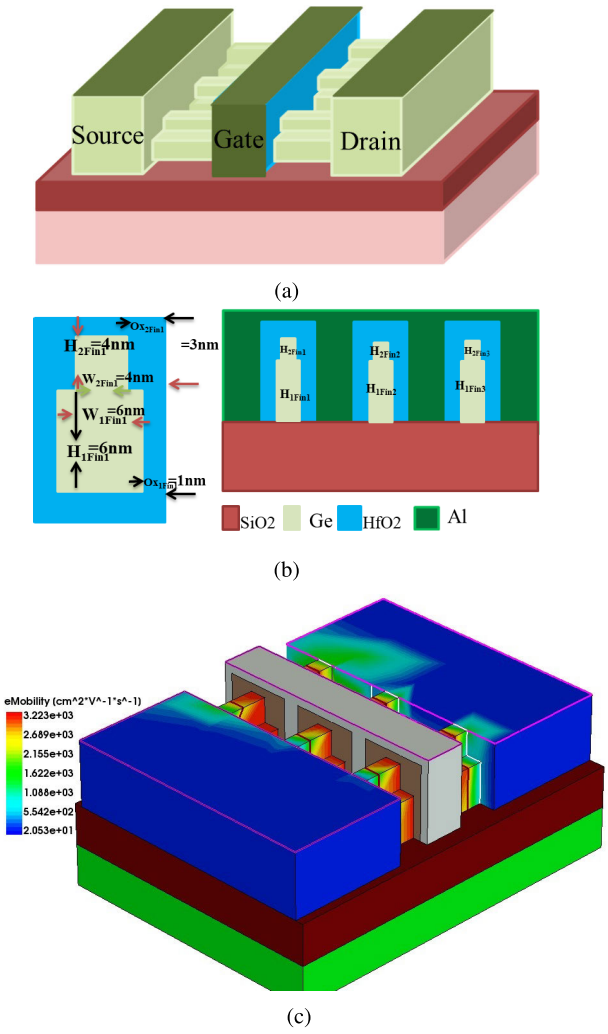

FIGURE 1. M_{ch}- step FinFET structure is illustrated in (a) a 3D view, (b) a 2D cross-section view, and a front view with dimensions, and (c) a simulated view.

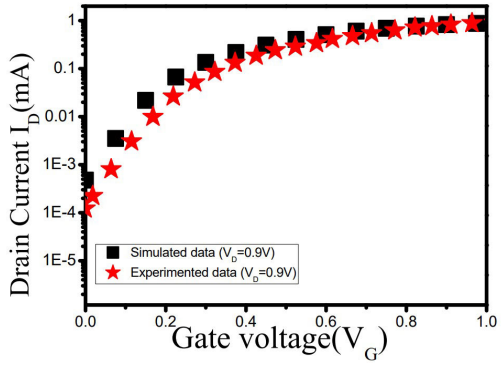

FIGURE 2. (a) Calibration of simulated result with experimental data.

performance. In TMG FinFET, the surface potential is higher than the conventional FinFET, which reduces the electric field effect at the drain end and enhances the driving current.

Saha et al. [6] introduced a step FinFET configuration incorporating both Si and Ge as channel materials. The study includes a comprehensive comparison of different device output metrics. It is concluded that the Ge-based step FinFET structure outperforms its Si counterpart, showcasing superior ON current, switching ratio, and lower intrinsic delay.

In 2019, Chakkikavil et al. proposed [7] a wavy FinFET structure, which is the combination of FinFET and ultra-thin Body FET structure on SOI (silicon on insulator) substrate. This innovative design seamlessly combines the benefits of both FinFET and ultra-thin Body FET structures on an SOI substrate. The wavy FinFET not only enhances current-driving capabilities but also maximizes device density without compromising spatial efficiency. The research also delved into various optimization strategies, including gate engineering, work-function engineering, and spacer engineering, to address issues such as leakage current and lower threshold values. Remarkably, the proposed device, incorporating these channel engineering techniques, achieved a substantial reduction in leakage current by approximately 40%, while a lower gate work-function contributed to a significant 35.48% reduction in leakage current.

Medury et al. [8] discussed the various short channel characteristics such as threshold voltage, DIBL, and SS for fully depleted (FD) underdoped symmetric SOI FinFETs. The impact of channel length and drain bias on the proposed device is studied by considering semi-classical and quantum confinement circumstances. It is demonstrated from this work that the performance of SCEs parameters is optimized considering the semi-classical case than quantum confinements. Narendar and Mishra [9] has designed a rectangular gate-all-around (RE-GAA) FinFET. Poisson's equation derives the proposed model along with boundary conditions.The model presents the electrostatic potential, SS, DIBL, on current, and off current. A good accuracy can be noticed in the proposed model with simulated results. Kumar [10] presents a gate-all-around (GAA), triple-gate (TG), and double-gate (DG)) FinFETs model which are solved by Poisson's equation. It is observed that GAA FinFET channel potential has shown better electrostatic control than other structures. The most comfortable way to evaluate the performance of any FinFET geometry in-circuit application is to realize a digital inverter, the fundamental building block of every digital circuit. Vallabhuni et al. [11] analyzed the 18nm FinFET technology-based 6T SRAM cells to optimize the leakage current and compared it with standard conventional MOSFET. The abovementioned structures have a single Fin where multiple numbers of Fins increase the number of channels, consequently expanding the total effective channel width. Presently, researchers are demonstrating interest in constructing FinFET devices based on multiple channels or Fins, known as Multi-Fin FinFET. References [12] and [13] configuration is the updated FinFET device where multiple Fins are placed in between the source and drain regions. To the authors' best knowledge, the multi-channels step FinFET (M_{ch} step FinFET) device structure is not explored yet.

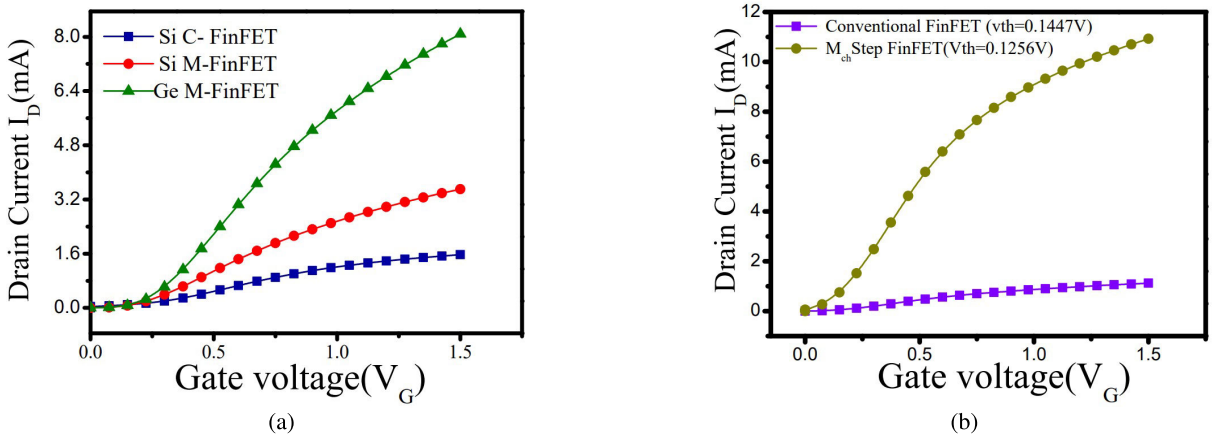

FIGURE 3. (a) Drain current performance of conventional FinFET, Si Multi-Fin FinFET (M-FinFET), and Ge Multi-Fin FinFET (b) Drain current performance of conventional FinFET and M_{ch}-step FinFET.

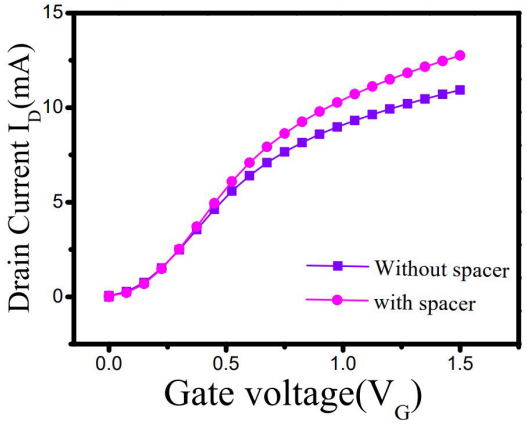

FIGURE 4. Transfer characteristics of proposed M_{ch}- step FinFET in presence and absence of spacer.

TABLE 1. Analytical comparison of the proposed device with existing Ge-based FinFET structures.

References	Device structure	Parameter	Output performance
Vandal *et al.* [14]	Ge n FinFET	L_g=40nm	I_{ON}=0.5mA,
Bansal *et al.* [15]	negative capacitance (NC) Ge FinFET	L_g=20nm	I_{ON}=0.01mA,
Thirunavukkarasu *et al.* [16]	Ge junctionless FinFET	L_g=3nm	I_{ON}=1 mA,
Proposed work	Ge M_{ch} step FinFET	L_g=7nm	I_{ON}=10.92mA

On the other hand, spacer engineering is very significant in reducing the gate tunneling problem. High K-dielectric materials help to minimize the surface roughness scattering of the device [17]. Sreenivasulu and Narendar in 2020, proposed [18] 5nm gate length based tri-gate (TG) FinFET device, and the impact of spacer engineering are discussed to observe the RF/analog performance. The spacer has increased the distance between the source and drain contact terminals reducing the ON current. However, the introduction of a high K spacer enhances the ON current. The single spacer has fringe capacitance components that degrade the output performance. The exploration of dual-k spacer yields intriguing results, showcasing a reduction in parasitic capacitance and an enhancement in both I_{ON} and subthreshold characteristics. This effect is achieved through the innovative integration of an inner high-k spacer with an outer low-k spacer. Vandana et al.in 2021, [19] present a systematic discussion regarding the importance of high-k spacer on inverted (IT) junctionless (JL) FinFET devices. The proposed structure IT JL FinFET device implements the RF/analog performance in the presence of temperature variation. This simulation work concludes that the proposed structure with high-k spacer materials improves the RF/analog performance with optimum SCEs parameters.

Biswas et al. [20] analyzed the electrical characteristics of junction-less accumulation mode (JAM) bulk FinFETs. The importance of various spacer materials and their length on the performance of JAM bulk FinFETs are studied. It is observed from this simulation study that high-k dielectric spacer materials improve the analog and RF performance, and the increased value of spacer length optimized the various short channel effects performance.

A symmetric high-k spacer hybrid FinFET structure is proposed by Pradhan et al. [21] to improve the performance. Hybrid FinFET combines the ultra-thin body (UTB), three-dimensional FinFETs, and high-k spacer, which is developed on SOI technology. It is understood that the proposed device exhibits more remarkable performance in drain current over conventional FinFET and mitigates the short-channel effects as much as possible. Sharma et al. [22] analyzed the importance of a high K spacer on the underlap SOI device and showed that SOI device with high K spacer increases the ON current and gate capacitance. To the best knowledge of the authors, no research to date studied the impact of the spacer of the multi-channel step FinFET, which would be very useful for CMOS technology.

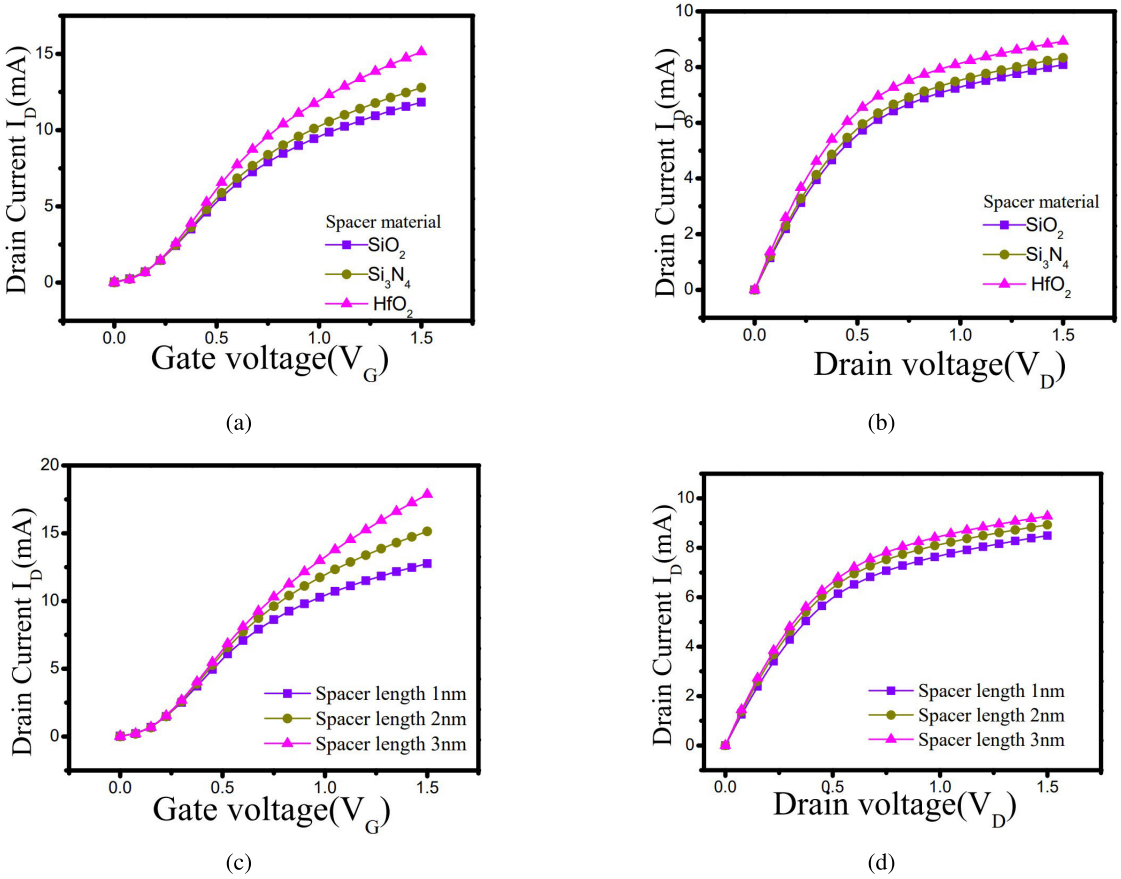

FIGURE 5. Drain current performance with respect gate and drain voltage of M_{ch}-step FinFET for (a) & (b) variation of spacer material (c) & (d) for variation of spacer material length.

This paper's main contribution is to develop a new design of FinFET to improve the device's performance, which would be beneficial for low-power applications. We have introduced a 'Multi-channel step FinFET' architecture to study the significance of spacer material.

The research paper is organized into the following sections: Section II details the proposed structure, including dimensions, and outlines various activated models used for the simulation study. In Section III, the simulation performance is thoroughly discussed. The paper concludes with Section IV, offering final observations.

II. PROPOSED DEVICE AND ANALYSIS

The proposed structure's 3D cross-sectional view has been presented in Fig. 1a. The front view with dimensions and 3D simulated view of a single Fin are shown in Fig. 1b and 1c. In the multi-channel step FinFET, three parallel Fins with similar measurements are taken between the source and drain region. Fin spacing is to be considered 4nm. Germanium (Ge) is regarded as a channel material. To control the channel, aluminum (Al) as gate material is taken instead of poly-silicon, and its thickness is supposed to be 1nm. SiO_2 dielectric material is accounted for buried oxide material whose thickness is 10 nm and height is 15nm. The length of the gate is to be considered 7nm, whereas the length of the source/drain is assumed to be 15nm. A lower gate length value (=7nm) reduces the surface roughness scattering in the device, enhancing the drain current. The source and drain regions are enriched with arsenic impurities at a concentration of 10^{20} cm^{-3}, while the channel region incorporates Boron impurities with a concentration of 10^{17} cm^{-3}. To address mobility degradation, the channel region is lightly doped. Since we have proposed the step FinFET structure, introduces a non-uniform Fin, resulting in different Fin height/width at the upper and lower parts. The height of the Fin at lower and upper sections (H_1Fin1, H_2Fin1) is considered 6 nm and 4 nm, and the Fin width at lower and upper sections (W_1Fin1, W_2Fin1) is to be assumed 6 nm and 2 nm. The thickness of oxide at the lower and upper areas (ox_1Fin1, ox_2Fin1) is considered 1 nm and 3 nm. The calibration of the TCAD model with experimental data in [14] is shown in Fig. 2. The proposed structure was placed on Synopsys's 3D simulator tool Sentaurus TCAD provider with proper biasing [23]. When dealing with nano-scale device structures, different models must be utilized to conduct simulation studies effectively. The carrier transportation is modeled using the Boltzmann transport model and the drift-diffusion model. To address mobility impact in the source/drain

region, Phonon scattering, and Coulomb scattering models are incorporated. The mobility Masetti model is used to study the mobility effect. The Shockley-Read-Hall (SRH) model is activated to capture recombination and generation processes. The high field saturation model is considered to examine the velocity saturation effect. The Old SlotBoom model is applied for the doping profile. Additionally, the quantum density gradient model is employed to incorporate the quantization correction effect.

III. RESULTS AND DISCUSSIONS

In this section, we study the impact of multiple channels and the significance of spacer material to evaluate the DC/analog performance. Throughout the entire simulation study, a drain-to-gate voltage of 0.5V is employed.

The drain current performance among Si conventional FinFET (Si C-FinFET), Si multi-Fin FinFET (Si M-FinFET), and Ge multi-Fin FinFET (Ge M-FinFET) is summarized and illustrated in Fig. 3a. The C-FinFET features a single channel, while a M-FinFET incorporates three Fins, effectively increasing the device's channel width.The other attributes of C-FinFET and M-FinFET are considered to be constant. Observations reveal that the driving current in Ge M-FinFET is amplified by 4 times compared to C-FinFET and 2.5 times compared to Si M-FinFET. The subthreshold swing (SS) value of Ge M-FinFET also shows improvement over the C-FinFET device. The increased number of Fins (channels) facilitates a greater electron flow from the source to the drain, enhancing the coupling effect with nearby Fins.

A comparative analysis of the proposed structure is conducted in comparison to other existing Ge-based structures, both fabricated and simulated, as summarized in Table 1. Based on the findings from the literature survey on Ge-based FinFET devices, it is evident that Ge-based M_{ch}-FinFETs have the potential to emerge as strong contenders within the semiconductor industry.

Fig. 3b shows the drain current performance of conventional FinFET (C-FinFET) with single Fin and Multi-channels step FinFET (M_{ch}- step FinFET) with 3 Fins. It is observed that M_{ch}- step FinFET exhibits more drain current than the conventional FinFET. The step FinFET presents distinct advantages over the conventional FinFET by incorporating a non-uniform oxide thickness and Fin width. The strategic implementation of Inconsistent oxide thickness significantly diminishes leakage current, particularly with a thicker thickness at the upper portion. However, the gate has less control over the channel owing to the higher width of the oxide layer. Conversely, the increase in gate controllability on the channel, made possible by the lesser Fin width, is more pronounced, ultimately enlarging the device's driving efficiency.

Fig.4 demonstrates the comparison of drain current characteristics of M_{ch}- step FinFET in the presence and absence of spacer where HfO_2 as spacer material used. It is observed that the device with HfO_2 spacer shows a better performance compared to without spacer. This is due to the increase of coupling effect between the gate and source/drain region that reduces the series resistance. The spacer in a device provides a large electric field with minimum leakage current.

The drain current performance for various spacer materials is shown in Fig. 5a and 5b. SiO_2, Si_3N_4, and HfO_2 are different dielectric materials considered spacers or sidewalls where spacer length is considered 2nm.

As the device dimensions scale down, these parasitic capacitances and resistances increase, contributing significantly to the overall capacitance of the nanoscale device. The increased value of parasitic capacitances and resistance enhanced the propagation delay, and leakage current. By introducing a spacer, these parasitic capacitances and resistances are reduced by creating more physical space between voltage terminals. The introduction of the spacer has increased the gate controllability. However, the insertion of a spacer between the source/drain and the gate induces a high resistance that negatively impacts the device's performance. To address this issue, high-k spacers are implemented to enhance I_{ON} and this phenomenon is known as fringe-induced barrier lowering [24]. Introducing symmetric dual K-spacers on both channel sides has significantly improved device characteristics. It is observed that the M_{ch}- step FinFET device with HfO_2 spacers improved the drain current performance linearly with increasing gate bias and drain bias. The high k spacer HfO_2 increased the gate fringe electric field, reducing the series resistance and allowing more charge carriers to flow from the source to the drain region. The performance can be further improved by varying the spacer length. The drain current performance has been observed by varying the gate and drain bias for spacer length variation shown in Fig. 5c and 5d. The length of the spacer is varied while keeping the spacer as HfO_2. It is noticed that the higher length of HfO_2 spacer offers more drive current with maximum saturation current.

Analog attributes such as transconductance (G_m), drain conductance (G_d), transconductance gain factor (TGF) or device efficiency, and intrinsic gain (A_v) that play a crucial role in achieving high-efficiency device performance shown in Fig. 6.

The performance of G_m for various spacer materials is shown in Fig. 6a. Transconductance is defined as the ratio of the change in drain current (dI_D) to the change in gate-source voltage (dV_{GS}), is a crucial parameter for assessing the sensitivity of a transistor and its ability to be controlled by the gate voltage. It is evident from the observation that the transconductance exhibits a consistent rise with an increase in the gate bias, reaching a point where it experiences a sudden decline in the saturation region, primarily attributed to mobility degradation.

Drain or output conductance (G_d) is primarily employed to measure the gain of the device and assess its driving capability. A high drain conductance delivers a larger output current for a given change in the input voltage, which is desirable in many applications. In the linear region, the

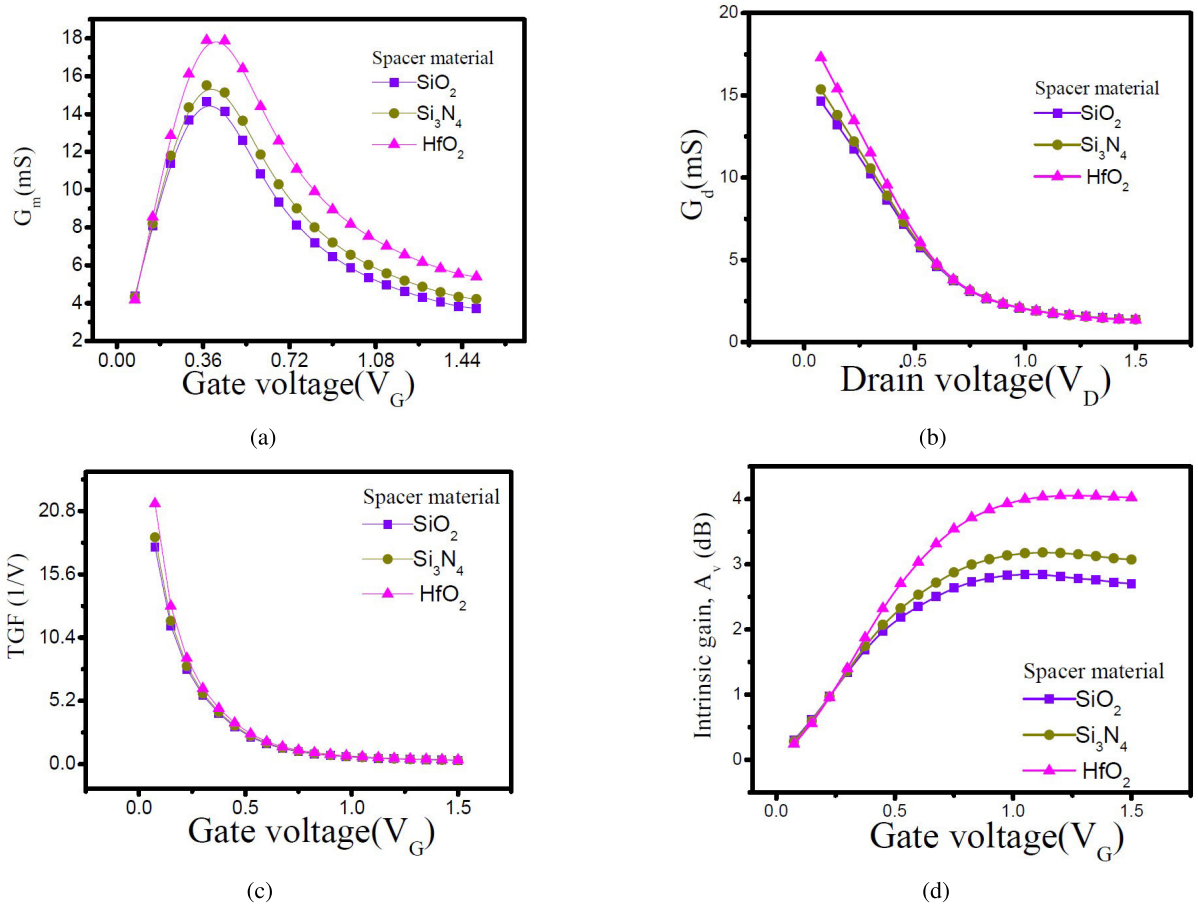

FIGURE 6. Analog performances of M_{ch}-step FinFET (a) transconductance (G_m) (b) drain conductance (G_d), (c) transconductance gain factor (TGF) and (d)intrinsic gain (A_v)for variation of spacer material.

G_d value is notably high but decreases as drain voltages exceed the pinch-off voltage. In the saturation region, the performance of G_d remains consistent across all FinFET variations as shown in Fig. 6b.

Another significant analog parameter to consider is the TGF, represented as TGF $= G_m/I_D$. TGF is sometimes referred to as device efficiency since it quantifies how effectively the current (I_D) is utilized to achieve a specific transconductance value (G_m). The peak TGF value is typically achieved in the weak inversion region, where the reduction in drain current owing to lower gate voltage is more noticeable than the increase in G_m. As a result, the TGF value is highest at lower gate voltage, and HfO_2 spacer material offers maximum TGF compared to other materials as shown in Fig.6c. A high TGF indicates that the device is more sensitive to changes in the input voltage, resulting in a larger output voltage for a given change in the input voltage. This is desirable in many amplifier applications, providing a high gain.

On the other hand, intrinsic gain, denoted as A_v and calculated as the ratio of transconductance to output conductance [2], is a critical parameter. Maximizing the intrinsic gain involves increasing G_m while decreasing G_d. HfO_2 spacer has improved A_v as compared to other spacer materials as shown in Fig. 6d.

The various DC/analog attributes performances are shown in Fig.7. The peak performance of G_m, TGF, G_d, and A_v is depicted, both with and without the presence of spacer material shown in Fig.7a. Notably, the inclusion of HfO_2 spacer material results in significant enhancements in analog characteristics, with G_m, G_d, TGF, and A_v experiencing improvements of 46.12%, 22.55%, 23.24%, and 88.57%, respectively. Observation also revealed that the M_{ch}-step FinFET with HfO_2 spacer has enhanced ON current. Furthermore, the switching ratio performance in the presence and absence of spacer materials is shown in Fig.7d. The ON/OFF ratio called the switching ratio is an essential figure of merits (FOMs) that should be high for better switching speed. It is seen that the proposed device with HfO_2 spacer has an optimum value of switching ratio due to a maximum value of OFF current that decreases the ON/OFF ratio. And device provides a higher threshold voltage with HfO_2 spacer that has improved by 60.1%. Fig. 8 has shown the transit frequency performance with respect to gate voltage of M-step FinFET. Transit frequency, or 'cut-off' frequency, fT, is a measure of a transistor's intrinsic speed. The transit

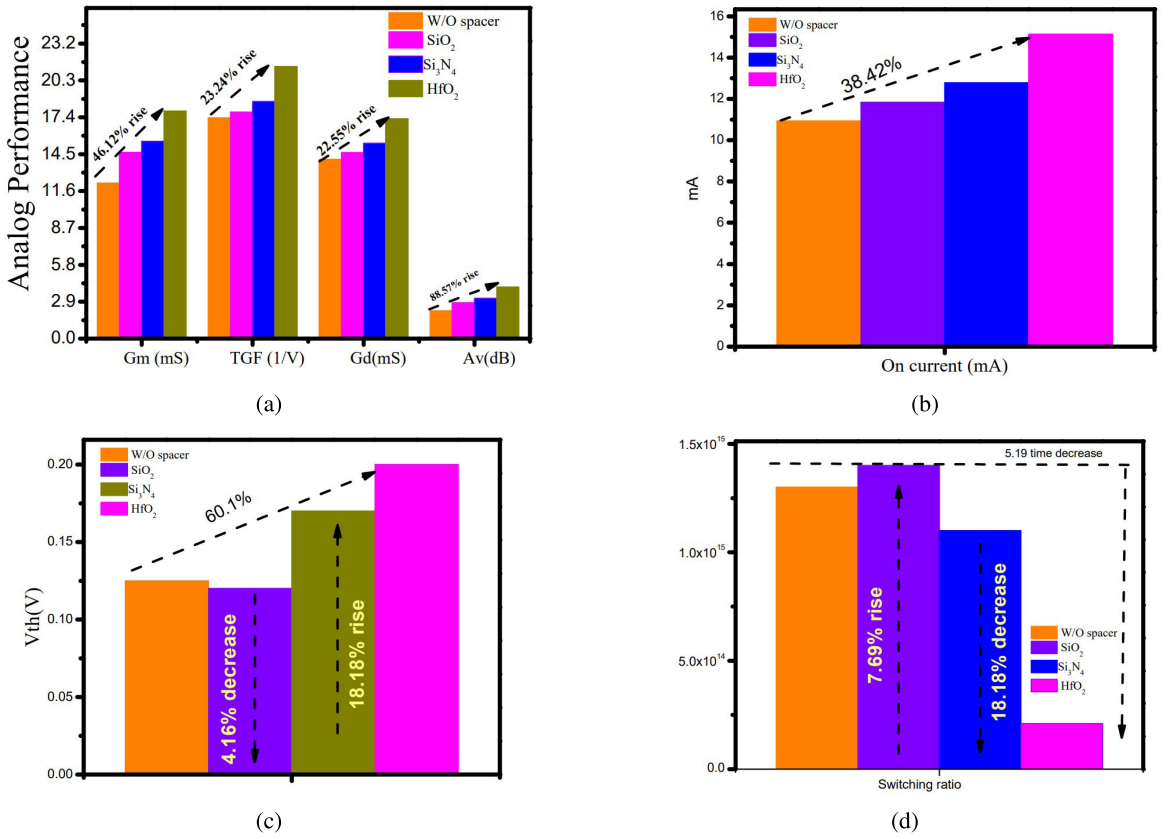

FIGURE 7. M_{ch}- step FinFET structure (a) Analog performances (b) ON current (c) V_{th} (d)Switching ratio for variation of spacer material.

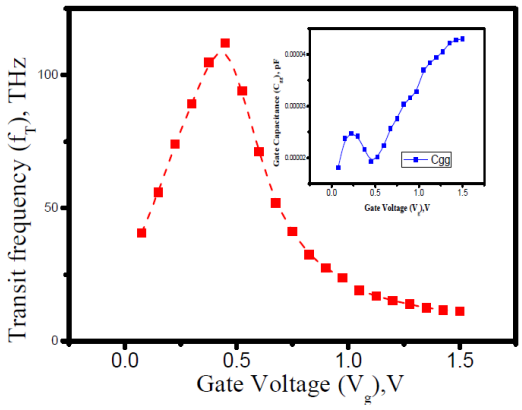

FIGURE 8. Transit frequency of M_{ch}-step FinFET.

frequency [25] can be determined by

$$f_T = G_m/2\pi C_{gg} \quad (1)$$

Transit frequency is influenced by its gate-source capacitance (C_{gg}) and transconductance (G_m). When C_{gg} increases, the impact on f_T is more significant compared to the decrease in G_m, leading to a reduction in the transit frequency.

A comparative analysis of various output performances concerning various device parameters is shown in Table 2. It is concluded that the higher value of Fin width has increased the ON current and transconductance performance. The increased ON current and transconductance have improved the device efficiency (TGF). However, intrinsic gain performance degrades due to higher value drain conductance with higher Fin width. On the other hand, the larger Fin height also improves I_{ON} and G_m leading to a high TGF value. An increase in the Fin width/Fin height leads to a reduction of the threshold voltage that improves the leakage current. It is also observed that an increase in temperature degrades the performance in terms of ON current and G_m which degrades the analog performances. Increasing channel doping reduces the drain current (ON current) owing to mobility degradation by impurity scattering. On the other hand, the enhanced value of doping concentration in the source/drain region increases the drain current, switching ratio, and analog performance.

We are comparing how well our proposed structure performs with other FinFET devices, both single and multi-Fin (channel), and the results are tabulated in in Table 3. We have also included all the references along with their normalized device sizes. The table concluded that the proposed device outperforms others in terms of ON current, SS, and switching ratio, making it promising for future CMOS technology.

TABLE 2. Comparative analysis of various performance matrices of Ge multi-channel step FinFET (W_1 = Fin width of the lower section, W_2 = Fin width of the upper section, H_1 = Fin height of the lower section, H_2 = Fin height of the lower section, N_A = doping concentration of channel region, N_D = doping concentration of source/drain region, spacer material: HfO_2, spacer length:3nm.

Device Parameters	Dimensions/values	I_{ON}, mA	G_m (Max) mS	TGF, V-1	G_d (max) mS	A_V, dB	V_{th}	Switching ratio
Fin Width	W_1= 8 nm, W_2=4 nm	24.48	23.9	16.75	23.93	5.22	0.1542	262.09
	W_1=10nm W_2=6 nm	30.11	29.2	13.18	29.73	3.97	0.144	135.63
Fin Height	H_1=6nm, H_2=2nm	18.28	19.9	21.37	19.35	5.31	0.154	$1.33x10^{15}$
	H_1=8 nm, H_2=4 nm	19.91	22.1	18.21	21.04	5.03	0.137	$1.71x10^{15}$
Temperature (T)	400K	16.17	15.2	11.76	16.27	5.02	0.118	$1.63x10^{11}$
	500K	11.84	10.7	8.99	12.27	4.72	0.083	$6.18x10^{8}$
Doping concentration, (cm-3)	$N_A=10^{15}$, $N_D=10^{19}$	1.17	2.29	19.40	2.84	10.14	0.093	$9.25x10^{11}$
	$N_A=10^{17}$, $N_D=10^{20}$	4.55	5.38	22.64	5.15	6.21	0.146	$4.56x10^{12}$

TABLE 3. Comparative analysis of Ge multi-channel step FinFET with other single and multi-channel (Fin) FinFET devices.

References	Device structure	Parameter performances
Das *et al.* [25]	Ge M_{ch} FinFET	I_{ON}=8.08mA, SS=85mV/dec, V_{th}=0.249V,switching ratio=$1.36x10^{15}$, G_{mpeak}=8.7mS, At L_g=10nm T_{ox}=1nm and V_D=0.5V T=300K
Hirapara *et al.* [26]	Multi-Fin FinFET, Si as channel	L_g=30nm T_{ox}=1.5nm,V_D=0.5V, Φ=4.5eV, SS=79.92mV/dec, V_{th}=0.39V, I_{ON}=0.01mA
Vasanthan *et al.* [27]	Ge Junctionless FinFET	L_g=3nm, I_{ON}=1mA, DIBL= <10mV/V. SS= 64mV/dec,V_{th}= 0.31V, V_D=0.7V
Myoungsu *et al.* [28]	SOI-u-shaped FinFET,Si as channel material	L_g=16nm,V_D=0.7V,EOT=1.05, I_{ON}=0.1mA G_{mpeak}=0.65mS,TGF=$40V^{-1}$
Ajay *et al.* [29]	GaN SOI FinFET structure (ZrO_2: dielectric constant and GaN as channel)	L_g=8nm,T_{ox}=1nm, V_D=0.1V,V_{th}=0.6V, I_{ON}=0.9mA,switching ratio=1.2x, 10^9 G_{mpeak}=0.9mS,TGF=$135V^{-1}$, SS= 75mV/dec
Bhavya *et al.* [30]	GAA FinFET(Si as channel,TiN as gate material, HfO_2+SiO_2 as dielectric constant)	L_g=7nm, T_{ox}=1nm I_{ON}=0.19mA, V_D=0.5V, T=300K, SS=105mV/dec, V_{th}=0.39V, switching ratio=1.2x, 10^4, G_{mpeak}= 0.037mS, TGF= $45V^{-1}$
Proposed work	Ge M_{ch}-step FinFET	I_{ON}=10.92mA,SS=67.1mV/dec, G_{mpeak}=14.48mS, $I_{ON/OFF}$=$9.4x10^{14}$ At L_g=7nm T_{ox}=1nm and V_D=0.5V, T=300K

There are several practical implications for using the proposed device for building circuits. Reducing leakage currents with better electrostatic control can improve the performance of various logic circuits. For example, the switching performance of the ring oscillator and SRAM can be improved with Multi-channel step FinFET technology. The multi-channel FinFET configuration has better electrostatic control capability with less leakage current than conventional FinFET. The performance improvement of ring oscillator circuits has a direct implication in designing PLLs that make extensive use of ring oscillators and are used in a wide range of applications. SRAMs find use in in-memory computing, and improvements in switching performance can improve the inference performance of neural networks implemented with such devices.

IV. CONCLUSION

This work introduced a new configuration called germanium (Ge) based M_{ch}-step FinFET to enhance the driving capability more efficiently. M_{ch}-step FinFET device improved ON current by 8 times compared to conventional FinFET. It is found that the proposed device with spacer engineering improved drain conductivity and other DC/analog performance. Analog attributes such as G_m, G_d, TGF, and A_v has enhanced by 46.12%, 22.55%, 23.24%, and 88.57%, respectively.

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