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RESEARCH ARTICLE

Phase Locked-Loop Design of High-Order Automotive Frequency Modulated Continuous Wave Radar Based on Fast Integration Structure

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ABSTRACT In recent years, frequency-modulated continuous-wave (FMCW) radars have been widely used in the automotive field to measure the relative distance and speed of external targets. To address the problems of poor sensitivity, narrow measurement range, and poor stability of current FMCW radar systems, a high-order all-digital phase-locked loop (ADPLL) based on a fast-integration structure was designed for the FMCW radar. According to the measurement principle of the distance and velocity of objects using radar, the loop structure was designed using integrated circuit chip technology. A Z-domain model of the loop system was built using MATLAB software, and stability analyses and comparisons were performed. The loop program was written using the hardware description language and simulated using the MODELSIM software. Simulation results were combined to verify the accuracy of the hardware design. The experimental results showed that the ADPLL effectively increased the phase-locking frequency, expanded the frequency modulation range by nearly ten times, reduced the system delay by approximately 36%, and improved system stability.

INDEX TERMS Frequency modulated continuous wave radar, fast integration, high-order all-digital phase-locked loop, integrated circuit.

I. INTRODUCTION

Automotive radar (AR) is one of the most promising technologies for automotive safety applications, whereas phase-locking technology is the main obstacle to AR development [1], [2], [3]. In recent years, phase-locked loop (PLL) technology has made remarkable progress through continuous exploration by domestic and foreign scholars. Traditional digital phase-locked loop systems aim to obtain stable oscillation control data using a loop filter with low-pass characteristics. For high-order all-digital phase-locked loops, digital filters often use DSP-based arithmetic circuitry. When the loop bandwidth is narrow, the implementation of the loop filter requires a large amount of circuitry, which creates certain difficulties in the application of application-specific integrated circuits and the design of system-on-chip (SoC) systems [4], [5], [6], [7]. Another type of all-digital phase-locked loop uses a pulse-train low-pass filter counting circuit as a loop filter, such as a random wandering sequence filter or an N before M sequence filter [8], [9], [10]. These circuits obtain the oscillation control parameters of the controllable oscillator module by counting the phase-error

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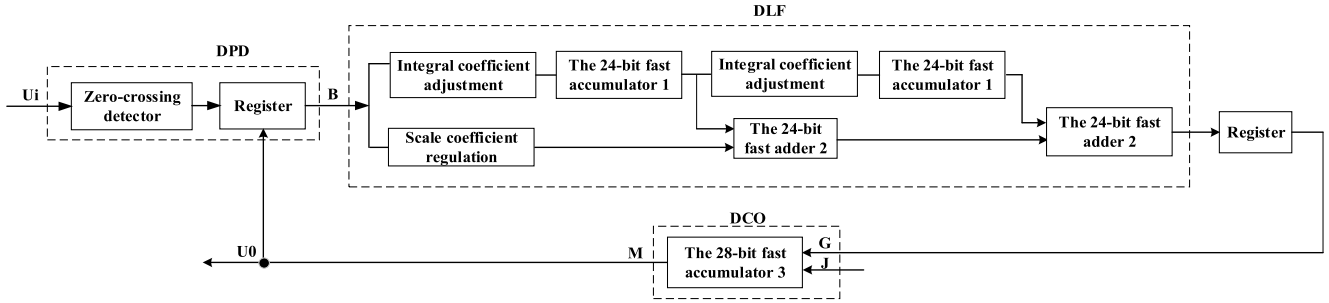

FIGURE 1. Third-order PI ADPLL plot based on fast integration structure.

pulses generated by the module [11]. Because the pulse train low-pass filter counting method is a relatively complex nonlinear processing method, it is difficult to make a linear approximation. Therefore, the analysis method of the system transfer function cannot be used to determine the design parameters of the phase-locked loop, and the decoupling control and analysis of the high-order digital phase-locked loop performance indicators cannot be realized, which cannot meet the high application requirements [12], [13].

The continuous wave radar sensor is an integrated radar sensor with a detection target distance and speed capacity [14], [15], [16]. Although phase-modulation radar is becoming an alternative to deep nano processing, frequency modulation (FW) remains the most important type of modulation currently used [17], [18], [19]. The key component of the FW is the FMCW synthesizer, which is used to produce the radar signal and the required frequency regulation solution. Modern FMCW synthesizers are based on PLL. A PLL requires a clean low-frequency reference signal to generate the required output frequency based on a specific control signal [20], [21], [22]. The output frequency of the PLL can be an integer or a score multiple of the vibration frequency by adjusting the corresponding multiplication factor N to obtain an appropriate modulation scheme [23], [24]. However, while the traditional PLL improves performance, its loop stability gradually deteriorates, and even becomes unstable. At present, PLL sensitivity is low, the range of the locking phase is narrow, and the stability problem caused by it has not been resolved. The improvement of the ring structure still lacks a reliable solution [25], [26].

In response to the current FMCW synthesizer's low sensitivity, narrow measurement range, and poor stability, a high-order ADPLL with fast-point topology was designed [27]. The remainder of this paper is organized as follows: Section II introduces the top-level design of the loop system, and Section III presents the loop modeling and performance analysis. A comparison of the simulation analysis and hardware verification results was presented, and an experimental conclusion was drawn.

II. TOP-LEVEL DESIGN OF THE PHASE-LOCKED LOOP

The choice of the FMCW synthesizer PLL architecture depends mainly on the required PLL phase noise and output amplitude. Based on these requirements, the FMCW synthesizer in this study adopts a fast integral-type ADPLL based on third-order proportional integral (PI) control. The block diagram is shown in FIGURE 1.

The loop consisted of three parts: a forward zero sample phase detector (PD), a digital loop filter (DLF), and a digitally controlled oscillator (DCO). The integral module in the DLF is composed of a 24-bit fast integrator and the DCO consists of a 28-bit fast integrator.

In this loop, the DPD consists of a zero-detection module and register, namely, a D trigger. The input signal Ui is connected to the input terminal of the D trigger clock (Clk) and starts to operate when the D trigger detects the Ui rising edge. The phase code M output by the DLF is simultaneously transmitted to the input terminal D of the D trigger group at the same time. When the next rising edge of Ui arrives, the latched code group is output in parallel through the B terminal of the D trigger group. The output signal is the instantaneous phase code group B of the output signal (U0) and input signal (Ui).

To improve the phase-locking performance, a DLF module controlled by the PI was adopted, and phase error code group B was sent to the DLF. After the PI coefficient adjustment, the proportional control signal and second-order PI control signal can be obtained, and the signal obtained by adding 24-bit fast adder 2 is the third-order PI control word G. A register module is placed between the DLF and DCO, which is intended to store the PI control signal G and make G parallel to the input of the DCO at the next clock rise signal. Therefore, by reasonably selecting the proportional and integration coefficients, the third-order PI control word can be easily adjusted to realize the dynamic control of the DCO.

Assuming that the number of digits of the 28-bit fast integrator 3 in DCO is N [28], the input low array is NL, the high array is NH, the PI control word G is connected to the NL bit at the input end of the integrator, and the phase-locked frequency control code group J is connected to the NH bit at the input end of the integrator.

III. LOOP MODELING AND PERFORMANCE ANALYSIS

A. LOOP MODELING

The designed loop Z domain model relationship is shown in FIGURE 2, where K is the total gain of the closed loop, A is

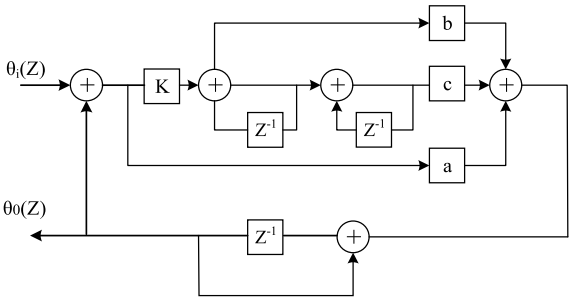

FIGURE 2. Loop Z domain model.

TABLE 1. Third-order ADPLL system stability analysis results.

K_1	K_2	K_3	System Status
2^{-3}	2^{-10}	2^{-11}	Unstable
2^{-3}	2^{-6}	2^{-9}	Critical
2^{-3}	2^{-6}	2^{-11}	Stabilize
2^{-2}	2^{-3}	2^{-11}	Stabilize

the proportional gain coefficient, and B and C are the first and second-order integral coefficients, respectively.

According to FIGURE 2, the closed -loop transmission function $H(Z)$ and error transmission function $HE\ (Z)$ of the loop transmission function are as follows (1) and (2), as shown at the bottom of the next page.

$K_1 = Ka$, $K_2 = Kb$, and $K_3 = Kc$.

B. STABILITY ANALYSIS

According to the NYQUIST judgment standard, if the closed-loop system is in a stable state, its characteristic equations must be located in the unit circle of the Z plane. Equation (3) provides the feature equation for a closed-loop system as follows:

$$Z^3 + (K1 + K2 + K3 - 3)Z^2 + (3 - 2K1 - K2)Z + K1 - 1 = 0 \quad (3)$$

Whether the system reaches a stable state can be determined based on the Jury Stable Guidelines. After derivative, the stable conditions of the third -order full digital lock ring system are as follows:

$$K_3 > 0; K_3 + K_2 + 4K_1 < 8; |K1 - 1| < 1; \quad |K_1^2 - 2K_2| > |K_1^2 + K_1K_2 + K_1K_3 - 2K_1 - K_3| \quad (4)$$

The results of the third-order ADPLL stability analysis are listed in Table 1. The steady-state performance of the loop is regulated by adjusting the values of K_1, K_2, and K_3. The corresponding lock system was stable under certain conditions.

C. STABILITY ERROR ANALYSIS OF THE THIRD-ORDER SYSTEM

According to the error transmission function $He\ (Z)$, the steady -state tracking error of the loop in Table 1 can be

TABLE 2. Lock phase system steady state phase error.

Input Signal	$\theta_i(t)$, $t \geq 0$	$\theta_i(Z)$	$\Phi(\infty)$
Phase Step	θ	$\theta \dfrac{Z}{Z-1}$	0
Frequency Step	vt	$vT \dfrac{Z}{(Z-1)^2}$	0
Frequency Ramp	$\frac{1}{2}at^2$	$\dfrac{aT^2 Z(Z+1)}{2(Z-1)^3}$	0

calculated as follows:

$$\varphi(\infty) = \lim_{Z-1}[(Z-1)\varphi(Z)]$$
$$\varphi(Z) = He(Z) \bullet \theta i(Z), \quad (5)$$

where $\theta i(Z)$ is the Z transform of the input signal phase and $HE(Z)$ is the error transmission function. According to Equation (5), the steady-state errors corresponding to the level, frequency level jump response, and frequency oblique rising response can be determined, as shown in Table 2. The theoretical results show that, under the three input signal conditions, the steady-state tracking error corresponding to the third-order lock system is zero. While the steady-state error of the ordinary second-order phase-locked system is not zero under the frequency ramp response [28].

IV. PRINCIPLES OF FAST INTEGRATION STRUCTURE

Currently, additional operations are being serially performed. If the number of extensions increases, it is controlled by the position signal, which limits the operating speed of the circuit. For the delay of serial carry, a logical algorithm is proposed: when multiple digits are added, each position signal can be output in parallel simultaneously. The principle of fast entry is as follows:

When a multi-digit value is added, the logical relationship between the entire additional $S_i$and position C_i is as follows:

$$Si = Ai \oplus Bi \oplus Ci - 1 \quad (6)$$
$$Ci = AiBi + (Ai \oplus Bi)Ci - 1 \quad (7)$$

Two middle variables, G_i and P_i, are defined.

$$Gi = AiBi \quad (8)$$
$$Pi = Ai \oplus Bi \quad (9)$$

Equations (8) and (9) show that when A_i and B_i are assigned simultaneously, that is, the A_i and B_i input values are valid, then $P_i = 0$, $G_i = 1$, and G_i are effective levels; then, according to equation (7), to obtain carry $C_i = 1$, G_i is the carry to generate the signal. When A_i is not equal to B_i,

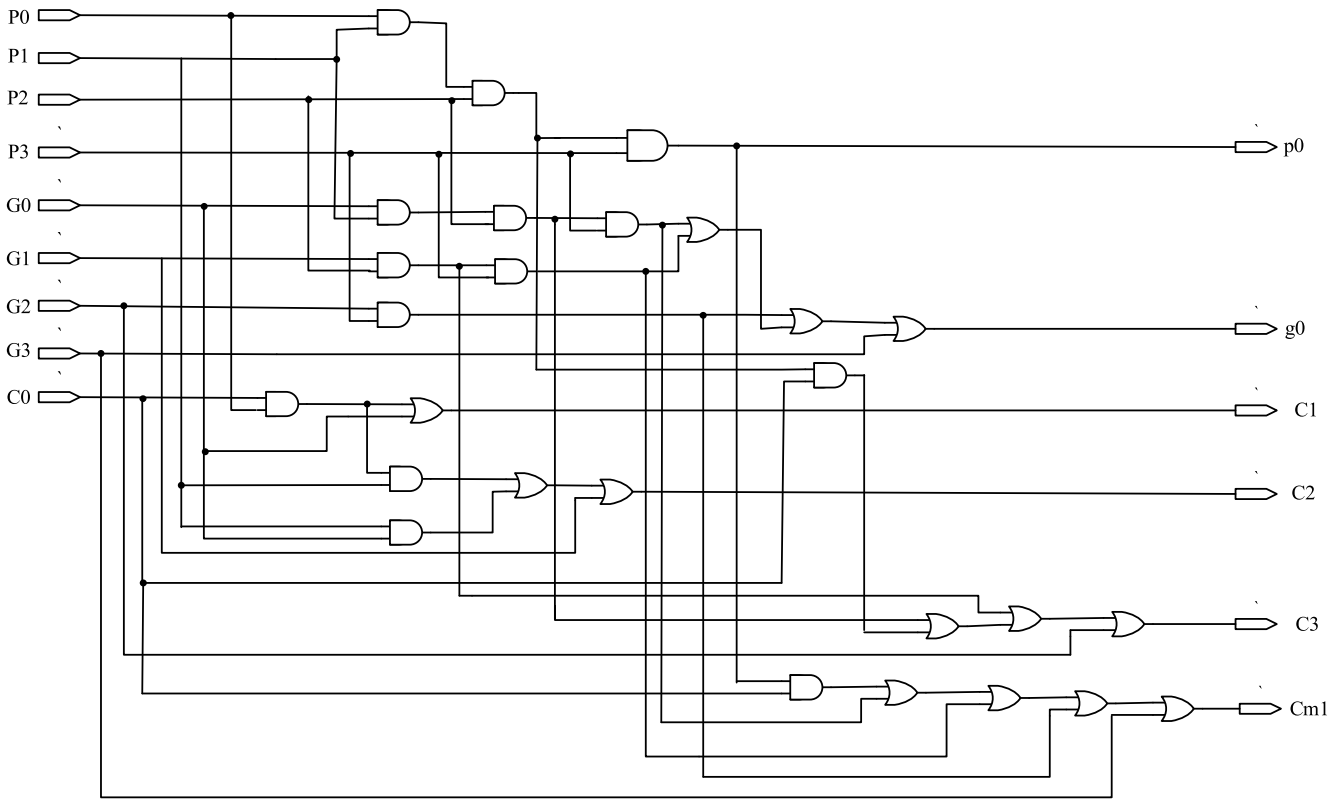

FIGURE 3. Parallel carry generation logic.

that is, A_i and B_i are valid when they are different, $G_i = 0$, $P_i = 1$, and P_i is the effective level. At this time, $C_i = C_{i-1}$; thus, P_i is the transmitted signal. The changes in G_i and P_i values are related only to A_i and B_i.

The comprehensive formula follows:

$$Si = Pi \oplus Ci - 1 \tag{10}$$

$$Ci = Gi + PiCi - 1 \tag{11}$$

The logical relationships in equation (11) are as follows:

$$C0 = G0 + P0C - 1 \tag{12}$$

$$C1 = G1 + P1G0 + P1P0C - 1 \tag{13}$$

$$C2 = G2 + P2G1 + P2P1G0 + P2P1P0C - 1 \tag{14}$$

$$C3 = G3 + P3G2 + P3P2G1 + P3P2P1G0 + P3P2P1P0C - 1 \tag{15}$$

Equations (12), (13), (14), and (15) show that position C_i is determined by the variable P_i, G_i, and the lowest position C_{-1} (its value is zero in the initial state), which is unrelated to C_{i-1}. G_i and P_i are determined by A_i and B_i, and each location is only related to A_i and B_i. A circuit structure with an advanced carry chain can be realized by building a logic gate circuit with an AND gate and an OR gate, in which the carry signal is transmitted in parallel. The parallel-carry generation logic is illustrated in FIGURE 3.

The 4-bit fast-added structure is shown in FIGURE 4, according to the principles of parallel advancement logic.

According to this advanced carry chain, the carry signal can be outputted in parallel, which significantly reduces the operation time. The above is only 4 fast-added. If the number of bits is increased to add more bits, the logic circuit structure becomes more complex. When the number of cascades increases, the operating speed is affected. Therefore, the grade connection method can be improved in parallel.

Parallel carry cascade refers to the advance carry connections between pieces. Let Equation (15) be:

$$p0 = P3P2P1P0 \tag{16}$$

$$g0 = G3 + P3G2 + P3P2G1 + P3P2P1G0 \tag{17}$$

$$H(Z) = \frac{(K1 + K2 + K3)Z^2 - (2K1 + K2)Z + K1}{Z^3 + (K1 + K2 + K3 - 3)Z^2 + (3 - 2K1 - K2)Z + K1 - 1} \tag{1}$$

$$He(Z) = \frac{(Z - 1)^3}{Z^3 + (K1 + K2 + K3 - 3)Z^2 + (3 - 2K1 - K2)Z + K1 - 1} \tag{2}$$

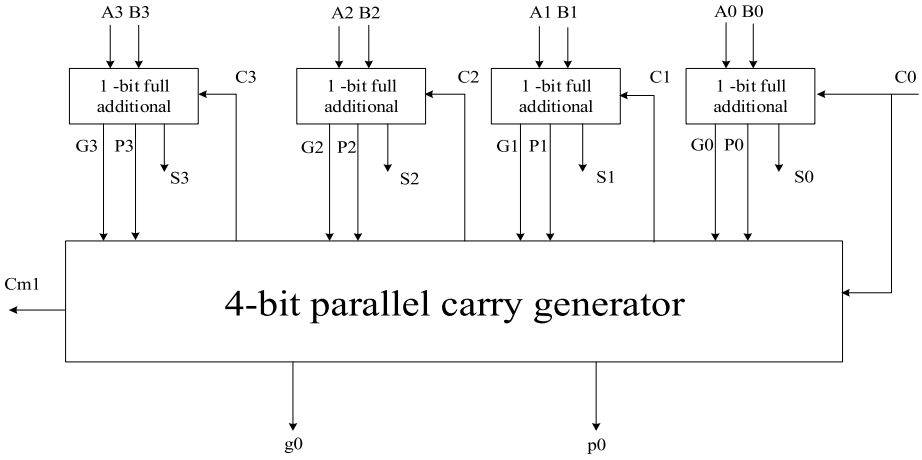

FIGURE 4. 4-bit fast-adder structure.

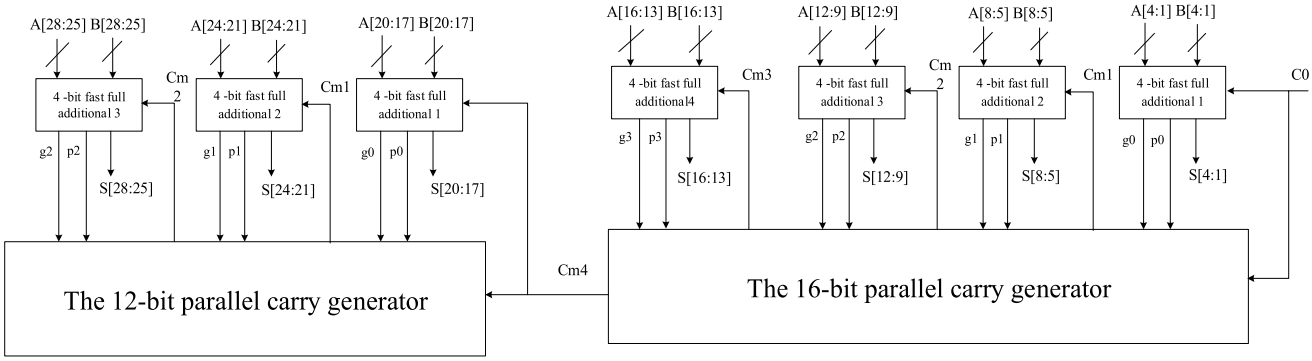

FIGURE 5. 28-bit fast full-adder circuit structure.

Therefore, equation (15) can be written as follows

$$C3 = g0 + p0C - 1 \tag{18}$$

Similarly:

$$C7 = g1 + p1C3 = g1 + p1g0 + p1p0C - 1 \tag{19}$$

$$C11 = g2 + p2g1 + p2p1g0 + p2p1p0C - 1 \tag{20}$$

$$C15 = g3 + p3g2 + p3p2g1 + p3p2p1g0 + p3p2p1p0C - 1 \tag{21}$$

The above expressions show that the entry signals C_3, C_7, C_{11}, and C_{15} are determined only by G_i, P_i, and C_{-1}, which are related only to A_i and B_i. Therefore, this parallel-level joint formula can be used to obtain 4-, 8-, 12-, and 16-bit advanced positions.

V. 28-BIT FAST INTEGRATOR STRUCTURE DESIGN

FIGURE 5 shows that the 28-bit fast all-additive circuit structure consists of two parts. The 16-bit fast all-duct consists of four sets of 4-bit fast all-additives and a set of 16-bit parallel carry generators. The lower 16-bit A[16:1] and B[16:1] are divided into four groups by a 4-bit fast all-adduct input, its output signal as a low 16-bit S of the 28-bit fast all-adduct output S[16:1], and the intermediate carry signals Cm1, Cm2, Cm3, and Cm4 are output by a 16-bit parallel carry generator simultaneously. The carry signal Cm4 is the serial output of the carry signal of a 16-bit fast adduct to the carry input of a 12-bit fast adduct. The second part is a 12-bit fast full adder composed of three groups of 4-bit fast full addition and one group of 12-bit parallel carry generators; the high 12 bits of A and B are divided into three groups and added by the 4-bit fast carry generator input; the output signal is output as the high 12 bits S[28:17] of the 28-bit fast full adder output S, and the carry signal Cm1 in the middle is generated in parallel by the 12-bit parallel carry generator simultaneously.

According to the structure shown in FIGURE 5, the RTL circuit of a 28-bit fast RTL circuit is generated. FIGURE 6 shows that the cla_12 and cla_16 modules have 12-bit and 16-bit fast addition respectively. These two modules jointly form a 28-bit fast full addition. A[28:1] and B[28:1] are the input code groups and S[28:1] is the output code group.

The RTL circuit of the 28-bit fast integrator is shown in FIGURE 7. CLA_28 is a 28-bit fast-added, and registor4 is a register module. After input code groups A[28: 1] and B[28: 1] are added, the output code set S[28: 1] is stored in the register. When the clock signal increases, the output Q[28:1]

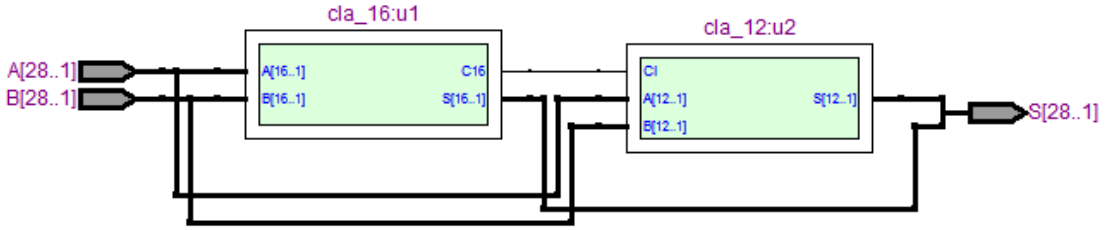

FIGURE 6. 28-bit fast full additional RTL circuit.

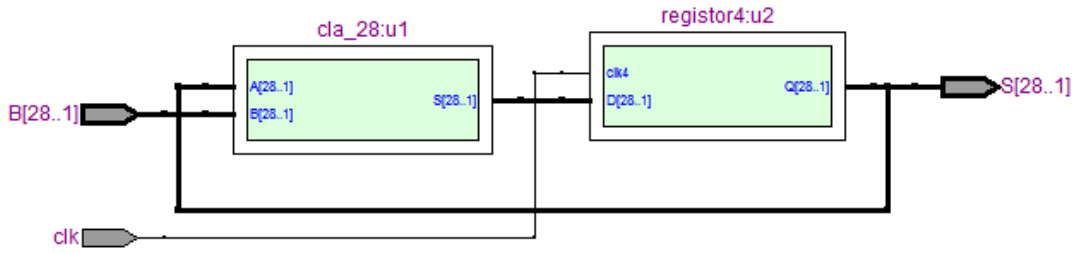

FIGURE 7. 28-bit fast integrator RTL circuit.

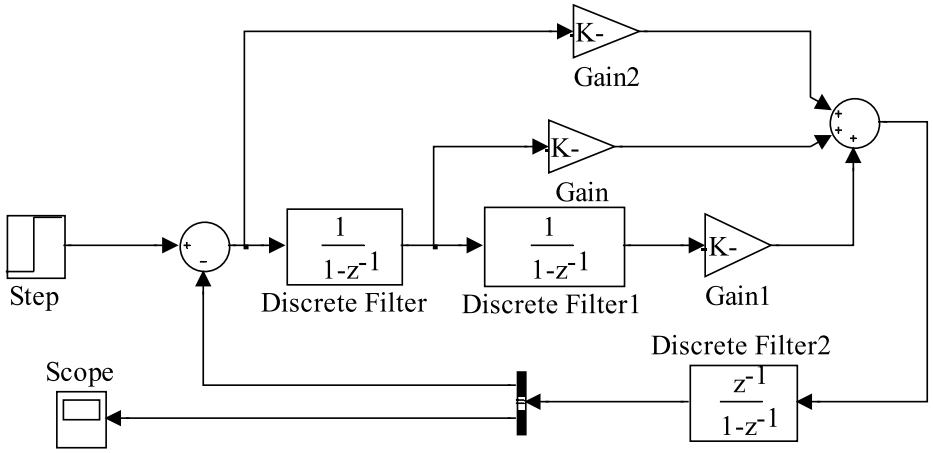

FIGURE 8. Z-domain circuit of the ADPLL.

of the output code group S[28:1] is fed back to the input code group A[28:1] to realize the accumulation function. A 24-bit fast integrator is available.

VI. SIMULATION ANALYSIS AND HARDWARE VERIFICATION

A. SIMULATION TEST ANALYSIS

A phase-locking loop was built using MATLAB, as shown in FIGURE 8. Different proportional coefficients a, first-order integral coefficients b, and second-order integral coefficients c and c were selected to regulate the values of K_1, K_2, and K_3 (K1=Ka, K2=Kb, and K3=Kc). When the input signal is a phase step, the system under different parameters is as shown in Table 1, and the simulation waveform curve of the third-order phase-locked system is obtained as shown in FIGURE 9.

The simulation results demonstrated the phase-locking speed and stability of the system. The design parameters in FIGURE 9(d) have a faster system phase locking.

The two sets of design parameters in FIGURES 9(c) and 9(d) are selected to obtain the error response curve under the input signal of the phase steps, frequency steps, and frequency slopes, as shown in FIGURES 10 and 11. Under the three input signal responses, the steady-state error of the third-order system was similar to zero, verifying the correctness of the theoretical analysis. Therefore, the third-order phase-locking system exhibited good stability. Comparing the simulation curves corresponding to the two sets of design parameters reveals that the system steady-state error in the parameter of FIGURES 9(c) is smaller, and the phase locking speed is faster. Therefore, the parameters shown in FIGURES 9(c) were selected for this design.

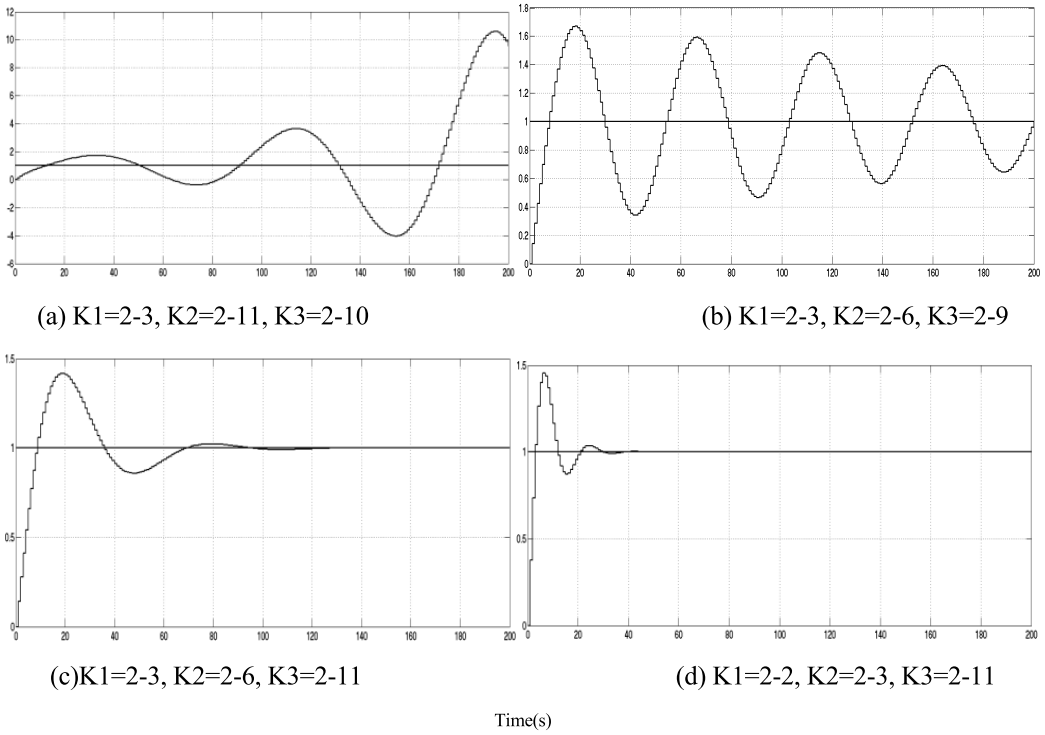

FIGURE 9. Response curve of third order ADPLL under unit step signal.

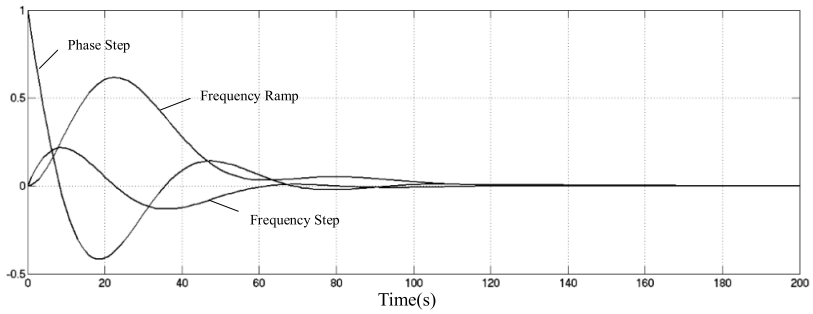

FIGURE 10. $K_1 = 2^{-3}$, $K_2 = 2^{-6}$, $K_3 = 2^{-11}$.

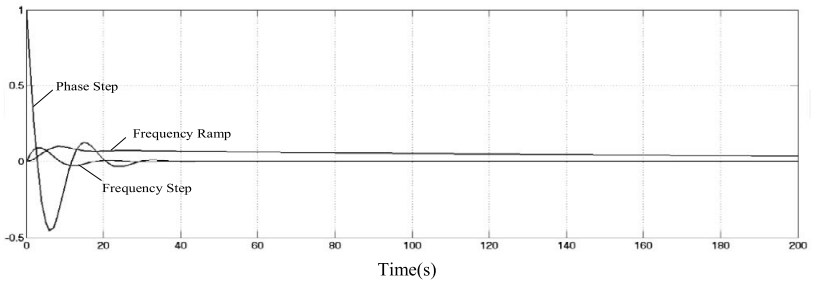

FIGURE 11. $K_1 = 2^{-2}$, $K_2 = 2^{-3}$, $K_3 = 2^{-11}$.

The hardware description language (VHDL) and MODELSIM software were jointly used to conduct an overall simulation of the loop system. Throughout the experiment, the maximum clock frequency allowed by the system was approximately 500 MHz, the integral proportion control word G=2^6, and the input signal u1 = clock signal (clk)/2^6. Subsequently, by adjusting the phase-locking frequency control code group J (adjusted by an integer multiple of 2), the

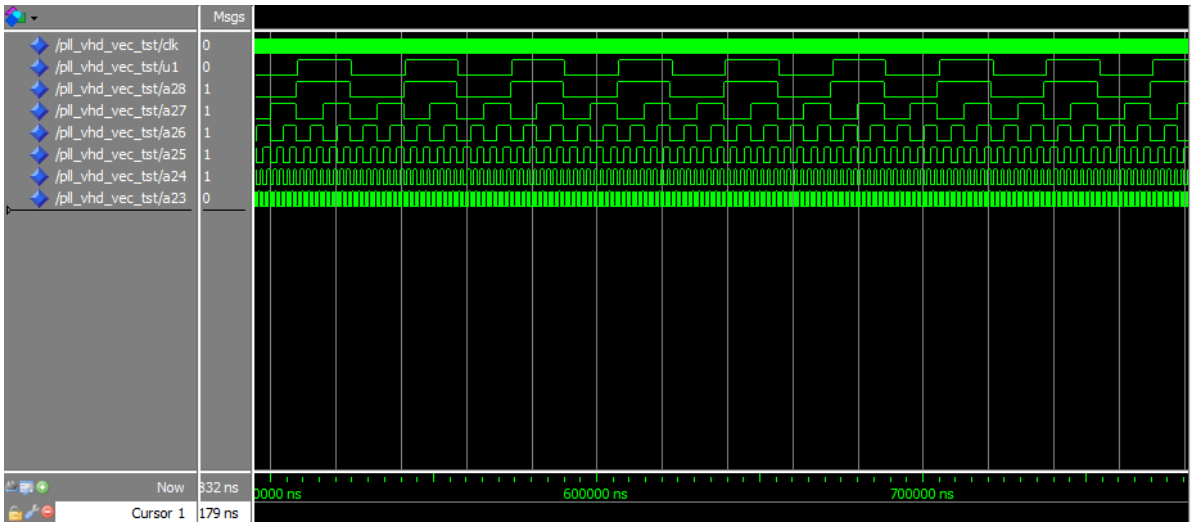

FIGURE 12. Simulation waveform at u1=0.03MHz.

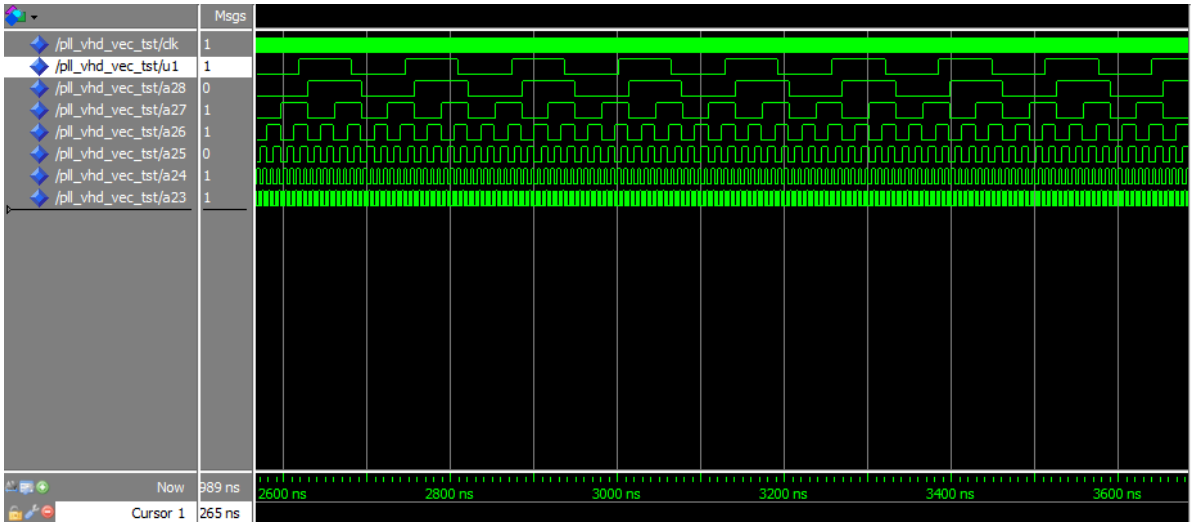

FIGURE 13. Simulation waveform at u1=7.83MHz.

maximum and minimum phase locking frequencies can be obtained. At this frequency, the minimum frequency allowed to enter the signal in the system lock phase is 0.03 MHz, as shown in FIGURE 12, where clk represents the system clock signal port, u1 is the input signal port, a23 to a28 is the PLL output port, a28 is the synchronization signal of the input signal, and a27 to a23 are 2 to 10 times the frequency signal of a28.

The maximum input frequency allowed by the system is 7.83 MHz. Fig.13 shows the simulation waveform output at a clk of 500 MHz, that is, the synchronous signal and frequency-doubling signal output by the system.

B. HARDWARE VERIFICATION AND RESULT COMPARISON

Hardware tests were performed using an EDA box and an oscilloscope were performed. Given that the maximum crystal vibration frequency in the box is 20MHz, the clock frequency cannot reach 500MHz. Therefore, the clock signal is adjusted to 20MHz to verify the correctness of the designed loop system. When the input signal is 312.5KHz, the waveform is shown in Fig. 14, where CH1 is the input signal, and CH2 is the output waveform. The results demonstrate that the loop system can realize a phase-locking function.

Considering the clock frequency of the system, the performance of the ordinary integral ADPLL and third-order ADPLL based on fast integration is 500 MHZ is assessed,

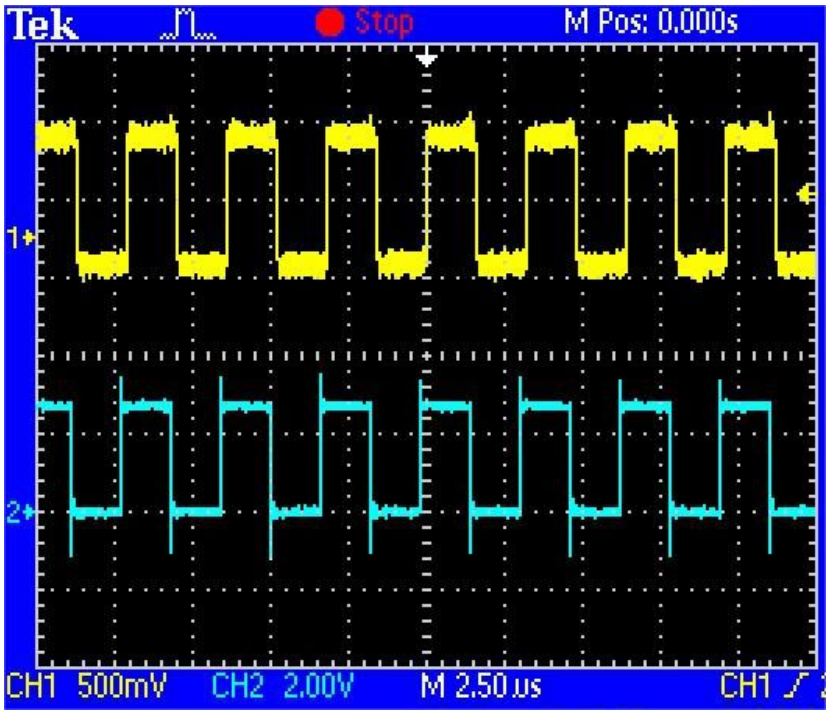

FIGURE 14. Phase-locking system hardware test waveform.

TABLE 3. Results of the comparative analysis of ADPLL.

	Delay (ns)	Number of logical resources	Lock phase range (MHz)
Common integral type ADPLL	10.561	78/232960	0.25–0.98
Third-order ADPLL based on fast integration	6.757	124/232960	0.03–7.83

as shown in Table 3. The results show that compared with the ordinary integral ADPLL, the ADPLL chip has a certain increase, its delay is lower, and the phase-locking frequency range is expanded by nearly ten times.

VII. CONCLUSION

In this study, a high-end automotive FM continuous wave radar phase-locked loop based on a fast integration structure is proposed, which is designed using EDA technology and implemented using programmable logic devices. The new type of ADPLL, through a rapid integration structure and third-order PI control method, optimized the loop system through simulation, made phase locking faster under the loop system, reduced delay by approximately 36%, further improved the phase locking frequency, expanded the loop phase-locking range by nearly ten times, and improved system stability. Therefore, the PLL can be embedded in the SoC as a functional block to provide fast, stable, and high-accuracy synchronization signals for various control systems. In the radar field, it can be used as an FMCW synthesizer for frequency adjustment.

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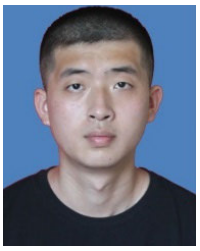

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