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RESEARCH ARTICLE

# New DTMOS Based High Frequency Memristor Emulator and Its Nonlinear Applications

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**ABSTRACT** A new proposition of passive (no external DC bias) memristor emulator (MRE) utilizing DTMOS technique which consists of four MOSFETs and a capacitor has been presented. The proposed MRE exhibits high operating frequency (∼ 500 MHz), zero static power and shows incremental behavior. The conventional mathematical equation of MRE has been derived considering the second-order effects of all the MOSFETs utilized. The proposed circuit has been simulated by the Cadence Virtuoso (IC617) spectre tool using 180 nm technology parameters. The layout occupies 1305$\mu$m$^2$ area. The experimental verification has been carried out utilizing ALD1116 and ALD1117 dual N-channel and P-channel MOSFET arrays to demonstrate the practical viability. Finally, different possible applications namely; analog filters, oscillators (simple and chaotic), Schmitt trigger, Amoeba learning have been realized using proposed MRE to show its neuromorphic capability. Also, new logical AND & OR and NOT circuit configurations have been designed using proposed MRE.

**INDEX TERMS** Memristor, emulator, MOSFET, DTMOS, memductance, hysteresis loop, high frequency, chaotic, logical, neuromorphic, learning.

## I. INTRODUCTION

Announcement of another fundamental circuit element, "Memristor," by Chua [1] led to unfolding of new research interest in the areas of memory-based circuits and their applications. The first fabricated memristor [2] has been presented in 2008, and more such memristors have emerged and evolved in literature [3], [4], [5]. Work in [6] and [7] provides a good overview and understanding of memristor characteristics. Memristor still lacks widespread commercial use as compared to Resistor ($R$), Inductor ($L$), and Capacitor ($C$). To make memristors more viable and easy to fabricate, various research works on memristor emulators (realizing memristor characteristics through combinations of transistors, $R$, $L$ and $C$ ) can be found in [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], and [40].

MREs can be broadly categorized as Active type (requiring DC biasing) and Passive type (not requiring DC biasing). Active MREs provide external electronic tunability, dissipate power, and involve less complexity in their mathematical depictions (in general). In contrast, passive MREs dissipate zero energy, have a small circuit size (as compared to active

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MREs), provide no external electronic tunability, and have, comparatively, more complex mathematical depictions.

There have been several significant works undertaken in MRE realization. In research work [8], memristor emulator realized using famous Diode Bridge with First Order Parallel RC Filter, while in [9] memristor emulator has been explained using PTC (Positive Temperature Coefficient) and NTC (Negative Temperature Coefficient) thermistors. Other few significant work utilizes combinations of readily available building blocks such as OTA (Operational Transconductance Amplifier), OPAMP (Operational Amplifier), FPGA (Field Programmable Gate Array), CCII (Second Generation Current Conveyor), VDTA (Voltage Difference Transconductance Amplifier) and DVCCTA (Differential Voltage Current Conveyor Transconductance Amplifier). These building blocks have been shown therein created with a large number of MOSFETs helping realize MRE [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32] along with $R$ and $C$. Only few works [33], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [46] employ MOSFETs, $R$ and $C$ combinations to create new MREs. Memristor emulators offer non-volatile memory with simple circuit architecture compared to the conventional semiconductor memories, namely; SRAM (Static Random Access Memory), DRAM (Dynamic Random Access Memory), etc. The circuits based on the MRE can be made densely packed and high customization can be achieved through them, for a specific application. These MREs have numerous important applications in signal processing circuits like oscillators, filters, programmable analog circuits, A/D and D/A convertors, neuromorphic systems, and chaotic circuits [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], [48], [49], [50], [51], [52]. Apart from that, MREs can further be extended to Meminductor and Memcapacitor elements which can result in further applications [53], [54], [55]. It can be concluded from the survey of existing literature of memristors [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], [45], [46], [47], [48] that there is no MRE available in the open literature that has low power, more stability, relatively high operating frequencies, no external biasing, utilizing less number of active or passive elements and based on only MOSFETs. The DTMOS technique used in [35], [40], [43], [44], [45], [46], and [47] helps in stable and low power circuits but is unable to achieve high operating frequency. This provides the basis of our motivation to consider these shortcomings as the synthesis challenge for devising a new MRE.

Therefore, the objective of this paper is to propose a new circuit using MOSFET to achieve the memristor characteristics even at higher frequencies without using any external DC bias and dissipating zero static power. We intent

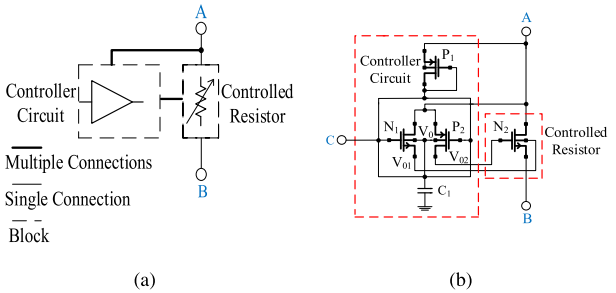


**FIGURE 1.** Proposed MRE (a) General block diagram depiction, and, (b) MOSFET circuit implementation.

to analyze this proposed MRE's attributes at different loads (resistive, capacitive, and inductive), evolving the mathematical model, and performing simulation and hardware experimentations. The organization of this communication is as follows. Section II presents the details of the synthesis of the proposed MRE using a new circuit configuration with the DTMOS technique for attaining high-frequency operation. In Section III, we present the simulation and experimental results of this memristor. Section IV shows the comparison of our proposition with other selected significant works. In Section V, we showcase the different applications of the proposed memristor, and finally, the present work has been concluded in Section VI.

## II. THE THEORY AND CMOS DESIGN OF PROPOSED MEMRISTOR EMULATOR

The general MRE design can be divided into two parts, (i) Controller Circuit and (ii) Controlled Resistor, as presented in Fig. 1a. In the proposed development of MRE, four MOSFETs (two nMOS ($N_1, N_2$) and two pMOS ($P_1, P_2$)) and one capacitor ($C_1$) have been used, along with ports A, B and C as shown in Fig. 1b. The design does not require any biasing, has zero static power, and employs a dynamic threshold technique modified for high frequency operation. MOSFETs $N_1, P_1$ and $P_2$ are connected in a way such that they are forced to operate in the saturation region only and serve the purpose of emulating the memristor characteristics alongside external capacitor. The dynamic threshold technique helps in reducing the threshold voltage and potential in the channel region which is being controlled by the body and gate. This results in high transconductance leading to faster current transport and high bandwidth, thus enhancing the circuit performance for low-power and low-voltage applications. The nMOS is used for controlled resistor because it has high speed and lesser threshold voltage than pMOS. For charging the $C_1$ of the controller circuit, $P_1$ is utilized due to its high noise immunity, and this voltage across $C_1$ is being used for controlling $N_2$. Here, the source of $N_1$ is used to provide controlling voltage to the body of $N_2$ which is of p-type. To provide controlling voltage to the gate of $N_2$, drain of $P_2$ has been used owing to its less likelihood of threshold voltage variation and noise than nMOS. The Voltage $V_0$ is being divided into $V_{01}$ and $V_{02}$ to drive $N_2$. $N_1$

and $P_2$ are being used as modified configuration for DTMOS based high-frequency memristor.

In Fig. 2, we present the proposed memristor configuration with considered internal capacitances (body-to-drain ($C_{BD}$), body-to-source ($C_{BS}$), gate-to-source ($C_{GS}$), gate-to-drain ($C_{GD}$), gate-to-body ($C_{GB}$) and drain-to-source resistance $r_{ds} \cong \frac{1}{\mu_N c_{ox}\left(\frac{W}{L}\right)_{N2}(V_{GS(N2)}-V_{TH(N2)})}$, where quantities $\mu$, $C_{ox}$, $W/L$, $V_{GS}$, and $V_{TH}$ carry their usual meaning. The resistance $r_{ds}$ depend on $V_{GS}$ ($N_2$) in the saturation region and are controlled by MOSFETs $N_1, P_1$, and $P_2$. The memory effect of the memristor and controlling memductance is obtained by $C_1$ and $N_2$. In the following, we describe the mathematical formulations of the proposed memristor.

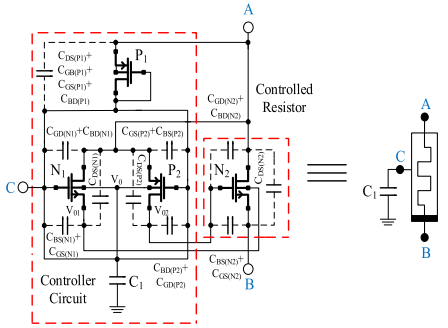


**FIGURE 2.** The MRE circuit of Fig. 1b along with internal parasitic capacitors and its equivalent symbol.

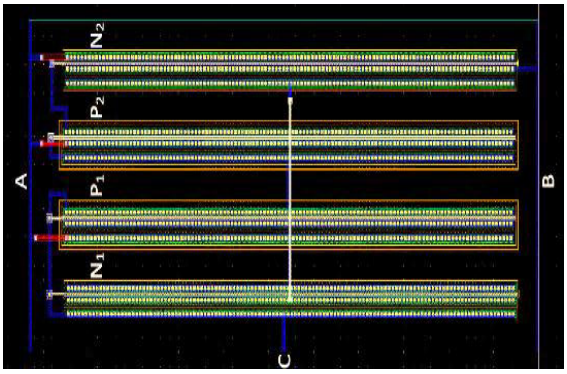


**FIGURE 3.** CMOS Layout of the proposed MRE.

At node A, in Fig. 1b, we consider voltage as $V_{\text{in}}(t)$, and at node B, we take $NV_{\text{in}}(t)$, where $0 \leq N < 1$. Now, considering the internal capacitances of Fig. 1b, as shown in Fig. 2, the equation of current through $N_1$ can be written as

$$C_1\frac{dV_0(t)}{dt} + C_{P1}\frac{d\left(V_{in}(t)-V_0(t)\right)}{dt} \cong K_{P1}(V_{SGP1}(t) - |V_{THP}|)^2 \quad (1)$$

Now taking, $C_{P1} = C_{GB(P1)} + C_{BD(P1)} + C_{GS(P1)} + C_{DS(P1)}$, $x = C_1/C_{P1}$ and $m(t) = V_{in}(t) + (x-1)V_0(t)$, where $x > 1$ and, process constant of $P_1$ is $K_{P1} = \frac{1}{2}\mu_P C_{ox}\left(\frac{W}{L}\right)_{P1}$, this yields eq. 1 to

$$\frac{C_1}{x}\frac{d(m(t))}{dt} \cong K_{P1}((2V_{in}(t) - m(t)) - (x+2)V_0(t)t. + |V_{THP}|)^2 \quad (2)$$

Now, eq. 2 can further be written as $\frac{C_1}{x}\frac{d(m(t))}{dt} \cong K_{P1}m^2(t)\left(-3 + \left(2 - \frac{2V_{in}(t)-(x+2)V_0(t)-|V_{THP}|}{m}\right)^2 - \frac{(2x+4)V_0(t)}{m(t)} + \frac{4V_{in}(t)}{m(t)} - \frac{6|V_{THP}|}{m(t)}\right)$ and as we have already taken $x > 1$, then, we can neglect the term $\left(2 - \frac{2V_{in}(t)-(x+2)V_0(t)-|V_{THP}|}{m(t)}\right)^2 - \frac{(2x+4)V_0(t)}{m(t)}$ as compared to other terms. Next, by considering $z(t) = m^{-1}(t)$ and $\frac{d(z(t))}{dt} = -\frac{1}{m^2(t)}\frac{d(m(t))}{dt}$, we get eq. 2 as

$$\frac{d(z(t))}{dt} + \frac{4xK_{P1}}{C_1}(V_{in} - 1.5|V_{THP}|)z(t) = \frac{3xK_{P1}}{C_1} \quad (3)$$

As eq. 3 resembles to a first-order linear non-homogeneous differential equation, it can be deduced that

$$Z(t) \cong Be^{-\int \frac{4xK_{P1}}{C_1}(V_{in}(t)-1.5|V_{THP}|)dt} + \frac{3}{4} \quad (4)$$

where $B$ is integration constant. From eq. 4, by using binomial expansion and exponential series (neglecting higher-order terms), $V_o(t)$ can be written as

$$V_0(t) \cong B_1 + \frac{B_2K_{P1}}{C_1}\emptyset_0(t) - B_3V_{in}(t) \quad (5)$$

where, input flux, $\emptyset_0(t) = \int (V_{\text{in}}(t) - 1.5|V_{THP}|)\,dt$ and $B_1 = \frac{12-16B}{9(x-1)}$, $B_2 = \frac{64Bx}{9(x-1)}$, $B_3 = \frac{1}{x-1}$ are constants. Next, by carefully examining Fig. 2, we can derive the voltage $V_{01}$ used for controlling the body voltage of $N_2$ as following equation

$$C_{GS(N1)}\frac{d\left(V_0(t)-V_{01}(t)\right)}{dt} + C_{DS(N1)}\frac{d\left(V_{in}(t)-V_{01}(t)\right)}{dt} + K_{N1}\left(V_{GS(N1)}(t) - V_{TH(N1)}(t)\right)^2 \cong 0 \quad (6)$$

Considering $y = C_{GS(N1)}/C_{DS(N1)}$, where we can take $y > 1$ (as gate-drain capacitance is often an order of magnitude smaller than the gate-source capacitance) and $K_{N1} = \frac{1}{2}\mu_N C_{ox}\left(\frac{W}{L}\right)_{P1}$. The body of the $N_1$ is connected to the gate, $V_{TH(N1)}(t) = V_{THN} + \gamma_N\left(\sqrt{|2\psi_{SN} + V_{SB(N1)}|}\sqrt{2\psi_{SN}}\right) \cong V_{THN} + K_{BN}V_{SB(N1)}$ where by replacing $w(t) = yV_{in}(t) + (y-1)V_{01}(t) - V_0(t)$ and the body constant of nMOS $K_{BN} \cong \gamma_N(2\psi_{SN})^{1/2}/2$, eq. 6 can be re-arranged as

$$C_{GS(N1)}\frac{d(w(t))}{dt} \cong K'_{N1}\left(w(t) - y\left(V_{01}(t) + V_{in}(t)\right) - \frac{V_{THN}}{1+K_{BN}}\right)^2 \quad (7)$$

Here by considering $K'_{N1} = K_{N1}\sqrt{1+K_{BN}}$, we can neglect the terms $\left(-2 + \frac{y\left((V_{01}(t)+V_{in}(t)) + \frac{V_{THN}}{1+K_{BN}}\right)}{w(t)}\right)^2 - \frac{6yV_{01}(t)}{w(t)}$. Now by taking $z_1(t) = w^{-1}(t)$ and $\frac{d(z_1(t))}{dt} = -\frac{1}{w^2(t)}\frac{d(w(t))}{dt}$,

eq. 7 will result in

$$\frac{d\,(z_1(t))}{dt} - \frac{6yK'_{N1}}{C_{GS(N1)}}\left(V_{in}(t) + \frac{V_{THN}}{1+K_{BN}}\right) z_1(t) \cong \frac{3\,K'_{N1}}{C_{GS(N1)}} \tag{8}$$

Again, we can see that eq. 8, resembles to a first-order linear non-homogeneous differential equation, one solution would be

$$z_1(t) \cong De^{\int \frac{6yK}{'}C1\left(V_{GS(N1)}(t)+\frac{V_{THN}}{1+K_{BN}}\right)dt} - \frac{1}{2y} \tag{9}$$

where $D$ is the integration constant. From eq. 9, using binomial expansion and exponential series (neglecting higher-order terms), $V_{01}(t)$ can be written in terms of $z_1(t)$, $V_0(t)$, and $V_{in}(t)$

$$V_{01}(t) \cong D_1 + \frac{D_2K_{P1}}{C_1}\emptyset_0(t) - \frac{D_3K'_{N1}}{C_{GS(N1)}}\emptyset_{01}(t) - D_4V_{in}(t) \tag{10}$$

where body flux is $\emptyset_{01}(t) = \int\left(V_{in}(t) + \frac{V_{THN}}{1+K_{BN}}\right)dt$ and $D_1 = \frac{-2y-4y^2D+B_1}{y-1}$, $D_2 = \frac{B_2}{y-1}$, $D_3 = -\frac{24y^2D}{y-1}$ and $D_4 = \frac{B_3+y}{y-1}$ constants. Again, by carefully examining Fig. 2, we can find $V_{02}$ used for controlling the gate voltage of $N_2$ by following the approach similar to eq. 5 - 10 as

$$V_{02}(t) \cong E_1 + \frac{E_2K_{P1}}{C_1}\emptyset_0(t) - \frac{E_3K'_{P2}}{C_{GS(P2)}}\emptyset_{02}(t) - E_4V_{in}(t) \tag{11}$$

where gate flux is $\emptyset_{02}(t) \cong \int\left(V_{in}(t) + \frac{|V_{THP}|}{1+K_{BP}}\right)dt$, and $K'_{P2} = K_{P2}\sqrt{1+K_{BP}}$ for body constant of $P_2$, $K_{P2} = \frac{1}{2}\mu_P C_{ox}\left(\frac{W}{L}\right)_{P2}$ and $K_{BP} \cong \gamma_P\left(2\psi_{SP}\right)^{1/2}/2$. Now considering $v = C_{GS(P2)}/C_{DS(P2)}$ and can take $v > 1$ always, wherein $E_1 = \frac{-2v-4v^2E+B_1}{v-1}$, $E_2 = \frac{B_2}{v-1}$, $E_3 = -\frac{24v^2E}{v-1}$ and $E_4 = \frac{B_3+v}{v-1}$ with $E$ being an integration constant. Further, we can write the inverse of memristance or memductance $W(\varnothing(t)$ of the proposed MRE as follows

$$W(\emptyset(t) = \frac{I_{in}(t)}{V_{in}(t)} \cong \frac{K_{N2}}{2}\left((K_{B(N2)}+1)(V_{02}(t)+K_{BN}V_{01}(t)+V_{(p)}\right) \tag{12}$$

where $V(p)$ is the extra voltage due to intrinsic capacitances, body effect, transistor mismatch, internal noise and parasitic (effects of these can be observed during postlayout simulation). Now from eq. 10 and eq. 11, we can re-write eq. 12 as

$$\frac{I_{in}(t)}{V_{in}(t)} \cong K'_{N2}\left(\begin{array}{c} G_1 + \frac{G_2K_{P1}}{C_1}\emptyset_0(t) - \frac{G_3K'_{N1}}{C_{GS(N1)}}\emptyset_{01}(t) \\ -\frac{G_4K'_{P2}}{C'_{GS(P2)}}\emptyset_{02}(t) - G_5V_{in}(t) + V_{(p)} \end{array}\right) \tag{13}$$

where $K'_{N2} = \frac{K_{N2}}{2}\left(K_{B(N2)}+1\right)$ and $G_1 = E_1 + K_{BN}D_1$, $G_2 = E_2 + K_{BN}D_2$, $G_3 = K_{BN}D_3$, $G_4 = E_3$, $G_2 = E_2 + K_{BN}D_2$ are constants. Finally, we can write the unity-gain bandwidth of the proposed memristor as $f_T \cong \frac{g_{m(N2)}+g_{mb(N2)}}{2\pi\left(C_{GS(N2)}+C_{GD(N2)}\right)}$ where

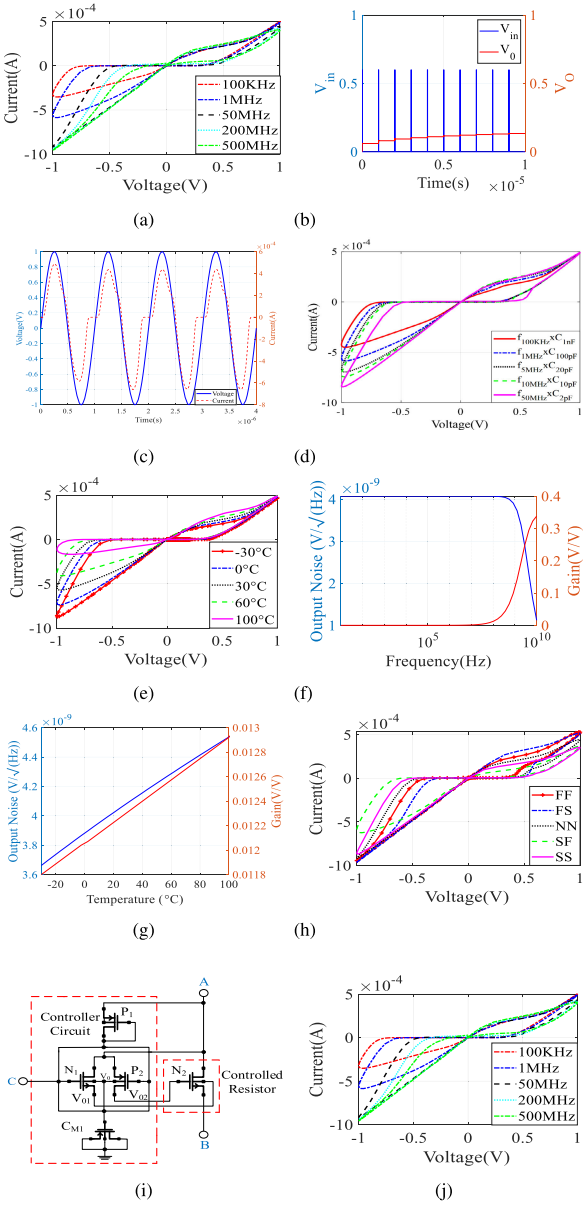


**FIGURE 4.** Simulation results of the proposed MRE with 1kΩ resistance connected to ground at port $B$ and $C_1 = 100pF$ (*a*) Pinched hysteresis loop for input voltage at different frequencies, (b) Transient response for pulsed input of 1$\mu$s period and pulse width of 10ns, (c) Transient response at 1MHz input, (d) Hysteresis loop comparison (constant frequency times $C_1$ ) at different frequency and capacitor values, (e) V-I curve for 1MHz input at different temperatures, (f) Output noise and gain plot with varying input frequency, (g) Output noise and gain plot with varying temperature at 100MHz input, (h) Different process corner V-I relationships at 50MHz input, (i) Proposed MRE design utilizing MOSCAP, and, (j) Corresponding pinched hysteresis loop at different input frequencies of Fig. 4i circuit.

transconductance of $N_2$ being $K'_{N2}\left(V_{02}(t)+K_{BN}V_{01}(t)\right) + \frac{\gamma_N}{2}\frac{\sqrt{2K'_{N2}(V_{02}(t)+K_{BN}V_{01}(t))}}{\sqrt{2|\psi_{SN}|+|V_{01}(t)|}}$. Now the $f_T$ is

$$f_T \cong \frac{K'_{N2}\left(V_{02}(t)+K_{BN}V_{01}(t)\right) + \frac{\gamma_N}{2}\frac{\sqrt{2K'_{N2}(V_{02}(t)+K_{BN}V_{01}(t))}}{\sqrt{2|\psi_{SN}|+|V_{01}(t)|}}}{\left(C_{GS(N2)}+C_{GD(N2)}\right)} \tag{14}$$

It can be observed from equations 5, 10 and 11, that the static and dynamic part of the flux voltages can be adjusted using $C_1$. We can deduct from eq. 13, that an incremental MRE is obtained from this circuit in which memristance increases when a positive or negative pulse train is applied. So, minimum current flows through the circuit when memristance is maximum and vice-versa, which means we can consider this situation as 0 and 1 in terms of digital circuits. From eq.13, it can also be noticed that change in $V_{TH}$ can be adjusted by circuit, and hence we can expect MRE to behave well with temperature variation, which we verified through simulation in the next section. By seeing eq. 14, we can make a note that utilizing the bulk-driven circuit and controlling the body and gate of $N_2$ helps in increasing the proposed MRE bandwidth. The memristance, from eq. 13, deviates from the ideal value due to the parasitic that influences the rate of change of memristance and produces a decrease in the area of the pinched hysteresis loop. As we can deduct from eq. 13 and eq. 14, the change in memristance and unitygain bandwidth due to parasitic can be compensated by carefully changing the aspect ratios of $N_1, N_2, P_1$ and $P_2$.

Now, to analyze the frequency characteristics of the proposed memristor, a sinusoidal input voltage is applied equal to $A_m \sin(2\pi ft)$ where $A_m$ and $f$ are the signal amplitude and frequency, respectively. Substituting input voltage in (eq. 12) and neglecting small threshold voltage, we get

$$W(\emptyset(t)) \cong K'_{N2}\left(\frac{G_1 + \frac{A_m \cos(2\pi ft)}{2\pi fC_1}}{\left(\frac{G_2K_{P1}}{C_1} - \frac{G_3K'_{N1}}{C_{GS(N1)}} - \frac{G_4K'_{P2}}{C_{GS(P2)}}\right)}\right) \quad (15)$$

As the frequency goes very high, the static part approaches zero, and so, the resultant memristor will act as the timeindependent resistor as we follow eq. 15. Hence, the ratio of the dynamic part coefficient and the static coefficient part can be written as

$$\partial = \frac{A_m\left(\frac{G_2K_{P1}}{C_1} - \frac{G_3K'_{N1}}{C_{GS(N1)}} - \frac{G_4K'_{P2}}{C_{GS(P2)}}\right)}{2\pi fC_1G_1} = \frac{1}{\tau f} \quad (16)$$

where the time constant of the proposed MRE, $\tau$, is $\frac{2\pi fC_1G_1}{A_m\left(\frac{G_2K_{P1}}{C_1} - \frac{G_3K'_{N1}}{C_{GS(N1)}} - \frac{G_4K'_{P2}}{C_{GS(P2)}}\right)}$.

As we decrease the value of $\partial$, frequency increases while $\tau$ must be updated in order to hold pinched hysteresis loop. The maximal pinched hysteresis loop is reached when $f = 1/\tau$. The pinched hysteresis loop is lost when $f$ is less than or equal to $1/\tau$, which means that the emulator circuit's time constant is smaller than the voltage signal source's period. Therefore, to guarantee the pinched hysteresis loop's behavior, the value of $\partial$ needs to be between 0 and 1.

## III. VALIDATION BY SIMULATION AND EXPERIMENTATION

The workability of the proposed MRE has been verified by simulation using Cadence Virtuoso Spectre Tool with 180nm CMOS GPDK parameter. The proposed circuit is also experimentally tested using market available MOSFET arrays such as ALD1116 (nMOS based) and ALD1117 (pMOS based) in which bulk is open which is better suited to correctly evaluate proposed circuit in real conditions. The CMOS layout of the proposed circuit in Fig. 2 has been shown in Fig. 3, which occupies an area of $1305\mu m^2(23.04\mu m \times 56.64\mu m)$ and shows a symmetrical layout design.

The proposed MRE needs no external biasing or supply voltage and hence the static power is zero. The circuit has been tested under no-load and load conditions ($R, L$ and $C$) to show the proposed MRE flexibility. The initial voltage across $C_1$ was selected as zero during the simulation as well as during the experiment. The worked-out aspect ratio of the MOSFETs of the proposed MRE are tabulated in Table 1.

**TABLE 1. Aspect ratios utilized for circuit configuration of fig. 2.**

| MOSFET | Aspect ratio (W/L) (in $\mu$m) |
|---|---|
| $N_1, N_2, P_1, P_2$ | 50/0.2 |

Simulations in Fig. 4 illustrates the proposed MRE with a resistive load of $1k\Omega$ connected at port C (Fig. 2). The proposed MRE hysteresis curve is displayed for various frequencies in Fig. 4a. The asymmetrical characteristics of the hysteresis loop can be ascribed to parasitic effects in MRE design [5], [9], as examined in the section- II mathematical derivation. The incremental behavior of the MRE is apparent in Fig. 4b on applying an input signal in the form of a pulse. The input voltage signal and corresponding current signal of the memristor for multiple cycles presented in Fig. 4c, which also shows incremental behavior of proposed MRE. Fig. 4d can be understood by considering eq. 16, where if we adjust frequency and capacitance such that their product is constant, we will get a similar type of hysteresis curve every time. This shows consistency and stability of the proposed MRE. The proposed memristor can work over a good range of temperature ($-30°C$ to $100°C$), which is depicted in Fig. 4e. Since noise impairs functionality, the suggested MRE's noise performance has subsequently been presented. The output noise and associated noise gain, which represents the transfer function from output to input noise, are displayed in Fig. 4f in relation to changing frequency. Similarly, Fig. 4g shows the output noise and matching noise gain in relation to changing temperature. The plot demonstrates how the proposed MRE's balanced design results in noticeably less noise. Fig. 4h presents a corner analysis that illustrates the circuit's performance under identical temperature conditions for FF, FS, SF, and SS scenarios. Thus, the proposed MRE demonstrates stability at various process corners. It is evident that, as would be expected, there is less current flowing in process corner SS and greater current flowing in process corner FF. The proposed MRE can be combined with MOSCAP ($C_{M1}$) too which shows the flexibility of the proposed design as shown in Fig. 4f. The $C_{M1}$ has been realized using pMOS having $W/L$ as $50\mu m/40\mu m$. Hysteresis loop for different frequency has been shown in Fig. 4g for circuit in Fig. 4f.

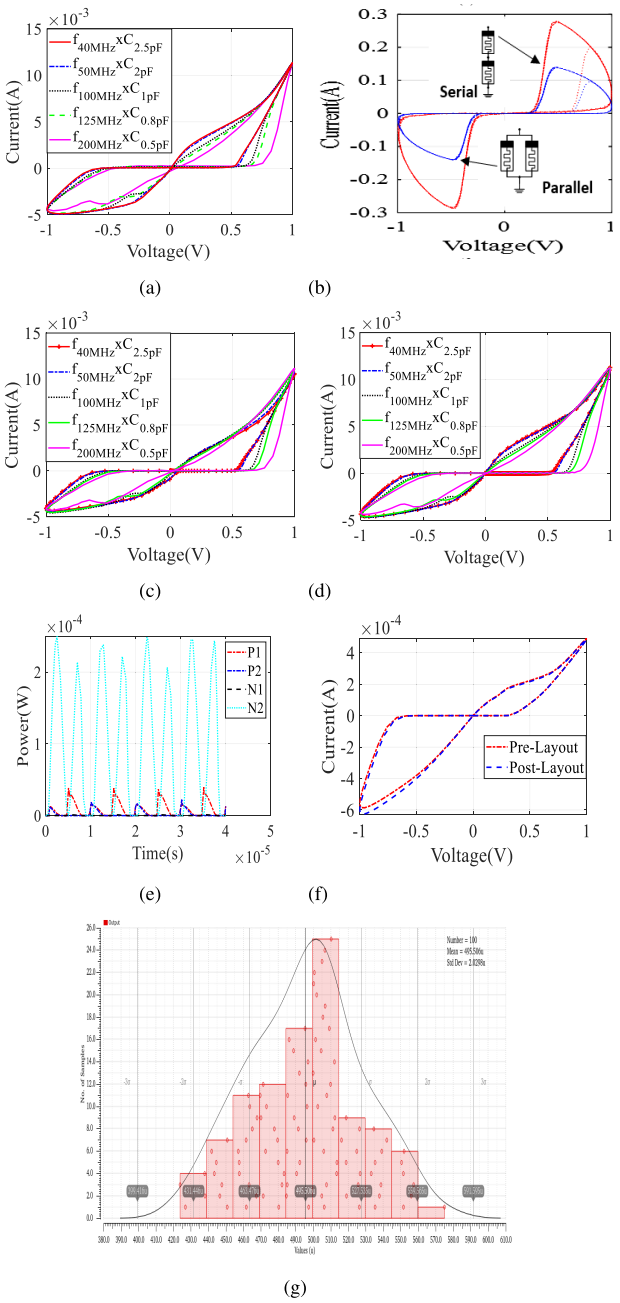


**FIGURE 5.** The MRE simulation results for different loads connected at port C (a) Grounded MRE hysteresis loop (frequency$XC_1$ = constant) graph, (b) Grounded MRE pinched hysteresis loop for parallel and serially connection for 50MHz sinusoidal input at $C_1$ = 500pF over 100cycles, (c) Hysteresis loop (frequency$XC_1$ = constant) graph for grounded 1nF capacitive load MRE, (d) Hysteresis loop (frequency$XC_1$ = constant) graph for grounded 1nH inductive load MRE, (e) Dynamic power output at input frequency 100KHz, C = 100pF and load 1 kΩ, (f) Pre-layout and Post-layout comparison at 1MHz input, C = 100pF and load 1 kΩ, and, (g) Monte-Carlo simulation for 100 runs due to process and mismatch parameters.

We can conclude that the proposed circuit with resistive load works as a memristor. The performance of the proposed MRE under grounded conditions, or without a load, have been displayed in Figs. 5a-5g. Fig. 5a illustrates that if both the frequency and the capacitor product remain constant, varying

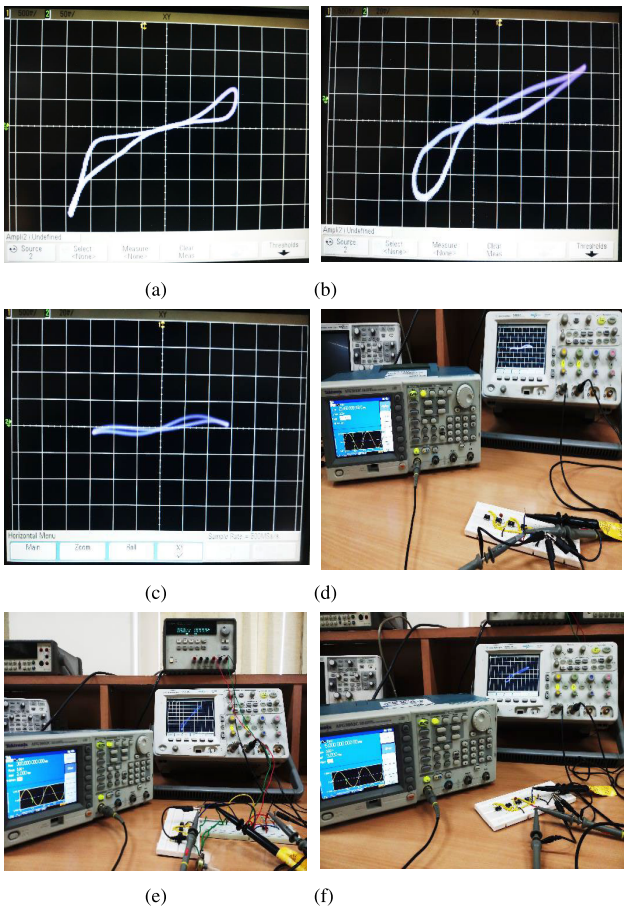


**FIGURE 6.** Experimental result for Pinched hysteresis loop and setup for MRE with grounded resistive load (a) At 100kHz, (b) At 5MHz, (c) At 25MHz, (d) Full experimental setup at operating frequency of 25MHz, (e) View of memristor experimental setup at 300kHz for grounded MRE, and, (f) Full experimental setup at 5MHz operating frequency for grounded capacitive load.

one of them will consistently result in a voltage-current curve that looks similar. One of the key features of a memristor is this. We have shown the suggested MRE behavior in series and parallel connections in Fig. 5b. Fig. 5c and 5d shows hysteresis loop is similar if frequency and capacitor product are constant for capacitive and inductive load, respectively. The dynamic power for each MOSFET used in the proposed MRE with an amplitude of $\pm 1V$ is shown in Fig. 5e. Fig. 5f displays a comparison of the pre- and post-layout for the proposed MRE at an amplitude of $\pm 1V$. The graph indicates a very small difference. A Monte-Carlo analysis, taking into account variations in process and mismatch parameters, was conducted to demonstrate the potential fabrication variation of the proposed MRE under grounded load resistance. The results are displayed in Fig. 5g at 492.5$\mu$A current output.

Further, in Fig. 6, experimental work has been done for MRE with resistive load. Fig. 6a - 6c presents a pinched hysteresis loop at different frequencies for MRE with resistive load. Fig. 6d shows the experimental setup view of resistive load. Experimental setup view of the proposed MRE for the grounded and capacitive load is shown in Fig. 6e and 6f,

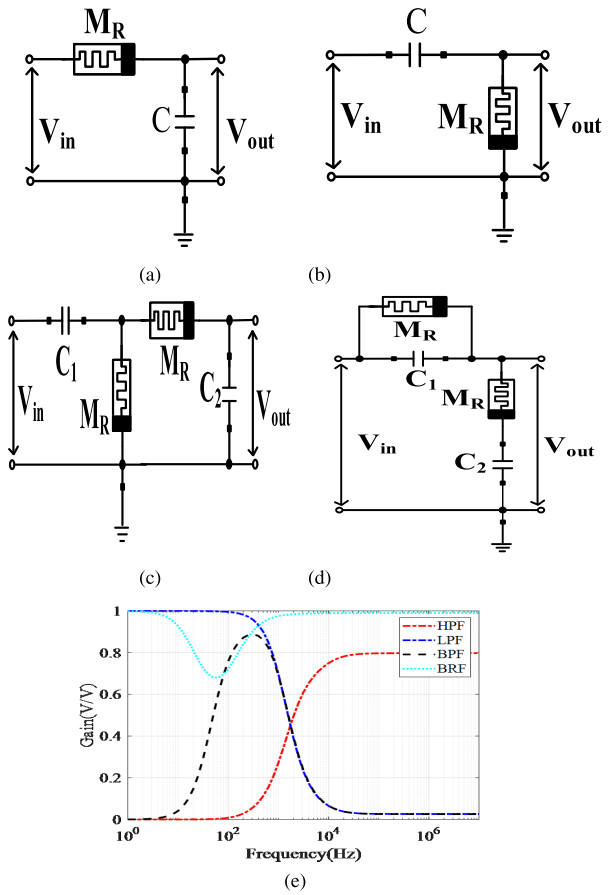


**FIGURE 7.** Proposed MRE application as filters (a) HPF circuit, (b) LPF circuit, (c) BPF circuit, (d) BRF circuit, and, (e) Frequency response for HPF and LPF at C = 1pF, BPF at $C_1$ = 30pF & $C_2$ = 1pF and *BRF* at $C_1$ = 30pF & $C_2$ = 25pF.

respectively. The simulations and experiment results show that DTMOS technique employed results in high frequency operation with zero static power and providing stability.

## IV. APPLICATIONS

Memristor emulators can be used in several real-time signal processing situations. A constant cut-off frequency is provided by the resistor-capacitor parallel circuit in a traditional filters, but an adjustable gain characteristic is provided by the use of a memristors. Furthermore, the ability to adjust the filter circuit's cut-off frequency is provided by the variation in the memristance value. To confirm the workability of the proposed MRE, Low Pass Filter (LPF), High Pass Filter (HPF), Band Pass Filter (BPF), Band Reject Filter (BRF), BPF based oscillator, Colpitts chaotic oscillator, and Schmitt trigger circuits have been considered for tests. In Fig. 7a, 7b, 7c and 7d shows circuit of filters such as HPF, LPF, BPF and BRF, respectively. Frequency response of HPF, LPF, BPF and BRF have been presented in Fig. 7e.

It is to be noted that the standard resistor has been replaced with the proposed MRE. The cut-off frequency of HPF and LPF filters can be written as $f_c = 1/\left(2\pi C\left(W^{-1}(\varnothing(t))\right)\right)$. The low and high cut-off frequency of BPF and BRF filters can

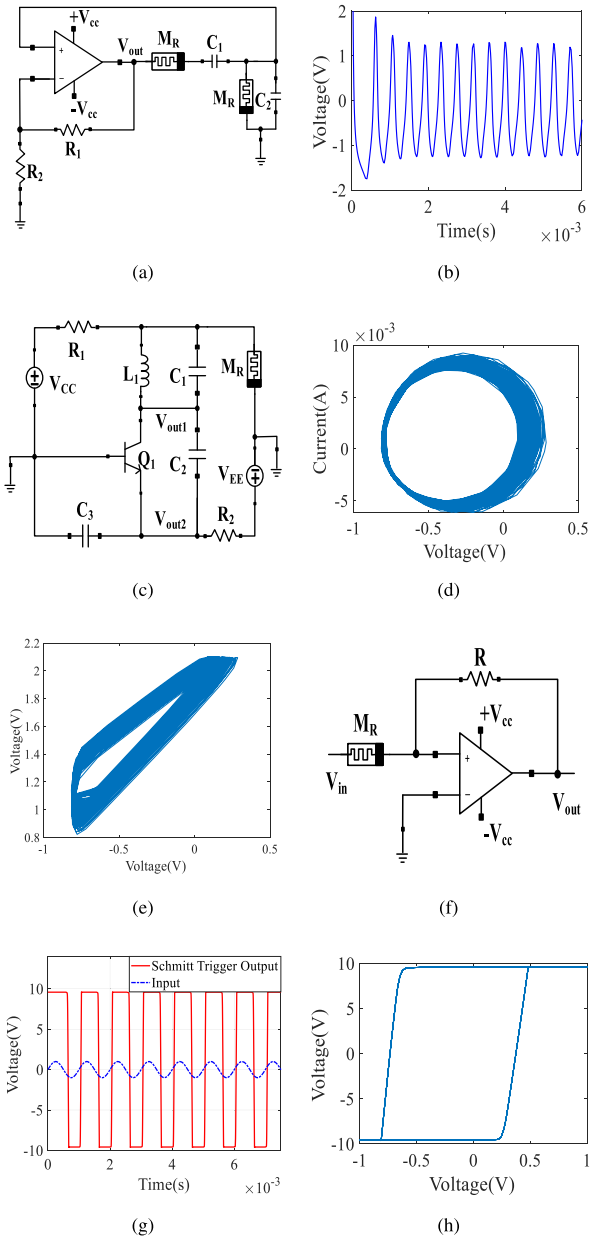


**FIGURE 8.** The proposed MRE application in different analog circuits (a) Oscillator circuit using BPF, (b) Transient response of circuit in Fig. 8a taken at $V_{out}$, (c) Colpitts chaotic oscillator circuit, (d) Hysteresis loop response of circuit in Fig. 8c taken $L_1$ current vs $V_{out1}$ , (e) Hysteresis loop response of circuit in Fig. 8c taken $V_{out1} - V_{out2}$ Vs $V_{out1}$ , (f) Schmitt trigger circuit, (g) Transient response of circuit in Fig. 8f at $V_{out}$, and, (h) Hysteresis curve output for Fig. 8f.

be written as $f_{cl} = \frac{1}{2\pi C_1\left(W^{-1}(\varnothing(t))\right)}$ and $f_{ch} = \frac{1}{2\pi C_2\left(W^{-1}(\varnothing(t))\right)}$ respectively. The cut-off frequency of HPF and LPF filters can be written as $f_c = 1/\left(2\pi C\left(W^{-1}(\varnothing(t))\right)\right)$. The low and high cut-off frequency of BPF and BRF filters can be written as $f_{cl} = 1/\left(2\pi C_1\left(W^{-1}(\varnothing(t))\right)\right)$ and $f_{ch} = \frac{1}{2\pi C_2\left(W^{-1}(\varnothing(t))\right)}$, respectively [32].

Memristors can be well utilized in Oscillator related circuits. The proposed MRE has been utilized in the BPF oscillator, Colpitts chaotic oscillator, and Schmitt trigger, as as shown in Fig. 8a, 8c, and 8f, respectively.

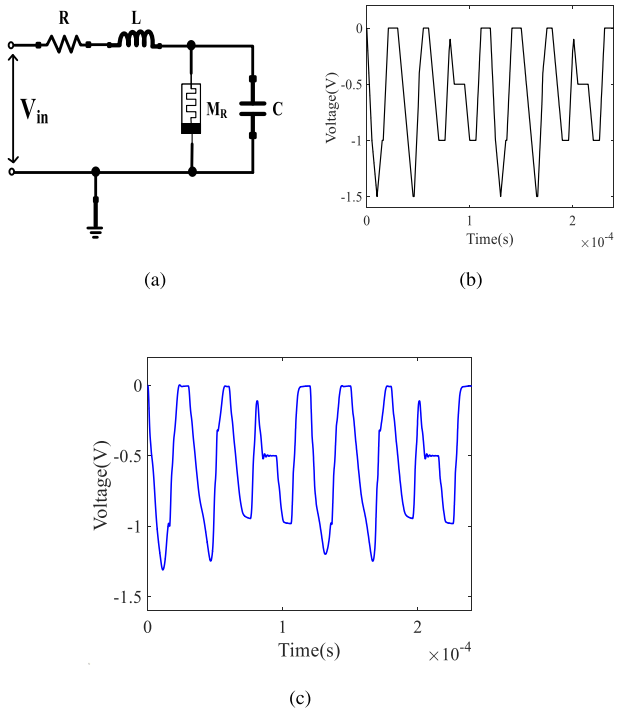


**FIGURE 9.** Proposed MRE possible application. (a) Adaptive amoeba learning circuit, (b) Input voltage as temperature variation (c) Output voltage as locomotive speed.

The transfer function of the Band Pass Filter can be written as $\frac{s\left(W^{-1}(\varnothing(t))C_1\right.}{s^2+s\left(W^{-1}(\emptyset(t))(C_2+C_1)+C_1C_2\left(W^{-1}(\varnothing(t)\right)^2\right.}$ and condition of oscillation is $s\left(\left(1+\frac{R_2}{R_1}\right)\left(W^{-1}(\emptyset(t))C_1-\left(W^{-1}(\emptyset(t))\left(C_2+C_1\right)\right)\right)=0.$

Fig. 8b shows oscillator output taken at $V_{\text{out}}$ as in Fig. 8a. Colpitts chaotic oscillator circuit has been presented with $V_{CC} = 2V$ and $V_{EE} = -2V$. Fig. 8d and 8e show a spiral $C_1/C_2/C_3 = 100pF/1\mu F/1\mu F, L = 10\text{mH}, R_1 = 35\Omega, R_2 = 1.5\text{k}\Omega$, chaotic attractor, plotted against the current at $L$ vs $V_{\text{out }1}$ and $V_{\text{out }2} - V_{\text{out}1}$ vs $V_{\text{out }2}$. A Schmitt trigger circuit shown in Fig. 8f [36], has been analyzed with the integration of the proposed MRE. The supply voltage $(\pm V_{CC})$ is considered for biasing the Op-Amp as $\pm 10$ V. The resistance value $R_1 = 20\text{M}\Omega$ is chosen with the sinusoidal supply of 1kHz and $\pm 1V$. Fig. 8g shows non-inverting Schmitt trigger response. The hysteresis curve is shown in Fig. 8h.

The memristive based systems have the memory computing capability similar to that of the brain, so they can have many applications in neuromorphic computing. A large amoeba-like cell, learns and changes its response, subject to a periodic environmental changes. One of the simplest eukaryotic life, an amoeba, has evolved as a primitive nervous system [50], [51]. This behavior can be mapped to the simple electronic circuit which consists of $R, L, C$ and a memristive system.

As shown in Fig. 9a, an adaptive amoeba learning circuit using proposed MRE has been shown. The oscillations using

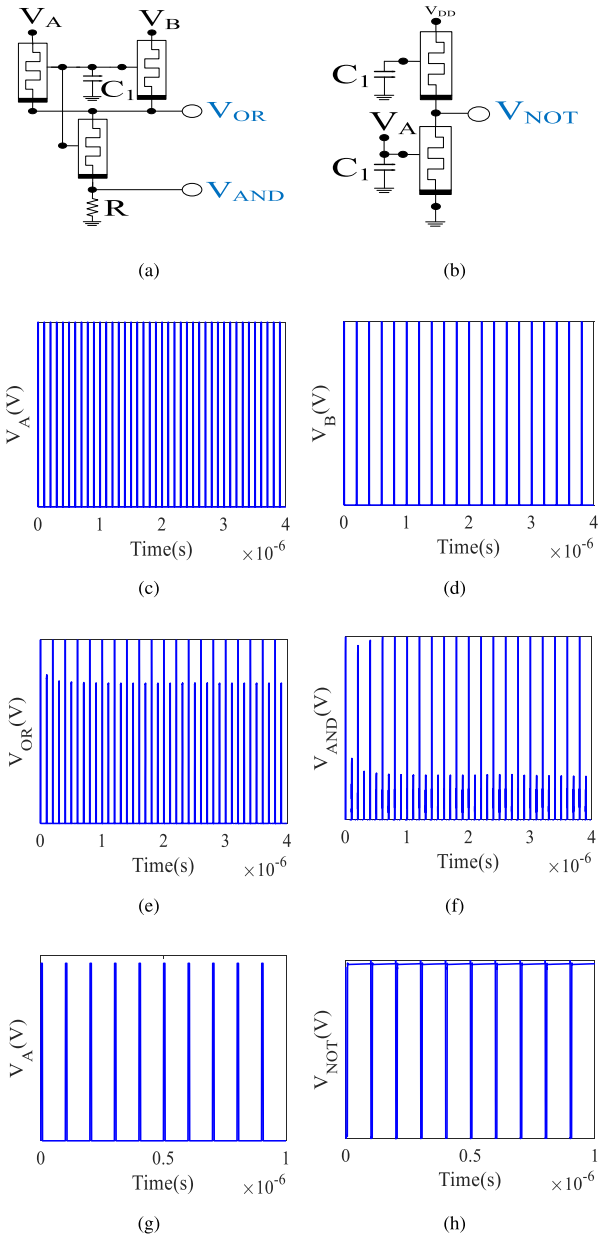


**FIGURE 10.** Proposed new logical gate design using proposed MRE. (a) Logical AND and OR circuit, (b) Logical NOT circuit, (c) Input voltage, $V_A$ with amplitude 1 V, period 100 ns and pulse width 5 ns, (d) Input voltage, $V_B$, with amplitude 1 V, period 200 ns and pulse width 5 ns, (e) OR output, (f) AND output, (g) Input voltage, $V_A$, with amplitude 0.6 V, period 100 ns and pulse width 5 ns, and, (h) NOT output.

$LC$ component can be utilized as the simulation for biological oscillators. The impedance and dissipation inside the amoeba can be simulated using $R$. Proposed MRE can be utilized as the memory mechanism. The temperature variations that impacts the motion of the amoeba has been show here as the external voltage, Vin and presented in Fig. 9b. that controls the circuit. The response of circuit, in Fig. 9c, taken at C shows the behavior or locomotive speed of the amoeba based on stimulus given as $V_{\text{in}}$ . The temperature variations during learning phase makes the amoeba motion slow-moving. This learning behavior has been found in our circuit model. Hence,

**TABLE 2.** The comparison among different memristor emulator.

| Ref. No. | MOSFET Count | Passive Component Count | Experiment Done | Floating/ Grounded | Technology Used | Operating frequency | Power Consumption |
|---|---|---|---|---|---|---|---|
| [13] | 17 | C-1 | Yes | Floating | 0.18 $\mu m$ | $1MHz$ | NA |
| [16] | 16 | R-2, C-1 | Yes | Floating | 0.18 $\mu m$ | $50MHz$ | NA |
| [17] | 40 | R-2, C-1 | No | Grounded | 0.35 $\mu m$ | $1MHz$ | NA |
| [19] | 30 | R-3, C-1 | Yes | both | 0.25 $\mu m$ | $10MHz$ | NA |
| [20] | 16 | C-1 | No | Floating | 0.18 $\mu m$ | $FewHz$ | $8.05\mu W$ |
| [31] | 24 | R-3, C-1 | Yes | Grounded | 0.18 $\mu m$ | $1.7MHz$ | NA |
| [32] | 29 | R-1, C-1 | Yes | Grounded | 0.18 $\mu m$ | $26.3MHz$ | $9.567\mu W$ |
| [34] | 4 | 0 | Yes | Grounded | 0.18 $\mu m$ | $100kHz$ | $40\mu W$ |
| [35] | 3 | 0 | Yes | both | 0.18 $\mu m$ | $20/30MHz$ | 0 |
| [36] | 3 | C-1 | Yes | Floating | 0.18 $\mu m$ | $13MHz$ | 6.725nW |
| [37] | 4 | 0 | Yes | Grounded | 0.18 $\mu m$ | $100MHz$ | NA |
| [38] | 3 | C-1 | No | Grounded | 0.18 $\mu m$ | $100kHz$ | 0 |
| [39] | 7 | C-1 | Yes | Grounded | 0.18 $\mu m$ | $50MHz$ | NA |
| [40] | 6 | C-1 | No | Floating | 0.18 $\mu m$ | $10Hz$ | NA |
| [41] | 7 | 0 | No | Floating | 0.13 $\mu m$ | $1MHz$ | NA |
| [42] | 4 | 0 | Yes | Floating | 0.09 $\mu m$ | $50MHz$ | $2.6\mu W$ |
| [43] | 4 | C-1 | Yes | Floating | 0.18 $\mu m$ | $3MHz$ | $8.24\mu W$ |
| [44] | 9 | C-1 | No | Grounded | 0.045 $\mu m$ | $2kHz$ | NA |
| [46] | 3 | C-1 | Yes | Grounded | 0.18 $\mu m$ | $24MHz$ | 0 |
| [47] | 1 | R-1, C-1 | Yes | both | 0.045 $\mu m$ | $80MHz$ | 0 |
| This work | 4 | C-1 | Yes | both | 0.18 $\mu m$ | $500MHz$ | 0 |
| This Work | 5 | 0 | Yes | both | 0.18 $\mu m$ | $500MHz$ | 0 |

proposed MRE is suitable for adaptive learning models. In Fig. 9a, $R = 1k\Omega$, $L = 1$mH and $C = 100$nC. The responses of amoeba adaptive learning are similar to existing results presented [51].A logical OR-AND gate circuit has been designed using proposed MRE as shown in Fig. 10a. The circuit in Fig. 10a provides both OR and AND output using only 3 proposed MRE, 1 capacitor, 1 resistor and two input voltages $V_A$ and $V_B$, respectively. Using the proposed MRE, a new NOT circuit has been designed, as shown in Fig. 10b, which consists of two MRE, a DC voltage of 1 V and an input voltage, $V_A$. Fig. 10c and 10d, input voltage applied in ORAND circuit. While, Fig. 10e and 10f shows output OR and AND logic circuits, respectively. Similarly, Fig. 10g shows input voltage applied to NOT gate and corresponding inverted output presented in Fig. 10h.

## V. COMPARISON AND DISCUSSION

Table 2 details a comparative summary of selected previous MREs [13], [16], [17], [19], [20], [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], [46], [47] based on active/passive elements, circuit structure, and simulation/experimental validations. MOSFET counts is more in [13], [16], [17], [19], and [20]. The operating frequency is not very high in [32], [33], [34], [35], [36], [37], [38], [39], [40], [41], [42], [43], [44], and [46]. While [42] operates on a high frequency but dissipates certain power. This work presents 4-MOSFET MRE utilizing passive capacitor/MOSCAP which operates on high frequency than all other previous works with zero static power.

## VI. CONCLUSION

Adding to the current research on existing MREs, the proposition of this communication presents a new MRE, which has the following salient features, a combination of which makes it unique.

1) New circuit configuration with DTMOS utilizing modified dynamic threshold feature of MOSFET.
2) A complete mathematical depiction of the MRE considering internal capacitances.
3) No biasing is required.
4) Consumes zero static power.
5) Good operating temperature range ($-30$°C to 100°C).
6) Layout occupying a silicon area of $1305\mu m^2$.
7) Works for all types of load conditions such as resistive, capacitive, inductive, no load and series/parallel combination.
8) Much larger bandwidth ( 500MHz) in comparison to earlier propositions.
9) Works with passive capacitor as well as MOSCAP.
10) Applications in various analog filters such as LPF, BPF, BRF, BPF oscillator, Colpitts chaotic oscillator and adaptive amoeba learning circuit.
11) Two new logical circuit has been designed using proposed MRE. The logical OR & AND realized using

single circuit configuration only and logical NOT has been realized using only memristors which has not been presented before in open literature.

To the authors' best knowledge, the proposed MRE with the above features is unique in open literature so far.

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