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RESEARCH ARTICLE

FPGA Implementation of Nerve Cell Using Izhikevich Neuronal Model as Spike Generator (SG)

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ABSTRACT The neuron is sometimes referred to as the ''head'' or ''central'' cell of the nervous system since it has the ability to communicate with other neurons or cells via electrical impulses. The hardware realization and simulation of these neurons are critical in neuromorphic engineering. In this paper, we made a device that generates 4 different spiking patterns of the nervous system as a Spike Generator (SG) using a hybrid approximation of the target model called the Piece-Wised Power-2 Based Izhikevich Model (PWP2BIM). This proposed model works in a low-cost state to achieve a correct digital implementation of the Izhikevich model, one of the main neuron models (i.e. decreasing hardware resources and enhancing speed and accuracy). The proposed model successfully reproduces the behavioral traits of the initial neuron model. To verify the results of the mathematical simulation, the proposed model was synthesized and implemented on the Zynq XC7Z010 (3CLG400) reconfigurable board (FPGA). The findings of hardware synthesis and applications of the suggested paradigm demonstrate that certain biological behaviors may be duplicated more effectively and at a significantly lower cost. The suggested model's frequency can be increased using this technique (implemented on the Zynq board) at least by 3.6 times compared to the original model, and power consumption can be decreased by 28%. High-frequency design of neuronal models with low-cost attributes is required for application-based types of equipment in case of high-speed operations of these components. Thus, using our approach, the desired goals of application-based features are to be fulfilled. In addition, because the suggested model uses fewer hardware resources than the original model, it is feasible to construct a significantly higher number of neurons (approximately 5 times) on a single Zynq board.

INDEX TERMS Izhikevich, FPGA, digital FPGA realization, neuron, hardware implementation, low-cost.

I. INTRODUCTION

Aspects of neuromorphic engineering have lately been the focus of neuroscientists' investigation. In this area of research, modeling and creating systems that are analogous to the brain is essential to understanding how the brain functions [1], [2], [3], [4]. As a result, it is important to properly study the essential parts of the nervous system. Axons and synaptic terminals link the neurons that make up the brain. The dynamic activity of neuron networks is

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replicated by a variety of neuron models. The intricacy of the mathematics and the biological veracity of these models vary. The simplest method is $I\&F$, which just results in a simple spiking pattern [5]. A collection of simple equations involving two connected variables that produce all spiking patterns is provided by the Izhikevich model [6]. Differential equations with an exponential term are used by the AdEx biological model, [7] to produce spiking patterns. The Wilson model [2] uses a third-order variable, two linked equations, and a third-order variable. The cerebral thalamus is monitored via the Hindmarsh-Rose (HR) model [8], which includes three connected variables with nonlinear internal functions. To describe the onset and development of the squid's large axon action potential, Alan Hodgkin and Andrew Huxley created the Hodgkin-Huxley mathematical model [9]. Condensed versions of the Hodgkin-Huxley (HH) model are used in the FitzHugh-Nagumo (FHN) model, which accurately depicts the deactivation and activation patterns of spiking neurons [10]. The Ca^{2+} and K^{+} conductance-related rhythmic patterns in the large barnacle muscle fiber were accurately reconstructed by the Morris-Lecar model (ML), which was designed by Catherine Morris and Harold Lecar [11].

Two ways enable the implementation of mathematical neuron models on hardware. In the analog case, a circuit that reproduces the descriptive equation set of the neuron model is built using CMOS circuits. These analog realizations take a while to construct, while being rapid and efficient [12]. A different approach is a digital implementation. Digital implementation offers several benefits, including increased flexibility, quick development, low power supply sensitivity, decreased thermal noise, and others. A significant chunk of this technique uses FPGAs [13], [14], [15]. There are different methods to implement FPGA neuronal models such as PWL, Base-2, LUT, etc. [13], [14], [15]. Based on nonlinear function formation and the target neuronal model, one of these approximation methods or a combination of them can be applied for digital FPGA realization.

In the case of approximate calculations, there are some methods. The neuron models and their nonlinear components influence the choice of approximation techniques. Examples include Piece-Wised Linear (PWL), fast dynamic reduction, trigonometry, hyperbolic, power-2, LUT, etc. The total overhead costs may be lower when utilizing the Piece-Wised Linear (PWL) technique, but accuracy will also likely be less as there will be some error levels. One or more differential equations are eliminated using the fast-dynamic-reduced method. Although the overhead costs are decreased in this situation, accuracy may suffer as a result. Trigonometric approximation may be advantageous because of its high precision, but it may increase final FPGA resources and costs. The exponential terms are first transformed to hyperbolic functions in the hyperbolic-based technique before the exponential terms are then changed to power-2-based functions, which might increase overhead expenses. The phrases that can be transformed into shifters, however, have been employed in power-2-based techniques. In this method, all multiplications have been converted into low-cost digital shifters and adders. With the benefits of PWL and precise, low-cost trigonometric approximation, this technique is a good example.

There are similar works in this field of research [1], [16], [17], [18], [19]. The mentioned works use different methods such as Piece-Wised Linear (PWL), hyperbolic-based, COordinate Rotation Digital Computer (CORDIC), and multiplier-based. In [1], the hyperbolic-based method is used. This method is high-accurate and low-cost due to high-matching attributes, but because of converting the exponential terms to base-2 terms, it may reduce the final matching and also, increase the final overhead costs. In [16], the PWL method is applied. The method used in this article can be improved due to its low accuracy (high error due to piecewise linearity). The problem of this method in hardware implementation is to reduce the matching due to its piecewise linearity. In [17] and [18], the CORDIC approach is applied. This method is highly high-accurate and has low error, but also is high-cost and not suitable for large-scale implementation. In [19], the multiplier-based method is considered without any modifications. They have implemented the original model of neurons without the use of any approximation method. Thus, in their realization, the overhead costs will be increased, and the maximum frequency will be reduced, significantly and not suitable for large-scale realization. Also, for recent research in this field [20], [21], [22], [23], although they have acceptable accuracy, they used more hardware resources, and thus are not suitable for large-scale approaches. Finally, in our method, the base-2 approximation is applied. Indeed, using this method, both low-cost implementation and high-accurate attributes are considered suitable for large-scale digital implementation. Finally, in our method, the base-2 approximation is applied. This method is low-cost and high-accurate. Indeed, using this method, both low-cost implementation and high-accurate attributes are considered suitable for large-scale digital implementation.

To achieve an effective digital implementation of the Izhikevich neuron model by reducing hardware resources and increasing speed and accuracy, this study proposes a set of multiplierless mathematical equations using the hybrid approximation method. The behavioral characteristics of the original neuron model are successfully replicated by this model, known as the Piece-Wised Power-2 Based Izhikevich Model (PWP2BIM). Thanks to the methodology's streamlined form of term segments, all high implementation cost operands, such as nonlinear equations, multiplications, and divisions, are converted to the digital shift, addition, and subtraction. The original equations are then implemented digitally on the FPGA using these approximations in conjunction with discretization. The implementation's outcomes show that the proposed model is very precise and closely

TABLE 1. Neuronal parameters produce various spiking patterns.

Neuron Type	a	b	c	d	I
Tonic spiking	0.02	0.20	-65	6	14
Phasic spiking	0.02	0.25	-65	6	0.5
Tonic bursting	0.02	0.20	-50	2	15
Phasic bursting	0.02	0.25	-55	0.05	0.6
Mixed mode	0.02	0.20	-55	4	10
SFA	0.01	0.20	-65	8	15
Class 1	0.02	-.10	-55	6	0
Class 2	0.20	0.26	-65	0	0
Spike latency	0.02	0.20	-65	6	7
Sub. Osc.	0.05	0.26	-60	0	0
Resonator	0.10	0.26	-60	-1	0
Integrator	0.02	-0.10	-55	6	0
Rebound spike	0.03	0.25	-60	4	0
Rebound burst	0.03	0.25	-52	0	0
Threshold variability	0.03	0.25	-60	4	0
Bistability	1	1.50	-60	0	-65
DAP	1	0.20	-60	-21	0
Accomodation	0.02	1	-55	4	0
IIS	-0.02	-1	-60	8	80
IIB	-0.02	-1	-45	0	80

reflects the workings of the original model. The suggested models operate at least 3.6 times more frequently than the original model did. In other words, in this approach, we have used a combined method based on which the accuracy of the system increases, and also considering that only one base-2 term is calculated at any moment, the final speed of the design will increase. Therefore, the two goals of precision and high frequency are achieved.

This paper has the following format. Izhikevich original neuron model is discussed in Section II, and Section III introduces the proposed (PWP2BIM) model. Section IV discusses the hardware implementation procedure. The conclusion is given in Section V.

II. ORIGINAL IZHIKEVICH MODEL

To raise the voltage of biological neurons, Na^+ ions enter the cell. Na^+ ions start pouring into the neuron at a specific moment when the floodgates open. The neuron's internal voltage (spike) is triggered as a result. However, at this point, the K^+ gates open, allowing a large number of K^+ ions to exit the neuron and generate a sharp voltage drop. The membrane potential (V) is the voltage in this situation. The membrane recovery variable (U) is K^+ as well.

In 2003 [4], Izhikevich introduced a brand-new spiking neuron model that simply makes use of two differential equations. These equations use V to represent the neuron's membrane potential, I to represent the synaptic current, and u to represent a membrane recovery parameter that provides negative feedback to the voltage. This model is described by the equations shown below [4]:

$$\begin{cases} \dfrac{dV}{dt} = 0.04V^2 + 5V + 140 - U + I \\ \dfrac{du}{dt} = a(bV - U) \\ if V \geq 30mV, then \begin{cases} V \leftarrow c \\ U \leftarrow U + d \end{cases} \end{cases} \tag{1}$$

The $0.04V^2 + 5V + 140$ was created by modeling the spike initiation dynamics of actual neurons, where V is measured in mV and t is measured in milliseconds. The voltage at rest ranges from -70 to -60 mV.

In the equation (1), the recovery variable U's time scale is described by a, the sensitivity of U to changes in V is described by b, the value of V's after-spike reset, which is typically -65mV, is described by c, and d defines the usual value of U's after-spike reset, which is typically 2.

The four constants (a, b, c, and d) may all be changed to almost all of the brain reactions observed in research studies. As a result, the model is almost as thorough as the Hodkin-Huxley model at a quarter of the calculation cost. This model can reproduce all 20 spiking patterns of the human brain. The mentioned parameter sets for generating all spiking patterns in the Izhikevich neuronal model, Table 1 presents the required fixed parameters for this goal.

The Izhikevich neuron model's nonlinear term, V^2, which forces the original model's realization to be high-cost and low-frequency, poses the fundamental barrier to its digital implementation. Indeed, to increase the speed-up and decrease the overhead costs of FPGA design, this nonlinear term must be modified with a digital-friendly one.

III. PROPOSED PWP2BIM EVALUATIONS

A modified form of the original neuron model is presented in this section. The PWP2BIM approach, which is based on the 4-segment power-2, may be used to approximate nonlinear equations. Accuracy and implementation costs must be balanced in each of the approaches. With this study, we wanted to propose a hardware version of the Izhikevich neuron model that was more accurate and tolerably complicated. Since the selected model is built on transforming nonlinear functions to base-2 functions, there are no multiplication operators in it.

To provide a complete understanding of the recommended technique, we reformulate the voltage equation of the original Izhikevich neuron model as follows:

$$\frac{dV}{dt} = F(V) + 5V + 140 - u + I \tag{2}$$

where

$$F(V) = \begin{cases} 79 \times 2^{-0.027V} - 100; & -78 < V \leq -20 \\ 79 \times 2^{-0.016V} - 83; & -20 < V \leq 0 \\ 79 \times 2^{0.016V} - 83; & 0 < V \leq 20 \\ 79 \times 2^{0.027V} - 100; & 20 < V \leq 32 \end{cases} \tag{3}$$

We can approximate the polynomial nonlinear term with a base-2 function because of the symmetrical structure of this function, which can be seen in Fig. 1(a). On the other hand, considering that the range of voltage changes in Izhikevich's neuron model is between -78 and $+32$, we considered the first part of Fig. 1 in this range to reach an accurate approximation. Also, if we look at equation 3, we can see this symmetry. In fact, the first and fourth rules as well as the second and third rules are symmetrical and only the positive and negative signs of their exponential function arguments change. So, we have a symmetric approximation that can

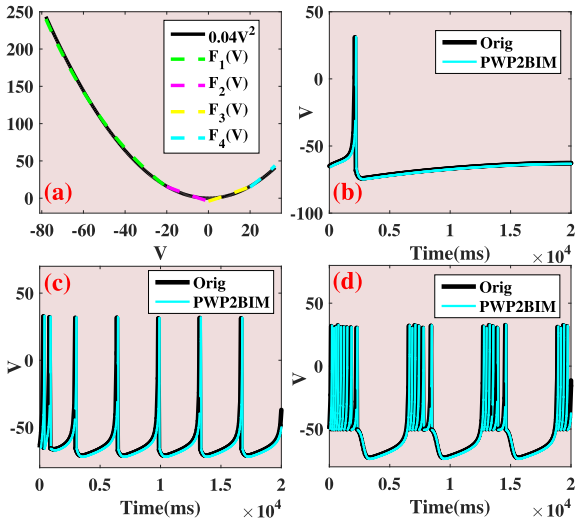

FIGURE 1. (a) Comparing the accuracy of the nonlinear terms of the original and PWP2BIM. (b)-(d) Different spiking patterns of the models.

help reduce hardware costs during digital implementations. This function significantly resembles a base-2 wave. We have extracted optimum parameters based on equation (3) using an exhaustive search method. The scaling parameters were changed to produce a high degree of resemblance and matching between the original polynomial term and the suggested PWP2BIM that is shown in Fig. 1 (based on various input triggers and other constants). Using this method, we were able to create a new PWP2BIM that closely mirrored the original Izhikevich model. On the other hand, utilizing this approximation to easy-to-implement basic operators, all multiplications in the main model can be approximated. The hardware section has further information about this. A claim that has to be looked into and verified is the presentation of this suggested model. Digital shifts and add can be used to create these fixed coefficients base-2 functions, eliminating all multiplications and speeding up the proposed system. The hardware implementation section goes into great depth on how this works.

A. DYNAMICS AND ERROR

The correctness of the proposed model may be assessed using both time domain simulation and dynamic assessment. It is crucial to understand how the two nullclines equations interact to understand how the resting mode becomes the bifurcation mode [14] and [15]. In the nullclines equation, crossings take place around points of equilibrium. This strategy requires us to take into account a dynamic system with two variables.

These points (equilibrium locations) are provided for characterizing the connection of the V and U variables:

$$\begin{cases} W = \dfrac{dV}{dt} = 0.04V^2 + 5V + 140 - U + I \\ Z = \dfrac{dU}{dt} = a(bV - U) \end{cases} \tag{4}$$

TABLE 2. Error values for Izhikevich neuron model.

Izhikevich Variables	RMSE	MAE	Corr%
V	1.631	0.042	94.315
U	0.371	6.952×10^{-3}	88.110
Average	1.001	0.0245	91.2125

The bifurcation analysis of the equilibrium locations requires the Jacobian matrix and eigenvalues [14], [15]. The Jacobian matrix is as follows:

$$J(V, U) = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \tag{5}$$

where

$$\begin{cases} A = \dfrac{\partial W}{\partial V}, & B = \dfrac{\partial W}{\partial U} \\ C = \dfrac{\partial Z}{\partial V}, & D = \dfrac{\partial Z}{\partial U} \end{cases} \tag{6}$$

The shapes of the equilibrium points and phase portraits demonstrate a high level of accuracy. These shapes for different sets of triggers (a, b, c, d, and I) are shown in Fig. 2. As can be seen in this figure, the dynamical behaviors of original and proposed models are compared. In this approach, for three basic patterns (tonic spiking, tonic bursting, and phasic spiking) dynamical shapes and their stability points positions are compared. Moreover, by removing the time scale, phase portrait shapes also have been presented for three mentioned spiking patterns. As can be seen, in these two factors, our proposed model can follow the original model, accurately.

B. ERROR ARITHMETIC

Fig. 1 and Fig. 2 show how well the provided model reproduces the actions of the original model. Three key methods–MAE (Mean Absolute Error), RMSE (Root Mean Square Error), and Corr (Correlation)–were used to estimate the numerical values of the error to assess the recommended model's soundness in this section [13], [14], [15]. The numbers for the 3 faults listed for the Izhikevich neuron model can be found in Table 2.

C. NETWORK BEHAVIOR

Another method for validating the accuracy of the proposed model is a Raster plot for 1000 connected neurons. In this method, neurons are randomly coupled to each other and are classified as either excitatory or inhibitory, 4 to 1. We have used the MRE error criterion to check and analyze the accuracy of the proposed model in this method. By calculating and comparing the amount of this error in Raster Plot with previous similar articles and works, it is quite clear that the amount of this error is at a very good level and this is another confirmation of the accuracy of the proposed model presented in this article. The enhanced model is used at the network scale by simulating a network with 1000 randomly linked neurons. Fig. 3 displays the simulations' raster graphs. There are several structural parallels between the PWP2BIM and

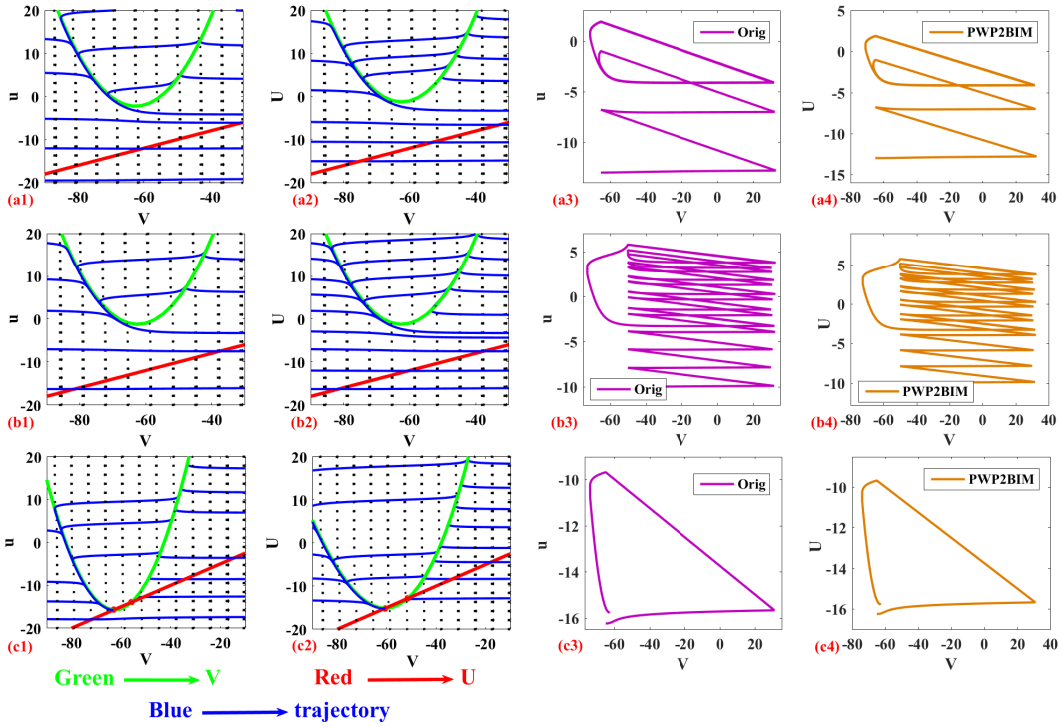

FIGURE 2. (a1)-(a4) Dynamics and phase portraits for tonic spiking (original and proposed PWP2BIM models). (b1)-(b4) Dynamics and phase portraits for tonic bursting (original and proposed PWP2BIM models). (c1)-(c4) Dynamics and phase portraits for phasic spiking (original and proposed PWP2BIM models).

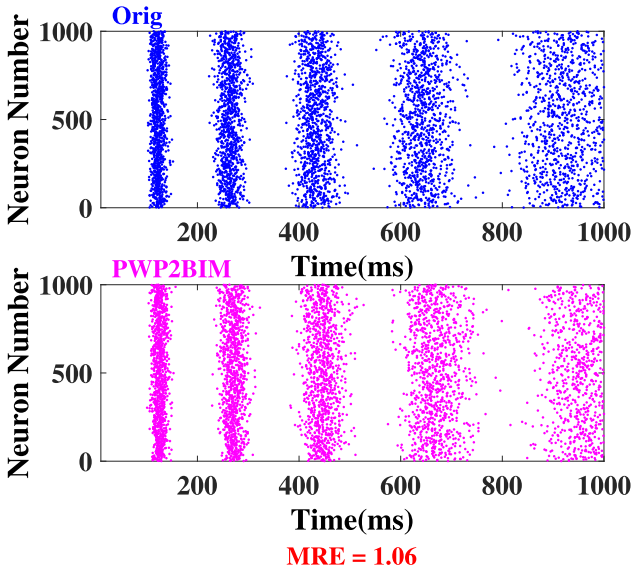

FIGURE 3. Raster plot representation of the original and proposed models. Blue corresponds to the original model and pink corresponds to the proposed model (PWP2BIM).

the original network behaviors model. As can be depicted in this figure, we have simulated 1000 randomly connected original and proposed Izhikevich neuron, separately to test the population behaviors. Indeed, in this test, neurons will be desynchronized in time duration. Thus, this behavior must be evaluated between original and proposed models to validate the simulation of neuron network in low-error states. The original and proposed network behavior models are contrasted using Mean Relative Error (MRE). The value of this error parameter is also shown in Fig. 3. Fig. 3's error levels and the behavior of the original and suggested models at the network size are comparable, which provides further evidence of the suggested model's correctness.

IV. HARDWARE PROCEDURE

In this part, the Izhikevich neuron model is presented together with a low-cost digital hardware architecture. We must first choose the bit width for the digital implementation before we can execute this idea. It is crucial to choose the bit width in such a way as to prevent overflow with left and right shifts. In the second stage, the differential equations are discretized using the Euler technique, and the architectural diagram is generated for every variable. Prior to being implemented on the Zynq FPGA device, the scheduling diagrams must first be evaluated using the Hardware Description Language (HDL) in the third phase. The details of these acts are listed below.

A. DISCRETE METHOD

To adapt the suggested model to the FPGA board, the equations are discretized. The Euler method is used in this discretization. With two typical variables (Y and J), the Euler technique is:

$$\frac{dY}{dt} = J(t) \tag{7}$$

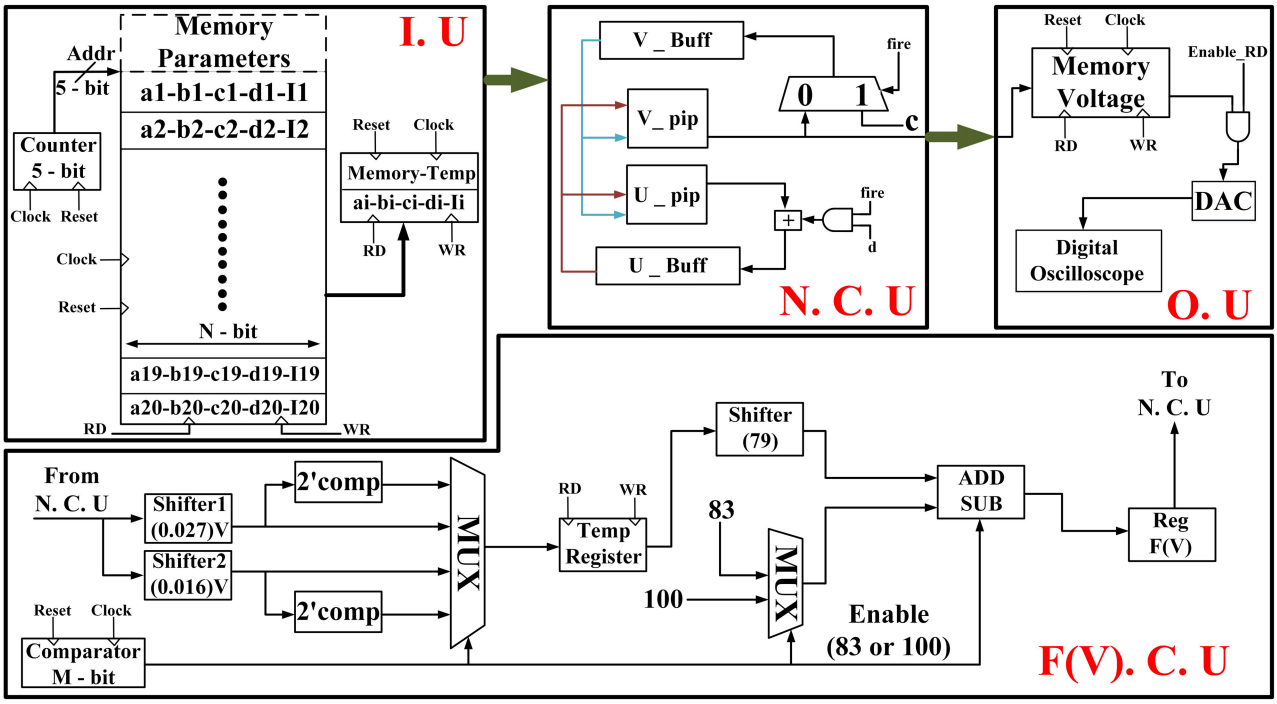

FIGURE 4. Proposed model's overall structure.

where

$$\frac{Y[i+1]-Y[i]}{dt} = J(t) \longrightarrow Y[i+1] = Y[i] + dtJ(t) \quad (8)$$

It should be noted that dt (time step) in discretized equations is equal to $\frac{1}{128}$, which can be digitally achieved with a 7-bit shift to the right.

B. SET THE BIT-WIDTH

We estimate the final bit-width in our suggested neuron models to be 31 bits, with 10 bits for the integer, 20 bits for the fraction, and 1 bit for the sign. Based on the biggest and smallest constant values, the number of bits (as a function of the greatest left and right shift), and the requirement to avoid any overflow, this is done.

C. PWP2BIM OVERALL STRUCTURE

Fig. 4 shows the proposed model's overall structure. This structure is composed of different blocks which are connected. As can be seen in Fig. 4, the first unit of this structure is the Input Unit (IU). This unit is responsible for generating the required parameters for all spiking patterns of the Izhikevich model. This is the information storage part and the required parameters of the proposed neuron model, which are included in a memory along with the values of the spike shape coefficients. This memory has 20 sections where the corresponding coefficients of 20 spiking modes are stored. We considered a counter for this memory that selects one of the constant coefficient values at each moment and sends it to a final temporary memory. The values of these 20 modes of coefficients are included in our hardware code and stored digitally so that we can select one of the parameter sets if needed.

Moreover, the Neuron Calculation Unit (NCU) is presented to calculate the final voltage signal based on the proposed PWP2BIM equations. The main signals of our proposed neuron are generated in this section. As seen in this section, we have used four memories. Two memories are for the original values of the neuron signals, and the other two memories are for storing return signals (according to the design of the pipeline, the signals are stored recursively to increase the hardware execution speed). Also, we used logic gates and multiplexers to control the conditional rule of the neuron model.

On the other hand, the F(V) Calculation Unit (F(V) CU) is designed to calculate the different values of the proposed internal function, F(V). This has the task of providing the internal signals and functions as well as the controller for the proposed neuron model. In fact, according to the approximation of non-linear functions in the proposed model, the production of these functions and the required signals is the responsibility of this department.

Finally, the voltage data is produced in the Output Unit (OU) with DAC. This is responsible for producing the final output on the oscilloscope. Our main signal in the neuron model is the voltage, which we considered a temporary memory for this signal. The output of this memory is rationalized with an activation signal so that we can control the generated output and send it to the oscilloscope at the right time. Finally, using a digital-to-analog converter (DAC), we can display the final information required on the oscilloscope.

It is noticeable that we have presented this architecture based on approximate equations as well as pipelining method. Using this architecture, we write our Hardware Description Language (HDL) code and observe the output signals after digital synthesis using an analog-to-digital converter. Using the pipelining method increases the hardware execution speed and thus increases the final frequency. Also, due to the use of the base-2 method in approximation equations, in addition to increasing the speed of implementation, the hardware resources used are significantly reduced. Therefore, based on the proposed architecture in Fig. 4 and the optimality of the approximate equations, we can achieve a low-cost and high-speed implementation.

D. RESULTS

The results of the Izhikevich neuron model's hardware digital implementation are shown in this section. On the FPGA platform Zynq XC7Z010 (3CLG400), the proposed PWP2BIM was developed. Due to the high processing power and having a large number of hardware resources, we have used the Zynq board to implement the proposed model so that in addition to having a high frequency, we can implement more neurons on a single FPGA (optimal digital implementation). Verilog (Hardware Description Language) was used to synthesize the models in the Xilinx ISE software. In the part of the implementation, we have employed the proposed approach for realizing a Spike Generator (SG) based on the PWP2BIM which provides 4 basic spiking patterns of the Izhikevich neuron model, as shown in Fig. 5. A collection of hardware-based physical realizations are shown in this picture. Significantly, the scales for implementation (voltage and time) and simulation are the same. The original model, as described above and shown by equation (1), makes heavy use of nonlinear functions. According to the hardware FPGA board used in our work, we have provided four spiking patterns based on the 4 main keys embedded on the board. In fact, our proposed model can generate all spiking patterns. These phrases, which are expensive to implement on hardware, have all been replaced in the suggested model with functions that are far more affordable to do so. By using this method, fewer hardware resources were used, and the frequency of FPGA operations increased (compared to the original model and any other versions that could be offered). Table 3 compares the suggested technique with the previously published studies and displays the hardware resources needed, frequency, power consumption, and Maximum Number of Neurons that may be implemented on the Zynq board (denoted by MNON). The comparison of resource usage provided in the aforementioned table clearly shows how much fewer hardware resources were used in the suggested model when compared to the original model and other proposed models that were offered. In this implementation, the results of the implementation table are based on the production of 4 different spiking patterns simultaneously on the FPGA board. According to the results of hardware synthesis and model implementations, it is possible to duplicate many biological behaviors more effectively and for significantly less hardware cost. Additionally, this method can increase the frequency of the suggested models by up to 3.6 times that of the original model and reduce power consumption by about 28% when compared to earlier similar attempts. Additionally, the proposed model's reduced use of hardware resources makes it possible to implement a significantly higher number of neurons (5 times compared to the original model) on an FPGA board. As a conclusion of the presented topic, we can point out the important issue that the implementation of biological neural networks and neural models on hardware can be of great help in the field of studying diseases and their treatment. In this field, there have been researches that have focused on diseases, hardware implementation with high accuracy, and neural networks [24], [25], [26], [27], [28], [29]. Having practical and low-cost hardware, which, of course, has a high operating speed, we can examine neuro-brain diseases such as Epilepsy, Alzheimer's, Parkinson's, etc., and provide practical solutions. The resource level in one FPGA core determines the number of neurons implemented. Indeed, this number can be limited by a maximum number of FPGA resources for two original and PWP2BIM models. Thus, the Resource Utilization Percentage (RUP) factor is presented for each resource as:

$$RUP(percentage) = \frac{Target\ \ Resources}{Full\ \ Resources} \tag{9}$$

In this case, the Maximum Resource Utilization Percentage (MRUP) is given as:

$$MRUP = Maximum\ RUP\ in\ [FPGA\ Resources] \tag{10}$$

By MRUP, the maximum number of original and PWP2BIM can be calculated on one FPGA core. In this approach, the FPGA Resources can be selected by the maximum percentage of the basic resources of FPGA core as *Slices*, *FFs*, *LUTs*, and *DSPs*. The parameter of maximum neuron number is calculated using the Maximum Number of Neurons (MNON) as the following equation:

$$MNON = \frac{100}{MRUP} \tag{11}$$

These numbers for original and PWP2BIM for different FPGA devices are presented in the last column of Table 3. As data indicates, the number of PWP2BIM models that could be implemented on FPGA is higher than that of other similar models. As depicted in this table, in our proposed model, the speed level (frequency) and also, the overhead cost are in better condition compared with the original model. It is noticeable that the parameter *MNON* is a basic factor for scaling the number of implemented PWP2BIM on one FPGA core. Indeed, multiplier modules increase the system cost leading to the high-area network. In this case, in our PWP2BIM model, all nonlinear and high-cost terms such as multipliers and dividers are eliminated to have a high-speed digital design. Indeed, multiplier-based realization causes

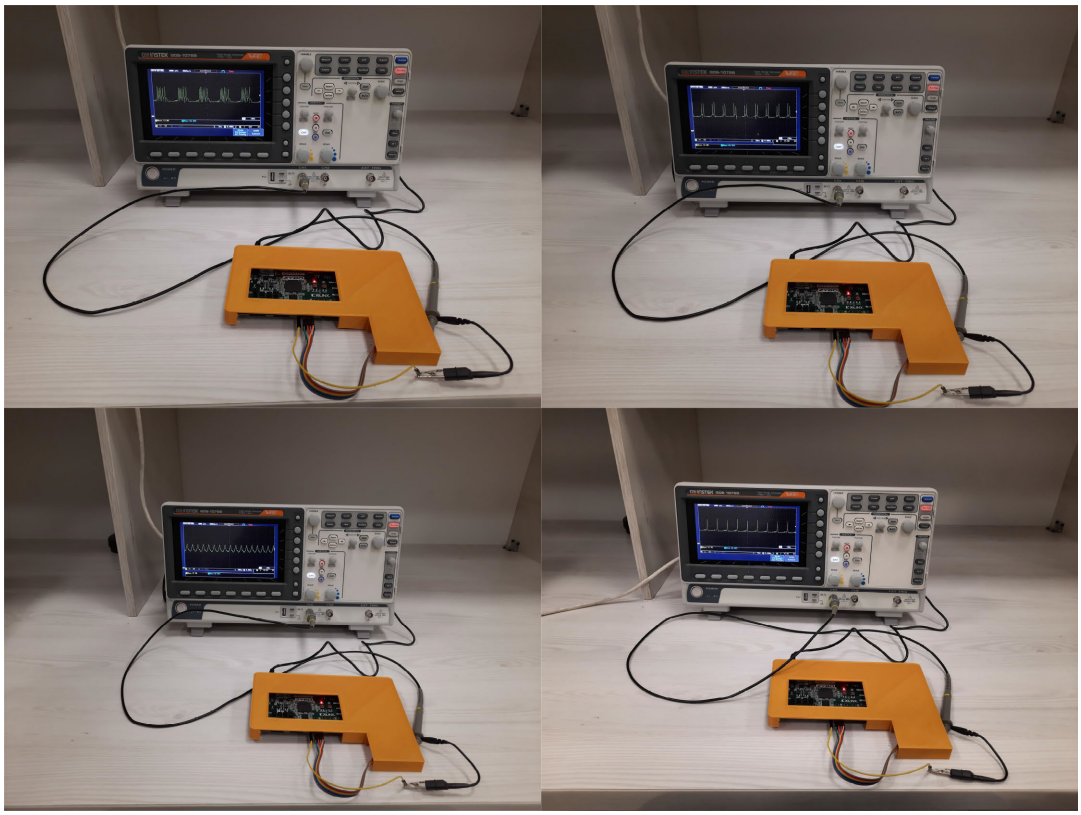

FIGURE 5. Implementation set of PWP2BIM as physical SG.

TABLE 3. Comparison between proposed method and previously published works for the Izhikevich neuron model. The references that not reported the value, is presented as N. R.

Reference	Slice Registers	Slice LUTs	Occupied Slices	DSP 48A	Frequency	Power Consumption	MNON	Device
Soleimani *et al.* **[16]**	493	617	N. R	0	241.9MHz	N. R	N. R	Virtex-II
Haghiri *et al.* **[1]**	490	459	N. R	N. R	240MHz	N. R	N. R	Virtex-II
Heidarpour*et al.* **[17]**	829	1221	N. R	0	134.3MHz	N. R	N. R	Spartan-6
Heidarpur *et al.* **[18]**	280	469	N. R	0	212.8MHz	0.071W	N. R	Spartan-6
Grassia *et al.* **[19]**	646	1048	N. R	11	105MHz	N. R	N. R	Virtex-5
Ghanbarpour *et al.* **[20]**	153	173	84	0	741.65MHz	0.08W	52	Zynq
Hedayatpour *et al.***[21]**	443	649	N. R	N. R	103MHz	N. R	N. R	Spartan 6
Wang *et al.***[22]**	648	1991	N. R	N. R	112.6MHz	0.0046W	N. R	Zynq
Leigh *et al.***[23]**	217	451	N. R	4	249.25MHz	0.007W	N. R	Spartan 7
Original Model	284	289	91	7	185.943MHz	0.10W	11	Zynq
This Work	139	151	79	0	673.112MHz	0.072W	55	Zynq
This Work	131	143	256	0	589.10MHz	0.065W	7	Virtex-II
This Work	133	148	289	0	573.21MHz	0.061W	2	Spartan-6
This Work	139	150	249	0	601.47MHz	0.067W	11	Virtex-5

the low-speed and high-cost system for the original model because of its large number of multipliers and dividers in the internal functions. This leads to a low-frequency system because of its long critical paths in the circuit implementation.

As presented in Table 3, our proposed model has been compared with most similar articles and methods. We have made the proposed model 3.6 times faster than the original model, but at the same time, our proposed model is more favorable than all previous similar works in terms of the number of hardware resources consumed. On the other hand, it is the issue of implementing the maximum number of adapted neurons in a board, which has been improved for our proposed model compared to the original model and all previous models.

V. CONCLUSION

The Izhikevich neuron model is used in this work and is digitally implemented without the need for multiplication. This solution accurately and consistently reproduces the biological behavior of the original models using an optimized hybrid approximation technique. This improved method may faithfully reproduce the nonlinear functions of various neuron models, in which the conventional approximation techniques (such as piecewise-linear, hyperbolic, etc.) may

fail to perform as well. By eliminating the nonlinear functions from the original model, we were able to get the estimated model. High frequency and low hardware cost are two features that may be attained with the right implementation. Using only SHIFT, ADD, and SUB modules, we were able to accomplish both of them when designing digital hardware. The recommended models accurately mimic the actual models' various spiking patterns and dynamics. The suggested model can increase frequency by at least up to 3.6 times in comparison to the previous model, according to the findings of FPGA implementation, and lower power consumption by roughly 28%. Additionally, the outcomes demonstrate that the proposed models outperform earlier implementations of related models in terms of maximum frequency and FPGA resource use.

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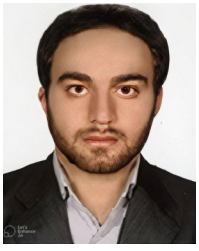

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