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RESEARCH ARTICLE

Enabling an On-Demand Frequency Doubling Mechanism Through a Capacitively Loaded Miniaturized Diplexer

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ABSTRACT This paper presents a diplexer design that generates a pair of fundamental and harmonic frequencies. The diplexer is based on a capacitively loaded resonator that is able to reconfigure its frequency pair with respect to capacitive loading. The system shows a fundamental and harmonic frequency pair of 5 GHz and 10 GHz without any capacitive loading and 2.5 GHz and 5 GHz when loaded with a 1pF/0.5 pF capacitor pair. The complete system is fabricated and tested where good agreement is obtained between the measured and computed results. The testing is performed for the two states of the diplexer, when the diplexer is unloaded and after loading it with the capacitor pairs. For both unloaded and loaded scenarios, the proposed design produces a maximum insertion loss of 0.6 dB with an isolation of at least 35 dB at the corresponding operational frequencies. The structure is also able to provide a minimum return loss of 25 dB at each port. The proposed diplexer is then integrated with a frequency doubler chip and the full system maintains an acceptable efficiency along with a high conversion gain of approximately 15 dB.

INDEX TERMS Diplexer, frequency doubling, resonators, miniaturization, capacitively loaded diplexer.

I. INTRODUCTION

The massive development of the Internet of Things has necessitated the design and implementation of new communication modules [1], [2], [3], [4] and sensing devices [5], [6], [7], [8], [9], [10], [11]. These devices are responsive to a variety of stimuli including human activity recognition [5], structural monitoring [6], and smart agriculture/farming [7]. In addition, the importance of wireless sensing in monitoring various parameters such as solar energy [8], biomarkers [9], humidity [10], or temperature [12] has been well established. All these Internet of Things devices that are implemented for communication or sensing may require diplexers at their core. Diplexers can be integrated in the design of tunable multifunction devices using silicone [12], or voltage-controlled meta-structure using liquid crystal [13] for communication purposes. Moreover, they can be implemented in sensing using electromagnetically induced absorption structures [14].

The purpose of this work is to introduce a capacitively loaded miniaturized diplexer that finds its application in harmonic radars. Harmonic radars and transponder-based systems have been proposed to solve the issues related to single frequency sensing architectures [15]. More specifically, when a radar interrogates a transponder at a fundamental frequency of f_0, the receiving transponder accepts the signal and transmits it back at a higher harmonic (mainly $2f_0$ [16]), which can be in turn detected by the original transmitting radar. Such technology [17] has advanced significantly since its emergence with many applications that can benefit from its implementation [18], [19], [20]. The adopted fundamental frequency varies depending on the application and technology. For example, the avalanche detector in [20]

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utilizes 0.917 GHz as a fundamental frequency whereas insect tracking applications [21], [22] operate using maritime radar frequencies ($f_0 \approx 9.4$ GHz) or at the ISM band (f_0 being 2.45, 5.8, or 5.9 GHz [23], [24]).

In this paper, a radio frequency resonator-based diplexer is proposed. Capacitively loading the diplexer enables its operation at a different frequency without modifying the structure's electrical length. In addition, the diplexer is integrated with a frequency doubler to achieve an on-demand harmonic frequency generation. Hence, for every pair of capacitive loading with a capacitive ratio of 2, the diplexer generates a different fundamental frequency as well as its corresponding harmonic frequency.

The proposed diplexer relies on generating the harmonic frequency on an active integrated frequency multiplier chip. The choice of a multiplier chip instead of a Schottky diode enables the circuit to evade the high conversion losses of the diode and ensures that high-power levels can be achieved. As a result, in this paper, we present a radio frequency diplexer that features two states of operation. The first state occurs when the diplexer is unloaded by any capacitor, thus ensuring an operation at 5 GHz and 10 GHz. The second state is when a pair of capacitors are integrated within the diplexer circuit. Such integration enforces the diplexer to operate over a lower frequency along its harmonic. Hence, this system is triggered by a variety of capacitive loading pairs and exhibits its detection through a generation of a unique fundamental frequency along its harmonic.

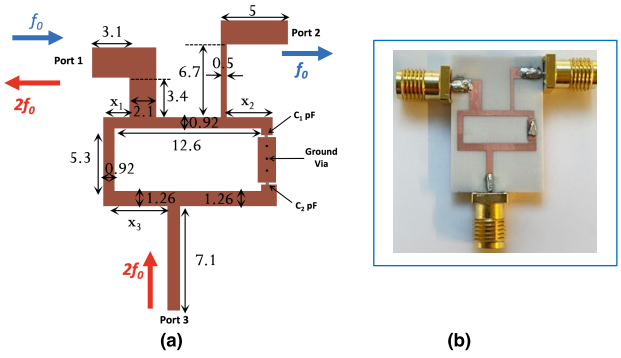

FIGURE 1. (a) The detailed dimensions of the proposed diplexer structure to sustain frequency doubling generation, (b) The corresponding fabricated prototype.

II. PROPOSED DIPLEXER DESIGN

The proposed RF diplexer is composed of one single common resonator section that is designed to ensure frequency operation at f_0 and $2f_0$ [25]. The diplexer is a modified stepped impedance resonator with a simplified topology composed of only two transmission lines. The modified topology is incorporated to ensure that it achieves a reconfigurable response when loaded by a capacitive load. In fact, the variable impedance resonator with the modified impedances and dimensions achieves similar performance as the half-wavelength stepped impedance resonator. In this case, the impedance ratio $k = Z_2/Z_1$ is > 1, which guarantees the generation of the fundamental as well as the first harmonic. Fig. 1(a) shows the detailed design of the presented diplexer where Z_1 is the impedance of the transmission line with a width of 0.92 mm and fed by port 1 and it is connected to output port 2. Z_2 is the impedance of the transmission line with a width of 1.26 mm and connected to the output port 3. The two output ports (ports 2 and 3) are connected to the core element through transmission lines of varying characteristic impedances. The choice of the appropriate impedances is tailored to achieve good matching at each output port and to enable an on-demand frequency generation. To that extent, this proposed modified topology reduces the number of resonators while maintaining the proper filtering properties of the structure.

The diplexer is designed using the dielectric substrate RO4003C with a dielectric constant of 3.55, a thickness of 0.81 mm, and a loss tangent of 0.0027. Port 1 is the common port and must be strongly coupled to ports 2 and 3 at f_0 and $2f_0$, respectively. Ports 2 and 3 must always be isolated at both frequencies. In addition, it is important to note that the locations of the three ports around the resonator are optimized. By tuning the distances of the ports from the edges of the resonator (i.e., x1, x2, and x3 in Fig. 1(a)), a desired operating pair of frequencies can be achieved while ensuring strong coupling and suppression of the desired modes simultaneously. In this work, we have determined x1 = 1.88 mm, x2 = 2.59 mm, and x3 = 4.25 mm. The detailed dimensions of the various parts that compose the diplexer are also included in the layout of the structure in Fig. 1(a). It is important to note that all the physical dimensions are varied iteratively until an acceptable behavior is obtained. More specifically, the main goal is to ensure that port 1 is simultaneously matched at 5 GHz and 10 GHz whereas ports 2 and 3 are matched at 5 GHz and 10 GHz respectively. Also, ports 1 and 2 are coupled at 5 GHz; ports 1 and 3 are coupled at 10 GHz while simultaneously ensuring that ports 2 and 3 are isolated at both frequencies.

A. SENSING THE CAPACITIVE LOADS

The diplexer is loaded at the resonator's edge with two capacitors (C_1, C_2) to study their effect. To ensure that the structure operates at exactly f_0 and $2f_0$, the ratio C_2/C_1 is enforced to be always equal to 2. The two capacitors (C_1, C_2) are integrated along the two open ends of the structure as also highlighted in Fig. 1(a). The grounding of the two integrated capacitors is done through three 0.2 mm diameter vias that connect the circuit to the substrate's bottom ground layer. The diplexer in the unloaded scenario is designed by accounting for the metallic pad along the three 0.2 mm diameter vias that are used to ground one end of the two integrated chip capacitors. Accordingly, the corresponding parasitic capacitance is accounted for during the design process of the unloaded structure. Fig. 2(a) shows the simulated transmission coefficients between port 1 and port 2 while Fig. 2(b) shows the transmission coefficients between port 1 and port 3. These transmission coefficients are generated

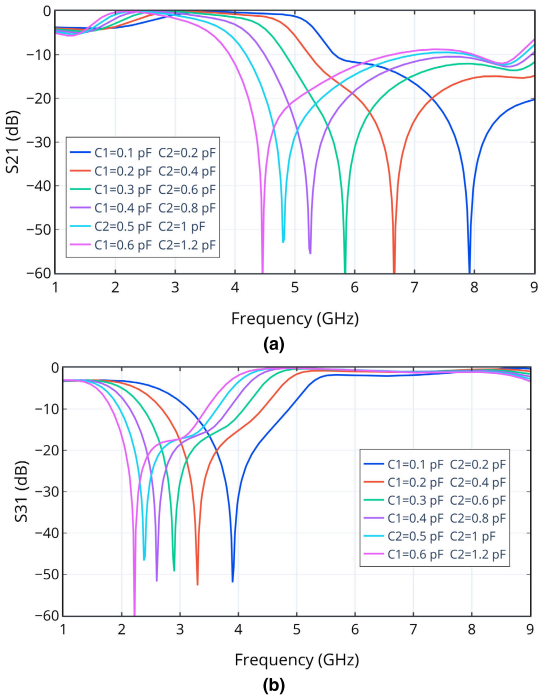

FIGURE 2. (a) The transmission coefficients for different load capacitor values between ports 1 and 2, and (b) ports 1 and 3.

after loading the diplexer with different values of capacitors. It can be noticed that capacitive loading results in lowering the structure's frequency of operation. For example, loading the diplexer with $C_1 = 0.5$ pF and $C_2 = 1$ pF decreases its operating frequency from 5 GHz and 10 GHz to 2.5 GHz and 5 GHz, thus reducing it by half. In addition, the transmission coefficient results indicate that the higher the capacitance values are, the lower the frequencies become. Accordingly, by varying the pair of capacitors an on-demand generation of different fundamental and harmonic frequencies is achieved. The operation of the proposed diplexer is validated under the two modes of operation shown in Fig. 3. More specifically, it is tested when it is kept open without any capacitive loading and after integrating the two capacitor pairs of 0.5 pF and 1 pF. Accordingly, one diplexer is fabricated for testing as shown in Fig. 1(b). The comparison between the simulated and measured S-parameters are presented in Fig. 4. More specifically, Fig. 4(a) shows the various S-parameters when the diplexer is not loaded by any capacitors. The diplexer operates at 5 and 10 GHz with almost complete transmission between port 1 and port 2 at 5 GHz while this behavior is obtained between port 1 and port 3 at 10 GHz. On the other hand, Fig. 4(b) shows the comparison between the simulated and measured S-parameters after loading it with the (0.5 pF, 1 pF) capacitors pairs.

The structure retains its functionality while shifting its frequency of operation to 2.5 and 5 GHz, respectively. Hence, by monitoring the operational frequencies of the diplexer, the capacitive pair loading can be deduced. The agreement between the simulated and measured results proves the validity of the proposed approach in achieving a miniaturized diplexer through a capacitive loading effect. It is important to note that the fabricated diplexer shows similar measured performance behavior to the data presented in Fig. 2 for the different values of the pair of capacitors.

A comparison between the proposed diplexer herein and commercially available ones is summarized in Table 1(a). In addition, Table 1(b) compares the work presented in this paper and other recent work available in the literature. Such comparison considers various parameters including the operational frequencies, the insertion loss of the design as well as the corresponding return loss, and the adopted technology used in the fabrication of the prototype. It is important to note that the proposed design stands in its ability to achieve an on-demand frequency doubling by reconfiguring its capacitive loads. Such capacitive loading also achieves a miniaturized design in comparison to an unloaded structure operating at the same span of frequencies.

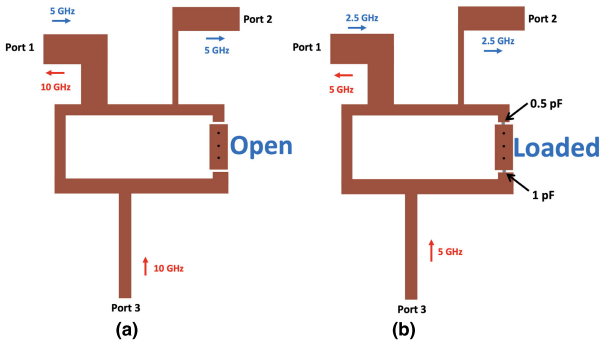

FIGURE 3. The two investigated modes of operation of the proposed diplexer: (a) Unloaded state, (b) Loaded with a capacitor pair of 0.5pF and 1 pF.

III. FREQUENCY DOUBLING SENSING

To further validate the operation of the proposed capacitively loaded miniaturized diplexer, a frequency doubler is connected between the two output ports of the design presented in section II. The corresponding frequency doubler chip used in this work is "XX1002-QH" from MACOM [29]. This chip combines an active doubler with an output buffer amplifier that delivers constant power over a range of input powers. The integrated frequency doubler requires a single positive bias supply of 5V. Fig. 5(a) shows the complete circuitry consisting of the proposed diplexer and the chip's landing pads along with the biasing network needed to supply the required DC current.

The design of the diplexer along with the integration of the frequency doubler chip were performed using ADS Keysight electromagnetic simulation and co-simulation in the layout. The integrated chip consists of three working ports: RF input, RF output, and a biasing port. The rest of the pins are grounded. To connect the frequency doubler to the diplexer, extensions of ports 2 and 3 are carefully designed and their line widths are optimized to maintain a 50 Ω matching at the end of lines after adding the chip. These multi-section

TABLE 1. The comparison of the proposed design with (a) commercial diplexers and (b) available diplexers in the literature.

(a)

Reference	Low-Pass Port (GHz)	High-Pass Port (GHz)	Return Loss (dB)	Insertion Loss (dB)	Isolation (dB)	Reconfigurable
ZDSS-5G6G [26]	DC-5	6-20	8	3	20	No
AE4300 [27]	DC-4.3	4.7-9	10.88	1	50	No
DPX162690DT [28]	1.88-1.92	2.496-2.69	16.5	1.2	13.4	No
Our Work	2-3/4-5.5	4-6/8-11	25	0.6	35	Yes

(b)

Reference	Center Frequency (GHz)	Reconfigurable	Insertion Loss (dB)	Return Loss (dB)	Technology
[30]	1.8 / 2.1	No	0.7	23	Waveguide
[31]	1.5 / 2.7	No	1.5	20	Multi-layer PCB
[32]	1.51, 2.41 / 1.92, 2.85	No	0.55	15	PCB
Our Work	5,10 / 2.5, 5	Yes	0.6	25	PCB

transmission lines are optimized to ensure a good matching for the two cases when the diplexer is unloaded and then loaded with $C_1 = 0.5$ pF and $C_2 = 1$ pF capacitors. The corresponding fabricated circuit is presented in Fig. 5(b).

In the proposed overall design, port 1 connects to the diplexer's input, through which the fundamental signal is injected into the circuit. Due to the strong coupling between ports 1 and 2 of the diplexer, the injected fundamental signal f_0 reaches port 2. Subsequently, it goes through the doubler chip and generates the second harmonic which reaches port 3. At the second harmonic frequency, $2f_0$, ports 3 and 1 are strongly coupled. Accordingly, the second harmonic signal reaches port 1 and is extracted from the diplexer. The smooth signal transmission also relies on the strong suppression of the fundamental and second harmonics between ports 2 and 3 of the diplexer.

As illustrated in the fabricated prototype shown in Fig. 5(b), there is only one port handling both the receiving and transmitting signals. A scattering parameter measurement is first carried out at this port to ensure that impedance matching is maintained at the corresponding frequencies after incorporating the frequency doubler with and without the two integrated capacitors. In fact, when the diplexer is loaded with 0.5 pF and 1 pF, port 1 is always matched at 2.5 GHz and 5 GHz with an S_{11} magnitude of –10.81 dB and −10.53 dB respectively. On the other hand, when the diplexer is open (no capacitors connected), port 1 remains matched at 10 GHz but is no longer matched at the fundamental frequency of 5 GHz. The diplexer is perfectly matched at 4.45 GHz and 8.9 GHz with a reflection coefficient of −24.5 dB and −21 dB. These two frequencies become the new operating frequencies when (1) no capacitors are connected to the diplexer and when (2) the diplexer is connected to the frequency doubler chip.

Since one port is shared by the transmitting and receiving signals, a directional coupler is necessary to detect the output second-harmonic power level during testing. Fig. 5(c) displays the block diagram of the measurement setup including the power transfer at the two frequencies. The signal generator connects to port 2 of the bi-directional coupler where the signal at the fundamental frequency f_0 is generated. This signal reaches port 1 of the coupler which is connected to the input port of the diplexer. The diplexer's

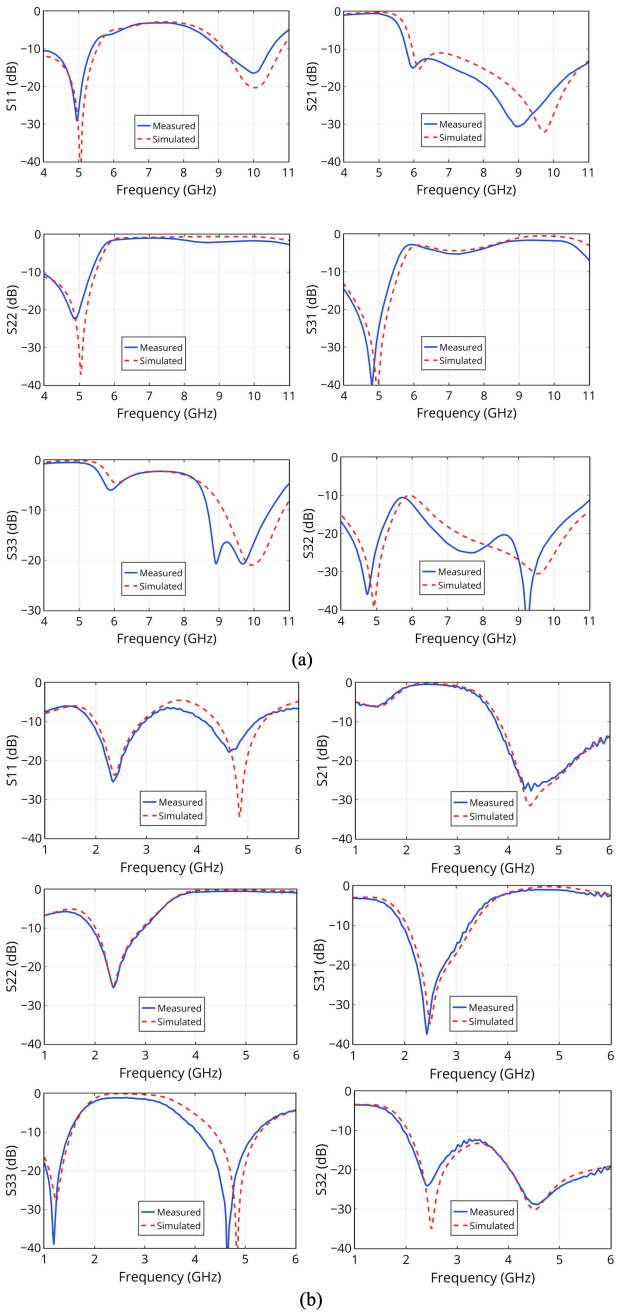

FIGURE 4. The simulated and measured S-parameters of the proposed diplexer: (a) when no capacitors are connected (b) with C1 = 0.5 pF and C2 = 1 pF.

doubler chip generates the second harmonic signal $2f_0$ and is coupled to port 3 of the coupler, which is in turn connected to the spectrum analyzer where the generated second-harmonic power level is displayed. The experimental realized setup is presented in Fig. 5(d) where a 20 dB directional coupler operating between 1 GHz and 20 GHz is employed to carry the measurements. It is important to mention that the frequency doubler requires a minimum of −3 dBm of input RF power. This measurement is performed to validate the operation of the proposed design in sensing applications such as harmonic radar for both the unloaded and loaded scenarios.

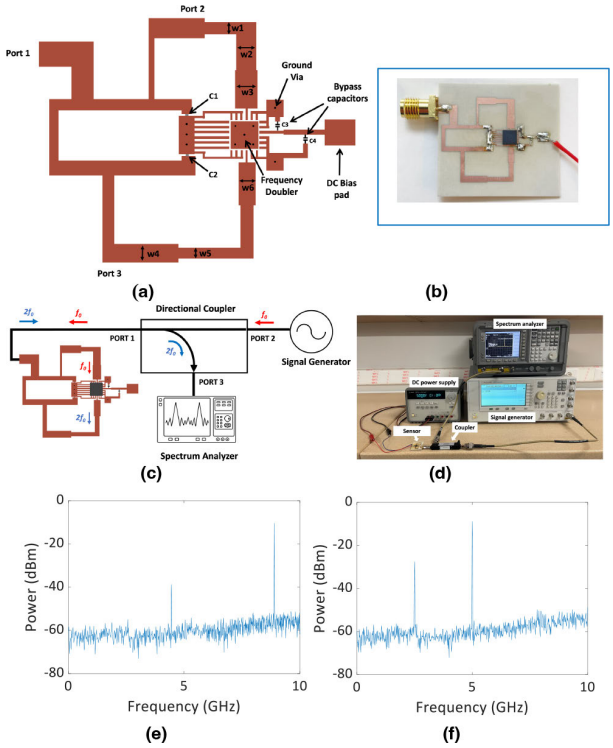

FIGURE 5. (a) The layout of the diplexer with the integrated frequency doubler (Dimensions: w1 = 1.18, w2 = 1.9, w3 = 2.16, w4 = 1.7, w5 = 1.15, w6 = 1.63, in mm), (b) The corresponding fabricated prototype, (c) The diagram for testing the operation of the proposed diplexer, (d) The corresponding experimental setup, (e) The spectrum analyzer display for a −3 dBm input power at 4.45 GHz when the diplexer is not loaded, (f) at 2.5 GHz when the diplexer is loaded.

Fig. 5(e) illustrates the spectrum analyzer display when a −3 dBm fundamental frequency signal is injected into the proposed diplexer. More specifically, when no capacitors are connected to the diplexer, a harmonic signal with a power level of −8.8 dBm is observed at 8.9 GHz while a −38 dBm signal is observed at the fundamental frequency of 4.45 GHz. On the other hand, when the diplexer is loaded with $C_1 = 0.5$ pF and $C_2 = 1$ pF capacitors, the harmonic signal power at 5 GHz is −8 dBm and the fundamental signal power is −27 dBm at 2.5 GHz as shown in Fig. 5(f). Such performance proves that this diplexer is triggered by the capacitive loading that is translated into a shift in frequencies. A conversion gain of almost 15 dB is achieved for both investigated scenarios. This is obtained by including the coupling coefficient of the coupler used in the experimental setup along with all the insertion losses of the coupler and the RF cables in addition to the reflection coefficient at the input of the coupler at the corresponding frequencies.

IV. CONCLUSION

In this paper, a new radio frequency diplexer that leverages capacitive loading as a trigger to shift its fundamental and harmonic frequencies is presented. The diplexer is designed to enable an on-demand generation of second harmonic frequencies from an integrated frequency doubler chip. This behavior is achieved by loading the proposed diplexer with a pair of capacitors. These two capacitors must retain a ratio of 2 to ensure the appropriate functioning of the overall system. To prove the validity of the design in sensing applications such as harmonic radars, an active frequency doubler chip is integrated into the proposed capacitively loaded diplexer. The design is fabricated and tested where good agreement is found between the simulated and measured data.

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