**RESEARCH ARTICLE**

# A Voltage Ripple Compensation Method for Constant On-Time Buck Converter

**JIANG-PING HE, XIN-RUI LIU, YAN-KUN XIA, YONG-QIANG CHEN,
AND CHANG-DONG WU, (Member, IEEE)**
School of Electrical Engineering and Electronic Information, Xihua University (XHU), Chengdu 611743, China

Corresponding author: Jiang-Ping He (hjp_dx@126.com)

**ABSTRACT** Subharmonic oscillation stands as a critical concern in the context of ripple-based constant-on-time (COT) controllers. While this issue can be mitigated through the application of the virtual inductor current (VIC) technique, it comes at the cost of load transient response. To achieve both high stability and rapid transient response, this paper introduces an Output Capacitor Voltage Ripple Compensation (VRC) technique. This technique minimizes the phase delay attributed to output capacitance by introducing a virtual output ripple ($V_{VOR}$) inversely related to the feedback voltage. The $V_{VOR}$ serves to expedite the load transient response by counteracting the additional virtual inductor current injection during load transients. Utilizing a $0.13\mu m$ BCD technology, a synchronous buck converter is integrated with the proposed VRC-COT controller, showcasing exceptional stability across a load current range of 0 to 8A, even when equipped with a 30% $88\mu F$ ceramic output capacitor. Additionally, the load transient response exhibits reduced overshoot and undershoot, measuring at 120mV and 130mV, respectively, in response to load steps from 0A to 8A within a $10\mu S$ timeframe.

**INDEX TERMS** Constant on-time (COT), ripple-based control, voltage ripple compensation (VRC), equivalent series resistor (ESR), subharmonic oscillation.

## I. INTRODUCTION

Ripple-based COT has drawn more and more attention in power supply due to its advantages such as simple structure, fast response speed and high light load efficiency [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13]. The quoted passage discusses the widespread application of a ripple-based COT structure in point-of-load (POL) power supplies [1], [2], [3], [4], [5], particularly in scenarios with demanding load transient requirements. It is also extensively employed in the Internet of Things (IoT) field [6], [7], [8], where stringent light load efficiency criteria are imperative. In comparison to conventional voltage control mode and peak current control mode switching power supplies, the discussed COT structure control mechanism effortlessly achieves a swifter response, owing to the load feed-forward characteristic inherent in the

directly coupled comparator. This is accompanied by the elimination of the slow-response compensation network and the time delay associated with the error amplifier [5], [14]. Moreover, during the transition from heavy load to light load conditions, this structural configuration rapidly extends the power devices' off-time. Consequently, the inductance current undergoes a rapid decline, facilitating a seamless shift from constant frequency continuous current mode (CCM) to low-frequency discontinuous current mode (DCM). This seamless transition culminates in the realization of high efficiency during light load applications [15], [16], [17], [18], [19], [20].

Figure 1 shows a basic ripple-based COT (RBCOT) structure and its critical signal waveforms. $V_{FB}$ can be obtained by dividing resistors $R_{FB1}$ and $R_{FB2}$. $V_{FB}$ is compared with internal reference voltage $V_{REF}$ to control the operation of power switches ($S_1/S_2$). When $V_{FB} < V_{REF}$, $S_1$ turns on and $S_2$ turns off. The maintenance time of this state is $T_{ON}$. Then
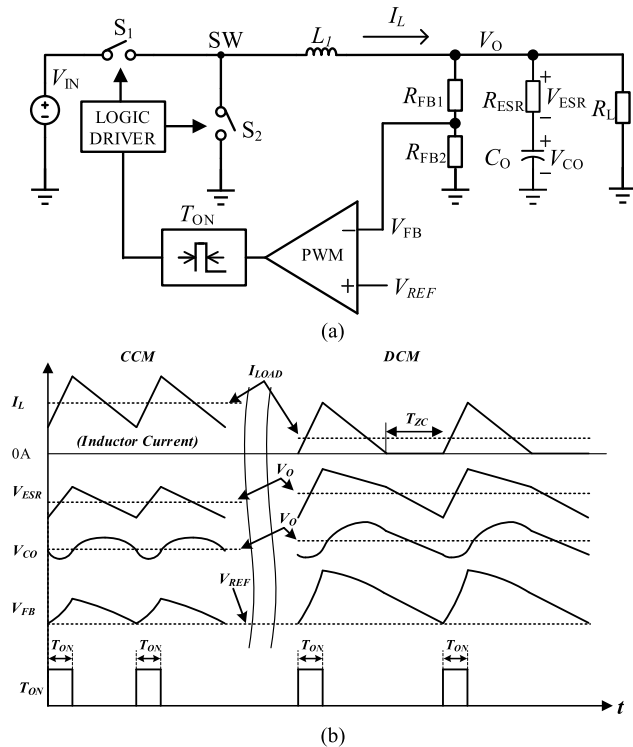
**FIGURE 1.** Circuit diagram and critical waveforms of a buck converter using RBCOT control. (a). The typical RBCOT structure. (b). The critical signals of the typical RBCOT.

$S_1$ turns off and $S_2$ on until $V_{FB} < V_{REF}$, and then $S_1$ turns on again. A stable output voltage is then acquired by $S_1/S_2$ periodical operating. When operating steadily, the inductor current is sampled and sent to the feedback loop to make the inductor current $I_L$ equal to the output load current in each cycle. If a ceramic capacitor is applied in the RBCOT topology, the parasitic equivalent series resistance (ESR) of ceramic can be used to sample the inductance current to achieve a simple and reliable power supply circuit with large ESR.

Nevertheless, the basic RBCOT control scheme encounters several challenges that impede its practical implementation. Primarily, the presence of a phase delay between the output capacitance ripple and the inductance current introduces instability issues, which are particularly pronounced in application circuits employing multilayer ceramic capacitors (MLCCs) with lower ESR. MLCCs are extensively utilized in power circuits due to the space constraints of electronic devices. Additionally, the basic RBCOT control loop, reliant on comparing the valley value of the output voltage with the internal reference, gives rise to a disparity between the valley and the average of the output voltage. Consequently, this discrepancy results in a DC shift when subjected to distinct load and output capacitance variations, thereby compromising the accuracy of the output voltage [21], [22].

In numerous studies, a variety of approaches have been proposed to enhance the stability of capacitors with low

ESR. The simplest method involves directly inserting a series resistance at the inductance terminal to augment the ripple of the inductance current [23]. However, this approach leads to an increase in power loss, offsetting the output voltage, and a reduction in transient response. In [21], [23], and [24], the inductive current signal is derived through the differential analysis of the output voltage. Subsequently, the signal is amplified and integrated into the RBCOT fast control circuit. Nevertheless, due to the inherent noise in the output voltage signal, which encompasses capacitance parasitic inductance and load change signals, the accuracy of current detection is compromised. Another method proposed in [25] involves paralleling an RC component with the inductor. By carefully selecting suitable values for RC, the poles generated by the RC component align with the zeros created by the parasitic resistance of the inductor, thereby enabling linear detection of the inductor current. Although this method resolves the instability issue without additional power consumption, it does introduce an output voltage offset. Expanding on this technique, [26], [27] incorporates a high-pass filter into the inductance parallel RC detection method to further enhance the DC offset characteristics while maintaining the response to load transients. Furthermore, by sampling the output capacitance current instead of the inductance current as explored in [28] and [29], the stability of low ESR applications can also be improved. Lastly, in [30] and [31], the switch node voltage is filtered to generate a ripple signal that is in phase with the inductive current and subsequently incorporated into the RBCOT control scheme. To summarize, the aforementioned approaches aim to augment the inductive current ripple signal generated by the ESR through the introduction of an additional ramp current. This enables the control loop to comply with the RBCOT stability criteria [5], [32]. However, the increase in compensatory inductive current ripple adversely affects the load transient response, causing it to slow down. In [33], a method known as DZC-NME is employed to address the phase delay in the output capacitor, thereby partly mitigating the trade-off between stability and load transient response. However, varying output voltages result in different phase leads, leading to instability and potential oscillations.

Numerous techniques have been proposed in [3], [8], [10], and [34] to enhance the load regulation of the RBCOT control scheme. In [8] and [34], a ripple-based $V^2COT$ method is introduced with the aim of improving load regulation within the RBCOT. This approach relies on two parallel feedback loops to control the output voltage. One loop, referred to as the fast control loop, utilizes the aforementioned feedback path to directly feed the output voltage to the comparator. The other loop consists of an error amplifier and a compensation network, where a comparison is made between the output voltage and the reference voltage. The output voltage from the error amplifier is then fed into the comparator, constituting the slow control loop. This method not only accomplishes the swift response characteristic of COT but also eliminates the DC offset in the output voltage. However, in applications

involving small ESR MLCCs, the fast control loop necessitates an additional slope compensation current, as mentioned earlier, to maintain stability in the COT loop. Consequently, the CMCOT [35] and hybrid COT [36] control schemes are proposed to address this requirement. Furthermore, in [3] and [10], the sample-hold method is employed to sample the valley value of the current feedthrough path, which is then sent to the COT loop to eliminate DC offset and achieve exceptional load regulation.

In this study, a modified ripple-based hybrid COT control scheme incorporating the output capacitor VRC method is presented. The aim is to address the trade-off between achieving a fast load transient response and ensuring stability. Moreover, the scheme aims to enhance stability even in scenarios involving small ESR MLCC applications. The conceptual framework of the proposed technique is outlined in Section II. Section III focuses on elucidating the key characteristics of the VRC control scheme. Subsequently, Section IV presents the analysis of experimental results. Finally, Section V concludes the paper, summarizing the findings and implications of the study.

## II. THE PROPOSED VRC-COT PRINCIPLE

In this section, the operating principle of the proposed output capacitor VRC-COT technique is initially described. Subsequently, the virtual generator for output capacitor voltage ripple and the topology of the VRC-COT are delineated. To further elaborate on the functioning and structure of the VRC-COT control scheme, the transfer function ($v_o(s)/v_c(s)$) between the output and the control voltage, obtained through the describing function (DF) method, is derived. The stability analysis of the controller is then presented based on the $v_o(s)/v_c(s)$ transfer function. Finally, the theoretical illustration of the load transient response for the implemented structure is provided.

### A. THE VRC-COT PRINCIPLE

The proposed VRC-COT control scheme, based on ripple analysis, exploits an integrator to generate a virtual voltage ripple that closely aligns with the output capacitor voltage ripple. Subsequently, the virtual voltage ripple is superimposed in an inverse manner with the actual output capacitor voltage ripple. This process aims to mitigate or even eliminate the phase delay induced by the output capacitor, thereby enhancing the stability of the COT controller.

The proposed hybrid ripple-based VRC-COT control scheme is illustrated in Figure 2. In Figure 2(a), the VRC-COT control block diagram is depicted, while Figure 2(b) showcases the critical signals of the controller.

Figure 2(a) comprises three key components: firstly, the basic $V^2$ COT controller [37], [38], represented by the black line; secondly, the hybrid COT controller [30], [40], indicated by the blue and black lines in Figure 2(a); and thirdly, an integrator (Integrator2) that generates a virtual output capacitor voltage ripple ($V_{VOR}$) through the integration of the virtual inductor current. Integrator2, in conjunction with
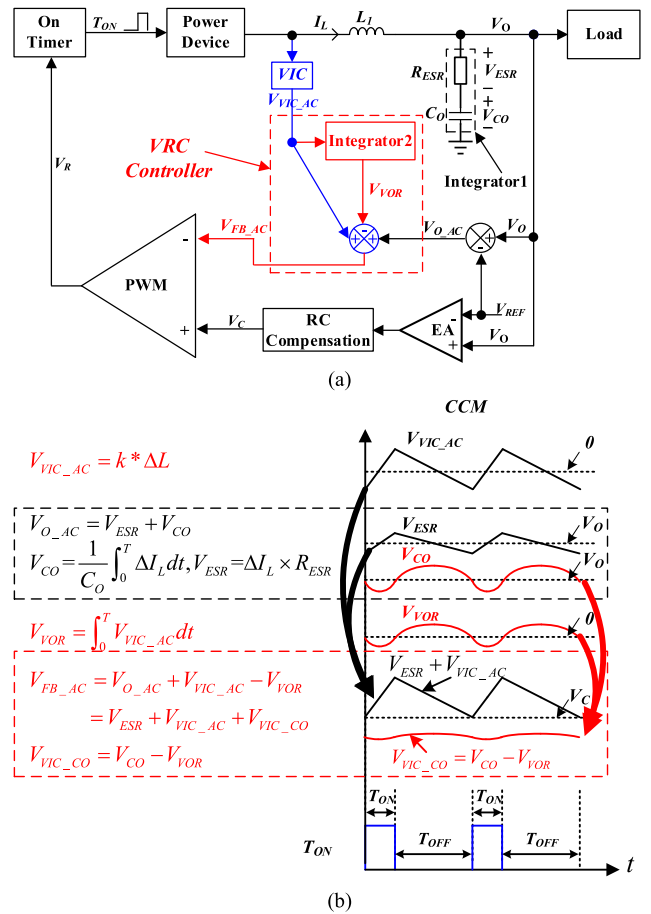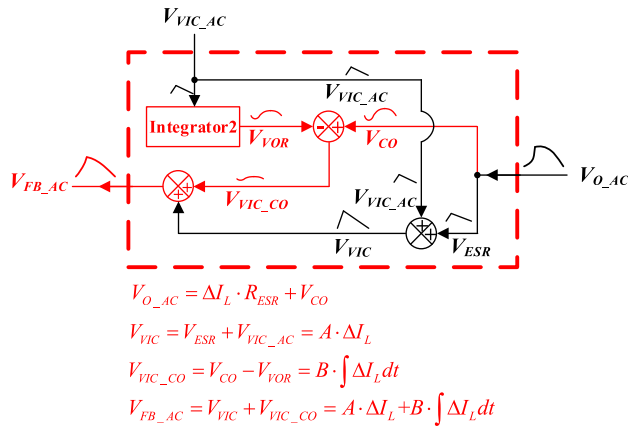


FIGURE 2. The proposed VRC-COT control strategy and critical signals. The parameter T denotes the period. $V_{O\_AC}$ is the AC feedback from output, $V_{VIC\_AC}$ is the virtual current sampling signal, $V_{FB\_AC}$ is the control signal of VRC-COT. $V_{VOR}$ is the virtual output capacitor voltage ripple. The k is constant parameter. $V_O$ is exclusively considered under alternating current conditions. (a). The proposed VRC-COT control strategy. (b). The critical signals of the proposed VRC-COT.

the hybrid COT controller, forms the proposed VRC-COT control scheme.

The operational principle of the proposed VRC-COT can be elucidated by referring to Figure 2(a)/(b) as depicted below:

①. In Figure 2(a), the structure depicted by the black line and the blue line illustrates a hybrid COT control scheme, the operational details of which are explained in [41] and [42]. The virtual inductor current signal is provided by the VIC block, represented as $V_{VIC\_AC}$ in Figure 2 (b). The sum of $V_{VIC\_AC}$ and the output voltage ripple, $V_{O\_AC}$, is then inputted into the negative terminal of the PWM and compared with $V_C$ (the error amplifier output signal, with RC compensation) to ascertain the next $T_{ON}$ generation.

②. Founded upon the hybrid COT control scheme, the devised VRC-COT incorporates an integrator, denoted as Integrator2, dedicated to processing the virtual output capacitor voltage ripple ($V_{VOR}$) derived from the virtual inductor current ($V_{VIC\_AC}$). Subsequently, the $V_{VOR}$ is inversely

$$V_{O\_AC} = \Delta I_L \cdot R_{ESR} + V_{CO}$$

$$V_{VIC} = V_{ESR} + V_{VIC\_AC} = A \cdot \Delta I_L$$

$$V_{VIC\_CO} = V_{CO} - V_{VOR} = B \cdot \int \Delta I_L dt$$

$$V_{FB\_AC} = V_{VIC} + V_{VIC\_CO} = A \cdot \Delta I_L + B \cdot \int \Delta I_L dt$$

**FIGURE 3.** The VRC controller diagram. Where, $V_{O\_AC}$ is the AC feedback from output, $V_{VIC\_AC}$ is the virtual current sampling signal, $V_{FB\_AC}$ is the control signal of VRC-COT.

superimposed and amalgamated with the actual output voltage ripple ($V_{O\_AC}$), and this combined signal, along with $V_{VIC\_AC}$, contributes to the generation of $V_{FB\_AC}$. The $V_{FB\_AC}$ is then introduced to the negative terminal of the comparator (PWM) to instigate the determination of the next $T_{ON}$.

③. The $V_{FB\_AC}$ of the VRC-COT is shown as:

$$V_{FB\_AC} = V_{VIC\_AC} + V_{O\_AC} - V_{VOR} \tag{1}$$

wherein, $V_{VIC\_AC}$ represents the virtual current corresponding to the inductor current $I_L$, exhibiting a similar phase to $I_L$. $V_{VOR}$ is derived from the integration of $V_{VIC\_AC}$ utilizing Intergrator2. $V_{O\_AC}$ denotes the output voltage ripple, comprised of $V_{ESR}$ and $V_{CO}$. $V_{ESR}$ signifies the ESR voltage generated by the input/output current of the capacitor $C_O$, synchronously aligning with the phase of the inductor current $I_L$. $V_{CO}$ represents the actual output capacitor voltage ripple, yielded through the integration of $I_L$ by the capacitor $C_O$. Consequently, $V_{CO}$ and $V_{VOR}$ are obtained through the integration of $I_L$ and $V_{VIC\_AC}$, respectively. Consequently, $V_{VOR}$ exhibits a phase similarity with $V_{CO}$, since $V_{VIC\_AC}$ maintains a phase alignment with $I_L$. The difference between $V_{CO}$ and $V_{VOR}$ is defined as $V_{VIC\_CO}$, serving as the residual output capacitor voltage ripple. Thus, equation (1) can be expressed as formula (2):

$$\begin{cases} V_{FB\_AC} = A \cdot \Delta I_L + B \cdot \int \Delta I_L dt \\ A = \dfrac{V_{ESR}}{R_{ESR}} + \dfrac{V_{VIC\_AC}}{\Delta I_L}, \quad B = \dfrac{V_{CO} - V_{VOR}}{C_O}, \\ \Delta I_L = I_L - I_{LOAD} \end{cases} \tag{2}$$

Wherein, $\Delta I_L$ represents the ripple in the inductor current, $R_{ESR}$ indicates the actual equivalent-series-resistor, $C_O$ denotes the output capacitor, $V_{CO}$ signifies the actual voltage ripple across the output capacitor, $I_L$ represents the inductor current, and $I_{LOAD}$ corresponds to the load current.

In Figure 3, an intricate diagram of VRC controller is depicted. As $V_{VOR}$ increases, the residual equivalent

integration component of $\Delta I_L$ undergoes a reduction. The phase relationship between $V_{FB\_AC}$ and $I_L$ is illustrated in Figure 4.

When $V_{VOR} = 0$, $V_{VIC\_CO} = V_{CO}$, the integration part of $\Delta I_L$ in $V_{FB\_AC}$ keeps the same as the previous 4 types of ripple-based COT control scheme [39] (named as RBCOT, $V^2$COT, CMCOT, hybrid COT);

When $V_{VOR} = 0$, $V_{VIC\_CO} = V_{CO}$, and the integration segment of $\Delta I_L$ within $V_{FB\_AC}$ remains consistent with the preceding four types of ripple-based COT control schemes [39] (referred to as RBCOT, $V^2$COT, CMCOT, hybrid COT).

In the range of $0 < V_{VOR} < V_{CO}$, signifying $0 < V_{VIC\_CO} < V_{CO}$, the integration component of $\Delta I_L$ in $V_{FB\_AC}$ diminishes with the increasing $V_{VOR}$, leading to a proportional reduction in the phase delay between $V_{FB\_AC}$ and $I_L$.

When $V_{VOR} = V_{CO}$, resulting in $V_{VIC\_CO}$ being zero, only the linear portion of $\Delta I_L$ is present in $V_{FB\_AC}$ as the integration component of $\Delta I_L$ in $V_{FB\_AC}$ approaches zero. Consequently, the phase delay between $V_{FB\_AC}$ and $I_L$ diminishes to zero.

When $V_{VOR} > V_{CO} \rightarrow V_{VIC\_CO} < 0$, the $\Delta I_L$ is induced by the leading phase of $V_{VIC\_CO}$. Consequently, $I_L$ is led by the phase of $V_{FB\_AC}$.

In Figure 4, the augmentation of the virtual output voltage ripple, $V_{VOR}$, can be likened to the gradual elevation of the $C_O$. As $V_{VOR}$ transitions from 0 to $V_{CO}$, $V_{VIC\_CO}$ undergoes a gradual reduction, potentially approaching zero. This progression is analogous to $C_O$ gradually ascending towards infinity. Consequently, within the range of $0 < V_{VOR} < V_{CO}$, the proposed VRC-COT mitigates the $2R_{ESR}C_O > T_{ON}$ constraint [32] (where $R_{ESR}$ represents the virtual output capacitance equivalent series resistance), thereby diminishing or even obviating it. Consequently, the VRC-COT exhibits exceptional stability when applied to MLCC capacitor scenarios characterized by small $R_{ESR}$.

### B. THE $V_{VOR}$ GENERATOR AND VRC-COT TOPOLOGY

In the envisioned VRC-COT control scheme, the generation of $V_{VOR}$ results from the integration of the virtual inductor current, $V_{VIC\_AC}$. The functionality is realized through the circuitry depicted in Figure 5.

The power stage and $V_{VOR}$ generator of the proposed VRC-COT control scheme are illustrated in Figure 5(a). The essential signals are delineated in Figure 5 (b).

In the CCM, the SW node voltage is a square waveform. When $T_{ON}$ is logic "1", $V_{SW} = V_{IN}$ (input power supply). When $T_{ON}$ is logic "0", $V_{SW} = GND$. The virtual inductor current $V_{VIC\_AC}$ is derived by a low-pass filter (composed of $R_{LPF1}$ and $C_{LPF1}$,). The product of $C_{RLF1}C_{LPF1}$ should be larger than $5T_{SW}$ ($T_{SW}$ is the switching duty). The relationship between the $V_{VIC\_AC}$ and the actual inductor ripple can be shown as:

$$\frac{\Delta V_{VIC\_AC}}{\Delta I_L} = \frac{L}{R_{LPF1} \cdot C_{LPF1}} \tag{3}$$
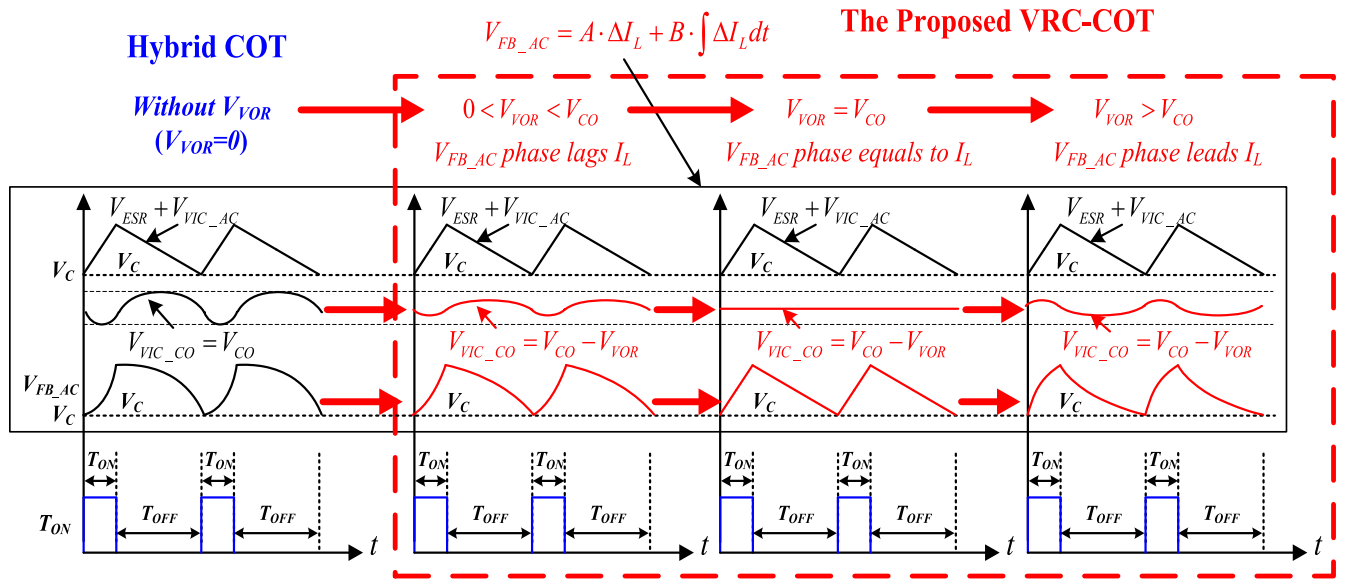
**FIGURE 4.** The VRC controller diagram. Where, $V_{O\_AC}$ is the AC feedback from output, $V_{VIC\_AC}$ is the virtual current sampling signal, $V_{FB\_AC}$ is the control signal of VRC-COT.

Where, $\Delta V_{VIC\_AC}$ and $\Delta I_L$ are the virtual inductor current ripple and the actual one, respectively. L is the inductor, $R_{LPF1}$ and $C_{LPF1}$ make up the low-pass filter.

Integrator1 and Integrator2 integrate $I_L$ and $V_{VIC\_AC}$, respectively, giving us the $V_{CO}$ and $V_{VOR}$, as shown in formula (4):

$$\begin{cases} V_{CO}(t) = \dfrac{1}{LC_O}\left[\displaystyle\int_0^{T_{ON}}(V_{IN}-V_{OUT})t\,dt - \int_{T_{ON}}^{T_{SW}} V_{OUT}\,t\,dt\right] \\[2mm] V_{VOR}(t) = \dfrac{1}{\tau_1 \cdot \tau_2}\left[\displaystyle\int_0^{T_{ON}}(V_{IN}-V_{OUT})t\,dt - \int_{T_{ON}}^{T_{SW}} V_{OUT}\,t\,dt\right] \\[2mm] \tau_1 = R_{LPF1}\cdot C_{LPF1}, \quad \tau_2 = R_{LPF2}\cdot C_{LPF2} \end{cases}$$

(4)

Where, $V_{CO}(t)$ and $V_{VOR}(t)$ are the actual output capacitor voltage ripple and the virtual one, respectively. $V_{IN}$ is the input DC voltage, $V_{OUT}$ is the output DC voltage, $R_{LPF2}$ and $C_{LPF2}$ make up the Integrator2. $\tau_1$ and $\tau_2$ are the product of $R_{LPF1}C_{LPF1}$ and $R_{LPF2}C_{LPF2}$, respectively.

In Formula (4), $V_{CO}(t)$ and $V_{VOR}(t)$ share identical integral terms, differing solely in their coefficients. Consequently, $V_{VOR}$ and $V_{CO}$ exhibit congruent waveforms with differing amplitudes. The adjustment of the amplitude in $V_{VOR}$ and $V_{CO}$, illustrated in Figure 5, is achievable through the manipulation of the ratio among $\tau_1$, $\tau_2$, $LC_O$. Based on the Figure 5 circuit, the ratio between $V_{OR}$ and $V_{CO}$ can be shown as equation (5):

$$\frac{V_{VOR}}{V_{CO}} = \frac{LC_O}{R_{LPF1}\cdot C_{LPF1} \cdot R_{LPF2}\cdot C_{LPF2}}$$

(5)

Where L is the inductor, $C_O$ is the output capacitor, the $R_{LPF1}C_{LPF1}$ and $R_{LPF2}C_{LPF2}$ are the same as formula (4).

The illustrated VOR-COT control topology is presented in Figure 6. Within the circuit, the high-speed comparator PWM

features multiple input terminals. The virtual inductor ripple, denoted as $V_{VIC\_AC}$, along with the virtual output capacitor voltage ripple $V_{RPRC\_AC}$, and the actual output capacitor voltage ripple $V_{CO\_AC}$, are fed to the various input terminals of the PWM comparator.

## III. ANALYSIS OF VRC-COT CHARACTERISTICS
Loop stability and load transient response stand as pivotal characteristics within the context of the COT control scheme. In this section, we commence by deriving the control-to-output transfer function $(v_o(s)/v_c(s))$ for the VRC-COT control scheme, employing the describing function (DF) method. Subsequently, an analysis of the load transient response operation of the VRC-COT structure is undertaken.

### A. VRC-COT LOOP STABILITY ANALYSIS
To scrutinize the loop characteristics of the proposed VRC-COT control scheme, an accurate model of the output-to-control relationship is imperative for system design. This model must account for the sideband effect within the high-frequency range.

#### 1) CONTROL-TO-OUTPUT TRANSFER FUNCTION OF THE VRC-COT
The describing function (DF) method stands out as the pre-eminent approach for deriving small signal models in PWM controllers, primarily attributed to its efficacy in addressing the nonlinearity inherent in pulse-width modulation (PWM) control schemes. Numerous small signal models [2], [9], [11], [12], [13], [15], [32] for COT control have been established through the describing function method. This methodology ensures the comprehensive inclusion of both sidebands associated with inductor current and capacitor voltage, extending
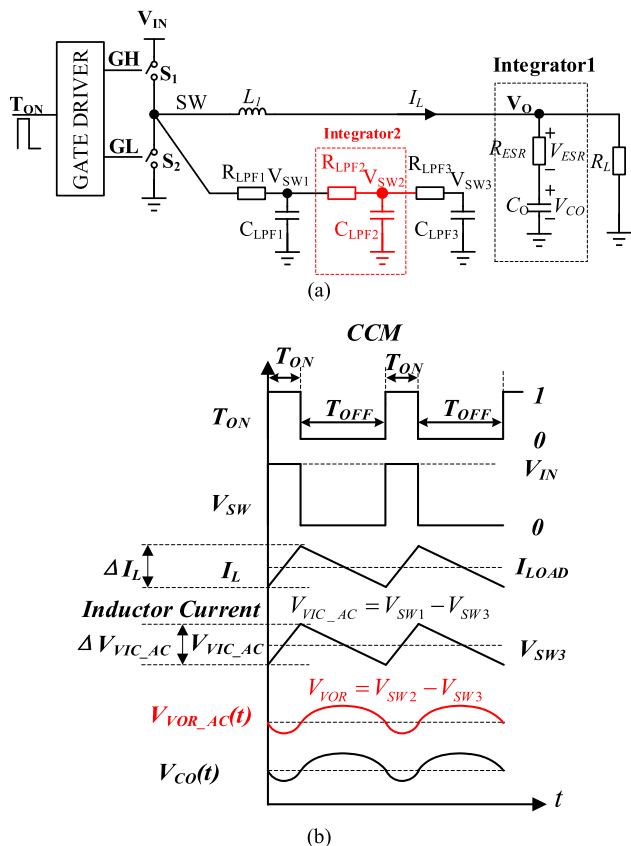
**FIGURE 5.** The $V_{VOR}$ generator of the proposed VRC-COT controller and the critical signals. (a). The $V_{VOR}$ generator, where the red line is the Integrator2, which composes of a RC low pass filter. (b). The critical signals of the reverse phase ripple generator. Where $V_{VIC\_AC}$ is the virtual inductor current ripple, the $V_{VOR}$ is the virtual output capacitor voltage ripple of the proposed VRC-COT.
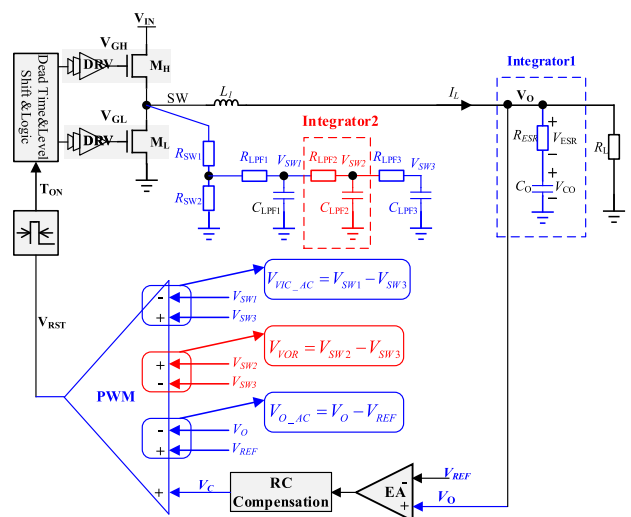


**FIGURE 6.** The topology of the proposed VRC-COT control scheme.

the model's accuracy to the switching frequency. The proposed small signal transfer function for VRC-COT is likewise derived utilizing the DF approach.

Based on Figure 2(a), the proposed VRC-COT equivalent small signal is shown in Figure 7. The on-time $T_{on}$ is fixed,

the off-time $T_{off}$ is modulated by the perturbation signal $v_c(t)$: $\hat{v}_c(t) = \hat{r}\sin(2\pi f_m t + \varphi)$, $\hat{r}$, $f_m$, and $\varphi$ are the amplitude, frequency, and initial phase of the perturbation signal $v_c(t)$, respectively. When $V_{FB\_AC}$ equals to $V_C$, the off-time $T_{off}$ ends, and $T_{on}$ of the next cycle is turned on. So, the DF formula of this VRC-COT is shown as formula in (6), as shown at the bottom of the next page.

Where:

$T_{off}(i)$---the $i_{th}$ cycle off-time,

$T_{on}$------the high side switch on time,

$V_{IN}$------the input power voltage DC value,

$V_O$------the output voltage DC value,

$v_c(t)$------the perturbation signal,

$K_1$------the virtual inductor current sensing ratio,

$K_2$------the virtual output capacitor voltage ripple sensing ratio by Integrator2,

$L$------the inductance,

$R_L$------the output loading,

$R_{ESR}$-----the ESR of the output capacitors,

$C_O$------the output filter capacitor,

$i_L(t)$---the inductor current,

$v_o(t)$----the output voltage (including DC and ac compone- nts).

Applying Laplace transformation to formula (6) through Fourier and trigonometric function transformations, and subsequently employing Pade approximation, yields formula (8), which expresses the transfer function between the output voltage $v_o$ and the perturbation signal $v_c$.

Where,

$T_{SW}$---the switching duty,

$C_Y$---- the equivalent output capacitor.

Upon comparing formula (8) with $v_o(s)/v_c(s)$ in [32] and [45], similar formula structures and parameters emerge. The primary distinctions manifest in the DC gain and equivalent output capacitance. $T_1(s)$ and $Z_o(s)$ remain consistent with those in the preceding four control schemes [32], [39], [45]. The DC gain in the proposed VRC-COT is expressed as $C_Y/C_O$, diverging from the value of approximately 1 found in [32] and [45]. Notably, in formula (8), the VRC-COT controller's output capacitor takes the form of an equivalent output capacitor $C_Y$, in contrast to the actual output capacitance $C_O$ present in the preceding ripple-based COT controller. According to [32], [39], [44], and [45], the stability criterion is stipulated as $R_{ESR}C_O > T_{on}/2$. In this study, the existence of the virtual inductor current $V_{VIC\_AC}$ and the virtual output capacitor voltage ripple $V_{VOR}$ modifies the stability criterion to $(R_{ESR}+K_1)C_Y > T_{on}/2$, with $K_1$ and $C_Y$ as defined in formulas (6) and (7), as shown at the bottom of the next page.

When $R_{LPF1}C_{LPF1}R_{LPF2}C_{LPF2} > LC_O$, $C_Y > C_O$, $0 < V_{VOR} < V_{CO}$, $C_Y$ escalates inversely with the reduction of the product $R_{LPF1}C_{LPF1}R_{LPF2}C_{LPF2}$, consequently leading to an increase in DC gain proportionate to $C_Y/C_O$.

When $R_{LPF1}C_{LPF1}R_{LPF2}C_{LPF2} = LC_O$, $C_Y$ approaches infinity, $V_{VOR} = V_{CO}$, resulting in complete neutralization
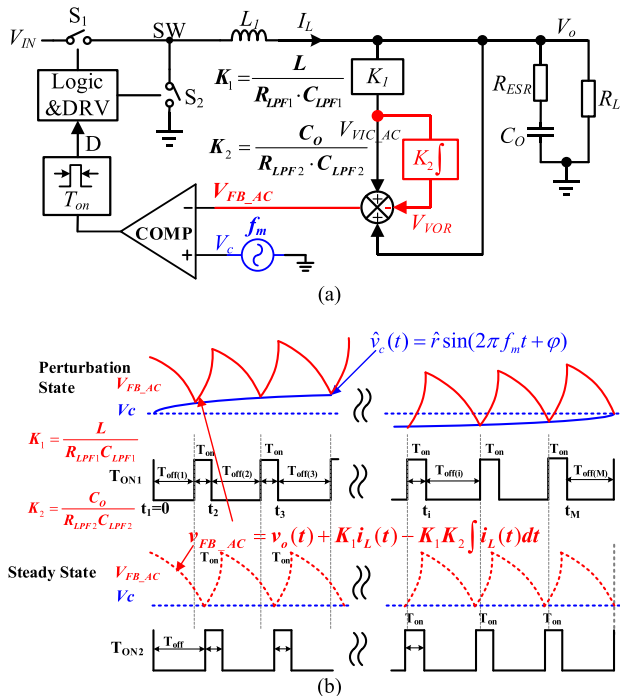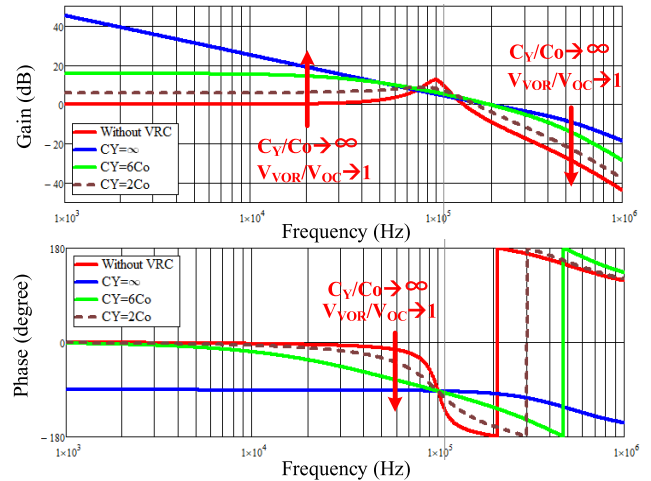
**FIGURE 7.** The linear model of the VRC-COT controller. (a) The equivalent diagram of the VRC-COT. $T_{ON1}$ is perturbation state parameter. $T_{ON2}$ is steady state parameter. The CCM operation waveform in stable-state.



**FIGURE 8.** Based on formula (7), the Bode plot of $v_o(s)/v_c(s)$ with different $C_Y/C_O$ of the proposed VRC-COT structure. As the ratio $C_Y/C_O$ increasing from 1 to $\infty$, the GBW and the phase margin increase.

of the output capacitor voltage ripple. Simultaneously, the DC gain surges to infinity, inducing instability.

When $R_{LPF1}C_{LPF1}R_{LPF2}C_{LPF2} > LC_O$, the $C_Y/C_O$ is a negative number, $V_{VOR} > V_{CO}$. So, a negative DC gain introduced, which cannot satisfy the requirement of loop stability (induces a positive feedback in the whole control scheme).

The above operation conditions correspond exactly to the working states of $V_{VOR} = 0 \rightarrow V_{VOR} > V_{CO}$ as shown in Figure 4.

Hence, the control of the $V_{VOR}/V_{CO}$ ratio is contingent upon the interplay between $C_Y$ and $C_O$, with $C_Y/C_O$ being dictated by $LC_O/R_{LPF1}C_{LPF1}R_{LPF2}C_{LPF2}$ and $LC_O$. A judicious ratio configuration serves to enhance the stability of the VRC-COT.

2) THE VRC-COT'S $V_O(S)/V_C(S)$ PHASE MARGIN VS. $C_Y/C_O$

Attaining precise control over the $V_{VOR}/V_{OC}$ ratio proves challenging due to integrated circuit (IC) process variations and diverse application scenarios. In light of formula (7), variations in both application and process introduce shifts in the $C_Y/C_O$ values. Consequently, the impact of distinct $C_Y/C_O$ configurations on the performance of the VRC-COT is under scrutiny.

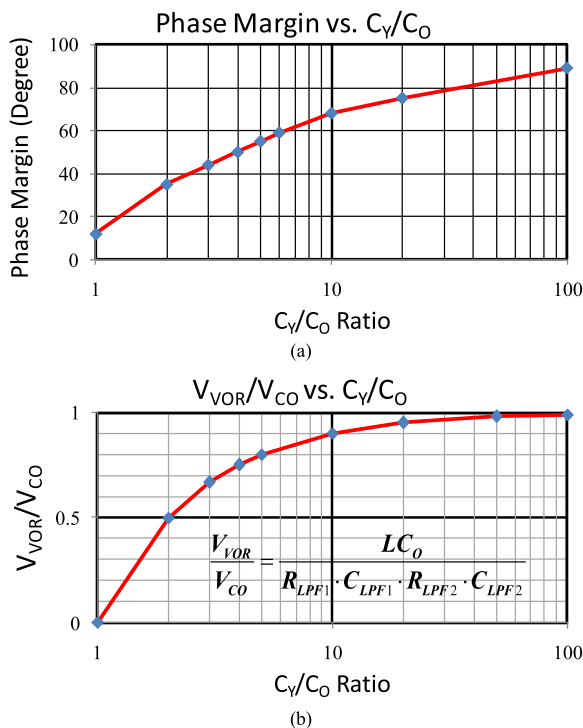From formula (5) and (7), the $V_{VOR}/V_{OC}$ can be expressed as:

$$\frac{V_{VOR}}{V_{CO}} = 1 - \frac{1}{C_Y/C_O} \tag{8}$$

From formula (8), the ratio of $V_{VOR}/V_{CO}$ is controlled by $C_Y/C_O$, which shown as Figure 9(b).

On the basis of formula (7), the Bode plot of $v_o(s)/v_c(s)$ with different $C_Y/C_O$ is shown in Figure 8. The simulation conditions are shown as: $V_{IN} = 5V$, $V_O = 1V$, $L = 1\mu H$, $C_O = 88\mu F$, $R_{ESR} = 5m\Omega$, switching frequency $F_{sw} = 200KHz$, setting $K_1 = L/R_{LPR1}C_{LPR1} = 1$, $K_2 = C_O/R_{LPR2}C_{LPR2}$ in the range of 0 to 1, that means that the

$$\begin{cases} \hat{v}_c(t_{i-1}+T_{off(i-1)})+s_n T_{on} - s_f T_{off(i)} - K_1 K_2 \int_{t_{i-1}+T_{off(i-1)}}^{t_i+T_{off(i)}} i_L(t)/C_O dt + \int_{t_{i-1}+T_{off(i-1)}}^{t_i+T_{off(i)}} [(i_L(t) - \frac{v_o(t)}{R_L})/C_O]dt = \hat{v}_c(t_i + T_{off(i)}) \\ s_n = (R_{ESR} + K_1)\frac{(V_{IN} - V_O)}{L}, \quad s_f = (R_{ESR} + K_1)\frac{V_O}{L}, \quad K_1 = \frac{L}{R_{LPF1}C_{LPF1}}, \quad K_2 = \frac{C_O}{R_{LPF2}C_{LPF2}} \end{cases} \tag{6}$$

$$\begin{cases} \frac{v_o(s)}{v_c(s)} = \frac{C_Y}{C_O} \cdot T_1(s) \cdot \frac{1}{1 + \frac{s}{Q_2\omega_2} + \left(\frac{s}{\omega_2}\right)^2} \cdot Z_o(s), \quad Q_2 = \frac{T_{sw}}{\left[(R_{ESR} + K_1)C_Y - T_{on}/2\right]\pi}, \quad \omega_2 = \frac{\pi}{T_{sw}} \\ T_1(s) = \frac{1}{1 + \frac{s}{Q_1\omega_1} + \left(\frac{s}{\omega_1}\right)^2}, \quad Q_1 = \frac{2}{\pi}, \quad \omega_1 = \frac{\pi}{T_{on}}, \quad Z_o(s) = \frac{(1 + R_L C_O s)(R_{ESR}C_O s + 1)}{(R_L + R_{ESR})C_O s + 1} \\ C_Y = \frac{C_O}{1 - K_1 K_2} \rightarrow \frac{C_Y}{C_O} = \frac{1}{1 - \frac{LC_O}{R_{LPF1}C_{LPF1}R_{LPF2}C_{LPF2}}} \end{cases} \tag{7}$$

## Phase Margin vs. $C_Y/C_O$



(a)

## $V_{VOR}/V_{CO}$ vs. $C_Y/C_O$



$$\frac{V_{VOR}}{V_{CO}} = \frac{LC_o}{R_{LPF1} \cdot C_{LPF1} \cdot R_{LPF2} \cdot C_{LPF2}}$$

(b)

**FIGURE 9.** The virtual output capacitor voltage ripple and the Phase Margin of $v_o(s)/v_c(s)$ of the proposed VRC-COT with different $C_Y/C_O$ ratio. (a) The $v_o(s)/v_c(s)$ Phase Margin with different $C_Y/C_O$. As the ratio $C_Y/C_O$ increasing from 1 to $\infty$, the Phase Margin increases from 12 degree to nearly 90 degree. (b).The $V_{VOR}/V_{CO}$ vs. $C_Y/C_O$ plot.

maximum ratio of $V_{VOR}/V_{OC}$ is nearly 1. Accordingly, the ratio of $C_Y/C_O$ is in the range of 1 to $\infty$.

When $K_2 = 0$, the equivalent output capacitor $C_Y = C_O$, $V_{VOR} = 0$. In the absence of virtual output capacitor voltage ripple compensation, the Bode plot of $v_o(s)/v_c(s)$ mirrors that of the hybrid COT [31], and its transfer function aligns with the previous four types of ripple-based COT controllers [39]. As $K_2 = 0.5/0.833/1$, $C_Y = 2C_O/6C_O/\infty$, the DC gain and phase margin of the proposed VRC-COT controller exhibit a gradual increase, accompanied by a slight enhancement in the GBW.

With the conditions as in Figure 8, the escalation of the $C_Y/C_O$ ratio from 1 to 100 yields a notable augmentation in phase margin, progressing from 12 degrees to nearly 90 degrees, accompanied by a DC gain elevation from 0dB to 40dB. Details are illustrated in Figure 9(a).

Examining Figure 9(b), under analogous conditions to Figure 8, the ascent of the $V_{VOR}/V_{CO}$ ratio (equivalent to $LC_O/R_{LPF1}C_{LPF1}R_{LPF2}C_{LPF2}$) from 0 to approximately 0.8 corresponds to a Phase Margin of $v_o(s)/v_c(s)$ surge from 12 degrees to nearly 55 degrees. In this scenario, the DC gain registers a modest increase from 0dB to 6dB.

So as long as $C_Y/C_O > 1$, the proposed VRC-COT's phase margin will be superior to that of the conventional ripple-based COT controller.

In the majority of BCD processes, the corner variations of integrated resistors and capacitors typically fall within the

range of $\pm20\%$. Consequently, the product of RC spans from 0.64 to 1.44. Applying formula (7) and assuming a preset value of $LC_O/R_{LPF1}C_{LPF1}R_{LPF2}C_{LPF2}$ at 0.55, the resulting ratio of $C_Y/C_O$ is estimated to be within the range of 1.6 to 7.1. The corresponding phase margin is anticipated to range from 37 to 63 degrees, demonstrating a substantial enhancement compared to the earlier hybrid COT control scheme. Even in the presence of variations in integrated circuit processes, the proposed VRC-COT controller consistently delivers a noteworthy improvement in phase margin within the context of small equivalent series resistance (ESR) multilayer ceramic capacitor (MLCC) applications.

### B. THE VRC-COT CONTROLLER LOAD TRANSIENT OPERATION

Comparing the proposed VRC-COT control scheme with the four preceding ripple-based COT control strategies (namely RBCOT, V$^2$COT, CMCOT, and Hybrid COT) [29], [30], [31], [39], [41], [42], [43], it is evident that the former delivers an expedited response to load transients, even when accommodating a substantial compensation of virtual inductor current. This superior performance can be attributed to the compensatory action of the virtual output capacitor voltage ripple, effectively mitigating the additional impact of virtual inductor current injection.

The preceding ripple-based COT control scheme employs MLCCs as output capacitors. To achieve optimal stability, a greater equivalent $R_{ESR}$ (output capacitor equivalent series resistance) is necessitated, a requirement that becomes more pronounced with diminishing output capacitor size. Amid load transients, the heightened equivalent $R_{ESR}$ detrimentally impacts the load transient response of RBCOT, as the signal generated by the equivalent inductor current, induced by $R_{ESR}$, opposes the variation in output capacitor voltage.

In all instances, whether considering the preceding four categories of ripple-based COT [29], [30], [31], [41], [42], [43], or the newly proposed VRC-COT control scheme, the relationship holds: $V_{FB\_AC} = V_{O\_AC} + V_{VIC\_AC} - V_{VOR}$. Within the antecedent four ripple-based COT controllers, $V_{VOR} = 0$. In contrast, within the proposed VRC-COT, $V_{VOR}$ is higher than zero and increases with the increasing $C_Y/C_O$. Consequently, during a transition from light load to heavy load ($I_{LOAD}$), the rate of decline of $V_{FB\_AC}$ in the VRC-COT structure outpaces that observed in the antecedent four types of ripple-based COT controllers. The suggested VRC-COT structure demonstrates an accelerated entry into the subsequent $T_{on}$ and exhibits a swifter transient response. Analogous improvements manifest when the load undergoes a reverse variation.

Hence, in comparison to the erstwhile ripple-based COT controller, the newly proposed VRC-COT controller affords a more expeditious transient response and enhanced stability.

### IV. THE SCHEME AND CIRCUIT IMPLEMENTATION

In reference to Fig.6, the VRC-COT employs an enhanced PWM with multiple input terminals (depicted as PWM) in

contrast to the traditional ripple-based COT. This enhanced PWM, in conjunction with the integrator (illustrated as Integrator2), is utilized to generate the virtual voltage ripple ($V_{VOR}$). To enhance the stability of DCM, a DCM Ramp Generator has been incorporated into the circuit design.

The proposed enhanced PWM inner scheme, illustrated in Figure 11, integrates five transconductance amplifiers and a comparator. Gm1 represents the transconductance responsible for generating the virtual inductor current ($V_{VIC}$), while $G_{m2}$ facilitates the generation of the virtual output capacitor voltage ripple ($V_{VOR}$). By independently adjusting $G_{m1}$ and $G_{m2}$, distinct gains for $V_{VIC}$ and $V_{VOR}$ amplitudes can be obtained. The currents produced by the differential pairs are overlaid on resistors $R_1$ and $R_2$, enabling the amplification and superimposition of the ripple voltage. The resultant differential voltage is fed into the comparator (COMP) to achieve the $V_{RST}$, implemented through a conventional high-speed comparator circuit within the COMP block. $G_{m3}$ to $G_{m5}$ adopt an identical structure as $G_{m1}$ and $G_{m2}$.

## A. THE VIRTUAL OUTPUT CAPACITOR VOLTAGE RIPPLE GENERATOR

In the VRC-COT PWM, there are several voltage ripples need to be added together, such as the virtual inductor current ripple, virtual output capacitor voltage ripple, etc. The PWM generator employs a transconductance amplifier, depicted in Figure 12, to efficiently fulfill this function. The structural configuration succinctly achieves this objective. Among them, $V_{SW1}$, $V_{SW2}$, and $V_{SW3}$ are connected to the RC filters shown as Figure 12(a). Furthermore, $V_O$ and $V_{REF}$ establish connections with the output voltage terminal and the internal reference voltage, respectively.

The schematic diagram of the virtual output capacitor voltage ripple generator is presented in Figure 12. Comprising three filters and a transconductance amplifier, this circuit is delineated in detail. The left segment of Figure 12(a) encompasses the SW voltage divider circuit and three RC filters. Among them, $R_{SW1}$ and $R_{SW2}$ divides the SW voltage, which is used to set the DC value of the inductor current ripple and output voltage ripple, making $V_{SW1}$/$V_{SW2}$/$V_{SW3}$ meet the input range of PWM comparator in a wide range of $V_{IN}$. $R_{LPF1}$/$C_{LPF1}$, $R_{LPF2}$/$C_{LPF2}$ and $R_{LPF3}$/$C_{LPF3}$ are responsible for generating the virtual inductor current ripple, virtual output capacitor voltage ripple, and SW DC value, respectively. The right portion of Figure 12(a) features a differential transconductance amplifier with multiple input terminals. This amplifier serves to magnify the inductor current ripple and the virtual output capacitor ripple individually. Subsequently, the amplified signals are overlaid onto resistors $R_1$ and $R_2$, yielding a voltage signal denoted as $V_{o1}$-$V_{o2}$.

According to the buck converter working principle, while high side (HS) switches turn on, low side (LS) switches turn off, $V_{SW} = V_{IN}$. When the HS switches turns off, the LS switches turn on, $V_{SW} = GND$.

Hence, $V_{SW\_AVG} = D \cdot V_{IN} = V_{OUT}$, where, $V_{SW\_AVG}$ is the average voltage of SW, D is the HS switches on duty cycle, $V_{IN}$ is the input voltage, $V_{OUT}$ is the output voltage.

When $R_{SW1}/R_{SW2} \ll R_{LPF1}$, $R_{LPF1}C_{LPF1} > R_{LPF3}C_{LPF3} \gg R_{LPF2}C_{LPF2} \gg 5T_{SW}$ ($T_{SW}$ is the switching duty), the voltage relationship between $V_{SW1}$, $V_{SW2}$ and $V_{SW3}$ is shown as:

$$\begin{cases} V_{SW1\_AVG} = V_{SW2\_AVG} = V_{SW3\_AVG} = K_3 V_{SW\_AVG} \\ K_3 = \dfrac{R_{SW2}}{R_{SW1} + R_{SW2}} \end{cases}$$
(9)

The AC signal of each node can be expressed as:

$$\begin{cases} v_o(s) = v_{o1}(s) - v_{o2}(s) = \big[ G_{m1} \cdot v_{VIC\_AC}(s) \\ \qquad\qquad - G_{m2} \cdot v_{RPRC\_AC}(s) \big] \times R_1 \\ R_1 = R_2 \\ v_{VIC\_AC}(s) \approx K_3 \cdot V_{SW\_DIV} \dfrac{1}{1 + R_{LPF1} \cdot C_{LPF1} \cdot s} \\ v_{RPRC\_AC}(s) \approx v_{sw1}(s) \dfrac{1}{1 + R_{LPF2} \cdot C_{LPF2} \cdot s} \end{cases}$$
(10)

Where, $v_o$ is the summation of the virtual inductor current ripple and the reverse virtual output capacitor voltage ripple, $V_{VIC\_AC}$ is the virtual inductor current, $V_{VOR}$ is the virtual output capacitor voltage ripple, $V_{SW\_DIV}$ is SW DC voltage division by resistor divider $R_{SW1}$ and $R_{SW2}$. $G_{m1}$ and $G_{m2}$ is the transconductance for $V_{VIC\_AC}$ and $V_{VOR}$, $R_1$/$R_2$ is the resistors for this transconductance amplifier. $K_3$ shown as formulas (9).

When $R_{LPF1} \cdot C_{LPF1} \cdot s \gg R_{LPF2} \cdot C_{LPF2} \cdot s \gg 1$, the ripple signals, as illustrated in Figure 12(b), manifest as $V_{SW1}$ and $V_{SW2}$. Utilizing formulas (3), (4), and (10), the magnitudes of $V_{VIC\_AC}$ and $V_{VOR}$ can be modulated through the parameters $G_{m1}$, $G_{m2}$, $R_1$ and $R_2$.

## V. EXPERIMENTAL RESULTS AND DISCUSSIONS
The proposed VRC-COT architecture was used in an integrated single phase buck converter, which is used in laptop computer main board for USB connected peripherals power supply. The converter functions with an output voltage set at 5.1V and is capable of accommodating an output current of up to 8A. Implementation of this buck converter has been realized using a cutting-edge $0.13 \mu m$ 24V BCD process. The critical specifications of the experimental converter are listed in Table 1.

Within this buck converter, the internal $V_{REF}$ is maintained at 0.8V. It embraces the ACOT structure [35] and employs a Frequency-Locked Loop (FLL) to achieve CCM at a constant frequency. Simultaneously, to mitigate audio noise in DCM, the incorporated Ultra-Sonic Mode (USM) ensures that the minimum operating frequency of DCM exceeds 30KHz. Additionally, it can operate in conventional DCM mode to enhance efficiency under light load conditions. The schematic depiction of the typical application circuit is delineated in Figure 13.

**The previous 4 types ripple-based COT**

**The Proposed VRC-COT**
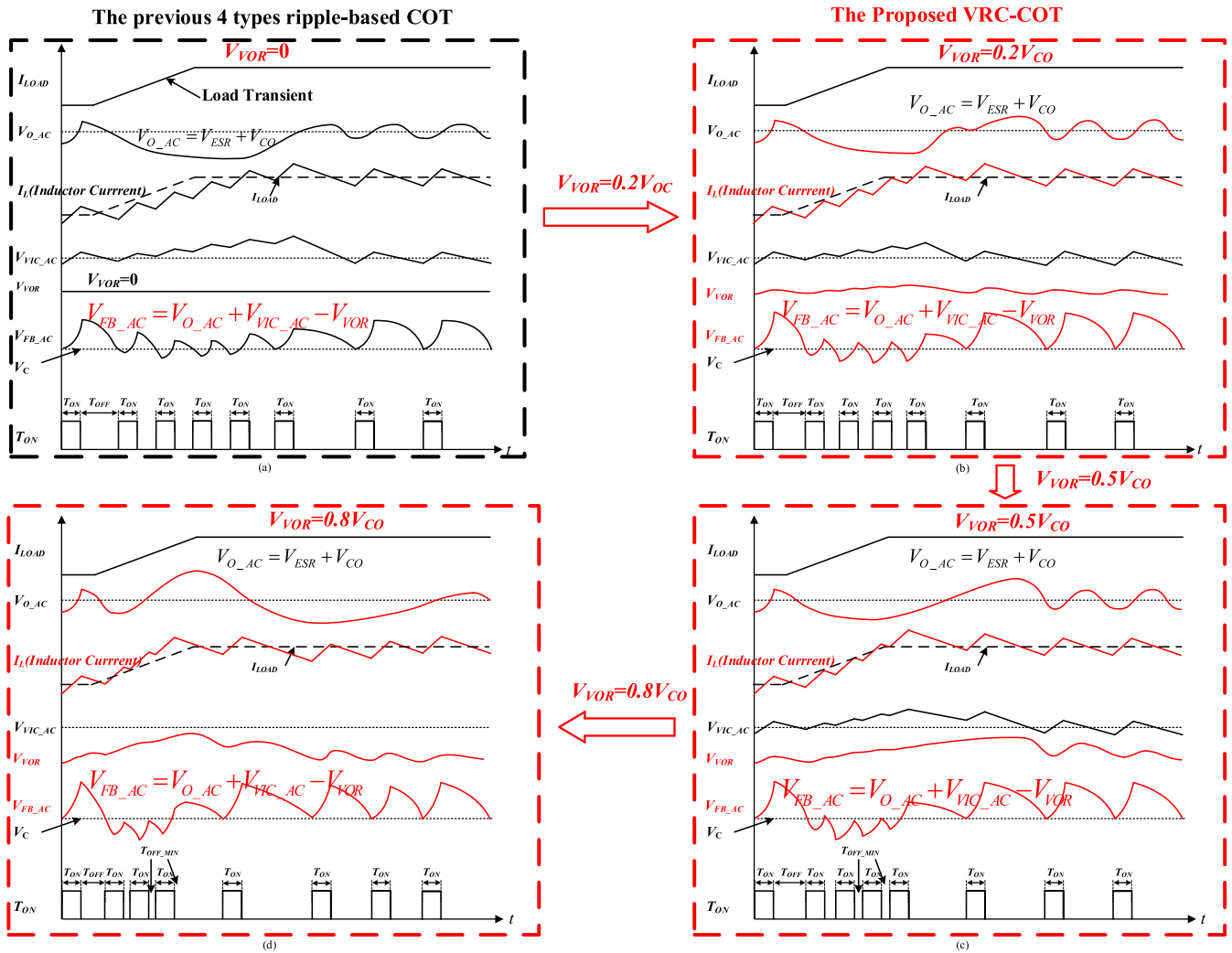


**FIGURE 10.** Load from light to heavy step response comparison between the conventional ripple-based COT and the proposed VRC-COT. (a) The previous ripple-based COT transient response. (b~d) The proposed VRC-COT controller transient response. As $C_Y/C_O$ increasing, the $V_{VOR}$ increasing and the decreased speed of Toff increasing, the load transient response timer decreasing.
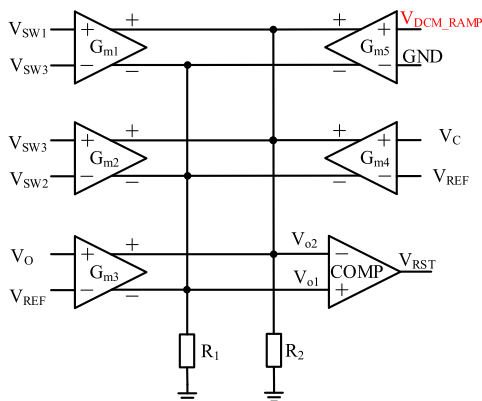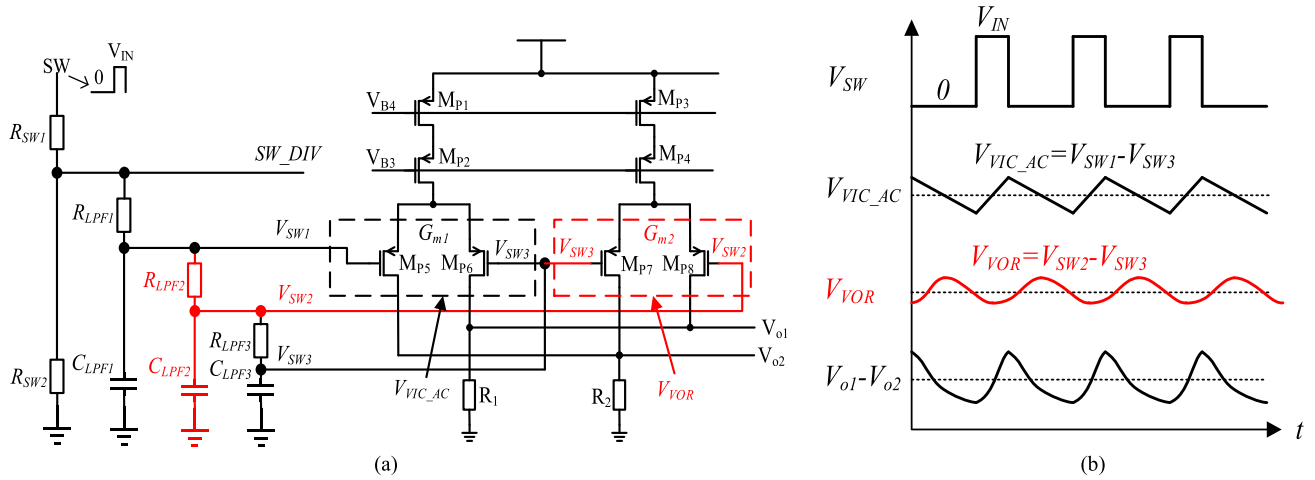


**FIGURE 11.** The inner scheme of the PWM generator.

**TABLE 1.** Performance of the COT converter.

| Name | DESCRIPTIONS | Value | Units |
|---|---|---|---|
| $V_{IN}$ | Input voltage | 6-24 | V |
| $V_{OUT}$ | Output voltage | 5.1 | V |
| $I_{LOAD}$ | Load range | 0--8 | A |
| $L_1$ | Inductor | 1.5 | μH |
| $F_{OSC}$ | Switching frequency CCM | 570 | KHz |
| $C_{OUT}$ | Output capacitor(MLCC) | 22*4 | μF |
| $Eff_{max}$ | Maximum efficiency | 94 | % |

devices is approximately 19mΩ, while that of the LS power devices is measured at about 9mΩ. The switching frequency operates at around 570KHz. Equipped with a 1.5uH inductor, the buck converter is capable of sustaining a maximum

In Figure 13, $U_1$ is the buck converter with power device integrated. Within this segment, the R dson of the HS power

**FIGURE 12.** The virtual output capacitor voltage ripple generator and the virtual inductor current generator. $V_{IN}$ is the input supply voltage (a) The RC filters to generate virtual inductor current ripple and virtual output capacitor voltage ripple with DC value elimination. (b) The critical signal for the ripple generation.
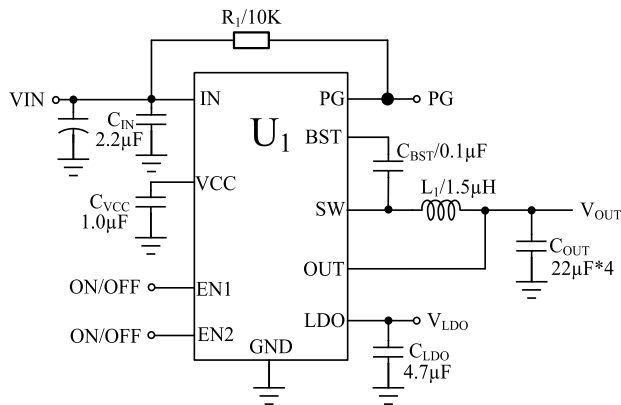


**FIGURE 13.** Typical application circuit of the buck converter integrated the proposed VRC-COT architecture.
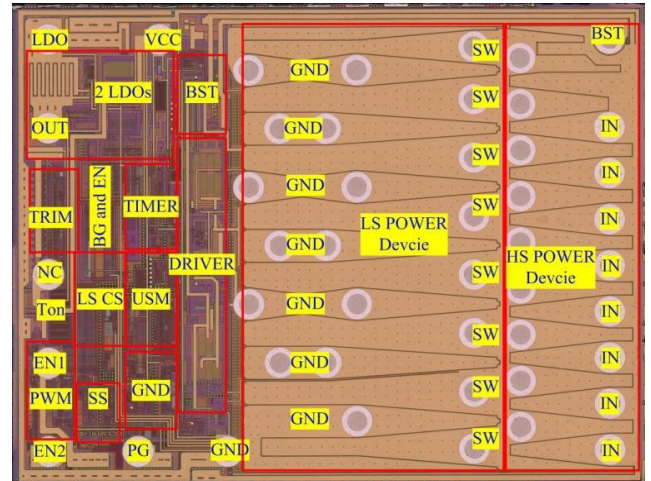


**FIGURE 14.** Microphotograph of the experimental single phase integrated buck converter.

continuous current loading of 8A. The low ESR MLCC is connected parallel at $V_{OUT}$-GND. In this section, the analog blocks encompass 2 LDOs, a voltage reference, components related to Ton, BST, USM, DRIVER, and others. A microphotograph is depicted in Figure 14.

Based on the Figure 13, the experimental buck converter measurement results are shown as follows:

### A. STATIC PERFORMANCE VERIFICATION

Aiming to investigate detailed stable operation of the experimental part in typical operation conditions, the operating waveforms based on Figure 13 application circuits are shown as Figure 15. The test conditions are: $V_{IN} = 19V$, the buck switching frequency $F_{SW} = 570KHz$ (CCM), $L_1 = 1.5\mu H$, $C_{OUT} = 88\mu F$, $V_{OUT} = 5.1V$.

Figure 15(a) illustrates the stable operating waveforms under load = 0. During this phase, the device operates in DCM, with the $T_{on}$ occurring once every 20mS as a

mandatory turn-on event. The $T_{on}$ duration is approximately 470nS, mirroring that of the CCM. However, the off time for both HS and LS switches extends to about 20mS. In response to the imperative of achieving high efficiency under light load conditions, most internal circuits within the device can be deactivated during this 20mS off period. Only a select few circuits remain active, resulting in a substantial reduction in operating current and the attainment of high efficiency under light load conditions. Figure 15(b)/(c) present the test waveforms under loads of 4A and 8A, respectively. These output waveforms exhibit striking similarities, with the amplitudes of $V_{out}$ voltage ripple and inductor current ripple being precisely identical. The primary distinction lies in the DC value of the inductor current. Following the operational principle of the buck converter, the average inductor current equates to the load current. Furthermore, the $V_{out}$ ripple voltage (peak to peak) reaches 80mV, a magnitude significantly higher
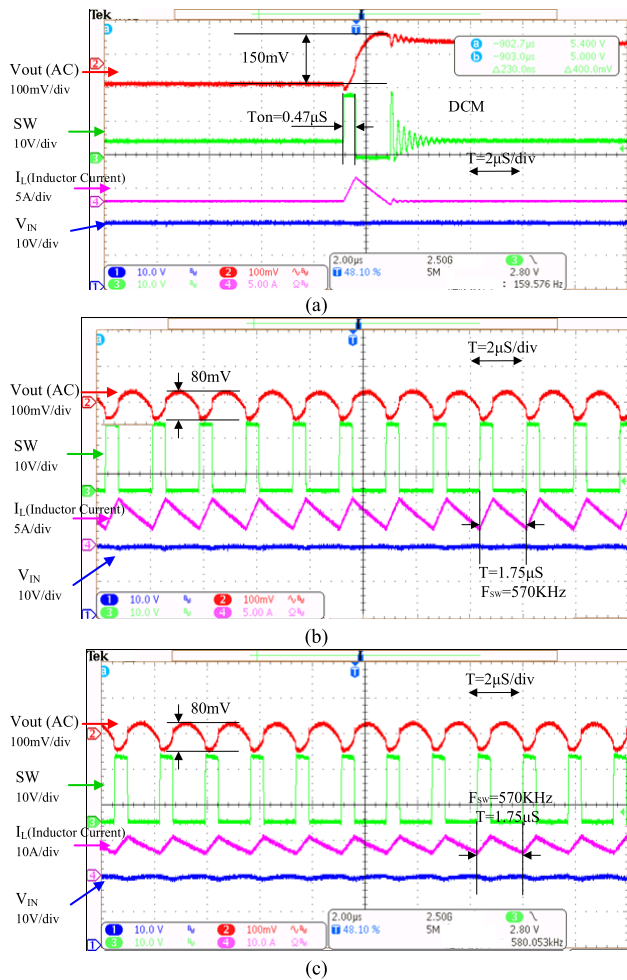
FIGURE 15. The operating waveforms based on the typical application circuits at different current load. (a) The load is zero current. (b) The load is 4A. (c) The load is 8A.
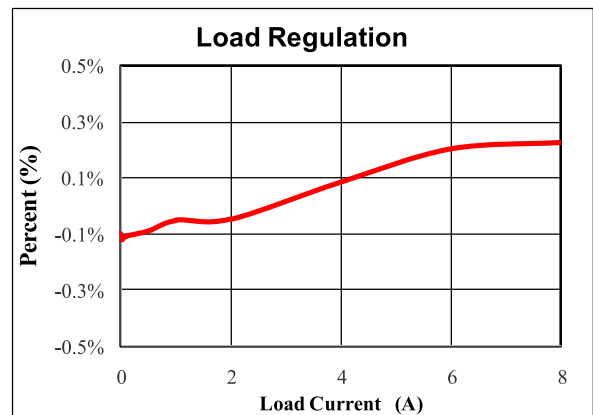


FIGURE 16. The Vout DC value at different load current.
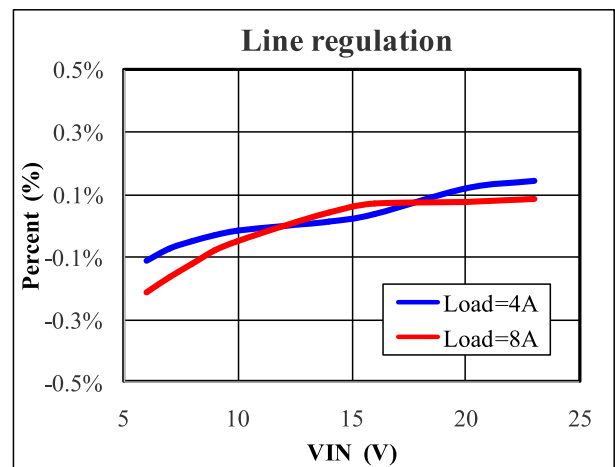


FIGURE 17. The output voltage line regulation with output current at 4A and 8A.

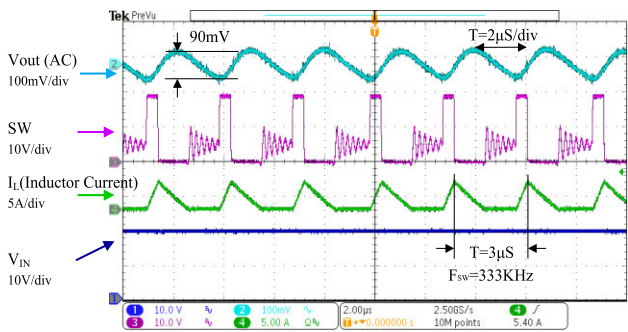than theoretical calculations. This discrepancy arises from the rapid decrease in MLCC capacitance with the elevation of $V_{out}$ DC value and operating switching frequency [36].

In the VRC-COT configuration, a high-gain EA circuit is employed to mitigate the $V_{OUT}$ DC offset. As depicted in Figure 16, the graph elucidates the load regulation across the output current range from 0 to 8A. The $V_{OUT}$ variation is constrained to less than ±0.2%. Grounded in the internal $V_{REF} = 0.8V$, the FB equivalent DC offset measures approximately 3.264mV, which is competitive with some advanced industry products (i.e., NB679A [37], RT6228C [38]).

In the realm of most applications, line regulation stands as a critical performance parameter. As illustrated in Figure 17, the experimental results delineate line regulations remaining below ±0.15% when the output current load is set at 4A and 8A, surpassing the performance of select advanced industry products [37], [38].

## B. STATIC PERFORMANCE VERIFICATION
The VRC-COT proposed here leverages reverse phase ripple to mitigate the phase delay inherent in the output capacitor,

thereby enhancing system stability. Load transient response waveforms, derived from the application circuit illustrated in Figure 13, are depicted in Figure 18.

Figure 18(a) showcases the fluctuation of the load current, $I_{LOAD}$, ranging from 0 to 8A and vice versa. During the transition from 0A to 8A, Vout initially experiences a rapid decline followed by a subsequent rise. The amplitude of overshooting throughout this process remains under 120mV. Similarly, in the reverse transition from 8A to 0, Vout exhibits a swift drop followed by a subsequent increase, with a peak overshooting voltage of approximately 130mV and a recovery time of less than $40\mu S$. An analogous pattern emerges during the step transition of $I_{LOAD}$ from 1A to 6A and back, depicted in Figure 18(b). Here, the output voltage demonstrates an overshooting of about 75mV and an undershooting of about 65mV. The recovery time is approximately $40\mu S$.

Figure 19 presents the operational waveforms of the VRC-COT in DCM. The $T_{on}$ is maintained at approximately 470nS, while $T_{off}$ increases automatically with a decrease in load current. A periodic off time is observed in DCM, during which both the HS power switches and LS power switches

## REFERENCES

[1] V. Li, Q. Li, F. C. Lee, and P.-H. Liu, "State-trajectory control with single-cycle response for point-of-load converters," *IEEE Trans. Ind. Electron.*, vol. 67, no. 4, pp. 3157–3166, Apr. 2020.

[2] Y. Yan, F. C. Lee, S. Tian, and P. Liu, "Modeling and design optimization of capacitor current ramp compensated constant on-time $V^2$ control," *IEEE Trans. Power Electron.*, vol. 33, no. 8, pp. 7288–7296, Aug. 2018.

[3] X. Ming, Y.-L. Xin, T.-S. Li, H. Liang, Z.-J. Li, and B. Zhang, "A constant on-time control with internal active ripple compensation strategy for buck converter with ceramic capacitors," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 9263–9278, Sep. 2019.

[4] J. Cortés, V. Švikovic, P. Alou, J. A. Oliver, and J. A. Cobos, "Improved transient response of controllers by synchronizing the modulator with the load step: Application to $V^2I_c$," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1577–1590, Mar. 2015.

[5] R. Redl and J. Sun, "Ripple-based control of switching regulator—An overview," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2669–2680, Dec. 2009.

[6] S. S. Amin and P. P. Mercier, "A fully integrated Li-ion-compatible hybrid four-level DC–DC converter in 28-nm FDSOI," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 720–732, Mar. 2019.

[7] P.-H. Chen, T.-Y. Su, and P. M. Fan, "Thermoelectric energy harvesting interface circuit with capacitive bootstrapping technique for energy-efficient IoT devices," *IEEE Internet Things J.*, vol. 5, no. 5, pp. 4058–4065, Oct. 2018.

[8] X. Liu, L. Huang, K. Ravichandran, and E. Sánchez-Sinencio, "A highly efficient reconfigurable charge pump energy harvester with wide harvesting range and two-dimensional MPPT for Internet of Things," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1302–1312, May 2016.

[9] C.-F. Nien, D. Chen, S.-F. Hsiao, L. Kong, C.-J. Chen, W.-H. Chan, and Y.-L. Lin, "A novel adaptive quasi-constant on-time current-mode buck converter," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 8124–8133, Oct. 2017.

[10] W.-H. Yang, C.-J. Huang, H.-H. Huang, W.-T. Lin, K.-H. Chen, Y.-H. Lin, S.-R. Lin, and T.-Y. Tsai, "A constant-on-time control DC–DC buck converter with the pseudowave tracking technique for regulation accuracy and load transient enhancement," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 6187–6198, Jul. 2018.

[11] S. Tian, F. C. Lee, J. Li, Q. Li, and P.-H. Liu, "A three-terminal switch model of constant on-time current mode with external ramp compensation," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7311–7319, Oct. 2016.

[12] Y.-C. Hsu, D. Chen, S.-F. Hsiao, H.-Y. Cheng, and C.-S. Huang, "Modeling of the control behavior of current-mode constant on-time boost converters," *IEEE Trans. Ind. Appl.*, vol. 52, no. 6, pp. 4919–4927, Nov. 2016.

[13] S. Tian, F. C. Lee, Q. Li, and Y. Yan, "Unified equivalent circuit model and optimal design of $V^2$ controlled buck converters," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1734–1744, Feb. 2016.

[14] L. Kong, D. Chen, S.-F. Hsiao, C.-F. Nien, C.-J. Chen, and K.-F. Li, "A novel adaptive-ramp ripple-based constant on-time buck converter for stability and transient optimization in wide operation range," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 3, pp. 1314–1324, Sep. 2018.

[15] I. Wei, Y. Lin, C. Chen, and D. Chen, "Stability issues and modelling of ripple-based constant on-time control schemes operating in discontinuous conduction mode," *IET Power Electron.*, vol. 7, no. 4, pp. 868–875, Apr. 2014.

[16] G.-Y. Lin, D. Chen, and Y.-J. Chen, "The DCM stability issue of voltage regulators using a current-mode constant on-time controller control," in *Proc. IEEE Energy Convers. Congr. Expo.*, Denver, CO, USA, Sep. 2013, pp. 813–816.

[17] A. Zafarana, O. Zambetti, G. Lingua, and S. Saggini, "Digital multiphase constant on-time regulator supporting energy proportional computing," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Charlotte, NC, USA, Mar. 2015, pp. 1946–1949.

[18] W.-L. Zeng, Z.-Y. Lin, C.-S. Lam, M.-K. Law, S.-W. Sin, F. Maloberti, M.-C. Wong, and R. P. Martins, "Design of KY converter with constant on-time control under DCM operation," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 10, pp. 1753–1757, Oct. 2019.

[19] W. Fu, S. T. Tan, M. Radhakrishnan, R. Byrd, and A. A. Fayed, "A DCM-only buck regulator with hysteretic-assisted adaptive minimum-on-time control for low-power microcontrollers," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 418–429, Jan. 2016.

[20] B. M. Cassidy, D. S. Ha, and Q. Li, "Constant ON-time 3-level buck converter for low power applications," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Montreal, QC, Canada, Sep. 2015, pp. 1434–1441.

[21] Y.-H. Lee, S.-J. Wang, and K.-H. Chen, "Quadratic differential and integration technique in $V_2$ control buck converter with small ESR capacitor," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 829–838, Apr. 2010.

[22] Q. U. Ain, D. Khan, B. G. Jang, M. Basim, K. Shehzad, M. Asif, D. Verma, I. Ali, Y. G. Pu, K. C. Hwang, Y. Yang, and K.-Y. Lee, "A high-efficiency fast transient COT control DC–DC buck converter with current reused current sensor," *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9521–9535, Aug. 2021.

[23] W. Huang, "A new control for multi-phase buck converter with fast transient response," in *Proc. APEC. 16th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2001, pp. 273–279.

[24] Y. Yen Mai and P. Mok, "A constant frequency output-ripple-voltage-based buck converter without using large ESR capacitor," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, no. 8, pp. 748–752, Aug. 2008.

[25] S. Ziegler, R. C. Woodward, H. Iu, and L. J. Borle, "Lossless inductor current sensing method with improved frequency response," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1218–1222, May 2009.

[26] document TPS53014, Datasheet, Texas Instrument, Dallas, TX, USA, May 2012. [Online]. Available: http://www.ti.com/lit/ds/symlink/tps53014.pdf

[27] document TPS549D22, Datasheet, Texas Instrument, Dallas, TX, USA, Aug. 2016. [Online]. Available: http://www.ti.com/lit/ds/symlink/tps549D22.pdf

[28] S. C. Huerta, P. Alou, J. A. Oliver, O. Garcia, J. A. Cobos, and A. Abou-Alfotouh, "Design methodology of a non-invasive sensor to measure the current of the output capacitor for a very fast non-linear control," in *Proc. 24th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Washington, DC, USA, Feb. 2009, pp. 806–811.

[29] Y. Yan, P.-H. Liu, F. Lee, Q. Li, and S. Tian, "$V^2$ control with capacitor current ramp compensation using lossless capacitor current sensing," in *Proc. IEEE Energy Convers. Congr. Expo.*, Denver, CO, USA, Sep. 2013, pp. 117–124.

[30] W.-W. Chen, J.-F. Chen, T.-J. Liang, L.-C. Wei, J.-R. Huang, and W.-Y. Ting, "A novel quick response of RBCOT with VIC ripple for buck converter," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4299–4307, Sep. 2013.

[31] Y.-C. Lin, C.-J. Chen, D. Chen, and B. Wang, "A ripple-based constant on-time control with virtual inductor current and offset cancellation for DC power converters," *IEEE Trans. Power Electron.*, vol. 27, no. 10, pp. 4301–4310, Oct. 2012.

[32] J. Li and F. C. Lee, "Modeling of $V^2$ current-mode control," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 9, pp. 2552–2563, Sep. 2010.

[33] W.-C. Chen, C.-S. Wang, Y.-P. Su, Y.-H. Lee, C.-C. Lin, K.-H. Chen, and M.-J. Du, "Reduction of equivalent series inductor effect in delay-ripple reshaped constant on-time control for buck converter with multilayer ceramic capacitors," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2366–2376, May 2013.

[34] C.-H. Tsai, S.-M. Lin, and C.-S. Huang, "A fast-transient quasi-$V^2$ switching buck regulator using AOT control with a load current correction (LCC) technique," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3949–3957, Aug. 2013.

[35] H.-C. Lin, B.-C. Fung, and T.-Y. Chang, "A current mode adaptive on-time control scheme for fast transient DC–DC converters," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2008, pp. 2602–2605.

[36] Murata Manufacturing Co. Ltd. *GRT32EC81A226KE13K Datasheet*. Japan. [Online]. Available: https://psearch.en.murata.com/capacitor/product/GRT32EC81A226KE13%23.pdf

[37] Monolithic Power Systems. (Jul. 2017). *NB679A Datasheet*. [Online]. Available: https://www.monolithicpower.com/en/documentview/productdocument/index/doc_url/L24vYi9uYjY3OWFfcjEuMDMucGRm/prod_id/MTA0OA/

[38] Richtek Technology Corp. (2018). *RT6228C Datasheet*. Taiwan. [Online]. Available: https://www.richtek.com/assets/product_file/RT6228A=RT6228B=RT6228C/DS6228ABC-02.pdf

[39] B. Wang, D. Chen, C.-J. Chen, and S.-F. Hsiao, "Stability prediction of integrated-circuit based constant ON-time controlled buck converters," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6838–6849, Jun. 2021.

[40] D. Goder and W. R. Pelletier, "$V^2$ architecture provides ultra-fast transient response in switch mode power supplies," in *Proc. HFPC*, 1996, pp. 19–23.

[41] K.-Y. Cheng, F. Yu, F. C. Lee, and P. Mattavelli, "Digital enhanced $V^2$-type constant on-time control using inductor current ramp estimation for a buck converter with low-ESR capacitors," *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1241–1252, Mar. 2013.

[42] Q. Sun, Y. Ma, Z. Ye, X. Wang, and H. Zhang, "A pseudo-constant frequency constant on-time buck converter with internal current ripple injection and output DC offset cancellation," *IEEE Access*, vol. 7, pp. 175443–175453, 2019.

[43] B. Yuan, M.-X. Liu, W. T. Ng, and X.-Q. Lai, "A fast-response RBAOT-controlled buck converter with pseudofixed switching frequency and enhanced output accuracy," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 1, pp. 79–88, Feb. 2021.

[44] S. Tian, F. C. Lee, P. Mattavelli, K. Cheng, and Y. Yan, "Small-signal analysis and optimal design of external ramp for constant on-time $V^2$ control with multilayer ceramic caps," *IEEE Trans. Power Electron.*, vol. 29, no. 8, pp. 4450–4460, Aug. 2014.

[45] S. Tian, F. C. Lee, P. Mattavelli, and Y. Yan, "Small-signal analysis and optimal design of constant frequency $V^2$ control," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1724–1733, Apr. 2015.

**YAN-KUN XIA** was born in Hubei, China, in 1984. He received the Ph.D. degree from Southwest Jiaotong University, Chengdu, China, in 2014. He is currently an Associate Professor with Xihua University. He is also a Researcher with the Traction Power State Key Laboratory, Southwest Jiaotong University. His recent research interests include modeling, Simulink, and measurement of power system and new technology.



**JIANG-PING HE** received the M.Sc. and Ph.D. degrees in microelectronics from the University of Electronic Science and Technology of China (UESTC), Chengdu, China, in 2004 and 2016, respectively. From 2004 to 2017, he was an Engineer, a Senior Engineer, and the Manager of the Chengdu Research and Development Center, Eutech Micro Inc., during where he focused on the switching power supply, LED driver and motor driver design, and finished more than ten IC's from design to mass production. He is currently a Lecturer with Xihua University (XHU), Chengdu. His current research interests include switching power supply, LED driver, load switch, and motor driver.



**YONG-QIANG CHEN** received the B.S. degree in physics education from Sichuan Normal University, Chengdu, China, in 1995, and the M.S. degree in electric power system and automation from Xihua University, Chengdu, in 2005. Since 1995, he has been working on electric power system research and development with XHU, where he is currently a Professor with XHU. His current research interests include distribution network optimization and power grid dispatching automation.



**XIN-RUI LIU** was born in Sichuan, China, in 1999. He received the B.S. degree in electrical engineering from the Tianjin Sino-German University of Applied Sciences, in 2022. He is currently pursuing the M.S. degree in electrical engineering with the Department of Electrical Engineering, Xihua University. His research interests include DC/DC power management and power integrated circuit design.



**CHANG-DONG WU** (Member, IEEE) received the M.Sc. degree in mechanical engineering from Southwest Jiaotong University (SJU), Chengdu, China, in 2008. Since 2008, he has been an Assistant Professor with Xihua University (XHU), Chengdu. His current research interests include signal processing and image processing.

• • •