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RESEARCH ARTICLE

A Control Strategy Based on Intermediate Bus Voltage Information for Wide-Range High-Efficiency Step-Up DC–DC Converters

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ABSTRACT With the increasing utilization of renewable energy generation, especially photovoltaic (PV) power generation, the technology for wide-range high-efficiency DC-DC converters is becoming increasingly important. This paper focuses on the control of high-efficiency step-up DC-DC converters with the multi-phase Boost and LLC (MPBLLC) converter. A control strategy based on intermediate bus voltage information is proposed to improve the efficiency over a wide input voltage range. The operation principle and the time domain model of the converter are analyzed first. Since the loss models in previous studies are not accurate and comprehensive enough, a loss modeling method for the variable voltage is proposed. It is based on the time domain analysis (TDA) and is available for a wide voltage range. By analyzing the level and influence factors of variables in the MPBLLC converter, a fast algorithm for loss modeling is also proposed. Further, the control strategy including the optimal bus voltage control is proposed for MPBLLC converter. Control modes are analyzed in detail. For the key part, four different control approaches are presented based on different variations of the intermediate bus voltage. Above all, the optimal bus voltage control is proposed based on the proposed variable bus loss model. Finally, a 500-W experimental prototype is built to verify the effectiveness of the proposed loss model and control strategy, which demonstrates good performance and high efficiency over a wide input voltage range.

INDEX TERMS Loss modeling, control strategy, high efficiency, intermediate bus voltage information, multi-phase boost and LLC (MPBLLC) converter, wide input voltage range.

I. INTRODUCTION

IN RECENT years, renewable energy such as photovoltaic energy has drawn a lot of attention, which is more abundant and cleaner compared to fossil energy [1], [2], [3]. As an important component of PV power generation systems, DC-DC converters have developed rapidly due to their inherent advantages in control, protection, increased voltage levels and efficiency [4], [5], [6], [7]. Fig. 1 illustrates the structure of PV generation integrated into the medium-voltage DC (MVDC) grid [4]. Fig. 2 shows a two-stage step-up converter that is widely used in this system. The multi-phase Boost (MPB) topology is applied in the front stage, which can match both centralized PV system and distributed PV system application scenarios. The LLC topology is employed in the back stage for isolation and boosting the voltage further. Efficiency and voltage range are important metrics of this two-stage converter, for which some optimization and improvement work has been done.

The efficiency can be improved by both parameter design and control strategy. Properly designing the magnetizing inductor in the LLC stage can extend the soft-switching range and reduce conduction losses [8]. However, the efficiency improvement is limited by optimizing only one parameter.

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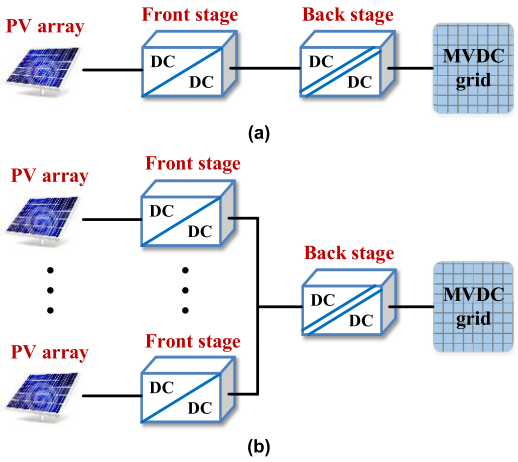

FIGURE 1. The structure of PV generation integrated into the MVDC grid. (a) Centralized PV system. (b) Distributed PV system.

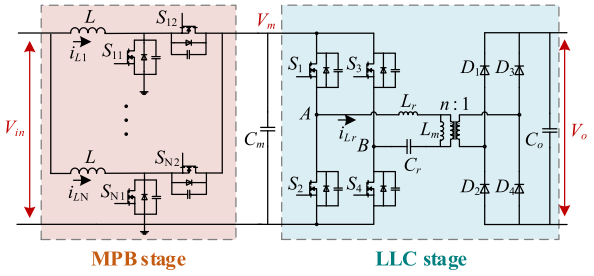

FIGURE 2. The MPBLLC converter.

In [9], in order to improve the efficiency, the duty cycle in the MPB stage is designed properly and the magnetic components in the LLC stage are optimized. The design methodology based on First-Harmonic Approximation (FHA) analysis and TDA has been well developed in previous studies. In contrast, the corresponding control strategy still need to be improved. In [10], the losses of the MPBLLC converter are roughly analyzed with simplified models. The rough analysis is still used for design. Control strategies require more accurate analysis to balance the efficiency of the front and back stages. In addition, optimizing the modulation strategy can improve the efficiency. A bipolar symmetric phase shift modulation strategy is proposed for integrated two-stage DC-DC converter to achieve high efficiency [11]. In [11], the currents of primary switches are analyzed. Accurate loss models remain to be developed.

One important feature of the two-stage converter is that it has an intermediate bus. The variation of the intermediate bus voltage has impact on the operating states of the front and back stages, which consequently affects the efficiency. A converter can switch between the full bridge and half bridge to control the bus voltage level, which improves light-load efficiency [12] and dynamic performance [13]. It only allows the bus voltage to switch between the two voltage levels. In [14], the MPB stage is replaced with the SEPIC topology in onboard battery charger applications, which proves to improve the efficiency. However, the control is performed only for the front stage and the LLC stage operates in open loop at the resonant frequency. The output voltage follows the intermediate bus voltage. When the LLC stage operates at the resonant frequency, the selection of the intermediate bus voltage is further considered [15]. In [16], an adaptive intermediate bus voltage control for different loads is proposed to improve the heavy-load efficiency. And it is still the goal that the LLC stage operates as close to the resonant frequency as possible. This can only lead to a high efficiency of the LLC stage. When the LLC stage operates below the resonant frequency, the effect of intermediate bus voltage on the efficiency of the MPB stage is not taken into account. To achieve the optimization of the overall efficiency, the losses below the resonant frequency need to be analyzed and modeled. Furthermore, the control needs to make full use of the intermediate bus voltage information.

In addition, some researches are investigated on evolved topologies and similar topologies. In [17] and [18], an evolved topology called two-phase interleaved buck-boost-LLC converter and the comprehensive optimal design method are proposed for miniaturization applications to achieve high efficiency. In [19], a two-phase interleaved boost integrated LLC converter is proposed for wide input voltage range. The modulation strategy of this converter is more complex than that of a two-stage converter consisting of basic topologies. A two-stage converter with variable frequency multiplier (VFX) LLC is proposed for offline power supply applications in [20]. The VFX technique is used to provide different voltage gains. In [21], a control strategy for the integrated Boost-LLC converter is proposed to achieve the constant intermediate bus voltage and output voltage. Its application is limited to the LED driver. A similar two-stage converter with buck-boost topology is proposed for wide output voltage range in [22]. The losses are still roughly evaluated and the LLC stage operates only at the resonant frequency. In [23], a similar two-stage converter with power factor correction Boost is proposed. Single controlled PWM technique is adopted, and the fixed-frequency control is still used in the LLC stage. Overall efficiency still cannot be optimized. Therefore, the control strategy aimed at efficiency improvement remain to be studied.

The contribution of this paper is to propose a control strategy based on intermediate bus voltage information. The control strategy contributes to a high efficiency of two-stage converter in a wide input voltage range. The accurate loss modeling method and the step-by-step fast algorithm based on TDA are also proposed in favor of the comparison, optimization and validation of control approaches. Further optimal bus voltage control is proposed.

This paper is organized as follows. The operation principles and TDA of MPBLLC converter are described in

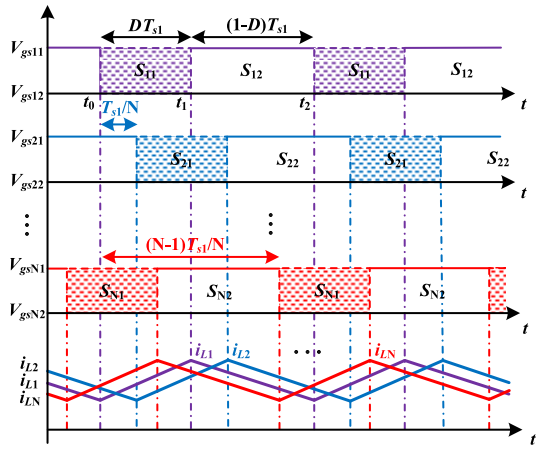

FIGURE 3. The operating waveforms in the MPB stage.

Section II. The loss modeling approach and the step-by-step fast algorithm for the variable bus voltage is proposed and analyzed in detail in Section III. In Section IV, the control strategy based on intermediate bus voltage information is proposed for the wide-input-voltage-range high-efficiency MPBLLC converter. And in the key part of the control strategy, 4 different control approaches are provided, including proposed optimal bus voltage control based on the loss model. In Section V, the steady-state performance, dynamic performance and efficiency of the experimental prototype with the proposed control strategy are verified. The proposed loss model is also demonstrated by experimental results for different control approaches. Finally, Section VI provides the conclusions.

II. PRINCIPLES OF THE MPBLLC CONVERTER

A. OPERATION PRINCIPLES OF THE MPB STAGE

Fig. 3 illustrates the operation waveforms of the MPB stage. The time difference between two adjacent phases is T_{s1}/N, where T_{s1} is the switching period and N is the number of phases. The operation of Phase 1 is as follows, and other $(N-1)$ phases work similarly.

$t_0 \sim t_1$: S_{11} is on. S_{12} is off. The voltage across the inductor L is V_{in}. The inductor current i_L increases linearly with a slope of V_{in}/L.

$t_1 \sim t_0 + T_{s1}$: S_{12} is on. S_{11} is off. The voltage across the inductor L is $V_{in} - V_m$. The inductor current i_L decreases linearly with a slope of $V_{in} - V_m/L$.

According to the volt-second balance, the following constraints is satisfied,

$$V_{in} \cdot DT_{s1} = (V_{in} - V_m) \cdot (1 - D)\, T_{s1} \tag{1}$$

where D is the duty cycle of the MPB stage.

Therefore, the voltage gain of the MPB stage is

$$M_{MPB} = \frac{V_m}{V_{in}} = \frac{1}{1 - D}. \tag{2}$$

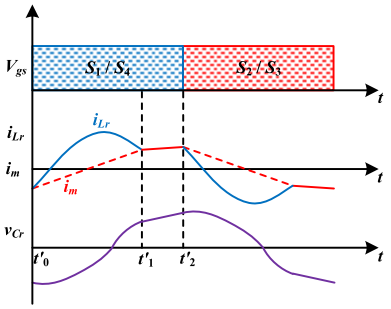

FIGURE 4. The operating waveforms in the LLC stage.

B. TIME DOMAIN ANALYSIS OF THE LLC STAGE

The TDA method for the LLC stage can obtain the voltage and current at each moment at different frequencies more accurately, which helps to build the loss model. To ensure high efficiency over the full voltage range, the LLC stage operates in PO mode (below the resonant frequency), as shown in Fig. 4. The operation mode of the LLC stage in half a switching period is as follows. It is symmetrical in the other half.

$t'_0 \sim t'_1$: S_1, S_4, D_1 and D_4 are on. S_2, S_3, D_2 and D_3 are off. The magnetizing inductor L_m is clamped by nV_o. The magnetizing current i_m increases linearly. L_r resonates with C_r. The input voltage to the resonant circuit is $V_m - nV_o$. The resonant current, the voltage across the resonant capacitor and the magnetizing current can be expressed as

$$\begin{cases} i_{Lr}(t) = \dfrac{V_m - nV_o - v_{Cr}(0)}{\omega_1 L_r} \sin(\omega_1 t) - I_m \cos(\omega_1 t) \\ v_{Cr}(t) = (V_m - nV_o) - (V_m - nV_o - v_{Cr}(0)) \cos(\omega_1 t) \\ \qquad\qquad -\omega_1 L_r I_m \sin(\omega_1 t) \\ i_m(t) = -I_m + \dfrac{nV_o}{L_m} t \end{cases} \tag{3}$$

where ω_1 is the resonant angular frequency of the L_r and C_r resonant circuit, called the first resonant angular frequency, and $\omega_1 = 1/\sqrt{L_r C_r}$. I_m is the maximum value of magnetizing current.

$t'_1 \sim t'_2$: S_1 and S_4 are on. D_1, D_2, D_3 and D_4 are all off. L_m, L_r resonate together with C_r. The input voltage to the resonant circuit is V_m. The secondary side circuit is disengaged. The primary side does not transfer energy to the secondary side. The resonant current, the voltage across the resonant capacitor and the magnetizing current can be expressed as

$$\begin{cases} i_{Lr}(t) = \dfrac{V_m - v_{Cr}(t'_1)}{\omega_2 (L_r + L_m)} \sin(\omega_2 (t - t'_1)) + i_{Lr}(t'_1) \cos(\omega_2 (t - t'_1)) \\ v_{Cr}(t) = V_m - (V_m - v_{Cr}(t'_1)) \cos(\omega_2 (t - t'_1)) \\ \qquad\qquad +\omega_2 (L_r + L_m) i_{Lr}(t'_1) \sin(\omega_2 (t - t'_1)) \\ i_m(t) = i_{Lr}(t) \end{cases} \tag{4}$$

where ω_2 is the resonant angular frequency of the L_r, L_m and C_r resonant circuit, called the second resonant angular frequency, and $\omega_2 = 1/\sqrt{(L_r + L_m)\, C_r}$.

By normalizing (3) and (4) and in angular coordinates, they can be transformed into (5) and (6), respectively.

When $0 \le \theta \le \theta_1$,

$$\begin{cases} i^*_{Lr}(\theta) = -I^*_m \cos\theta + (1 - M_{LLC} - v^*_{Cr}(0)) \sin\theta \\ v^*_{Cr}(\theta) = -I^*_m \sin\theta - (1 - M_{LLC} - v^*_{Cr}(0)) \cos\theta \\ \qquad\qquad +(1 - M_{LLC}) \\ i^*_m(\theta) = -I^*_m + \dfrac{M_{LLC}\theta}{k}. \end{cases} \tag{5}$$

When $\theta_1 \le \theta \le \theta_2$,

$$\begin{cases} i^*_{Lr}(\theta) = i^*_{Lr}(\theta_1)\cos(\dfrac{(\theta-\theta_1)}{\sqrt{1+k}}) + \dfrac{1-v^*_{Cr}(\theta_1)}{\sqrt{1+k}} \sin(\dfrac{(\theta-\theta_1)}{\sqrt{1+k}}) \\ v^*_{Cr}(\theta) = \sqrt{1+k}\, i^*_{Lr}(\theta_1) \sin(\dfrac{(\theta-\theta_1)}{\sqrt{1+k}}) \\ \qquad\qquad -(1 - v^*_{Cr}(\theta_1)) \cos(\dfrac{(\theta-\theta_1)}{\sqrt{1+k}}) + 1 \\ i^*_m(\theta) = i^*_{Lr}(\theta) \end{cases} \tag{6}$$

where M_{LLC} is the voltage gain of the LLC stage and $M_{LLC} = nV_o/V_m$. θ_1 is the angle corresponding to t_1'. k is the ratio of the magnetizing inductance to the resonant inductance and $k = L_m/L_r$.

The standardized expressions contain unknown parameters. The boundary conditions can be obtained from the relationship of the instantaneous voltage and current, as in (7).

$$\begin{cases} i^*_{Lr}(\theta_2) = I^*_m \\ v^*_{Cr}(\theta_2) = -v^*_{Cr}(0) \\ i^*_m(\theta_1) = i^*_{Lr}(\theta_1) \end{cases} \tag{7}$$

where θ_2 is the angle corresponding to t_2'.

In addition, the relationship between resonant current, magnetizing current and load can be expressed as

$$C_r(v^*_{Cr}(\theta_1) - v^*_{Cr}(0)) + C_r I^*_m \theta_1 - \frac{M}{2L_m\omega_1^2}\theta_1^2 = \frac{M_{LLC}}{Z_r}\frac{8}{\pi^2}\frac{QT_{s2}}{2} \tag{8}$$

where Z_r is the characteristic impedance and $Z_r = \sqrt{L_r/C_r}$. θ_1 is the angle corresponding to t_1'. Q is the quality factor and $Q = 1/R_{eq}\sqrt{L_r/C_r}$, where R_{eq} is the equivalent resistance that is converted to the primary side and $R_{eq} = 8n^2R_L/\pi^2$. T_{s2} is the switching period of the LLC stage.

Combining (7), (8) and the initial conditions, the equations of the numerical method is organized as

$$\begin{cases} I^*_m = i^*_{Lr}(\theta_1)\cos(\dfrac{(\theta_2-\theta_1)}{\sqrt{1+k}}) + \dfrac{1-v^*_{Cr}(\theta_1)}{\sqrt{1+k}} \sin(\dfrac{(\theta_2-\theta_1)}{\sqrt{1+k}}) \\ -v^*_{Cr}(0) = \sqrt{1+k}\, i^*_{Lr}(\theta_1) \sin(\dfrac{(\theta_2-\theta_1)}{\sqrt{1+k}}) \\ \qquad -(1 - v^*_{Cr}(\theta_1)) \cos(\dfrac{(\theta-\theta_1)}{\sqrt{1+k}}) + 1 \\ \dfrac{M_{LLC}\theta_1}{k} = -I^*_m \cos(\theta_1) + (1 - M_{LLC} - v^*_{Cr}(0)) \sin(\theta_1) + I^*_m \\ \theta_2 = \dfrac{\pi}{f_n} \\ i^*_{Lr}(\theta_1) = -I^*_m \cos(\theta_1) + (1 - M_{LLC} - v^*_{Cr}(0)) \sin(\theta_1) \\ v^*_{Cr}(\theta_1) = -I^*_m \sin(\theta_1) - (1 - M_{LLC} - v^*_{Cr}(0)) \cos(\theta_1) \\ \qquad +(1 - M_{LLC}) \\ \dfrac{M_{LLC}}{Z_r}\dfrac{8}{\pi^2}\dfrac{QT_{s2}}{2} = C_r(v^*_{Cr}(\theta_1) - v^*_{Cr}(0)) + C_r I^*_m \theta_1 \\ \qquad -\dfrac{M_{LLC}}{2L_m\omega_1^2}\theta_1^2 \end{cases} \tag{9}$$

where f_n is the normalized frequency and $f_n = f_{s2}/f_r$, where f_{s2} and f_r are the switching frequency and the first resonant frequency of the LLC stage, respectively.

The angles, voltages, currents at commutating time and the voltage gain (i.e., θ_1, θ_2, I^*_m, $v^*_{Cr}(0)$, $v^*_{Cr}(\theta_1)$, $i^*_{Lr}(\theta_1)$, and M_{LLC}) can be obtained with the help of numerical analysis software for the determined k, Q and f_{s2}. Then, t_1', t_2', I_m, $v_{Cr}(0)$, $v_{Cr}(t_1')$, $i_{Lr}(t_1')$ are found. k and Q can be obtained from the resonance parameters of the LLC stage. Therefore, above variables are as functions of f_{s2}. i_{Lr}, i_m, the secondary current i_s, and M_{LLC} can be expressed as (10)–(13), shown at the bottom of the next page.

The above voltage gain is completely derived from the time domain model. Therefore, it is accurate enough to be used for loss modeling and the analysis of different control methods.

III. THE PROPOSED LOSS MODELING APPROACH AND FAST ALGORITHM FOR THE VARIABLE BUS VOLTAGE

In this section, the loss modeling method with bus voltage as a variable is proposed. The modeling process is analyzed in detail.

A. LOSS MODELING OF THE MPB STAGE FOR THE VARIABLE BUS VOLTAGE

When a MOSFET is turned on, the current through it rises rapidly and its terminal voltage drops rapidly. However, during this process, the voltage and current changes are overlapping and turn-on losses are incurred. When a MOSFET is turned off, its terminal voltage rises rapidly and the current through it falls rapidly. However, during this process, the voltage and current changes are interleaved and turn-off losses are incurred. In practice, voltage or current spikes can be handled by snubber circuits. Therefore, the turn-on and turn-off processes can be linearized, as shown in Fig. 5 [24].

On average, there are $2N$ MOSFETs per period that undergo the turn-on process in the N-phase Boost stage.

Therefore, the turn-on losses of the MPB stage can be expressed as

$$P_{MPB\_turn\_on} = 2N \cdot f_{s1} \int_{t_A}^{t_A+t_{s(on)}} v_{s1}(t) i_{s1}(t) dt \tag{14}$$

where f_{s1} is the switching frequency of the MPB stage. t_A is the initial moment of turning on. $t_{s(on)}$ is the turn-on time of the MOSFET, which can be found in the datasheet. $v_{s1}(t)$ represents the terminal voltage as a function of time during the turn-on process. $i_{s1}(t)$ represents the current through the MOSFET as a function of time during the turn-on process.

According to the waveforms of $v_{s1}(t)$ and $i_{s1}(t)$ shown in Fig. 5(a), the turn-on losses can be further deduced as

$$P_{MPB\_turn\_on} = 2NV_m I_L t_{s(on)} f_{s1} \tag{15}$$

where I_L is the average value of the inductor current.

The current flowing through the inductor in each phase of the MPB stage can be expressed as

$$I_L = \frac{P_{in}}{NV_{in}} \tag{16}$$

where P_{in} is the power input to the converter.

Substituting (16) into (15), (17) is derived as

$$P_{MPB\_turn\_on} = 2\frac{V_m}{V_{in}} P_{in} f_{s1} t_{s(on)} = \frac{2P_{in} f_{s1} t_{s(on)}}{1-D}. \tag{17}$$

In the same way, the turn-off loss of the MPB stage can be derived as

$$P_{MPB\_turn\_off} = 2\frac{V_m}{V_{in}} P_{in} f_{s1} t_{s(off)} = \frac{2P_{in} f_{s1} t_{s(off)}}{1-D} \tag{18}$$

where $t_{s(off)}$ is the turn-off time of the MOSFET, which can be found in the datasheet.

The switching losses are the sum of turn-on losses and turn-off losses, which can be expressed as

$$\begin{aligned} P_{MPBswi} &= 2\frac{V_m}{V_{in}} P_{in} f_{s1} \left(t_{s(on)} + t_{s(off)}\right) \\ &= \frac{2P_{in} f_{s1} \left(t_{s(on)} + t_{s(off)}\right)}{1-D}. \end{aligned} \tag{19}$$

As can be seen that the switching losses are independent of the number of phases. When the input power is determined, the switching losses of the MPB stage increase as the intermediate bus voltage rises and decrease as the input voltage rises. Fig. 6 shows the curves of switching losses in the MPB stage as a function of D and P_{in}. As seen, the switching losses of the MPB stage increase as the duty cycle increases. Therefore, in order to ensure high efficiency, the duty cycle should not be too large.

The conduction losses of the MPB stage are mainly caused by the turn-on resistances ($r_{ds(on)}$) of MOSFETs and conduction resistances of inductors, which can be expressed as

$$P_{MPBcon} = N \cdot I_{L\_RMS}^2 (r_{ds(on)} + r_L) \tag{20}$$

where r_L is the equivalent resistance of the inductor, which can be tested by a high-precision impedance analyzer. I_{L_RMS} is the root-mean-square (RMS) value of the inductor current.

As the key variable in (20), the generic expression for i_{L_RMS} is

$$I_{L\_RMS} = \sqrt{\frac{1}{T_{on}} \int_{t_0}^{t_0+T_{on}} i_L^2(t) dt} \tag{21}$$

where T_{on} is the on-time of the lower-side switching device in the MPB stage and $T_{on} = DT_{s1} = (1 - V_{in}/V_m)T_{s1}$, where T_{s1} is the switching period of the MPB stage. t_0 is the starting

$$i_{Lr} = A(f_{s2}) = \begin{cases} \left(\dfrac{V_m - nV_o - v_{Cr}(0)}{\omega_1 L_r} \sin(\omega_1 t) - I_m \cos(\omega_1 t)\right)\Big|_{f_{s2}} \\ \left(t_0' \le t \le t_1'\right) \\ \left(\dfrac{V_m - v_{Cr}(t_1')}{\omega_2(L_r + L_m)} \sin(\omega_2(t - t_1')) + i_{Lr}(t_1') \cos(\omega_2(t - t_1'))\right)\Big|_{f_{s2}} \\ \left(t_1' \le t \le t_2'\right) \end{cases} \tag{10}$$

$$i_m = B(f_{s2}) = \begin{cases} \left(-I_m + \dfrac{nV_o}{L_m} t\right)\Big|_{f_{s2}} \left(t_0' \le t \le t_1'\right) \\ \left(\dfrac{V_m - v_{Cr}(t_1')}{\omega_2(L_r + L_m)} \sin(\omega_2(t - t_1')) + i_{Lr}(t_1') \cos(\omega_2(t - t_1'))\right)\Big|_{f_{s2}} \\ \left(t_1' \le t \le t_2'\right) \end{cases} \tag{11}$$

$$i_s = C(f_{s2}) = n(A(f_{s2}) - B(f_{s2})) = \begin{cases} \left(n\left(\dfrac{V_m - nV_o - v_{Cr}(0)}{\omega_1 L_r} \sin(\omega_1 t) \right.\right. \\ \left.\left. - I_m \cos(\omega_1 t) - \dfrac{nV_o}{L_m} t + I_m\right)\right)\Big|_{f_{s2}} \left(t_0' \le t \le t_1'\right) \\ 0 \left(t_1' \le t \le t_2'\right) \end{cases} \tag{12}$$

$$M_{LLC} = m(f_{s2}) = \left(1 - v_{Cr}^*(0) - \frac{i_{Lr}^*(\theta_1) + I_m^* \cos(\theta_1)}{\sin(\theta_1)}\right)\Big|_{f_{s2}} \tag{13}$$

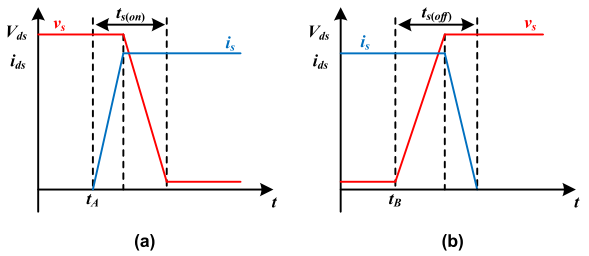

FIGURE 5. Equivalent linear switching process of the MOSFET. (a) Turn-on process. (b) Turn-off process.

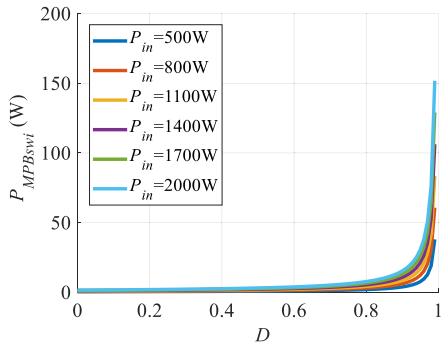

FIGURE 6. Switching losses versus the duty cycle D and the input power P_{in}.

moment of a period. $i_L\,(t)$ represents the inductor current as a function of time during a period.

According to Fig. 3, the instantaneous inductor current during the on-time can be expressed as

$$i_L(t) = \frac{V_{in}}{L}t + I_L - \frac{\Delta I_L}{2} \tag{22}$$

where ΔI_L is the ripple of the inductor current in each phase and $\Delta I_L = T_{on}V_{in}/L$.

Substituting (22) into (21), the conduction losses of the MPB stage can be further deduced as

$$P_{MPBcon} = \left[\frac{P_{in}^2}{NV_{in}^2} + \frac{NV_{in}^2}{12L^2f_{s1}^2}\left(1 - \frac{V_{in}}{V_m}\right)^2\right](r_{ds(on)} + r_L). \tag{23}$$

As can be seen that the conduction losses are also independent of the number of phases. When the input power is determined, the conduction losses of the MPB stage decrease as the input voltage rises.

The losses in the MPB stage are the sum of switching losses and conduction losses, which can be expressed as

$$P_{MPB} = \frac{2P_{in}f_{s1}V_m}{V_{in}}\left(t_{s(on)} + t_{s(off)}\right) + \left[\frac{P_{in}^2}{NV_{in}^2} + \frac{NV_{in}^2}{12L^2f_{s1}^2}\left(1 - \frac{V_{in}}{V_m}\right)^2\right](r_{ds(on)} + r_L). \tag{24}$$

From (24), it can be seen that when the electrical and circuit parameters are determined, the losses in the MPB stage increases with the increase of the intermediate bus voltage.

B. LOSS MODELING OF THE LLC STAGE FOR THE VARIABLE BUS VOLTAGE

The LLC stage often works in PO mode to ensure high efficiency, which enables zero voltage switching (ZVS) on the primary side and zero current switching (ZCS) on the secondary side. Therefore, the turn-on losses of the primary side can be ignored. When silicon carbide Schottky diodes are used for rectification on the secondary side, the reverse recovery current is almost non-existent. Thus, the switching losses on the secondary side can also be disregarded.

On average, there are 4 MOSFETs per period that undergo the turn-off process in the LLC stage. Thus, the turn-off losses of the LLC stage can be expressed as

$$P_{LLC\_turn\_off} = 4f_{s2}\int_{t_B'}^{t_B'+t_{s(off)}} v_{s2}(t)i_{s2}(t)dt \tag{25}$$

where t_B' is the initial moment of turning off. $v_{s2}\,(t)$ represents the terminal voltage as a function of time during the turn-off process. $i_{s2}\,(t)$ represents the current through the MOSFET as a function of time during the turn-off process.

Similar to the derivation of the turn-on losses in the MPB stage, the switching losses and the turn-off losses of the LLC stage can be deduced as

$$P_{LLCswi} = P_{LLC\_turn\_off} = 4V_mI_mt_{s(off)}f_{s2} \tag{26}$$

where I_m is the current flowing through the MOSFET at the initial moment of turning off, which is equal to the magnetizing current in O mode at this time.

The conduction loss of the LLC stage is divided into two main parts, the primary conduction loss and the secondary conduction loss. They can be expressed as (27) and (28), respectively.

$$P_{LLC\_pri\_con} = I_{r\_RMS}^2(r_{Lr} + 2r_{ds(on)} + r_{pw}) \tag{27}$$

$$P_{LLC\_sec\_con} = I_{s\_RMS}^2(r_{sw} + 2r_{ds(on)}) \tag{28}$$

where r_{Lr}, r_{pw} and r_{sw} are the equivalent resistances of the resonant inductor, the primary winding and the secondary winding of the transformer, respectively, which can be tested by a high-precision impedance analyzer. I_{r_RMS} and I_{s_RMS} are RMS values of the resonant current and secondary current, respectively.

According to the definition of RMS value and the half-cycle symmetry in the LLC stage, I_{r_RMS} and I_{s_RMS} can be expressed as (29) and (30), respectively.

$$I_{r\_RMS} = \sqrt{\frac{2}{T_{s2}}\int_{t_0'}^{t_0'+\frac{T_{s2}}{2}} i_{Lr}^2(\mathrm{t})dt} \tag{29}$$

$$I_{s\_RMS} = \sqrt{\frac{2}{T_{s2}}\int_{t_0'}^{t_0'+\frac{T_{s2}}{2}} i_s^2(\mathrm{t})dt} \tag{30}$$

where $i_{Lr}(t)$ and $i_s\,(t)$ refer to (10) and (12).

The voltage gain variation versus switching frequency of LLC stage in PO mode is monotonic. So (31) can be derived

from (13).

$$f_{s2} = m^{-1}\left(M_{LLC}\right) \tag{31}$$

Thus, i_{Lr} and i_s can be expressed as functions with respect to the bus voltage V_m, as in (32) and (33).

$$i_{Lr} = A\left(m^{-1}\left(M_{LLC}\right)\right) = A\left(m^{-1}\left(\frac{nV_o}{V_m}\right)\right) \tag{32}$$

$$i_s = C\left(m^{-1}\left(M_{LLC}\right)\right) = C\left(m^{-1}\left(\frac{nV_o}{V_m}\right)\right) \tag{33}$$

Based on the above analysis, the conduction loss of LLC stage can be derived as

$$\begin{aligned} P_{LLCcon} &= 2f_{s2}\left(\int_{t_0'}^{t_2'} A^2\left(m^{-1}\left(\frac{nV_o}{V_m}\right)\right)dt \cdot \left(r_{Lr} + 2r_{ds(on)} + r_{pw}\right)\right. \\ &\quad \left. + \int_{t_0'}^{t_1'} C^2\left(m^{-1}\left(\frac{nV_o}{V_m}\right)\right)dt \cdot \left(r_{sw} + 2r_{ds(on)}\right)\right). \end{aligned} \tag{34}$$

According to the Steinmetz equation and its correction formula under square wave excitation, the core losses of the resonant inductor and the transformer can be calculated as in (35).

$$\begin{aligned} P_{core} &= k_{Lr} V_{e\_Lr} \left(f_{s2}\right)^{\alpha_{Lr}} \left(\frac{I_{r\_\max} L_r}{N_{Lr} A_{e\_Lr}}\right)^{\beta_{Lr}} \\ &\quad + \frac{8}{\pi^2} k_T V_{e\_T} \left(f_{s2}\right)^{\alpha_T} \left(\frac{I_m L_m}{N_P A_{e\_T}}\right)^{\beta_T} \end{aligned} \tag{35}$$

where k_{Lr}, k_T, α_{Lr}, α_T, β_{Lr}, and β_T are the coefficients related to the core materials of the resonant inductor and the transformer, which can be obtained from the loss density characteristic curve of the core material in the datasheet. V_{e_Lr} and V_{e_T} are the effective volumes of the resonant inductor and transformer, respectively. A_{e_Lr} and A_{e_T} are the effective cross-sectional areas of the resonant inductor and transformer, respectively. The above parameters can be found in the data sheets of cores. N_{Lr} and N_P are the turn numbers of the resonant inductor windings and the primary windings of the transformer, respectively. I_{r_max} is the maximum value of resonant inductor current, which is obtained from the time domain equations in (9).

Finally, the total loss of LLC stage can be derived as

$$\begin{aligned} P_{LLC} &= 2f_{s2}\left(\int_{t_0'}^{t_2'} A^2\left(m^{-1}\left(\frac{nV_o}{V_m}\right)\right)dt \cdot \left(r_{Lr} + 2r_{ds(on)} + r_{pw}\right)\right. \\ &\quad \left. + \int_{t_0'}^{t_1'} C^2\left(m^{-1}\left(\frac{nV_o}{V_m}\right)\right)dt \cdot \left(r_{sw} + 2r_{ds(on)}\right) + 2V_m I_m t_{s(off)}\right) \\ &\quad + k_{Lr} V_{e\_Lr}\left(m^{-1}\left(\frac{nV_o}{V_m}\right)\right)^{\alpha_{Lr}} \left(\frac{I_{r\_\max} L_r}{N_{Lr} A_{e\_Lr}}\right)^{\beta_{Lr}} \\ &\quad + \frac{8}{\pi^2} k_T V_{e\_T}\left(m^{-1}\left(\frac{nV_o}{V_m}\right)\right)^{\alpha_T} \left(\frac{I_m L_m}{N_P A_{e\_T}}\right)^{\beta_T}. \end{aligned} \tag{36}$$

As can be seen from (36), when the output voltage and circuit parameters are determined, the losses in the LLC stage vary with the intermediate bus voltage. The higher the intermediate bus voltage, the lower the losses of the LLC stage.

C. THE OVERALL LOSS MODEL OF MPBLLC CONVERTER

Total losses of the MPBLLC converter are the sum of losses in the MPB stage and losses is the LLC stage, which can be derived as

$$\begin{aligned} P_{MPBLLC} &= \frac{2P_{in} f_{s1} V_m}{V_{in}}\left(t_{s(on)} + t_{s(off)}\right) \\ &\quad + \left[\frac{P_{in}^2}{NV_{in}^2} + \frac{NV_{in}^2}{12L^2 f_{s1}^2}\left(1 - \frac{V_{in}}{V_m}\right)^2\right]\left(r_{ds(on)} + r_L\right) \\ &\quad + 2f_{s2}\left(\int_{t_0'}^{t_2'} A^2\left(m^{-1}\left(\frac{nV_o}{V_m}\right)\right)dt \cdot \left(r_{Lr} + 2r_{ds(on)} + r_{pw}\right)\right. \\ &\quad \left. + \int_{t_0'}^{t_1'} C^2\left(m^{-1}\left(\frac{nV_o}{V_m}\right)\right)dt \cdot \left(r_{sw} + 2r_{ds(on)}\right) + 2V_m I_m t_{s(off)}\right) \\ &\quad + k_{Lr} V_{e\_Lr}\left(m^{-1}\left(\frac{nV_o}{V_m}\right)\right)^{\alpha_{Lr}} \left(\frac{I_{r\_\max} L_r}{N_{Lr} A_{e\_Lr}}\right)^{\beta_{Lr}} \\ &\quad + \frac{8}{\pi^2} k_T V_{e\_T}\left(m^{-1}\left(\frac{nV_o}{V_m}\right)\right)^{\alpha_T} \left(\frac{I_m L_m}{N_P A_{e\_T}}\right)^{\beta_T}. \end{aligned} \tag{37}$$

The efficiency of the MPBLLC converter can be expressed as

$$\eta_{MPBLLC} = \frac{P_{in} - P_{MPBLLC}}{P_{in}}. \tag{38}$$

As can be seen from (37) and (38), when the electrical and circuit parameters are determined, total losses and the efficiency vary with the intermediate bus voltage. Although the influence of V_m on the losses in the MPB stage and in the LLC stage is opposite, the trend of total losses and the efficiency is still uncertain because it is related to the relative magnitude of the influence of the two parties and the control method.

Based on the above analysis and modeling of MPBLLC losses, the total losses can be minimized by adjusting the bus voltage. Therefore, a control strategy for high-efficiency MPBLLC converter in a wide input voltage range is proposed. In addition, the above loss modeling helps to analyze the efficiency that can be achieved by different control approaches.

D. FAST ALGORITHM IMPLEMENTATION FOR LOSS MODELING

The loss model established above is slightly complicated, so it is necessary to implement the above loss model with the help of a fast algorithm, especially for LLC stage.

In order to implement a fast algorithm, it is important to have a clear understanding of where each variable is located and how it is affected. Variables about loss analysis of MPBLLC converters can be divided into 3 levels as shown

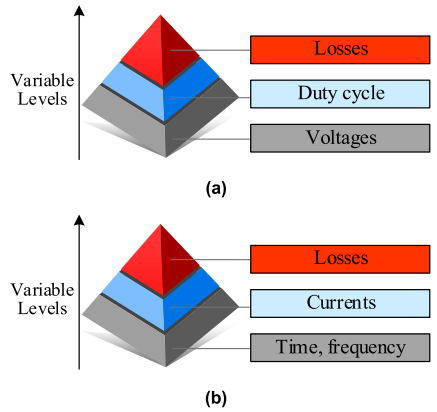

FIGURE 7. Different levels about loss analysis of MPBLLC converters. (a) MPB stage. (b) LLC stage.

TABLE 1. Physical lof MPBLLC converters at a glance.

Physical quantities	MPB stage	LLC stage
Constants	$L, N, P_{in}, f_{s1}, r_{ds}, r_w, r_L, t_r, t_f$	$V_o, R_L, L_r, C_r, L_m, n, k, Q, f_r, r_{ds}, r_{pw}, r_{sw}, r_{Lr}, t_f$
Variables	$V_m(i), V_{in}(k), D(i,k), P_{MPB}(i.k)$	$V_m(i), f_{s2}(i), t(j), i_{Lr}(i,j), i_s(i,j), P_{LLC}(i)$

in Fig. 7. Constants and variables of MPBLLC converters are summarized in Table 1. The intermediate bus voltage, time and the input voltage are three independent variables in the bottom level. i, j and k are the sampling numbers of them, respectively. Thus, the three variables can be expressed as $V_m(i)$, $t(j)$ and $V_{in}(k)$. The switching frequency in the LLC stage is related to $V_m(i)$. Thus, it can be expressed as $f_{s2}(i)$ in the bottom level. In the MPB stage, the duty cycle is determined by $V_m(i)$ and $V_{in}(k)$. It can be expressed as $D(i,k)$ in the middle level. The loss P_{MPB} is determined by $D(i,k)$ and $V_{in}(k)$ according to (19) and (23). It can be expressed as $P_{MPB}(i,k)$ in the top level. In the LLC stage, the instantaneous resonant current and secondary side current are related to $f_{s2}(i)$ and $t(j)$. Thus, they can be expressed as $i_{Lr}(i,j)$ and $i_s(i,j)$ in the middle level, respectively. The RMS values of the resonant current and secondary current are calculated by averaging the integral of the instantaneous currents over time according to (29) and (30). Thus, they are related to $f_{s2}(i)$, and they can be expressed as $i_{r\_RMS}(i)$ and $i_{s\_RMS}(i)$ in the middle level, respectively. The loss P_{LLC} is calculated by $f_{s2}(i)$, $i_{r\_RMS}(i)$ and $i_{s\_RMS}(i)$ according to (26)-(28) and (35). It can be expressed as $P_{LLC}(i)$ in the top level.

The loss algorithm for MPB stage is relatively simple. In contrast, the general algorithm for LLC stage can easily take a lot of operation time due to the presence of the time domain numerical iteration method. Since The instantaneous resonant current and secondary side current are jointly affected by $f_{s2}(i)$ and $t(j)$, the general algorithm needs to solve the time domain equations $i \times j$ times. However, combined with the above analysis, time and frequency are two

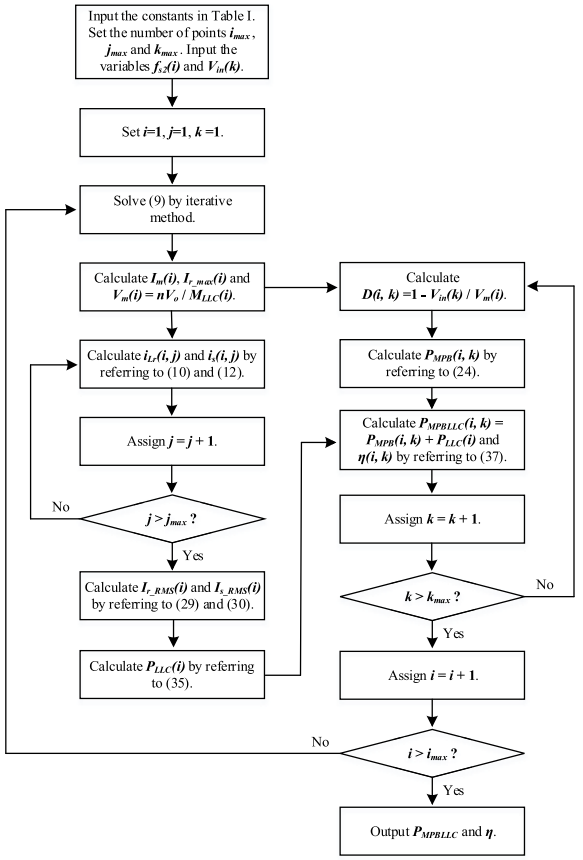

FIGURE 8. The proposed fast algorithm for MPBLLC losses.

TABLE 2. Comparison of the proposed algorithm and the general algorithm.

Algorithm	The general algorithm	The proposed algorithm
Number of iterative algorithm operations	$i \times j$	i
Runtime of 50×100 points with MATLAB	31.62s	10.31s

independent variables, and the time domain equations are solved for currents at commutating time and the intermediate bus voltage at a fixed frequency. Therefore, the iterative algorithm can be run at different frequencies to solve for the intermediate bus voltage. Then the currents at different moments are expanded with time variable. In this way the iterative algorithm only needs to be performed i times, which greatly saves operation time.

The proposed fast algorithm for MPBLLC losses is shown in Fig. 8. Combined with the analysis about variable levels, the variables related to the same sampling number are calculated together, and the variables are calculated sequentially according to variable levels in the fast algorithm. The comparison between the proposed algorithm and the general algorithm is shown in Table 2. When $i = 50$ and $j = 100$, the runtime of the proposed algorithm saves 21.31s compared

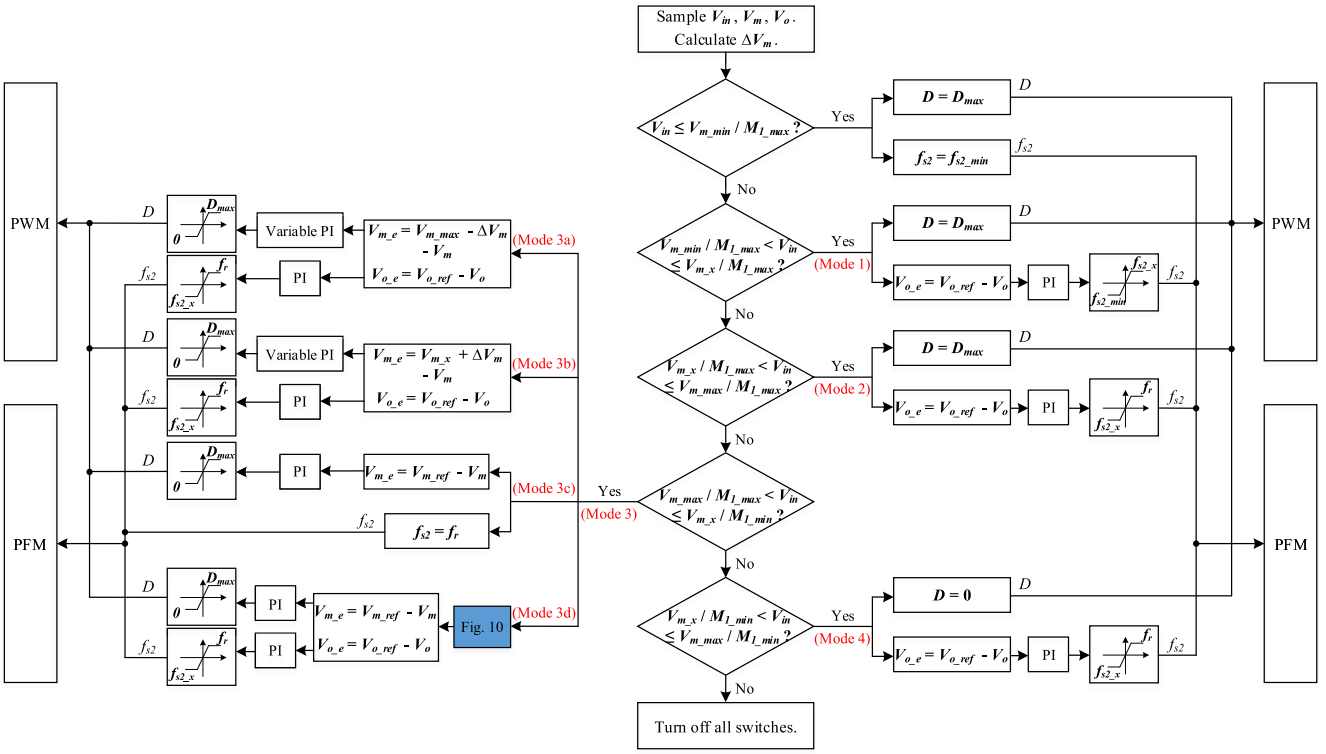

FIGURE 9. The proposed overall control strategy for the wide-range high-efficiency MPBLLC converter.

to the general algorithm with MATLAB. If i continues to increase, the time gap will be longer.

IV. PROPOSED CONTROL STRATEGY FOR THE MPBLLC CONVERTER

A. THE CONTROL STRATEGY FOR THE WIDE INPUT VOLTAGE RANGE MPBLLC CONVERTER

As a two-stage converter, MPBLLC has one more degree of freedom of control than the typical single-stage converter, the intermediate bus voltage V_m. The loss model and algorithm for the variable V_m have been built in Section III. The change in V_m has a significant effect on the losses. Thus, this degree of freedom can be utilized to minimize losses and achieve soft switching and high efficiency over the full voltage range. At the same time, MPBLLC can also extend the input voltage range with the help of an appropriate control strategy. And the fit between its two stages becomes particularly important.

Therefore, an overall control strategy based on intermediate bus voltage information is proposed for a wide-range high-efficiency MPBLLC converter, as shown in Fig. 9. In particular, when $V_{m\_max}/M_{1\_max} \le V_{in} \le V_{m\_x}/M_{1\_min}$, the optimal bus voltage control method (Mode 3d) is proposed. The variables are defined as shown in Table 3.

The main objectives of this control strategy are (1) to achieve the operation over a wide input voltage range, (2) to achieve high efficiency, and (3) to achieve good dynamic performance. The control strategy is divided into 4 main control modes. For Mode 3, four control options are available, Mode 3a, Mode 3b, Mode 3c and Mode 3d. According to the loss model and algorithm in Section III, the advantages and disadvantages of first three control approaches can be evaluated for converter applications with different parameters. Mode 3d, based on the proposed loss model, is superior to the first three control approaches and is able to regulate the intermediate bus voltages to maximize the two-stage efficiency.

TABLE 3. Definition of variables.

Variables	Definition
D_{max}	The maximum duty cycle set.
f_{s2_min}	The lowest switching frequency set in the LLC stage.
f_{s2_x}	The critical switching frequency that ensures that LLC operate in PO mode over the full voltage range.
M_{1_min}	The voltage gain of the MPB stage when $D = 0$. $M_{1\_min} = 1$.
M_{1_max}	The voltage gain of the MPB stage when $D = D_{max}$.
M_{2_x}	The voltage gain of the LLC stage when $f_{s2} = f_{s2\_x}$.
M_{2_max}	The voltage gain of the LLC stage when $f_{s2} = f_{s2\_min}$.
V_{m_min}	$V_{m\_min} = V_o/M_{2\_max}$.
V_{m_x}	$V_{m\_x} = V_o/M_{2\_x}$.
V_{m_max}	$V_{m\_max} = V_o$.
V_{o_ref}	The given output voltage.
V_{m_ref}	The calculated or given intermediate bus voltage.

1) MODE 1

When $V_{m\_min}/M_{1\_max} < V_{in} \le V_{m\_x}/M_{1\_max}$, it enters the control range of MPBLLC converter. At this time, constant duty cycle (CD) is applied to reduce the burden on the

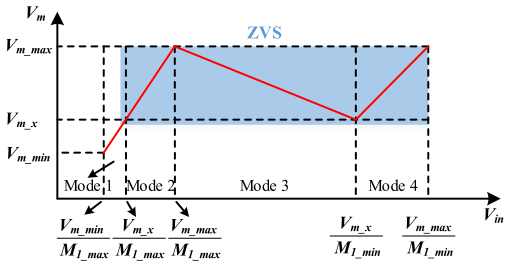

FIGURE 10. Soft-switching working area of MPBLLC converter.

controller in the MPB stage, and the duty cycle is set to the maximum. The insufficient step-up ratio is completely supplemented by the LLC. In the LLC stage, variable frequency (VF) control is employed. The output voltage keeps stable at the given value. The frequency variation ranges from f_{s2_min} to f_{s2_x}.

2) MODE 2

When $V_{m\_x}/M_{1\_max} < V_{in} \leq V_{m\_max}/M_{1\_max}$, the control enters Mode 2. CD and VF controls are still used. The duty cycle is set to the maximum. The intermediate bus voltage can be maintained in the range of V_{m_x} to V_{m_max}. The frequency variation ranges from f_{s2_x} to f_r. The LLC stage operates in PO mode over the full voltage range to maintain high efficiency.

3) MODE 3A

When $V_{m\_max}/M_{1\_max} < V_{in} \leq V_{m\_x}/M_{1\_min}$, the control enters Mode 3. In Mode 3, the intermediate bus voltage can be controlled to be variable or constant, which can lead to a significant difference in efficiency.

The first control approach is that the intermediate bus voltage varies inversely with the input voltage, that is, Mode 3a. The variation of V_m can be deduced as

$$\Delta V_m = \frac{V_{in} - \frac{V_{m\_\max}}{M_{1\_\max}}}{\frac{V_{m\_x}}{M_{1\_\min}} - \frac{V_{m\_\max}}{M_{1\_\max}}} \left(V_{m\_\max} - V_{m\_x}\right). \tag{39}$$

V_{m_ref} can be further derived as

$$V_{m\_ref} = V_{m\_\max} - \Delta V_m. \tag{40}$$

The controller parameters need to change accordingly to achieve good control performance. Variable PI variable voltage (VPIVV) control is applied in the MPB stage. VF control is still used in the LLC stage. If V_{in} changes from V_{m_max}/M_{1_max} to V_{m_x}/M_{1_min}, V_m will change from V_{m_max} to V_{m_x}, the duty cycle in the MPB stage will change from D_{max} to 0, and the switching frequency in the LLC stage will change from f_r to f_{s2_x}.

4) MODE 3B

In Mode 3, the second control approach is that the intermediate bus voltage varies positively with the input voltage, i.e.,

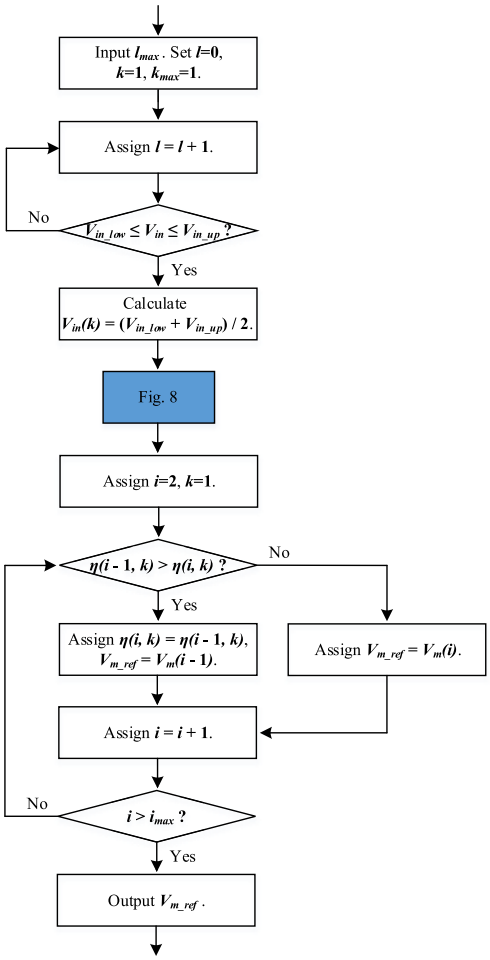

FIGURE 11. Optimal bus voltage control algorithm for high efficiency (Mode 3d).

Mode 3b. Under the circumstances, V_{m_ref} can be derived as

$$V_{m\_ref} = V_{m\_x} + \Delta V_m. \tag{41}$$

Similarly, the controller parameters need to change to achieve superior performance. VPIVV and VF controls are still used. If V_{in} changes from V_{m_max}/M_{1_max} to V_{m_x}/M_{1_min}, V_m will change from V_{m_x} to V_{m_max}, the duty cycle in the MPB stage will change from a larger value to a smaller value, without reaching the upper and lower limits., and the switching frequency in the LLC stage will change from f_{s2_x} to f_r.

5) MODE 3C

In Mode 3, the third control approach is to keep the intermediate bus voltage constant, i.e., Mode 3c. In this case, V_{m_ref} can be chosen to be any value between V_{m_x} and V_{m_max}. Constant PI constant voltage (CPICV) control is applied in the MPB stage. Since V_m is controlled to be constant, the constant frequency (CF) can be employed in order to reduce the burden on the controller in the LLC stage.

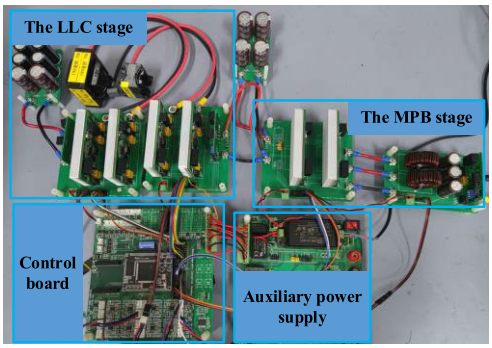

FIGURE 12. Experimental prototype for test.

TABLE 4. Detailed specifications.

Parameters	Symbol	Values
Power rating	P_o	500 W
Input voltage	V_{in}	52 V~260 V
Output voltage	V_o	260 V
Critical intermediate bus voltage	V_{m_min}, V_{m_x}, V_{m_max}	173.3 V, 200 V, 260 V
Critical MPB voltage gain	M_{1_max}	10/3
Critical LLC voltage gain	M_{2_x}, M_{2_max}	1.3, 1.5
Critical MPB duty cycle	D_{max}	0.7
MPB switching frequency	f_{s1}	100 kHz
LLC switching frequency	$f_{s2\_min} \sim f_{s2\_x} \sim f_r$	46 kHz ~ 50 kHz ~ 70 kHz
Equivalent resistors in the MPB stage	$r_{ds(on)\_S11}$, r_L	90 $m\Omega$, 156 $m\Omega$
Equivalent resistors in the LLC stage	$r_{ds(on)\_S1}$, r_{Lr}, r_{pw}, r_{sw}	135 $m\Omega$, 61 $m\Omega$, 250 $m\Omega$, 242 $m\Omega$
MPB inductors	L_1, L_2	160 μH
Resonant components	L_r, C_r, L_m	92.06 μH, 56 nF, 367.23 μH
Devices	Symbol	Model number
MPB MOSFET	S_{11}, S_{12}, S_{21}, S_{22}	C3M0075120J
LLC MOSFET	$S_1 \sim S_4$	C3M0120090J
Controller	/	TMS320F28335

6) MODE 4

When $V_{m\_x}/M_{1\_min} < V_{in} \leq V_{m\_max}/M_{1\_min}$, the control enters Mode 4. Under the circumstances, the MPB stage can be straight through, and only the LLC stage is used to boost the voltage, which can improve efficiency as much as possible. Thus, CD and VF controls are adopted and the duty cycle is set to 0. The frequency variation ranges from f_{s2_x} to f_r.

The proposed control strategy takes full advantage of the soft switching capability of the converter. The critical intermediate bus voltage V_{m_x} is the boundary of the PO mode in the LLC stage. When the input voltage can be boosted above V_{m_x} by the MPB stage, the LLC stage is controlled to be in PO mode all the time to achieve soft switching, such as Mode 2, Mode 3 and Mode 4. This makes full use of the soft switching range of the converter. And the converter operates in soft-switching state at different input voltages, which improves efficiency. Thereby, the soft-switching working area of the converter can be plotted as shown in Fig. 10.

When $V_{m\_min}/M_{1\_max} < V_{in} \leq V_{m\_x}/M_{1\_max}$, the LLC stage is in PN or PON mode, and ZVS can be achieved in some areas. When $V_{in} > V_{m\_x}/M_{1\_max}$, the LLC stage is controlled in PO mode by the proposed control strategy, and ZVS is achieved in all areas.

In practice, the sampling frequency can be set to the highest switching frequency in both stages of the converter. This ensures that the samples are taken once per switching period. Further, the duty cycle and frequency are updated once per switching period. The sampling frequency should not be set to more than two times the switching frequency. Otherwise, the operations of duty cycle and frequency may not be completed within one sampling cycle, which affects the control.

B. OPTIMAL BUS VOLTAGE CONTROL FOR HIGH EFFICIENCY (MODE 3D)

In Mode 3, the first three control approaches are formulated for different control cases of the intermediate bus voltage. However, it is known from (37) that there exists an intermediate bus voltage that makes the two-stage efficiency highest for a certain input voltage. No optimization is made for this in the first three control approaches.

Therefore, the optimal bus voltage control is proposed to improve the two-stage conversion efficiency, i.e., Mode 3d. The corresponding algorithm is shown in Fig. 11. It is unrealistic to find the optimal bus voltage for each input voltage, because the input voltage is not constant but is continuously fluctuating in small increments in practice. And if the intermediate bus voltage changes frequently, the controller obviously does not achieve good real-time performance. Hence, the input voltage range is divided into many intervals. When the actual input voltage falls within the corresponding interval, the average value of the current interval is used as the input voltage to calculate the optimal intermediate bus voltage reference. l_{max} is the number of intervals and l is the current interval code. The lower and upper bounds of the interval can be derived as (42) and (43).

$$V_{in\_low} = \frac{V_{m\_\max}}{M_{1\_\max}} + \frac{l-1}{l_{\max}}\left(\frac{V_{m\_x}}{M_{1\_\min}} - \frac{V_{m\_\max}}{M_{1\_\max}}\right) \quad (42)$$

$$V_{in\_up} = \frac{V_{m\_\max}}{M_{1\_\max}} + \frac{l}{l_{\max}}\left(\frac{V_{m\_x}}{M_{1\_\min}} - \frac{V_{m\_\max}}{M_{1\_\max}}\right) \quad (43)$$

Then, as shown in Fig. 9, the variable voltage (VV) and VF controls are applied to keep the intermediate bus voltage optimal and the output voltage stable.

In the actual design, offline computation is used because the algorithm, especially the iterative algorithm, affects the real-time performance of the controller. Only voltage sensors need to be placed at the input, intermediate bus and output, and no current sensors are required.

V. EXPERIMENTAL VERIFICATION

A 500-W experimental prototype of MPBLLC converter with two-phase Boost is built to verify the proposed loss model and control strategy, as shown in Fig. 12. The detailed specifications are listed in Table 4. The values of components

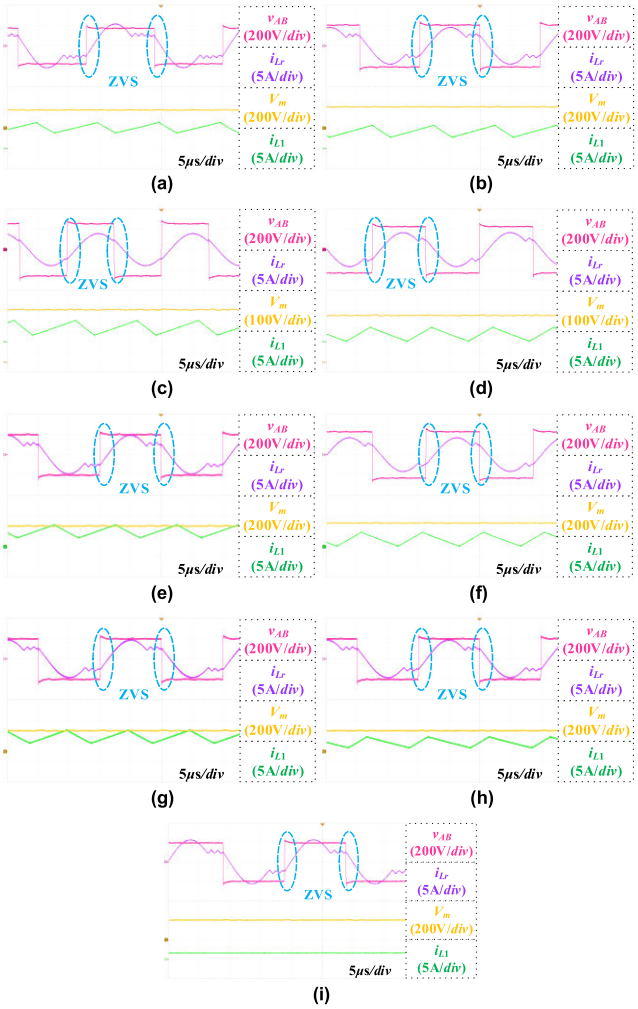

FIGURE 13. Key waveforms for each mode when P_o = 500W. (a) Mode 1. V_{in} = 53V. (b) Mode 2. V_{in} = 63V. (c) Mode 3a. V_{in} = 80V. (d) Mode 3a. V_{in} = 140V. (e) Mode 3b. V_{in} = 80V. (f) Mode 3b. V_{in} = 140V. (g) Mode 3c-200. V_{in} = 80V. V_m = 200V. (h) Mode 3c-200. V_{in} = 140V. V_m = 200V. (i) Mode 4. V_{in} = 202V.

and wires are obtained by actual testing with the precision impedance analyzer, Agilent 4294A.

A. STEADY-STATE AND DYNAMIC EXPERIMENTS

Fig. 13 shows the key experimental waveforms for each mode when P_o = 500W. It can be seen that the soft switching of LLC MOSFETs is realized in all control modes, which will lead to high efficiency. Fig. 13(a) is located in the ZVS area of Mode 1. Fig. 13(b) to Fig. 13(f) show that Mode 2, Mode 3 and Mode 4 all achieve ZVS, which verifies the effectiveness of the proposed control strategy.

In Fig. 13(a), the converter works in Mode 1 when V_{in} = 56V. The duty cycle in the MPB stage is maximum. When the input voltage increases above 60V, the duty cycle remains unchanged and the switching frequency in the LLC stage increases. The intermediate bus voltage is increased above 200V. The converter comes into Mode 2, as shown in Fig. 13(b).

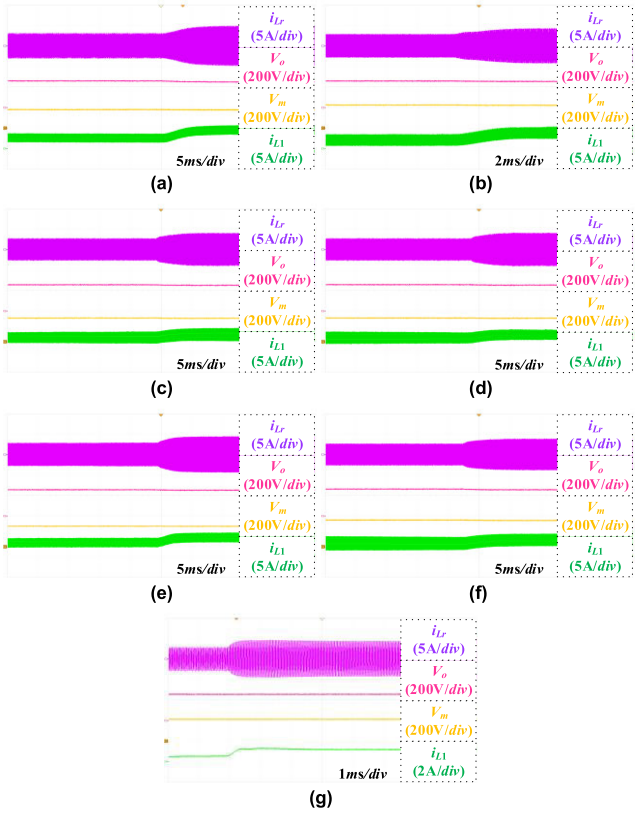

FIGURE 14. Dynamic experimental waveforms for each mode from half load to full load. (a) Mode 1. V_{in} = 54V. (b) Mode 2. V_{in} = 67V. (c) Mode 3a. V_{in} = 140V. (d) Mode 3b. V_{in} = 140V. (e) Mode 3c-200. V_{in} = 140V. V_m = 200V. (f) Mode 3c-260. V_{in} = 140V. V_m = 260V. (g) Mode 4. V_{in} = 212V.

The input voltage continues to increase above 78V and the converter enters Mode 3. In Mode 3a, as the input voltage increases, the intermediate bus voltage decreases, the duty cycle in the MPB stage decreases, and the switching frequency in the LLC stage decreases, as shown in Fig. 13(c) and Fig. 13(d). In Mode 3b, as V_{in} increases, V_m increases, D decreases, and f_{s2} increases, as shown in Fig. 13(e) and Fig. 13(f). In Mode 3c, as V_{in} increases, V_m remains constant, D decreases, and f_{s2} remains the same, as shown in Fig. 13(g) and Fig. 13(h).

When the input voltage increases above 200V, the duty cycle is set to 0. The upper switches in the MPB stage stay on and the lower switches stay off. The switching losses in the MPB stage are eliminated. The converter enters Mode 4, as shown in Fig. 13(i).

Fig. 14 shows the dynamic experimental waveforms for each mode from half load to full load. Fig. 15 shows the dynamic experimental waveforms for each mode from full load to half load. When the load changes, the current output voltage changes. The quality factor of the LLC stage changes with the load and therefore the gain of the LLC stage also changes abruptly. The current intermediate bus voltage changes accordingly. The duty cycle in the MPB stage and the frequency in the LLC stage will be regulated in the proposed control strategy so that the intermediate bus voltage

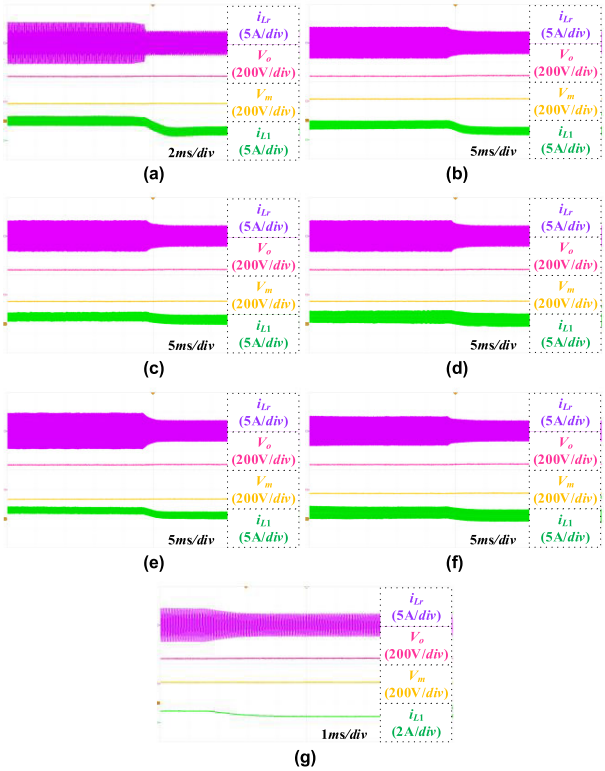

FIGURE 15. Dynamic experimental waveforms for each mode from full load to half load. (a) Mode 1. $V_{in} = 54$V. (b) Mode 2. $V_{in} = 67$V. (c) Mode 3a. $V_{in} = 140$V. (d) Mode 3b. $V_{in} = 140$V. (e) Mode 3c-200. $V_{in} = 140$V. $V_m = 200$V. (f) Mode 3c-260. $V_{in} = 140$V. $V_m = 260$V. (g) Mode 4. $V_{in} = 212$V.

and the output voltage are maintained at the given values. Eventually a new steady state is reached. As seen, whether the load is increased or decreased, the dynamic response time of the converter in all modes is within 5ms. And the voltage and current are changed without large spikes. Therefore, the converter has a good dynamic performance, owing to the proposed control strategy.

B. COMPARISON OF THEORETICALLY MODELED AND EXPERIMENTALLY MEASURED EFFICIENCY

Fig. 16 shows the efficiency curves from the proposed modeling and the measured efficiency curves in Mode 3a. As seen, whether for the MPB stage, the LLC stage or the whole converter, the modeled efficiency is consistent with the experimentally measured efficiency. In Mode 3a, as the input voltage increases, the intermediate bus voltage decreases. According to (24), the efficiency of MPB stage increases. The LLC stage operates away from the resonance point. And with reference to (36), the efficiency of LLC stage decreases. The efficiency of the MPB stage increases more than the efficiency of the LLC stage decreases, so the efficiency trend of the whole converter is close to that of MPB stage.

Fig. 17 shows the efficiency curves from the proposed modeling and the measured efficiency curves in Mode 3b. Again, it is observed that the modeled efficiency is identical to the experimentally measured efficiency in Mode 3b. In this

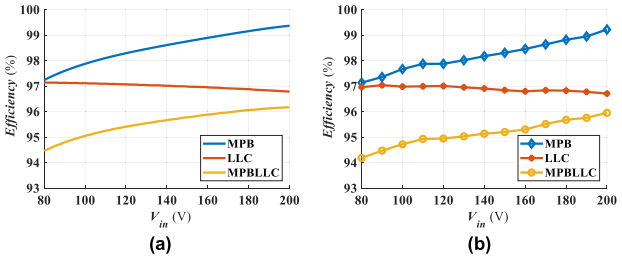

FIGURE 16. Efficiency curves in Mode 3a. (a) Efficiency from the proposed modeling. (b) Experimentally measured efficiency.

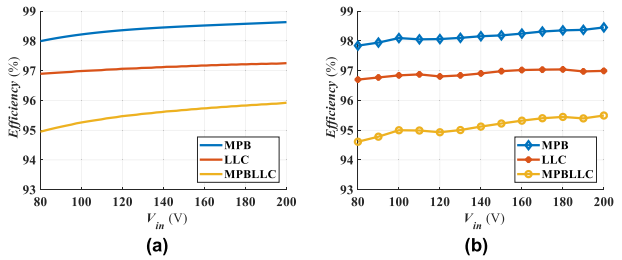

FIGURE 17. Efficiency curves in Mode 3b. (a) Efficiency from the proposed modeling. (b) Experimentally measured efficiency.

mode, as the input voltage increases, the intermediate bus voltage increases. The duty cycle of MPB stage decreases. according to (19) and (23), the efficiency of MPB stage increases. The LLC stage operates closer to the resonance point. And with reference to (36), the efficiency of LLC stage increases. The efficiency of both the MPB stage and the LLC stage increases, so the efficiency of the whole converter increases.

Fig. 18 shows the efficiency curves from the proposed modeling and the measured efficiency curves for different V_m in Mode 3c. As seen, the modeled efficiency is in line with the experimentally measured efficiency for different V_m in Mode 3c. In this mode, the intermediate bus voltage remains constant. According to (24), as the input voltage increases, the efficiency of MPB stage increases. Since the operation of LLC stage does not change, the efficiency of LLC stage hardly changes. Eventually, the efficiency of the whole converter increases following the efficiency of the MPB stage. In these three cases of intermediate bus voltage, the converter has the highest efficiency when $V_m = 200$V. Therefore, only Mode 3c-200 (Mode 3c when $V_m = 200$V) will be compared with other modes next.

Fig. 19 shows the loss distribution of the converter at full load when $V_{in} = 140$V and $V_m = 200$V. It can be seen that the largest share is the conduction losses of the LLC stage, which include the conduction losses of the switching devices, the resonant inductor and the transformer. This is due to the deviation of the switching frequency from the resonant frequency and the high circulating current. The switching and conduction losses of the MPB stage also account for a large portion of the total losses. The switching losses of the LLC stage are less due to the implementation of ZVS. The core losses in the transformer and the inductor account for the least of the total losses.

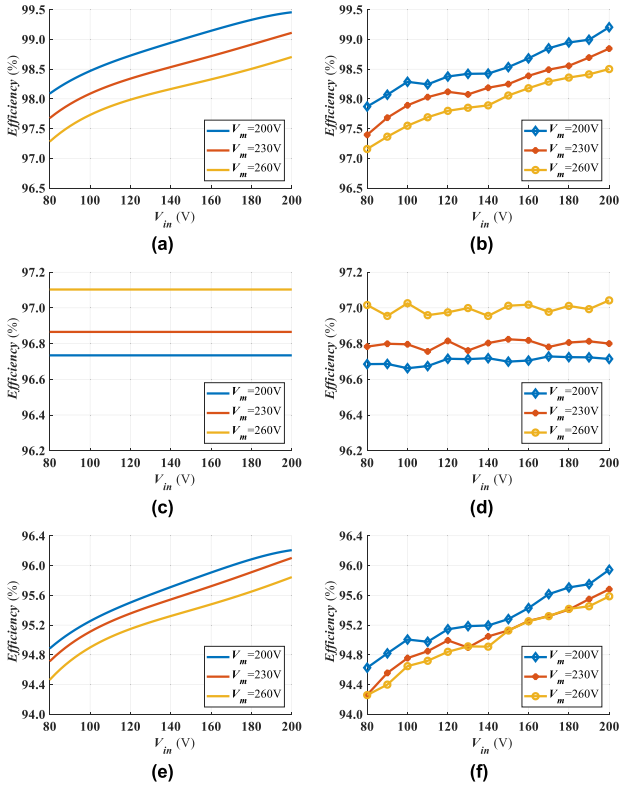

FIGURE 18. Efficiency curves in Mode 3c when V_m is 200V, 230V and 260V respectively. (a) Modeled efficiency of MPB. (b) Measured efficiency of MPB. (c) Modeled efficiency of LLC. (d) Measured efficiency of LLC. (e) Modeled efficiency of MPBLLC. (f) Measured efficiency of MPBLLC.

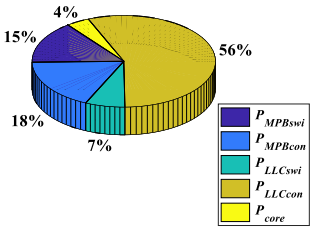

FIGURE 19. Loss distribution of MPBLLC converter at full load when V_{in} = 140V and V_m = 200V.

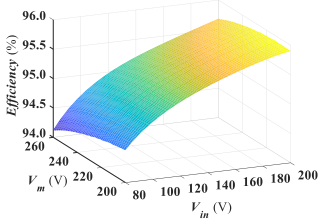

FIGURE 20. Efficiency surface of MPBLLC converter based on the proposed model.

Fig. 20 shows the efficiency surface of MPBLLC converter based on the proposed model. It can be seen that the efficiency generally increases as the input voltage increases and the intermediate bus voltage decreases. However, when the input voltage approaches 200V and the intermediate bus voltage

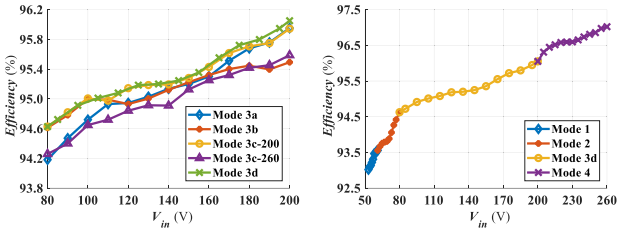

FIGURE 21. Measured efficiency of MPBLLC converter. (a) Efficiency comparison in Mode 3. (b) Overall efficiency.

also approaches 200V, the efficiency decreases somewhat. The highest efficiency is in the upper part of the surface and is not located at the edges. Therefore, when the input voltage is high, the intermediate bus voltage should not be reduced but should be increased appropriately to improve efficiency. It is achieved by the optimal bus voltage control proposed in this paper, where the most appropriate V_m is selected for different operating conditions or input voltages, aimed at high efficiency. And the control is verified by the efficiency comparison in Fig. 21(a). As seen, the efficiency of Mode 3d with the proposed optimal bus voltage control is the highest in Mode 3. When the input voltage is close to 200V, the advantage of efficiency improvement is obvious. Besides, the proposed control method significantly improves the efficiency of the converter compared to the conventional method (Mode 3c-260). Fig. 21(b) shows the overall efficiency of MPBLLC converter. As seen, the two-stage MPBLLC converter has good efficiency performance over a wide input voltage range and achieves a peak efficiency of 97%.

VI. CONCLUSION

In this paper, a loss modeling method for the variable bus voltage and the corresponding fast algorithm are proposed. Based on them, a control strategy including the optimal bus voltage control is proposed for MPBLLC converter. The control strategy achieves a wide voltage range of the converter while taking into account high efficiency. In the key part of the control strategy, four different control approaches are proposed and analyzed. The first 3 approaches (Mode 3a, Mode 3b, Mode 3c) are essentially different controls based on different variations of the intermediate bus voltage. The fourth approach (Mode 3d) is based on the proposed variable bus loss model to control the intermediate bus voltage so that the efficiency of two-stage converter is maximized, i.e., optimal bus voltage control. Finally, the experimental prototype verified the effectiveness of the proposed loss model and control strategy. The experimental results show that the prototype with the proposed control strategy has good steady-state and dynamic performance, wide input voltage range and high efficiency.

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