

Received 10 November 2023, accepted 29 November 2023, date of publication 7 December 2023, date of current version 20 December 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3340703

EXPOSITION

Re-Examination of DFIG-Based Wind Park Small-Signal Instability

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This work was supported by the Hong Kong Research Grant Council for the Research Project under Grant 25223118.

ABSTRACT Doubly-fed induction generator-based wind park (DFIG-WP) can interact with both series-capacitor compensated and weak (low short circuit ratio) grids, thus causing instability, and called as series-capacitor sub-synchronous oscillation (SSO) and weak grid SSO, respectively. However, the frequency spectra of phase voltage/current signatures of those two SSOs are significantly different. There is one dominant resonance frequency in series-capacitor SSO, but there are two frequencies (resonance and corresponding mirror frequencies) in weak grid SSO in addition to the fundamental frequency. To address this issue, this paper deeply analyzes the DFIG-WP instability mechanisms through impedance-based stability assessment (IBSA). Both the IBSA and electromagnetic transient (EMT) validation simulations demonstrated that the resonance takes place in the sub-synchronous range in a series-capacitor compensated grid and is mainly affected by the rotor-side converter (RSC) control parameters. However, the weak grid instability is found in the super-synchronous range with its mirror frequency in the sub-synchronous range and is affected by both the RSC and grid-side converter (GSC) control parameters. Therefore, the classification of weak grid SSO needs revision. The utilized DFIG impedance model in IBSA accounts for the DC coupling between RSC and GSC (AC-DC coupling phenomenon). The contribution of this coupling on DFIG impedance and its impact on DFIG-WP instability are demonstrated. In the considered test system, the AC-DC coupling provides a considerable amount of positive resistance in both resonance conditions. Hence, its omission may lead to pessimistic IBSA results. This paper also provides recommendations for instability prevention and/or mitigation through DFIG control parameter modification based on the guidance of the stability contour analysis.

INDEX TERMS DFIG, series-capacitor SSO, impedance-based stability analysis, weak grid instability.

ABBREVIATIONS

C1, C2	Case-1, 2.
D1, D2, D3	Disturbance-1, 2, 3.
DFIG	Doubly-fed induction generators.
DFIG-WP	DFIG-based wind park.
EMT	Electro-magnetic transient.
FSC-WP	Full size converter-based wind park.
GSC, GSS	Grid-side converter, Grid-side system.
IBSA	Impedance-based stability assessment.
MIMO	Multi-input multi-Output.

PCC, PoI	Point of common coupling, Interconnection.
PLL	Phase-locked loop.
RSC, RSS	Rotor-side converter, Rotor-side system.
SDC	Supplementary damping controller.
SISO	Single-input single-output.
SSCI	Sub-synchronous control interaction.
SSO	Sub-synchronous oscillation.
WT	Wind turbine.

I. INTRODUCTION

Doubly-fed induction generator (DFIG) based wind park (DFIG-WP) is of great importance to wind energy exploitation, especially for onshore applications [1]. However, DFIG-WPs can adversely interact with the series-capacitor

The associate editor coordinating the review of this manuscript and approving it for publication was Derek Abbott¹.

compensated or weak (low short circuit ratio) grids at sub-synchronous frequency range [2]. This phenomenon is called sub-synchronous oscillation (SSO) and has been confirmed with several real-world incidents [3].

The interaction between DFIG-WP and the series-capacitor compensated grid is called series-capacitor SSO, which occurred in Minnesota, Texas of USA, and North China [3]. The frequency spectrum of three-phase instantaneous currents shows a dominant resonance frequency in the sub-synchronous range in all series-capacitor SSO events [3]. The series-capacitor SSO is caused by the negative resistance brought by the induction generator effect [4] and can be worsened by the converter controllers of DFIG (sub-synchronous control interaction, SSCI) [5]. An equivalent circuit considering the induction generator and rotor-side converter (RSC) of the DFIG for series-capacitor SSO analysis is derived in [6]. The impacts of induction generator effect and SSCI are represented by a negative resistance and a frequency-dependent impedance with detailed analytical equations, respectively [6]. Low wind speed and high compensation level can exacerbate the instability, and a supplementary damping controller (SDC) may be needed to ensure the safe operation of the DFIG-WP under the risky operating conditions [7].

Although DFIG usually engages in series-capacitor SSO, some researchers already demonstrated the potential instability risk of weakly-tied DFIG-WP and proposed an adaptive grid-side converter (GSC) controller that has a parameter tuning strategy based on measured grid impedance [8], [9]. The negative impact of fast response PLL on DFIG-WP weak grid instability [10] is eliminated with a modified PLL structure in [11]. A quasi-resonant supplementary damping controller is proposed in [12] for weak grid instability mitigation in DFIG-WP. The adaptiveness of the controller in [12] is then improved by the resonance frequency identification algorithm [13]. In 2018, an interaction event between DFIG-WP and a weak grid happened in Northwest China, where the frequency spectrum contains 37 Hz and 63 Hz components [14], [15].

The frequency spectrum signatures of DFIG-WP phase currents are significantly different in series-capacitor and weak grid SSO. However, there is similarity between frequency spectrum signatures of DFIG-WP and full-size converter based wind park (FSC-WP) phase currents under weak grid conditions. When a weak grid instability occurs in an FSC-WP, the frequency spectrum of three-phase instantaneous currents contains not only the resonance frequency (f_r), but also its mirror frequency ($f_m = 2f_b - f_r$), in addition to the fundamental frequency (f_b). This is called mirror frequency effect [16]. The difference in frequency spectrum signatures of DFIG-WP phase currents in weak grid and series-capacitor SSO events was emphasized in both IEEE Task Force report and paper ([1] and [3], respectively). In [1] and [3], researchers were also encouraged to make further investigation on DFIG-WP instability mechanisms.

Impedance-based stability assessment (IBSA) is a commonly used method to analyze instability issues caused by inverter-based resources [17]. The analytical impedance model of DFIG has evolved over the years due to better precision requirements in IBSA. The early stage DFIG impedance model consists of only the series connection of induction generator (IG) and rotor-side converter (RSC) and ignores the grid-side converter (GSC) and its filter, as total impedance of IG and RSC is dominant in sub-synchronous range [18]. Then the DFIG impedance is represented by parallel connection of the rotor-side subsystem (RSS) that consists of IG and RSC impedances, and the grid-side subsystem (GSS) that consists of GSC and its output filter impedances. This type of impedance model is more accurate and widely used [19], [20]. However, it ignores the AC-DC coupling phenomenon i.e., the DC-side coupling between RSS and GSS. The most advanced DFIG impedance model in [15] and [21] accounts for the DC-side coupling and provides ultimate accuracy [22]. Hence, it is utilized in this paper to illustrate the impact of the AC-DC coupling phenomenon on DFIG instability.

As a response to the deep think question raised by the IEEE Task Force report and paper [1], [3], this paper aims to study the instability risks on a typical DFIG-WP test system with the most accurate analytical DFIG impedance model. The main contributions of this paper are:

- 1) The impacts of RSS, GSS and AC-DC coupling phenomenon on DFIG impedance characteristics are investigated for sub- and super-synchronous frequency ranges.
- 2) The instability risks and mechanisms of DFIG-WP in weak and series-capacitor compensated grids are re-examined. It illustrated that the series-capacitor SSO is in the sub-synchronous frequency range, whereas the weak grid instability is in the super-synchronous range. Hence, the classification of weak grid instability should be revised.
- 3) The impacts of RSS and GSS controllers on DFIG-WP stability in two grid conditions are re-examined. Recommendations are presented for instability prevention and/or mitigation through DFIG control parameter modification based on the guidance of the stability contour analysis.

The rest of this paper is as follows. Section II introduces the test system and the IBSA model. The DFIG-WP instability mechanisms and the DFIG control parameter impact are analyzed in section III and IV, respectively. Section V presents the electro-magnetic transient (EMT) validation simulations and provides recommendations for the safe operation of DFIG-WP through control parameter modification. Section VI concludes the paper.

II. TEST SYSTEM AND IBSA MODEL

A. DFIG WIND TURBINES AND CONTROL

The DFIG circuit and control diagrams are shown in Fig. 1, and the parameters are given in Table 1 of the Appendix B.

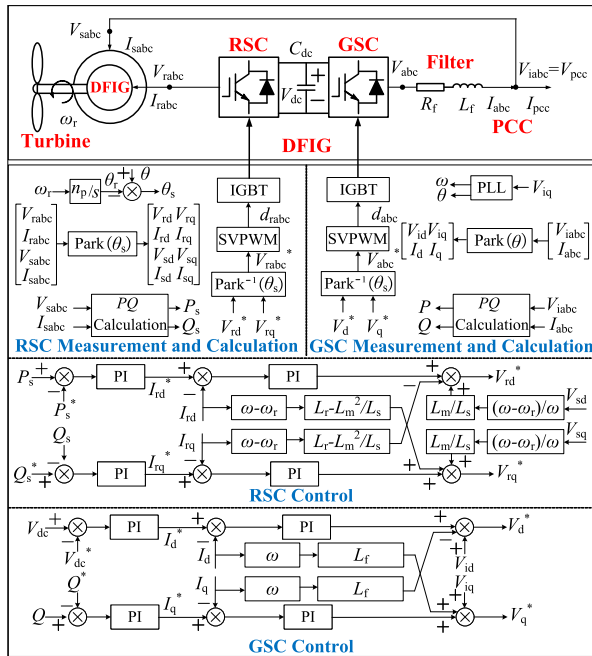


FIGURE 1. The circuit and control diagrams of the DFIG.

The RSC uses stator voltage orientation. The active power is controlled at d-axis outer loop (P control), and the reactive power is controlled at q-axis outer loop (Q control). The GSC uses grid voltage orientation. The DC voltage is controlled at d-axis outer loop (V_{DC} control), and the reactive power is controlled at q-axis outer loop (Q control). Current vector control is used by the inner loops of both RSC and GSC. The PLL tracks the voltage angle of the point of common coupling (PCC) and then provides the angle for the Park transformation and its inverse to realize the integration. For detailed modelling of DFIG, readers may refer to [1].

The DFIG control parameters are designed as follows. The RSC controller is designed considering only the IG parameters, which are stator resistance (R_s), stator leakage inductance (L_{ls}), rotor resistance (R_r), rotor leakage inductance (L_{lr}) and magnetizing inductance (L_m). The GSC controller is designed considering the equivalent impedance seen from the converter terminal of the aggregated DFIG [23]. Accounting external grid in GSC controller design ensures stable operation when it is connected to a weak grid [8], [9]. Further details can be found in [24]. The PI regulator parameters of the inner and outer controls (seen in Table 1 of the Appendix B) are similar to the ones in [25], which successfully imitated the actual transient behavior of a DFIG-WP.

B. INSTABILITY RISKS IN THE STUDIED TEST SYSTEM

The equivalent circuit of the test system is shown in Fig. 2 and the parameters are listed in Table 2 of Appendix B. The system simulation model contains an aggregated WT model, RL equivalent circuits of WT, and WP transformers referred to low-voltage side (i.e., the WT side). The DFIG converters

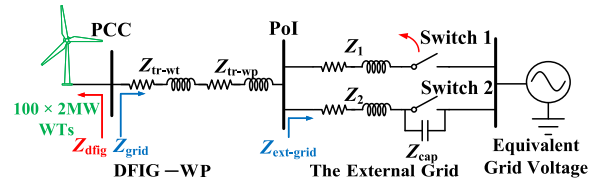


FIGURE 2. Circuit diagram of the system under study.

are represented with their average value models [26]. On the other side of the Point of Interconnection (PoI), the external grid is represented with parallel RLC circuits behind a voltage source referred to low-voltage side. Opening Switch 1 results in a weak grid condition when Switch 2 is closed. Opening Switch 2 results in radial connection of WP to a series capacitor compensated grid (with a 30 % effective compensation level) when Switch 1 is opened.

C. IMPEDANCE MODELLING AND VALIDATION

The dq multi-input multi-output (MIMO) impedance model of DFIG (Z_{dfig_dq}) includes the AC admittance of the RSS, AC admittance of the GSS and AC-DC coupling admittance [22], (see the block diagram in Fig. 3). The equation of Z_{dfig_dq} is:

$$Z_{dfig_dq} = [Y_{RSS_dq} + Y_{GSS_dq} + Y_{ACDC_dq}]^{-1} \quad (1)$$

where bold variables represent impedance matrices. The Y_{RSS_dq} , Y_{GSS_dq} and Y_{ACDC_dq} are:

$$Y_{RSS_dq} = Y_{12dq} \quad (2)$$

$$Y_{GSS_dq} = Y_{4dq} \quad (3)$$

$$Y_{ACDC_dq} = Y_a Y_b Y_{dc} + Y_c Y_d Y_{dc} + (Y_a Y_c + Y_b Y_b) Y_{dc} \quad (4)$$

where the DC-side admittance Y_{dc} is:

$$Y_{dc} = \frac{1}{sC_{dc} + Y_{2dc} + Y_{4dc}} \quad (5)$$

The $Y_a Y_b Y_{dc}$ term, $Y_c Y_d Y_{dc}$ term, and $(Y_a Y_c + Y_b Y_b) Y_{dc}$ term represent the DC-side admittance Y_{dc} coupled at AC-side through RSS, GSS, and RSS-GSS interaction channels, respectively. The three types of interactions are marked with red arrows in Fig. 3. The detailed matrices are given in the Appendix A, and not derived here. Readers can refer to [22] for further details.

Then the dq MIMO DFIG impedance model is transformed into the single-input single-output (SISO) sequence impedance model Z_{dfig_p} . This process includes a linear transformation and a model simplification. A linear transformation is applied to dq domain MIMO impedances Z_{dfig_dq} to obtain the modified sequence MIMO impedance Z_{dfig_pn} [16]:

$$Z_{dfig_pn} = \frac{1}{2} \begin{bmatrix} 1 & j \\ 1 & -j \end{bmatrix} Z_{dfig_dq} \begin{bmatrix} 1 & 1 \\ -j & j \end{bmatrix} \quad (6)$$

Then the model simplification is applied to modified sequence MIMO impedances to obtain the positive and

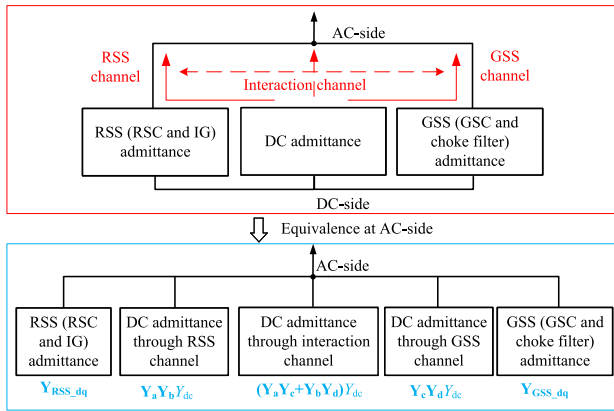


FIGURE 3. Block diagram explanation of AC-DC coupling phenomenon.

negative sequence SISO impedances (Z_{dfig_p} and Z_{dfig_n} , respectively) [16]:

$$\begin{aligned} Z_{dfig_p}(s) &= \frac{\det[\mathbf{Z}_{dfig_pn}(s - j\omega_b)]}{Z_{nn}(s - j\omega_b)} \\ Z_{dfig_n}(s) &= \frac{\det[\mathbf{Z}_{dfig_pn}(s + j\omega_b)]}{Z_{pp}(s + j\omega_b)} \end{aligned} \quad (7)$$

Validation of the analytical DFIG SISO sequence impedance model is done by comparing it with the EMT-level frequency scanning simulations as shown in Fig. 4. In this figure, the letters ‘‘p’’ and ‘‘n’’ denote the positive and negative sequence quantities, respectively.

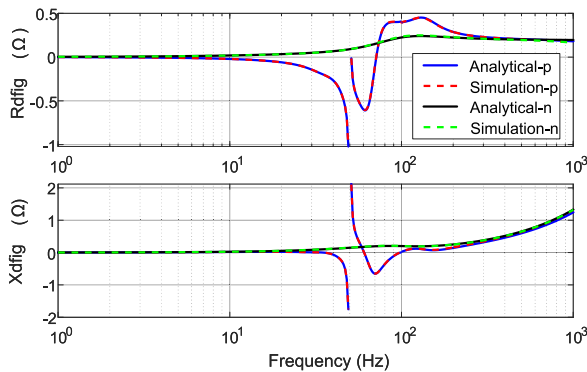


FIGURE 4. Validation of the analytical DFIG impedance model.

The grid impedance Z_{grid} includes the impedance of WT transformer, WP transformer and external grid (Z_{tr_wt} , Z_{tr_wp} , Z_{ext_grid} , respectively). The external grid impedance is represented by Z_2 when the weak grid instability is analyzed, and by $Z_2 + Z_{cap}$ when the series capacitor SSO is analyzed. It is worth noting that Z_2 includes line impedance Z_{line} and equivalent grid impedance Z_{eq_grid} (the Thevenin equivalent impedance series connected to the grid voltage). Therefore, the positive sequence SISO impedance model of the

grid is:

$$\begin{aligned} Z_{grid} &= Z_{tr_wt} + Z_{tr_wp} + Z_{ext_grid} \\ &= (R_{tr_wt} + R_{tr_wp} + R_2) \\ &\quad + s(L_{tr_wt} + L_{tr_wp} + L_2) + \frac{1}{sC_{cap}} \end{aligned} \quad (8)$$

III. DFIG-WP INSTABILITY MECHANISMS

A. IBSA METHOD

IBSA is conducted in both R-X and Bode diagrams. The R-X diagrams are used to explain the instability mechanism. The Bode diagram analysis results are used to provide the system resonance frequencies and phase margins. The Bode diagram is omitted for concise demonstration.

In the R-X diagram, instability occurs when the product of resistance and derivative of reactance is negative at reactance cross-over frequency f_0 [27]:

$$\left(R_{sys} \cdot \frac{dX_{sys}}{df} \right) \Big|_{f_0} < 0 \quad (9)$$

where

$$\begin{aligned} Z_{sysf} &= R_{sys}(f) + jX_{sys}(f) \\ &= R_{dfig}(f) + R_{grid}(f) + j[X_{dfig}(f) + X_{grid}(f)] \end{aligned} \quad (10)$$

In the Bode diagram, instability occurs when the absolute value of the phase difference is larger than 180° at the intersection frequency f_d of the DFIG and grid impedance magnitude curves [17]:

$$|Z_{dfig}(f_d)| = |Z_{grid}(f_d)| \quad (11)$$

$$|\angle Z_{dfig}(f_d) - \angle Z_{grid}(f_d)| > 180 \quad (12)$$

B. IMPEDANCE RESPONSE OF THE DFIG

The AC impedance responses of the DFIG, RSS and GSS in 1 - 100Hz are shown in Fig. 5 The DFIG impedance characteristics vary in different frequency ranges. Those frequency ranges may change under different parameter conditions, and this paper only shows the general trend.

In 1 - 35 Hz, DFIG impedance is inductive with negative resistance, which can interact with series-capacitor compensated grid and leads to series-capacitor SSO. In 35 - 50 Hz and 50 - 60 Hz (near fundamental frequency), DFIG becomes capacitive and inductive with negative resistances, respectively. Although the capacitive DFIG in 35 - 50 Hz can interact with an inductive AC grid, this scenario will be verified stable in section III-C. The DFIG impedance is capacitive with a negative resistance in 60 - 76 Hz and positive resistance in 76 - 100 Hz. DFIG can interact with an inductive AC grid in the super-synchronous range, which is the cause of the weak grid instability. Moreover, the negative resistance range may expand to 76 - 100 Hz and even above 100 Hz under certain parameter conditions.

C. IMPACT OF RSS AND GSS IMPEDANCES

The DFIG impedance consists of the RSS impedance, the GSS impedance and the AC-DC coupling impedance

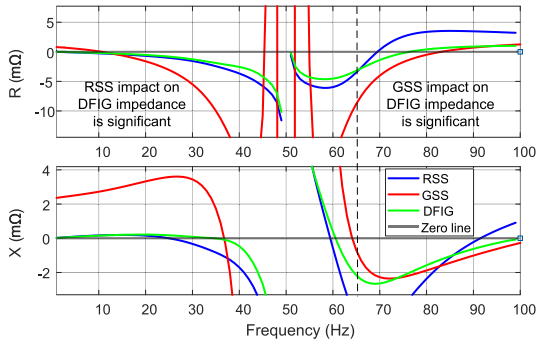


FIGURE 5. Impedance responses of the DFIG, RSS, and GSS.

reflected at AC-side. The impact of RSS and GSS impedances on the DFIG impedance is analyzed in Fig. 5. In the sub-synchronous range, the green curve is close to the blue curve, which means that the contribution of RSS impedance to the DFIG impedance is significant. The contribution of GSS is negligible. Hence, the impact of RSS on DFIG impedance is dominant in the sub-synchronous frequency range. However, the impact of GSS on series-capacitor SSO is limited and explains the findings in previous research such as [28] and [29]. Tuning RSC control parameters [28], [29] and implementing SDCs [30], [31] are effective ways for mitigation.

In the super-synchronous frequency range, the green curve is close to the blue curve in 50 - 65 Hz, but closer to the red curve in 65 - 100 Hz. Hence, the DFIG impedance in the super-synchronous range is influenced by both RSS and GSS impedances. However, the contribution of GSS becomes larger as the frequency increases. Ref. [8] and [9] proposed tuning the GSC inner current loop PI parameters considering the external grid impedance to mitigate the weak grid instability of DFIG-WP. Modifying RSC control parameters can also be effective considering the impact of RSS on DFIG impedance in the super-synchronous range.

D. IMPACT OF AC-DC COUPLING PHENOMENON

The majority of previous research based on simplified DFIG impedance model did not consider the AC-DC coupling phenomenon [17], [18], [19], [20]. Besides, the impact of this phenomenon on DFIG impedance model was not clearly presented in detail in the recent research [14], [21], [22] that use the most advanced DFIG impedance model. Hence, the impact of AC-DC coupling on the DFIG impedance characteristics and the IBSA accuracy is analyzed in depth using the R-X diagram. The impedance response of the AC-DC coupling admittance Y_{ACDC_dq} reflected at AC-side is shown in Fig. 6. It is worth noting that the curve is the positive sequence impedance difference ΔZ transformed from the dq-MIMO impedance difference ΔZ_{dq} between the most advanced and the simplified model. The equation of ΔZ_{dfig_dq} is given as:

$$\Delta Z_{dq} = Z_{dfig_dq} - [Y_{RSS_dq} + Y_{GSS_dq}]^{-1} \neq Y_{ACDC_dq}^{-1} \tag{13}$$

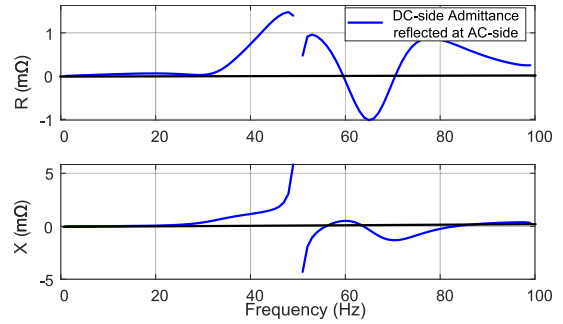


FIGURE 6. Impedance response of the AC-DC coupling admittance reflected at AC-side.

It can be seen in Fig. 6 that the AC-DC coupling provides positive resistance in the sub-synchronous range, and 50 - 60 Hz and 70 - 100 Hz in the super-synchronous range. Hence, the IBSA without considering the AC-DC coupling will give pessimistic results by predicting a stable system as unstable. It well explains the errors found in [22] due to the usage of the simplified DFIG impedance model, as a part of positive resistance is overlooked. It is also worth noting that if the resonance takes place in 60 - 70 Hz (can happen when the grid impedance increases to impractical values larger than 0.6 pu, see section III-C), the AC-DC coupling may provide negative resistance that worsens system stability.

E. DFIG-WP WEAK GRID INSTABILITY MECHANISMS

The IBSA of DFIG-WP in weak grid is shown in Fig. 7. As Z_{ext_grid} increases, the reactance cross-over frequency decreases in super-synchronous range. The resistance also decreases gradually and becomes minus when $Z_{ext_grid} = 0.6$ pu, hence the system becomes unstable at 72 Hz (for example the instability in [15] could be at 63 Hz). The magnitude of DFIG negative resistance at this frequency (see Fig. 5) is larger than the grid resistance, which leads to the negative system resistance and the instability. Although there are two other reactance cross-over frequencies (in 40 - 50 Hz and 60 - 70 Hz ranges, respectively), the product of resistance and derivative of reactance is positive in both cross-over frequencies and the system is stable. The SSO classification of weak grid instability fails in the considered system. On the other hand, the study in [8] and [9] also confirmed effective that tuning GSC control parameters considering the external grid equivalent impedance provides desired stability for DFIG under weak grid condition.

F. DFIG-WP SERIES-CAPACITOR SSO MECHANISMS

The IBSA of DFIG-WP in series-capacitor compensated grid is shown in Fig. 8. As the compensation level increases, the reactance cross-over frequency increases in sub-synchronous range. The resistance also decreases and becomes minus when the compensation level is above 30%, hence the system becomes unstable at 18 Hz, 24 Hz and 30 Hz, respectively. Similarly, the other three reactance cross-over frequencies

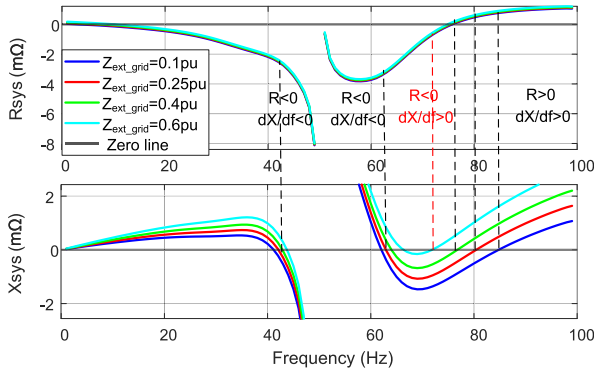


FIGURE 7. Impedance responses of the system for various SCRs.

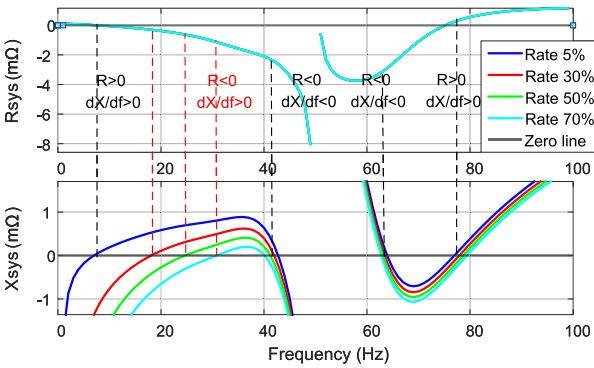


FIGURE 8. Impedance responses of the system for various compensation levels.

(in 40 - 50 Hz, 60 - 70 Hz and 70 - 80 Hz, respectively) will not lead to instability because of the positive products. The SSO classification of series-capacitor instability is validated in the considered system.

IV. IMPACT OF CONTROL PARAMETERS ON DFIG-WP INSTABILITY

A. IMPACTS OF RSC PI REGULATOR

The impact of RSC current PI regulator bandwidth on the DFIG-WP instability is shown in Fig. 9. With the increase of RSC current PI regulator bandwidth, the negative ranges of both the X_{dfig} and the R_{dfig} curves become wider in the super-synchronous range. The cyan line of the X_{dfig} is below zero in 60 - 100 Hz while the blue line is below zero only in 57 - 69 Hz. The cyan line of the R_{dfig} curve is below the zero line in 50 - 76 Hz while the blue line is below zero only in 50 - 61 Hz. Hence, the DFIG impedance has a larger magnitude of negative reactance value (i.e., more capacitive) and a more negative resistance value in the super-synchronous range. As the DFIG interacts with the inductive weak grid in the super-synchronous range, the above changes in reactance and resistance worsen the stability.

In the sub-synchronous range, the X_{dfig} curve slightly shifts downward, and the R_{dfig} curve shifts downward significantly. It can be seen from the cyan line below the blue line in both X_{dfig} and R_{dfig} curves. Hence, the DFIG impedance has a

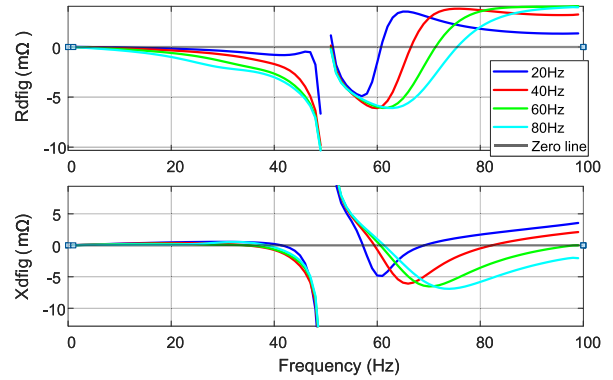


FIGURE 9. Impact of RSC current PI regulator on the impedance response of DFIG.

slightly larger magnitude of negative reactance value and a more negative resistance value. As the DFIG interacts with the capacitive series capacitor compensated grid in the sub-synchronous range, a more negative resistance worsens the stability, and the impact of slight change in reactance can be neglected. To conclude, fast RSC current control worsens stability in both grid conditions.

The impact of RSC PQ PI regulator on the impedance response of the DFIG can be analyzed in the same way, which shows similarity to the impact of current PI regulator but less significant as shown in Fig. 10. Hence, fast RSC PQ control also worsens stability.

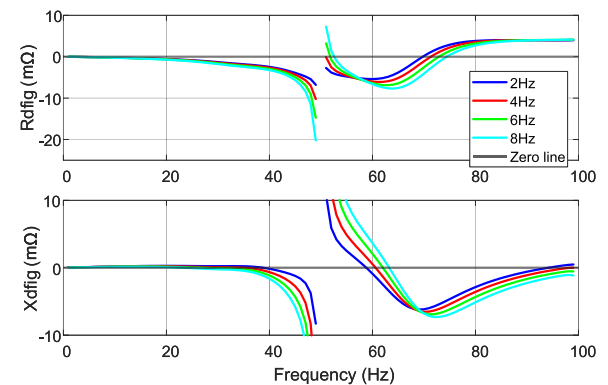


FIGURE 10. Impact of RSC PQ PI regulator on the impedance response of DFIG.

B. IMPACTS OF GSC PI REGULATOR

With the increase of GSC current PI regulator bandwidth, DFIG impedance becomes more capacitive, and the resistance increases in the risky frequency range (70 - 100 Hz, indicated in section III), as shown in Fig. 11. Hence, fast current control improves stability in weak grid. When the PLL PI regulator bandwidth increases, the DFIG impedance becomes more inductive, but the resistance decreases significantly in the risky super-synchronous range, as shown in Fig. 12. Therefore, fast PLL control worsens stability in weak grid. The impact of DC voltage PI regulator is similar to the current

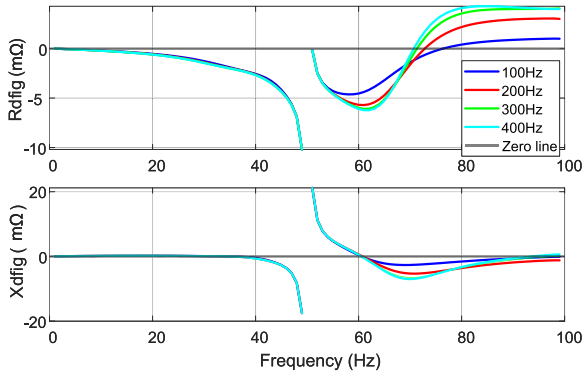


FIGURE 11. Impact of GSC current PI regulator on the impedance response of DFIG.

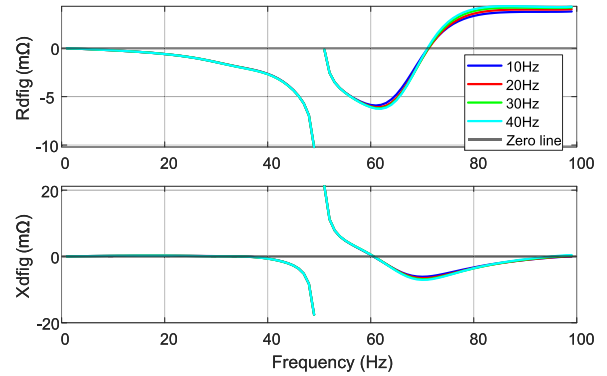


FIGURE 14. Impact of GSC DC Voltage PI regulator on the impedance response of DFIG.

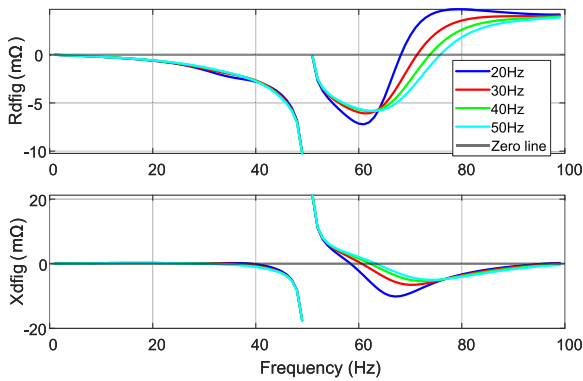


FIGURE 12. Impact of GSC PLL PI regulator on the impedance response of DFIG.

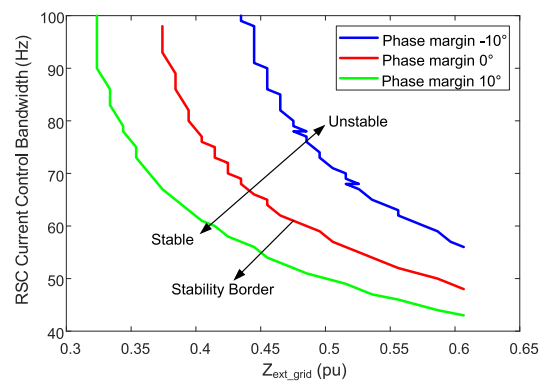


FIGURE 15. Stability contour diagram of varying RSC current PI regulator bandwidths and SCRs.

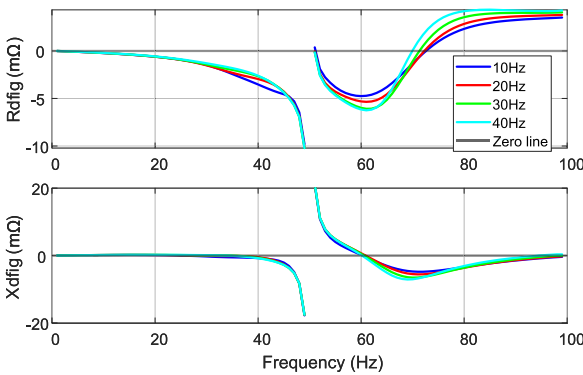


FIGURE 13. Impact of GSC DC Voltage PI regulator on the impedance response of DFIG.

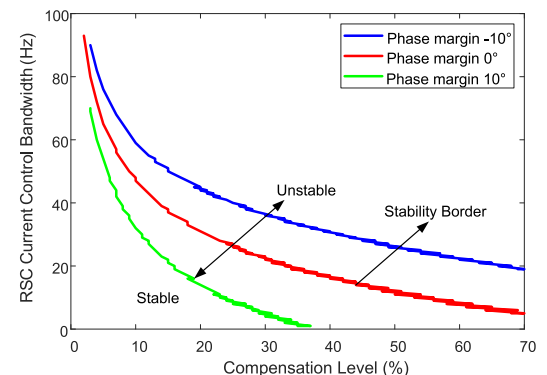


FIGURE 16. Stability contour diagram of varying RSC current PI regulator bandwidths and effective compensation levels.

PI regulator, but less significant, as shown in Fig. 13. The impact of reactive PI regulator can be neglected, as shown in Fig. 14.

C. STABILITY CONTOUR ANALYSIS

As the RSC current control bandwidth has significant impact on both series capacitor SSO and weak grid instability, the stability contours of 10°, 0° and -10° phase margins are drawn to guide the parameter selection with different external grid conditions (SCRs and effective compensation

levels may vary based on different system loading conditions and line outages, etc.), as shown in Fig. 15 and Fig. 16, respectively. The RSC current control bandwidth needs to be set lower as the external grid impedance increases and effective compensation level increases, which corresponds to the analysis of Fig. 9. In order to obtain a 10° phase margin under weak grid conditions ($Z_{ext-grid}$ no more than 0.6 pu in this paper), the RSC current control bandwidth should be set below 42 Hz to ensure safe operation. However, in the series compensated test system, 10° phase margin not only

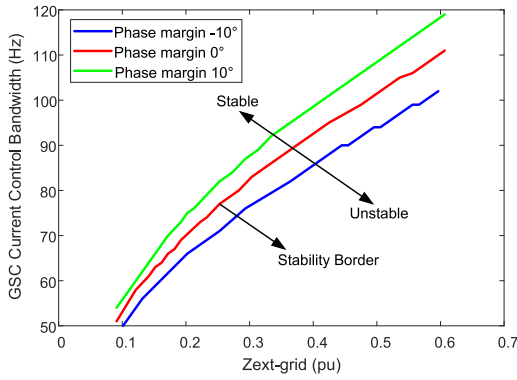


FIGURE 17. Stability contour diagram of varying GSC current PI regulator bandwidths and SCRs.

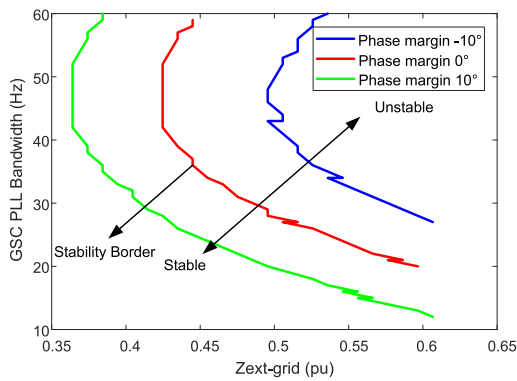


FIGURE 18. Stability contour diagram of varying GSC PLL PI regulator bandwidths and SCRs.

requires lower RSC current control bandwidth, but also the effective compensation level cannot be higher than 38%. It is worth noting that Z_2 consists of both the line and equivalent grid impedances (Z_{line} and Z_{eqgrid} , respectively). The effective compensation level (X_{cap}/X_2) is presented in Fig.16 and is well below the line compensation level (X_{cap}/X_{line}). The results might change based on different system structures, parameters and DFIG operating conditions.

As the GSC current control and PLL PI regulator bandwidths have significant impacts on weak grid instability, the stability contours of 10° , 0° and -10° phase margins are drawn to guide the parameter selection with different external grid conditions (varying SCRs), as shown in Fig. 17 and Fig. 18, respectively. The GSC current control bandwidth needs to be set higher and the PLL bandwidth needs to be set lower, as the external grid impedance increases, which corresponds to the analysis of Fig. 11 and Fig. 12, respectively. For a 10° phase margin under weak grid conditions, the GSC current control bandwidth should be higher than 120 Hz, and the PLL PI regulator bandwidth should be slower than 12 Hz. However, it may be too slow for the PLL performance of tracking grid voltage. Hence, the PLL PI regulator bandwidth can be adjusted 10 or 20 Hz higher, and the negative influence can be offset by slower

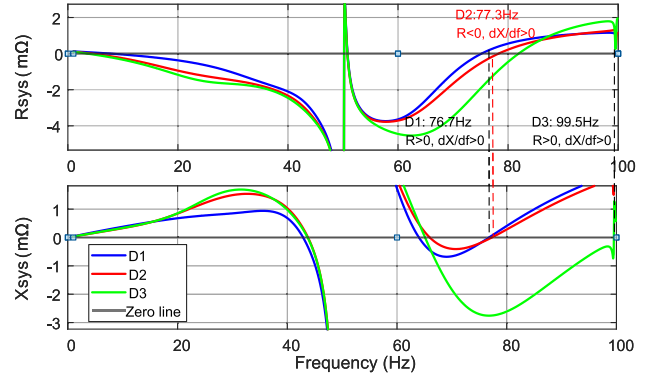


FIGURE 19. Impedance response of the system in Case-1.

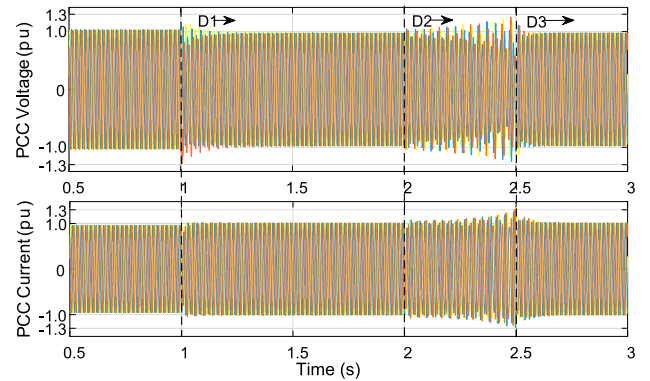


FIGURE 20. Phase voltages and currents at PCC (Case-1): Simulation results at time duration 0.5s - 3 s.

RSC current control and faster GSC current control. The three controls with significant impact on DFIG-WP instability need to be coordinated to ensure desired response during operation. The coordination of the three controls will be discussed in the Recommendation part of section V-C.

V. ILLUSTRATIVE EXAMPLES AND RECOMMENDATION FOR SAFE OPERATION OF DFIG-WP

A. DFIG-WP WEAK GRID INSTABILITY

In Case-1 (C1), initially both Switch 1 and Switch 2 are closed. The following disturbances/modifications are made:

- D1: Opening Switch 1 at $t = 1$ s, which results weak grid condition where the system remains stable.
- D2: Increasing the RSC current PI regulator bandwidth from 60 to 100 Hz at $t = 2$ s which causes instability.
- D3: Increasing the GSC current PI regulator bandwidth from 100 to 200 Hz at $t = 2.5$ s to stabilize the system.

The IBSA results are shown in Fig. 19, and confirmed with EMT simulations presented in Fig. 20 - Fig. 24. After D1, the system reactance cross-over frequency is 76.7 Hz, and the resistance is positive. The intersection frequency and stability phase margin obtained through Bode plot are 76.8 Hz and 11.1° , respectively. Hence, the system is stable after D1,

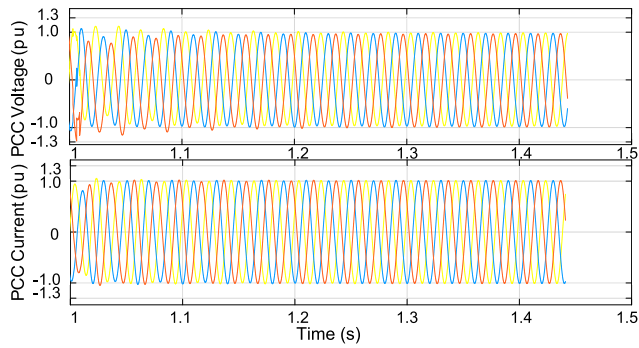


FIGURE 21. Zoom-in version of Fig. 20 at time interval 1 - 1.5s.

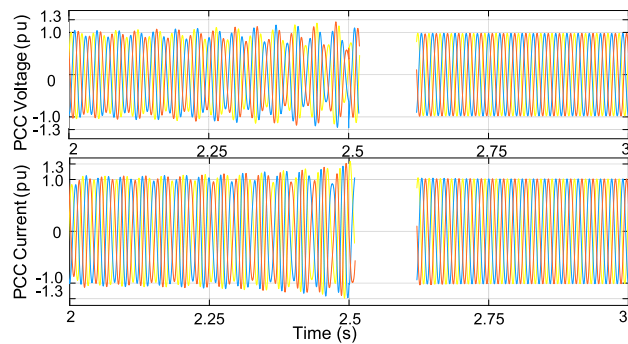


FIGURE 22. Zoom-in version of Fig. 20 at time interval 2 - 3 s.

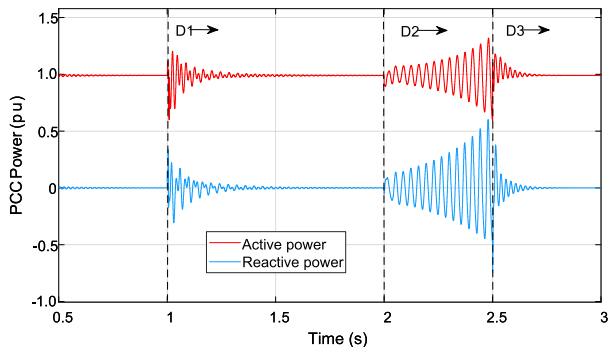


FIGURE 23. Active and reactive powers at PCC (Case-1).

so damped oscillation can be observed in Fig. 21 and Fig. 23 after D1 at $t = 1$ s.

D2 causes instability as fast RSC current control worsens stability in the considered system. After D2, the cross-over frequency shifts to 77.3 Hz and corresponding system resistance becomes negative. The intersection frequency and stability phase margin obtained through Bode plot are 77.5 Hz and -5.5° , respectively. Hence, the system is unstable after D2, so the waveforms of Fig. 22 and Fig. 23 show undamped oscillation after D2 at $t = 2$ s. The frequency spectrum of phase currents in $t = 2 - 2.5$ s shown in Fig. 24 contains a dominant 77.5 Hz frequency component and a mirror 22.5 Hz frequency component.

After D3, the cross-over frequency shifts to 99.5 Hz and corresponding system resistance becomes positive.

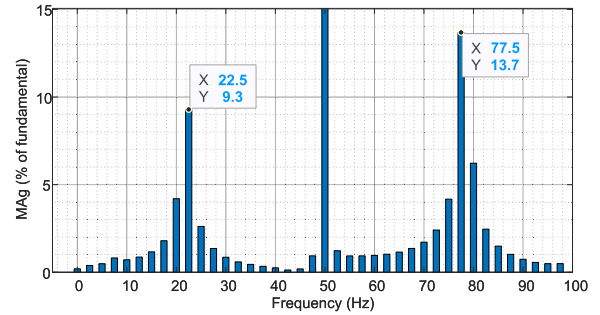


FIGURE 24. FFT analysis of distorted PCC phase currents in 2 - 2.5 s (Case-1).

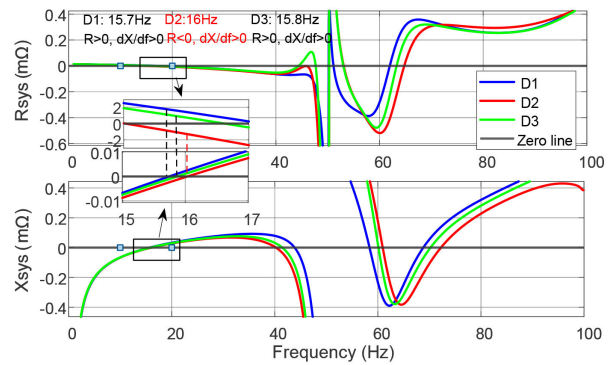


FIGURE 25. Impedance response of the system in Case-2.

The intersection frequency and stability phase margin obtained through Bode plot are 99.5 Hz and 8.2° , respectively. D3 stabilizes the system as fast GSC current control improves stability in weak grid. Hence, the system is stable after D3, so damped oscillations can be observed in Fig. 22 and Fig. 23 after D3 at $t = 2.5$ s.

B. DFIG-WP SERIES-CAPACITOR SSO

In Case-2 (C2), initially Switch 1 is closed and Switch 2 is opened so the series-compensated capacitors are in service. The following disturbances/modifications are made:

- D1: Opening Switch 1 at $t = 1$ s, which results series-capacitor compensated grid condition where the system remains stable.
- D2: Increasing the RSC PQ PI regulator bandwidth from 4 to 10 Hz at $t = 3$ s which causes instability,
- D3: Decreasing the RSC current PI regulator bandwidth from 21 to 18 Hz at $t = 5$ s to stabilize the system.

The IBSA results are shown in Fig. 25, and confirmed with EMT simulations presented in Fig. 26 - Fig. 30. After D1, the system reactance cross-over frequency is 15.7 Hz, and the resistance is positive. The intersection frequency and stability phase margin obtained through Bode plot are 15.8 Hz and 1.9° , respectively. Hence, the system is stable after D1, so damped oscillations can be observed in Fig. 27 and Fig. 29 after D1 at $t = 1$ s.

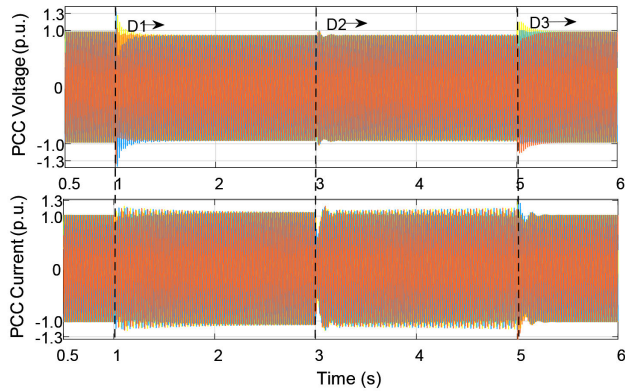


FIGURE 26. Phase voltages and currents at PCC (Case-2): Simulation results at time interval 0.5 - 6 s.

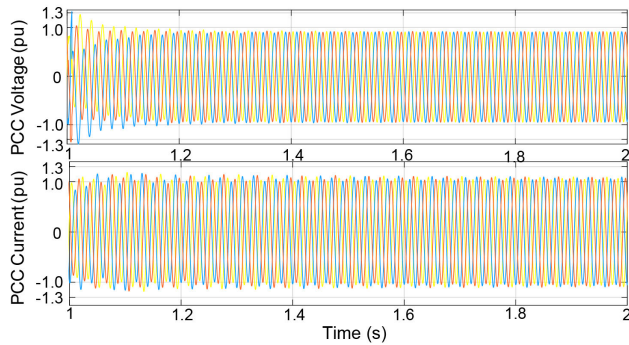


FIGURE 27. Zoom-in version of Fig. 26 at time interval 1 - 1.5 s.

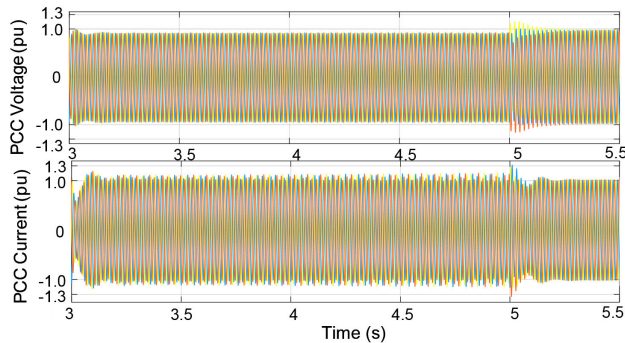


FIGURE 28. Zoom-in version of Fig. 26 at time interval 3 - 5.5 s.

After D2, the cross-over frequency shifts to 16 Hz and corresponding system resistance becomes negative. The intersection frequency and stability phase margin obtained through Bode plot are 16.1 Hz and -1.8° , respectively. D2 causes instability as fast RSC PQ control worsens stability in the considered system. Hence, the system is unstable after D2, so the waveforms Fig. 28 and Fig. 29 show undamped oscillation after D2 at $t = 3$ s. As the phase margin is higher than D2 of Case-1, the growing speed of the oscillation is also much slower. The frequency spectrum of phase currents in 4 - 5 s shown in Fig. 30 contains a dominant

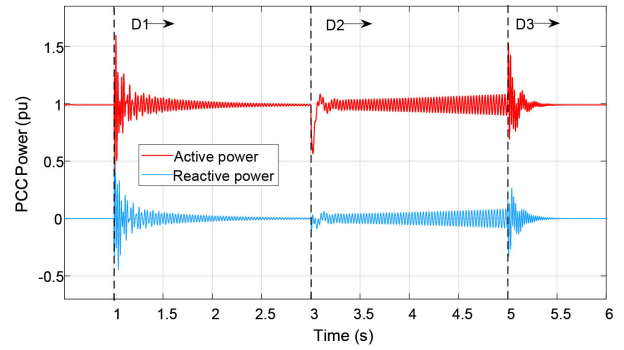


FIGURE 29. Active and reactive powers at PCC (Case-2).

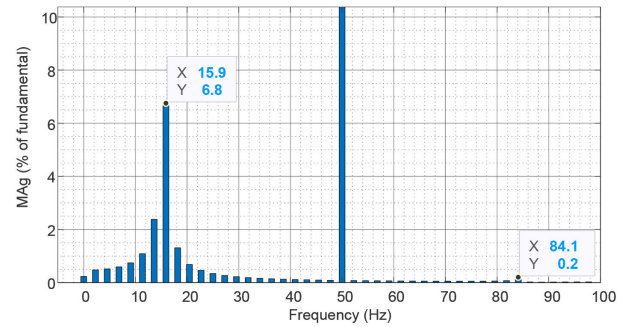


FIGURE 30. FFT analysis of distorted PCC phase currents in 4 - 5 s (Case-2).

15.9 Hz frequency component and a negligible mirror 84.1 Hz frequency component.

After D3, the cross-over frequency shifts to 15.8 Hz and corresponding system resistance becomes positive. The intersection frequency and stability phase margin obtained through Bode plot are 16.1 Hz and 1° , respectively. D3 stabilizes the system as slow RSC current control improves stability in series-capacitor compensated grid. Hence, the system is stable after D3, so damped oscillations can be observed in Fig. 28 and Fig. 29 after D3 at $t = 5$ s.

C. RECOMMENDATIONS FOR THE SAFE OPERATION OF DFIG-WP

This section presents the recommendations for the safe operation of DFIG-WP in terms of small-signal stability, which can be used either as pre-event design or post-event mitigation. As demonstrated in the previous sections, certain DFIG control parameters have significant impact on both the weak grid instability and series-capacitor SSO problems. Hence, the recommendations are based on DFIG control parameter modifications. However, the potential adverse impact of modified parameters on DFIG transient performance needs to be investigated. The recommendations are as follows:

- 1) The AC-DC coupling contribution to the DFIG impedance is not negligible. Hence, it is recommended

to use a DFIG analytical impedance model that accounts for the AC-DC coupling.

- 2) To achieve a 10° phase margin, the RSC current control bandwidth should be set lower than 42 Hz (equivalent to 8.3 ms rise time) to prevent weak grid instability (external grid impedance no more than 0.6 pu in this paper). For the prevention of series capacitor SSO, the RSC current control bandwidth needs to be further turned down, and the effective compensation level should not be higher than 38% (line compensation level will be higher). Typical RSC current control rise time such as 20 ms (equivalent to bandwidth 17.5 Hz) in [24] can be selected to provide phase margin of 3° for the effective compensation level 30% in the considered test system. The results might change with different system structures and parameters, and DFIG-WP operating conditions. Low wind speeds, WT outages, and connection of multiple compensated lines need to be considered for series capacitor SSO prevention. If desired phase margin cannot be achieved, an SDC is needed.
- 3) The GSC can also be used to mitigate weak grid instability by adjusting GSC current control and PLL control in addition to RSC current control. If the mitigation of weak grid instability is only achieved with GSC current control, a relatively fast GSC current control is needed with higher than 120 Hz bandwidth (equivalent to 2.9 ms rise time). If the mitigation of weak grid instability is only achieved with PLL, the PLL bandwidth needs to be lower than 12 Hz (equivalent to 29 ms rise time), which is too slow and impractical. Hence, the parameters of the three controls are recommended to be adjusted within feasible ranges and tuned together to ensure desired response during operation. As an example, typical parameter setting of 20 ms RSC current rise time, 10 ms GSC current rise time and 20 ms GSC PLL rise time can ensure the stable operation under both grid conditions in the considered test system. High wind speed is important to be considered in the system design for weak grid instability prevention.

VI. CONCLUSION

This paper provides a thorough re-examination of DFIG-WP instability phenomena observed in weak and series-capacitor compensated grids considering the AC-DC coupling phenomenon.

Instability takes place in sub-synchronous range in series-capacitor compensated grid and is mainly affected by the RSS (specifically, RSC control parameters). However, the weak grid instability occurs in super-synchronous range with its mirror frequency in sub-synchronous range, and it is affected by both the RSS and GSS (specifically, RSC and GSC control parameters). Classifying weak grid instability phenomenon as weak grid SSO due to

the presence of sub-synchronous frequency component causes misperceptions. There is a need to revise its classification.

For the considered DFIG, the AC-DC coupling makes a considerable resistive contribution to the DFIG impedance around the resonance frequency for both instability cases. Hence, its omission may lead to pessimistic IBSA results.

The impact of DFIG control parameters on instability mechanism and resonance frequency is also refined. Recommendations are provided for DFIG-WP instability prevention and/or mitigation through control parameter modification based on the guidance of stability contour analysis. Future work includes considering the trade-off between system transient response and small signal stability and providing additional guidelines accordingly.

APPENDIX A DETAILED MATRICES [22]

Y_{12dq} is:

$$Y_{12dq} = A_r^{-1} B_r$$

Y_{4dq} is:

$$Y_{4dq} = A^{-1} B$$

Y_{2dc} is:

$$Y_{2dc} = 1.5 \begin{bmatrix} I_{2d}^s/V_{dc} & I_{2q}^s/V_{dc} \end{bmatrix} (Z_{lmslip} - Z_{lr} Z_{lm}^{-1} Z_{ls}) Y_a - 1.5 \begin{bmatrix} V_{2d}^s/V_{dc} & V_{2q}^s/V_{dc} \end{bmatrix} Z_{lm}^{-1} Z_{ls} Y_a - P_r/V_{dc}^2$$

Y_{4dc} is:

$$Y_{4dc} = F - EA^{-1}C$$

Y_a is:

$$Y_a = -A_r^{-1} \begin{bmatrix} V_{2d}^s/V_{dc} & V_{2q}^s/V_{dc} \end{bmatrix}^T$$

Y_b is:

$$Y_b = 1.5 \begin{bmatrix} I_{2d}^s/V_{dc} & I_{2q}^s/V_{dc} \end{bmatrix} (Z_{lmslip} - Z_{lr} Z_{lm}^{-1} Z_{ls}) Y_{12dq} - 1.5 \begin{bmatrix} V_{2d}^s/V_{dc} & V_{2q}^s/V_{dc} \end{bmatrix} Z_{lm}^{-1} Z_{ls} Y_{12dq} + 1.5 \begin{bmatrix} I_{2d}^s/V_{dc} & I_{2q}^s/V_{dc} \end{bmatrix} Z_{lr} Z_{lm}^{-1} + 1.5 \begin{bmatrix} V_{2d}^s/V_{dc} & V_{2q}^s/V_{dc} \end{bmatrix} Z_{lm}^{-1}$$

Y_c is:

$$Y_c = A^{-1}C$$

Y_d is:

$$Y_d = D - EA^{-1}B$$

PI Regulators:

$$\begin{aligned} H_{pqr} &= K_{pqr} + K_{ipqr}/s \\ H_{cr} &= K_{pir} + K_{iir}/s \\ G_{pll} &= \frac{K_{ppll} + K_{ipll}/s}{V_{1d}^s(s + K_{ppll} + K_{ipll}/s)} \\ H_{dc} &= K_{pvdc} + K_{ivdc}/s \\ H_q &= K_{pq} + K_{iq}/s \\ H_c &= K_{pc} + K_{ic}/s \end{aligned}$$

Induction generator impedances:

$$\begin{aligned} \mathbf{Z}_{ls} &= \begin{bmatrix} R_s + sL_{sd} & -\omega L_{sq} \\ \omega L_{sd} & R_s + sL_{sq} \end{bmatrix} \\ \mathbf{Z}_{lm} &= \begin{bmatrix} sL_m & -\omega L_m \\ \omega L_m & sL_m \end{bmatrix} \\ \mathbf{Z}_{lm\text{slip}} &= \begin{bmatrix} sL_m & -\omega_{\text{slip}}L_m \\ \omega_{\text{slip}}L_m & sL_m \end{bmatrix} \\ \mathbf{Z}_{lr} &= \begin{bmatrix} R_r + sL_{rd} & -\omega_{\text{slip}}L_{rq} \\ \omega_{\text{slip}}L_{rd} & R_r + sL_{rq} \end{bmatrix} \end{aligned}$$

PLL impacts:

$$\begin{aligned} \mathbf{G}_{vp\text{pll}} &= \begin{bmatrix} 0 & V_{4q}^s G_{\text{pll}} \\ 0 & -V_{4d}^s G_{\text{pll}} \end{bmatrix} \mathbf{G}_{ip\text{pll}} = \begin{bmatrix} 0 & I_{4q}^s G_{\text{pll}} \\ 0 & -I_{4d}^s G_{\text{pll}} \end{bmatrix} \\ \mathbf{G}_{vr\text{pll}} &= \begin{bmatrix} 0 & V_{2q}^s G_{\text{pll}} \\ 0 & -V_{2d}^s G_{\text{pll}} \end{bmatrix} \mathbf{G}_{ir\text{pll}} = \begin{bmatrix} 0 & I_{2q}^s G_{\text{pll}} \\ 0 & -I_{2d}^s G_{\text{pll}} \end{bmatrix} \end{aligned}$$

Other matrices:

$$\begin{aligned} \mathbf{Z}_{fdq} &= \begin{bmatrix} R_f + sL_f & -\omega L_f \\ \omega L_f & R_f + sL_f \end{bmatrix} \\ \mathbf{V}_{idq} &= 1.5H_q \begin{bmatrix} 0 & 0 \\ V_{4iq}^s & -V_{4id}^s \end{bmatrix} \mathbf{I}_{pq} = 1.5H_q \begin{bmatrix} 0 & 0 \\ I_{4q}^s & -I_{4d}^s \end{bmatrix} \\ \mathbf{V}_{idr} &= 1.5H_{pqr} \begin{bmatrix} V_{1d}^s & V_{1q}^s \\ -V_{1q}^s & V_{1d}^s \end{bmatrix} \mathbf{I}_{pqr} = 1.5H_{pqr} \begin{bmatrix} I_{1d}^s & I_{1q}^s \\ -I_{1q}^s & I_{1d}^s \end{bmatrix} \\ \mathbf{A} &= H_c \mathbf{I} + \mathbf{Z}_{fdq} - H_c \mathbf{V}_{ipq} \\ \mathbf{B} &= \mathbf{I} + H_c \mathbf{G}_{ip\text{pll}} + \mathbf{G}_{vp\text{pll}} - H_c H_q \mathbf{I}_{pq} \\ \mathbf{C} &= -H_c [H_{dc} \quad 0]^T - \begin{bmatrix} V_{4d}^s/V_{dc} & V_{4q}^s/V_{dc} \end{bmatrix}^T \\ \mathbf{D} &= 1.5 \begin{bmatrix} I_{4d}^s/V_{dc} & I_{4q}^s/V_{dc} \end{bmatrix} \\ \mathbf{E} &= 1.5 \begin{bmatrix} V_{4d}^s/V_{dc} & V_{4q}^s/V_{dc} \end{bmatrix} \\ &+ 1.5 \begin{bmatrix} I_{4d}^s/V_{dc} & I_{4q}^s/V_{dc} \end{bmatrix} \mathbf{Z}_{fdq} \\ \mathbf{F} &= -P_r/V_{dc}^2 \\ \mathbf{A}_r &= H_{cr} \mathbf{V}_{ipqr} + (H_{cr} \mathbf{I} + \mathbf{Z}_{lr}) \mathbf{Z}_{lm}^{-1} \mathbf{Z}_{ls} - \mathbf{Z}_{lm\text{slip}} \\ \mathbf{B}_r &= (H_{cr} \mathbf{I} + \mathbf{Z}_{lr}) \mathbf{Z}_{lm}^{-1} + H_{cr} (-\mathbf{I}_{pqr} + \mathbf{G}_{ir\text{pll}}) + \mathbf{G}_{vr\text{pll}} \end{aligned}$$

APPENDIX B SYSTEM PARAMETERS

The parameters used in this paper are listed in Table 1 and Table 2.

TABLE 1. Parameter of the DFIG.

Parameters	Value
WT Base power and AC voltage (S, V_{rms})	2 MW, 690 V
WT Base phase voltage ($V_{ph\text{Amp}}$)	564 V
WT Base phase current ($I_{ph\text{Amp}}$)	2367 A
Induction Generator	
Stator resistance (R_s)	0.0016 Ω
Stator Leakage inductance (L_{ls})	35.18 mH
Mutual inductance (L_m)	3.6 mH
Rotor resistance (R_r)	0.0012 Ω
Rotor Leakage inductance (L_{lr})	15.00 mH
Pole pairs and rotor angular speed (n_p, ω_r)	2, 1.2 pu
Rotor-side converter	
Current PI Regulator (K_{pir}, K_{iir})	0.12, 15.80 (C1D1) 0.20, 43.88 (C1D2&D3) 0.043, 1.94 (C2D1&D2) 0.037, 1.42 (C2D3)
Active and Reactive Power PI Regulator (K_{ppqr}, K_{ipqr})	0.0002, 0.0368 (C1, C2D1) 0.0006, 0.1055 (C2D2&D3)
Grid-side converter	
DC voltage and capacitor (V_{dc}, C_{dc})	1100 V, 10 mF
L-type filter (R_f, L_f)	0.006 Ω , 37.887 mH
PLL PI regulator (K_{ppll}, K_{ipll})	130, 8388
DC voltage PI regulator (K_{pvdc}, K_{ivdc})	1.6841, 109.06
Current PI regulator (K_{pi}, K_{ii})	0.16, 35.31 (C1D1&D2) 0.33, 141.24 (C1D3)

TABLE 2. Parameter of the wind park and external grids.

Parameters	Value
Wind turbine and wind park transformers	
Equivalent resistance (R_{tr-wt}, R_{tr-wp})	0.002 pu, 0.003 pu
Equivalent reactance (X_{tr-wt}, X_{tr-wp})	0.006 pu, 0.12 pu
Grid line 1 and 2	
Resistance (R_{tr-wt}, R_{tr-wp})	0.015 pu, 0.06 pu
Reactance (X_1, X_2, X_{cap})	0.1 pu, 0.4 pu, 0.12 pu

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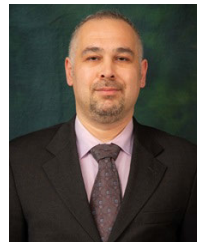
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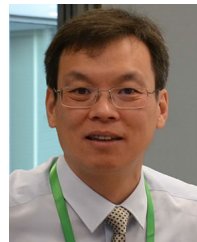


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