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RESEARCH ARTICLE

Predictive Deadbeat Average Model Control for Power Conversion System With LCL Filter

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ABSTRACT The inherent resonance issue of LCL filters in the power conversion system(PCS) will significantly degrade the system's stability. Researches indicate that decreasing the time delay contributes to the system's stability under converter-side current feedback(CCF) control. To improve the system's stability, this paper is devoted to alleviating the impact of time delay on the system's stability by the combination of time-delay compensation and time-delay reduction. Since the effectiveness of time-delay compensation provided by predictive control depends on the accuracy of the control model, a deadbeat average model (DBAM) for the CCF loop is established based on the use of the oversampling technique. The proposed control model, which ingeniously transforms conventional single-point sampling control into multi-point average control, improves the accuracy of the system description. Furthermore, through the introduction of predictive control combined with the double-updated PWM method, a predictive deadbeat average model (PDBAM) control method is proposed for the PCS. The proposed control method minimizes the impact of time delay on CCF loop, which enhances the system's stability and overcomes the resonance issue of LCL filter. Besides, the stable region of the PDBAM control is deduced. Simulation and experimental results demonstrate the effectiveness of the PDBAM control.

INDEX TERMS LCL filter, power conversion system, predictive control, system stability.

I. INTRODUCTION

The penetration of renewable energy sources in energy structure continues to increase due to their sustainability and cleaning characteristics. Dispatchable energy storage systems can provide efficient solutions for the degradation of stability and reliability of the grid caused by the fluctuation and intermittency of renewable energy generation [1]. Owing to the recent developments in battery chemistries, the battery energy storage system(BESS) with the characteristics of grid synchronization and DC power management capability is the most promising energy-storage technology [2], [3]. Connecting the battery and the grid, the power conversion system(PCS), including a three-phase bidirectional AC/DC converter and an LCL filter which can improve harmonic performance with a small filter size, is the key to the BESS [4], [5].

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However, the use of LCL filters will introduce their inherent resonance issue, significantly degrading the system's stability. In order to solve the resonance issue, conventional damping methods, including passive damping and active damping methods, have been proposed to provide additional damping terms [6], [7].

The passive damping method [8], directly introducing a set of physical resistors into the LCL filter, will increase the power loss, which is unappealing in PCS with the requirement for high efficiency. In contrast, the active damping methods without power loss have received more attention, such as filter capacitor current feedback [9], [10], [11], filter capacitor voltage feedforward [12], [13], [14], and notch filter-based method [15], [16], [17]. The active damping method suppresses the LCL resonance issue by establishing virtual impedance and resonant frequency cancellation through software. Nevertheless, the inherent time delay of digital system will inevitably impact the realization of active damping method. Researches [14], [15], [18], [19] have studied the impact of the inherent time delay on the capacitor

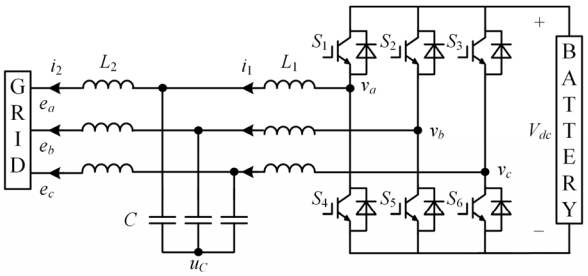

FIGURE 1. Topology of the PCS.

current feedback, filter capacitor voltage feedforward, and notch filter-based method, and conclude that the active damping characteristics will degrade or even disappear without exception due to the inherent time delay. Many publications [20], [21] indicate that decreasing time delay of digital systems contributes to the system's stability under converter-side current feedback(CCF) control. This paper is devoted to alleviating the impact of time delay on the CCF loop to improve the system's stability and overcome the LCL resonance issue.

In the PCS, the typical value of time delay in the digital system is 1.5 times a switching period($1.5T_s$) [14], [15], [19], [20], [21]. Generally, the methods to eliminate the impact of time delay can be classified into time-delay reduction methods and time-delay compensation methods [16], [18]. Time-delay reduction methods, such as sampling point shifting [21] and multi-updated PWM method [22], can reduce time delay to a degree, which is less than a control period. Time-delay compensation methods are mainly based on predictive control, including deadbeat control [23], [24] and linear predictor [25]; nevertheless, to ensure prediction accuracy, the predictive control is typically model-based and usually compensate for finite time delays that are integer multiples of the control period. Table 2, given in Appendix A, compares three advanced time-delay elimination methods for LCL-filter AC/DC converters with the proposed methods according to [21], [23], and [25]. Considering that time delay reduction methods and time delay compensation methods cannot eliminate the impact of time delay in the PCS independently, this paper adopts the combination of multi-updated PWM method and predictive deadbeat control.

In predictive control, the effectiveness of time-delay compensation depends on the accuracy of control model. Limited by computing resources, sampling aliasing, and system noise, the conventional control model usually sets the control frequency as the switching frequency and adopts a regular sampling method with a fixed sample point. Some studies [20], [26] claim that setting the sample point at the starting/middle point of a switching period can obtain the average value of the current. Essentially, the current waveform comprises the main sine-wave component and the secondary triangular-wave component. The physical meaning(average/peak/valley) of the fixed sample point, which is set according to the triangular-wave component, will be changed by the sine-wave components. Therefore, using the conventional model based on regular sampling to describe the average/peak/valley state of actual plants is inaccurate.

As is well known, the builds of discrete models are based on samples, and more effective samples make the discrete system closer to the continuous system [27], [28]. In fact, the sampling frequency determined by the sensor can be much higher than the control frequency. Unfortunately, the conventional control model cannot handle multi-point samples in a control period. Therefore, by using oversampling techniques and average process, this paper establishes a deadbeat average model with actual physical meaning, improving the accuracy of control model.

To ensure prediction accuracy, the predictive control typically provides time-delay compensation for a control period [17], especially when the prediction is based on the inaccurate conventional model. In this case, control delay can be compensated, but PWM delay still takes effect. Besides, PWM delay with the value of $0.5T_s$ is difficult to analyze when the time unit of digital systems is set as T_s; therefore, equivalence processes for PWM delay are typically required in [11], [12], [15], and [20] at the expense of the accuracy of the time-delay compensation. In this paper, predictive control based on the proposed control model can provide time-delay compensation for a switching period. With the introduction of double-updated PWM method, the time unit of the control system is halved to $0.5T_s$, so both control delay and PWM delay can be regarded as pure time-delay terms with the value of $0.5T_s$ in the proposed model, which can be easily compensated by the predictive control.

This paper establishes a deadbeat average model(DBAM) for the CCF loop and proposes a predictive deadbeat average model(PDBAM) control method for the PCS with LCL filters. Based on the application of the oversampling technique, the proposed control model, which has a clear physical meaning and describes the actual plants accurately, ingeniously transforms conventional single-point sampling control into multi-point average control. Furthermore, through the introduction of predictive control combined with double-updated PWM method, the proposed control method minimizes the impact of time delay on the CCF loop, which improves the system's stability and overcomes the resonance issue of LCL filter. Besides, the stable region of the PDBAM control method is deduced, which provides guidelines for the system parameter configuration of the PCS. Simulation and experimental results verify the effectiveness of the PDBAM control in stabilizing the system without additional damping methods.

This paper is organized as follows. Section II presents the build of the DBAM for the CCF loop in detail. Then, the PDBAM control is derived, and the control performance and stable region of the PDBAM control are analyzed in section III. In section IV, the results of our simulation and experiments are discussed in detail to verify the effectiveness and reliability of the PDBAM control method. Finally, the conclusions are drawn study in section V.

II. DEADBEAT AVERAGE CONTROL MODEL

Fig.1 shows the typical topology of PCS, which includes a DC-link, a three-phase bidirectional grid-connected AC/DC converter, an LCL filter, and the grid. The bidirectional converter(specifically the switching device $S_1 \sim S_6$ in the converter) is the control object. The LCL filter comprises converter-side inductors L_1, filter capacitors C, and gird-side inductors L_2(including the grid-side inductors of LCL filters and the grid inductors from grid-tied transformers), where the parasitic resistance is neglected to represent the worst case. In practical BESS, the PCS is commonly connected to the grid through a series of transformers. As a result, directly measuring the actual grid voltage is difficult, and the filter capacitor voltage is usually regarded as the point of common coupling(PCC) voltage. For economic viability and reliability of the system, the use of sensors should be minimized in industrial applications. In this paper, seven sensors are used for CCF control, including three current sensors, three AC voltage sensors, and a DC voltage sensor. Therefore, converter-side current, capacitor voltage, and battery voltage can be measured directly.

In the three-phase bidirectional AC/DC converter, the two switches in each arm should be operated in a complementary mode to avoid a short circuit. Therefore, the switching states of three phases can be described as: when $S_1/S_2/S_3$ is on, $S_a/S_b/S_c$ is equal to 1; when $S_1/S_2/S_3$ is off, $S_a/S_b/S_c$ is equal to 0. Suppose $\mathbf{S}$ and $\mathbf{S}_{com}$ as the switching states array and its common-mode component(coupling term), which can be expressed as

$$\begin{cases} \mathbf{S}_{com} = \dfrac{S_a + S_b + S_c}{3} [1, 1, 1]^T \\ \mathbf{S} = [S_a, S_b, S_c]^T - \mathbf{S}_{com} \end{cases}. \tag{1}$$

where the subscript, a, b, c, denotes the variable in the abc frame.

A. CONVENTIONAL CCF CONTROL MODEL

Since PCC voltage and battery voltage mainly depend on grid conditions and battery conditions, which are usually stable, single-loop current control is typically applied in the grid-connected converter, including CCF control and grid-side current feedback(GCF) control.

In the CCF loop, according to Kirchhoff's voltage law, the i-v equation of converter-side inductors can be expressed as

$$L_1 \frac{d\mathbf{i}_1}{dt} = \mathbf{v} - \mathbf{u}_C, \tag{2}$$

where $\mathbf{i}_1$, $\mathbf{u}_C$, and $\mathbf{v}$ denote the converter-side current array, capacitor voltage array, and converter voltage array, respectively, which can be expressed as $\mathbf{i}_1 = [i_{1a}, i_{1b}, i_{1c}]^T$, $\mathbf{u}_C = [u_{Ca}, u_{Cb}, u_{Cc}]^T$, and $\mathbf{v} = [v_a, v_b, v_c]^T$. Since $\mathbf{v}$ cannot be measured directly, $\mathbf{v}$ needs to be reconstructed by $\mathbf{v} = V_{dc} \cdot \mathbf{S}$.

In order to describe the system states in a switching period, the conventional control model typically adopts a regular sampling method to avoid sampling aliasing. Considering that the whole control strategy, including phase-locked loop(PLL), park transform, control algorithms, and space vector modulation(SVM) strategy, will cost huge computing resources, the control frequency cannot be much higher than switching frequency and control frequency typically is set as switching frequency.

From (2), the conventional control model can be expressed as [23], [29], and [30]

$$\frac{L_1}{T_s} [\mathbf{i}_1 - \mathbf{i}_1 (k)] = V_{dc} \cdot \mathbf{D} (k) - \mathbf{u}_C (k), \tag{3}$$

where (k) denotes the variables in period k, and $\mathbf{D}$ is defined as the duty cycle array, which can be expressed as

$$\begin{cases} \mathbf{D}_{com} = \dfrac{d_a + d_b + d_c}{3} [1, 1, 1]^T \\ \mathbf{D} = [d_a, d_b, d_c]^T - \mathbf{D}_{com} \end{cases}. \tag{4}$$

where $\mathbf{D}_{com}$ is the common-mode component(coupling term) of duty cycle.

In the SVM strategy, the conventional control method in the dq frame can be expressed as [31] and [32]

$$\begin{cases} v_d (k) = D (z) \left[i_{1d}^* - i_{1d} (k) \right] + \omega L_1 i_{1q} (k) + u_{Cd} (k) \\ v_q (k) = D (z) \left[i_{1q}^* - i_{1q} (k) \right] - \omega L_1 i_{1d} (k) + u_{Cq} (k) \end{cases}, \tag{5}$$

where the superscript, $*$, denotes the reference value, the subscript, dq, denotes the variable in the dq frame, and $D(z)$ is the transfer function of the digital controller, which depends on the adopted control method.

B. DEADBEAT AVERAGE CONTROL MODEL

In the digital control system, the circuit, as a continuous system, needs to be discretized. An accurate control model for the plant is the basis for obtaining the desired control effect. The builds of discrete models are based on samples, and more effective samples mean more accurate models.

Compared with the widely used regular sampling method, the oversampling technique, which can provide much more samples in a control period, is a practical choice to improve the accuracy of the discrete control model. As mentioned in the previous section, the current control based on the conventional model cannot handle multi-point samples. Therefore, building a new control model for properly handling multi-point samples is necessary.

Assuming n samples are available over the course of a control period with the use of oversampling technique. In the SVM strategy, a constant-frequency dual-edge PWM is always adopted, and the schematic diagram of the modulation signal, carrier signal, switching signal, and current wave are shown in Fig.2. In fact, since the 5/7-segment SVM is adopted in the three-phase converter, there are 5/7 switching states and current states exist in a switching period. Due to the superimposability of the circuit states, the effect of **S/D** on current states can be decomposed into the effect of S_a/D_a, S_b/D_b, S_c/D_c and $\mathbf{S}_{com}/\mathbf{D}_{com}$ on current states. To simplify the

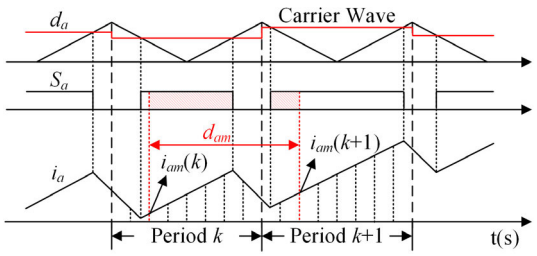

FIGURE 2. Schematic of oversampling.

description, take the effect of S_a/D_a on i_{1a} as an example in Fig.2.

From (2), the multi-point samples shown in Fig.2 can be given by

$$\begin{cases} L_1\left[\mathbf{i}_{10}(k+1)-\mathbf{i}_{10}(k)\right]=\int_{kT_s}^{(k+1)T_s}\left[\mathbf{v}_0(t)-\mathbf{u}_{C0}(t)\right]dt \\ \quad\vdots \qquad\qquad\qquad \vdots \\ L_1\left[\mathbf{i}_{1m}(k+1)-\mathbf{i}_{1m}(k)\right]=\int_{(k+\frac{m}{n})T_s}^{(k+1+\frac{m}{n})T_s} \\ \quad \left[\mathbf{v}_m(t)-\mathbf{u}_{Cm}(t)\right]dt \\ \quad\vdots \qquad\qquad\qquad \vdots \\ L_1\left[\mathbf{i}_{1n}(k+1)-\mathbf{i}_{1n}(k)\right]=\int_{(k+\frac{n}{n})T_s}^{(k+1+\frac{n}{n})T_s}\left[\mathbf{v}_n(t)-\mathbf{u}_{Cn}(t)\right]dt \end{cases}, \tag{6}$$

where the subscript, m, denotes the system state of sample point mth, $m \in (0, 1, 2, \ldots, n)$.

In (6), the value of $\mathbf{v}_m$ depends on the value of $\mathbf{D}_m$, and $\mathbf{D}_m$ will vary according to the position of the sampling point. The details are given in Appendix B. In order to obtain the control signal $\mathbf{D}$ in a control period for control purpose, the average process is introduced into (6), which can be expressed as

$$\frac{1}{n}\sum_{m=0}^{n} L_1\left[\mathbf{i}_{1m}(k+1)-\mathbf{i}_{1m}(k)\right] = \frac{1}{n}\sum_{m=0}^{n}\int_{(k+\frac{m}{n})T_s}^{(k+1+\frac{m}{n})T_s}\left[\mathbf{v}_m(t)-\mathbf{u}_{Cm}(t)\right]dt. \tag{7}$$

If a sufficient number of samples is available, (7) can be rewritten as (a detailed derivation is given in Appendix B)

$$\frac{L_1}{T_s}\left[\mathbf{I}_1(k+1)-\mathbf{I}_1(k)\right] = \frac{\mathbf{V}(k+1)+\mathbf{V}(k)}{2}-\frac{\mathbf{U}_C(k+1)+\mathbf{U}_C(k)}{2}, \tag{8}$$

where $\mathbf{I}_1$, $\mathbf{U}_C$, and $\mathbf{V}$ are the average system state arrays of converter-side current, capacitor voltage, and converter voltage in a control period, which can be expressed as $\mathbf{I}_1 = [I_{1a}, I_{1b}, I_{1c}]^T$, $\mathbf{U}_C = [U_{Ca}, U_{Cb}, U_{Cc}]^T$, and $\mathbf{V} = [V_a, V_b, V_c]^T$. $\mathbf{V}$ needs to be reconstructed by $\mathbf{V} = V_{dc} \cdot \mathbf{D}$.

Equation(8) is the difference equation of adjacent average current; the right side of the equation contains the average of voltage states in adjacent periods. Therefore, (8) is defined as the deadbeat average control model.

The conventional control model in (3) and the DBAM in (8) have some similarities in mathematical expressions since (3) and (8) are both derived from the i-v characteristic of inductors. The DBAM is obtained by introducing oversampling technique and average process, due to the superimposability of the circuit states and the symmetry of the carriers of dual-edge PWM strategy. The DBAM ingeniously transforms conventional single-point sampling control into multi-point average control. Fig.3 shows the converter-side current waveform in the conventional control model and the DBAM during stable operation of the system.

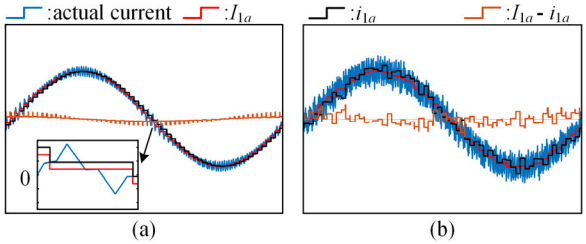

FIGURE 3. Converter-side current of the conventional control model and the DBAM (a) Without noise; (b) Under noise.

As shown in Fig.3, the actual current waveform is composed of the main sine-wave component and the secondary triangular-wave component. Therefore, I_{1a} obtained by oversampling in the DBAM is the average current of phase A in a control period, while i_{1a} obtained by single-point sampling in the conventional control model represents the instantaneous current of phase A at the sampling point. From Fig.3(a), the difference between i_{1a} and I_{1a} is obvious, and the difference increases as the rate of change of sinusoidal current increases, where the maximum difference occurs when the sinusoidal current crosses zero. Due to the varying differences between i_{1a} and I_{1a}, it is almost unachievable to obtain currents with clear physical meaning by single-point sampling, such as average, peak, or valley current.

Moreover, the large amounts of power consumed by the electronic devices in the PCS will lead to undesirable noise. From Fig.3(b), the multi-point sampling in DBAM shows better anti-interference performance than the single-point sampling in conventional control model.

Therefore, compared with the conventional model, the DBAM with a clear physical meaning can describe the average states of actual plants more accurately, providing an optimized control model for further time delay compensation.

III. PDBAM CONTROL AND CONTROL SYSTEM ANALYSIS

A. DEADBEAT AVERAGE CONTROL MODEL

In theory, the conventional control method in Section II-A could realize ideal control effects without any time delay. However, the inherent time delay, including control delay

t_{d1} and PWM delay t_{d2}, is inevitable in digital systems. Assuming the switching period is T_s, the control delay, equal to a control period, will make the control signal $\mathbf{D}(k)$ obtained in period k be updated in period $k+1$ instead of period k. The PWM delay, caused by the zero-order hold (ZOH) effect, will make the updated control signal activated half of a period later, as shown in Fig.4.

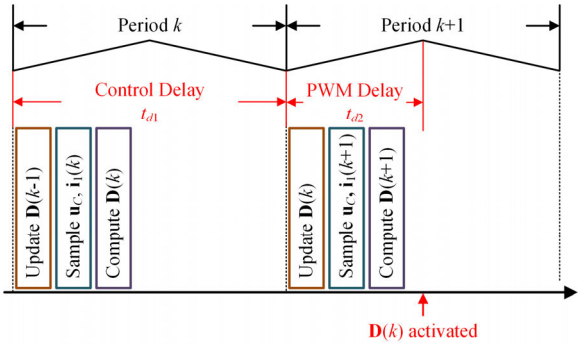

FIGURE 4. Time sequences of the conventional current control.

Time delay will degrade the system's stability, leading to the resonance issue of the LCL filter. In order to minimize the time delay of digital control, this paper proposed a PDBAM control method by the combination of time delay reduction method and time delay compensation method.

First, predictive control for time-delay compensation is adopted in DBAM, where $\mathbf{D}(k+1)$ can be obtained in period k, as shown in Fig.5.

In the DBAM, the oversampling process continues over the entire control period; therefore, the $\mathbf{I}_1(k)$ is obtained in period $k+1$ rather than period k. Thus, prediction for $\mathbf{I}_1(k)$ in (8) needs to be introduced. By applying recursion to (8), the predictive control based on DBAM can be given by

$$\begin{cases} \dfrac{L_1}{T_s}\left[\mathbf{I}_1(k) - \mathbf{I}_1(k-1)\right] = \dfrac{\mathbf{U}_1(k) + \mathbf{U}_1(k-1)}{2} \\ \dfrac{L_1}{T_s}\left[\mathbf{I}_1^* - \mathbf{I}_1(k)\right] = \dfrac{\mathbf{U}_1(k+1) + \mathbf{U}_1(k)}{2} \end{cases}, \quad (9)$$

where $\mathbf{U}_1 = \mathbf{V} - \mathbf{U}_C$, and $\mathbf{D}(k\text{-}1)$ and $\mathbf{D}(k)$ is obtained during period k-1 in the recursive algorithm, which means $\mathbf{U}_1(k\text{-}1)$ and $\mathbf{U}_1(k)$ is known in period k.

Equation(9) can be rewritten as

$$\frac{L_1}{T_s}\left[\mathbf{I}_1^* - \mathbf{I}_1(k-1)\right] = \frac{\mathbf{U}_1(k+1) + 2\mathbf{U}_1(k) + \mathbf{U}_1(k-1)}{2}. \quad (10)$$

From (10), the predictive control based on DBAM can provide time-delay compensation for a switching period T_s.

At this point, control period is set as a switching period. The control delay t_{d1} equal to a control period T_s can be compensated by predictive control, but PWM delay t_{d2} equal to $0.5T_s$ will still take effect, as shown in Fig.5.

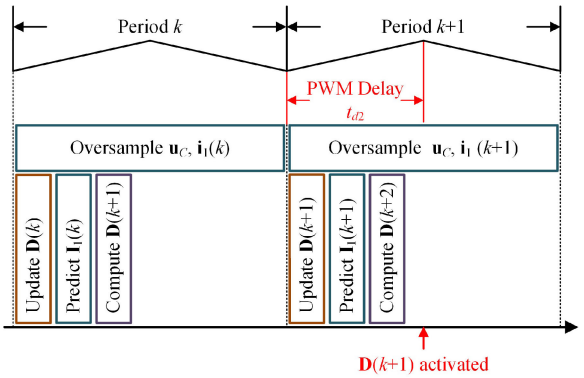

FIGURE 5. Time sequences of the predictive control based on DBAM.

Moreover, when the time unit of digital system analysis equal to a control period is T_s, the accuracy of system analysis tools is not enough for analyzing PWM delay with the value of $0.5T_s$. This is why equivalence processes for PWM delay are required in the conventional control model, causing inconvenience to the time-delay compensation and system analysis.

In this paper, the PWM delay will be regarded as a pure time delay term in the discrete domain, which requires t_{d2} to be an integral multiple of the time unit of digital system analysis. Considering that the predictive control in (10) can provide time-delay compensation for T_s, assuming both t_{d1} and t_{d2} can be compensated by (10), it can be expressed as

$$\begin{cases} t_{d1} + t_{d2} = T_s \\ t_{d2} = j \times \text{control period}, \quad j = 1, 2, 3, \ldots \end{cases} \quad (11)$$

When control period is equal to $0.5T_s$, the constraint condition in (11) can be satisfied. At this point, both control delay and PWM delay can be easily converted into pure time delay terms with Z-transform.

With double-updated PWM method, the control period can be halved to $0.5T_s$, and a switching period can be divided into two parts. From (10), the PDBAM control methods can be expressed as

$$\begin{cases} \dfrac{L_1}{T_s}\left[\mathbf{I}_1^* - \mathbf{I}_1(k_{0.0\sim1.0})\right] \\ = \dfrac{\mathbf{U}_1(k_{1.0\sim2.0}) + 2\mathbf{U}_1(k_{0.5\sim1.5}) + \mathbf{U}_1(k_{0.0\sim1.0})}{2} \\ \mathbf{D}(k_{1.5\sim2.0}) = \left[\mathbf{U}_1(k_{1.5\sim2.0}) - \mathbf{U}_C(k_{1.5\sim2.0})\right] \cdot V_{dc}^{-1} \end{cases}, \quad (12)$$

where $k_{0.0\sim1.0}$ denotes the value in the first and the second half of switching period k, and $k_{1.5\sim2.0}$ denotes the value in the second half of switching period $k+1$.

In PDBAM, predictive control combined with double-updated PWM method is applied, and both control delay and PWM delay of digital system can be compensated. The time sequences of the PDBAM control method are shown in Fig.6.

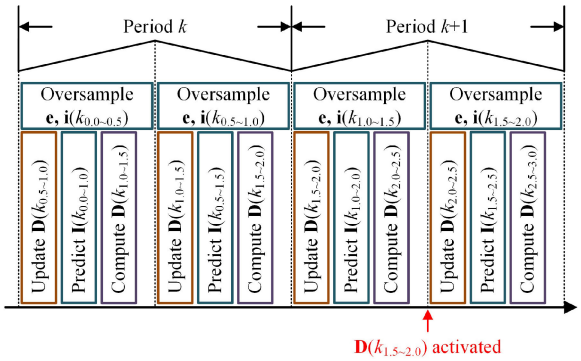

FIGURE 6. Time sequences of the PDBAM control.

In the dq frame, the PDBAM control methods can be expressed as

$$\begin{cases} \dfrac{L_1}{T_s}\left[I_{1d}^* - I_{1d}\left(k_{0.0\sim1.0}\right)\right] \\ = \dfrac{U_{1d}\left(k_{1.0\sim2.0}\right) + 2U_{1d}\left(k_{0.5\sim1.5}\right) + U_{1d}\left(k_{0.0\sim1.0}\right)}{2} \\ +\omega L_1\left[I_{1q}\left(k_{0.5\sim1.5}\right) + I_{1q}\left(k_{0.0\sim1.0}\right)\right] \\ \dfrac{L_1}{T_s}\left[I_{1q}^* - I_{1q}\left(k_{0.0\sim1.0}\right)\right] \\ = \dfrac{U_{1q}\left(k_{1.0\sim2.0}\right) + 2U_{1q}\left(k_{0.5\sim1.5}\right) + U_{1q}\left(k_{0.0\sim1.0}\right)}{2} \\ -\omega L_1\left[I_{1d}\left(k_{0.5\sim1.5}\right) + I_{1d}\left(k_{0.0\sim1.0}\right)\right] \end{cases}. \tag{13}$$

Note that the introduction of the double-updated PWM method will slightly break the symmetry of the DBAM based on a dual-edge PWM strategy, causing some nonlinearities to the system. To solve that problem, integral compensation terms can be introduced properly.

B. CONTROL SYSTEM ANALYSIS FOR PDBAVM CONTROL

In this section, the system's stability and the PDBAM control's control performance are discussed and analyzed. The system control block diagram under CCF control is shown in Fig.7.

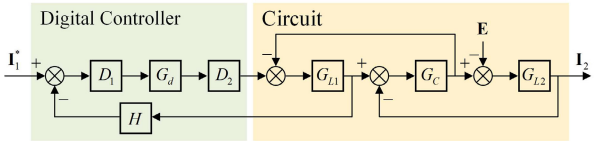

FIGURE 7. Control block diagram of the PCS.

The continuous transfer function of the LCL filter in CCF control $G_{LCL}(s)$ can be expressed as [20] and [21].

$$G_{LCL}(s) = \frac{CL_2s^2 + 1}{L_1CL_2s^3 + sL_1 + sL_2}. \tag{14}$$

The bode diagrams of the LCL filter are shown in Fig.8.

The phase of a stable system should avoid any $(2j\pm1)\pi$ crossing according to the Nyquist stability criterion.

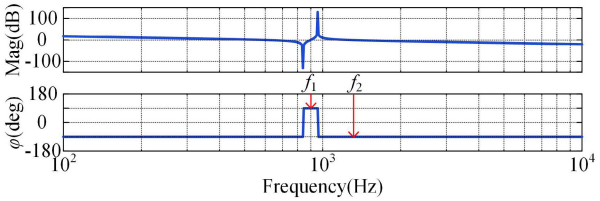

FIGURE 8. Bode diagrams of the LCL filter in CCF control.

From Fig.8, $\varphi(G_{LCL})$ jumps from 90° at f_1 to −90° at f_2. Besides, the phase of the time delay, including control delay t_{d1} and PWM delay t_{d2}, φ_{dealy} can be expressed as [14] and [21]

$$\varphi_{delay} = -\frac{f_{res}}{f_s} \times \frac{t_{d1} + t_{d2}}{T_s} \times 360° \tag{15}$$

where f_s is the switching frequency, f_{res} is resonance frequency, and $f_{res} = (2\pi)^{-1}\sqrt{(L_1 + L_2)\cdot(L_1L_2C)^{-1}}$.

It can be seen that the φ_{delay} is always negative and will decrease with the increase of time delay in a specific system. Therefore, time delay degrades the phase characteristic of control system, and decreasing the time delay will contribute to the stability of CCF control.

From PDBAM control, the transfer function of digital controller $D_1(z)$ can be expressed as

$$D_1(z) = \frac{2L_1(z+1)}{T_s\left(1+z^{-1}\right)^3}. \tag{16}$$

With the double-updated PWM method, the control period is set as $0.5T_s$, and then both control delay and PWM delay, which are equal to a control period, can be converted into a pure unit time delay z^{-1}. Therefore, the transfer function of time delay $G_d(z)$ can be given by

$$G_d(z) = z^{-2}. \tag{17}$$

D_2 presents the average processes in PDBM, which can be expressed as

$$D_2(z) = \frac{1}{2}\left(1 + z^{-1}\right). \tag{18}$$

Thus, the open-loop transfer function of the system $G_{open}(z)$ can be given by

$$G_{open}(z) = \frac{2L_1}{T_s\left(1+z^{-1}\right)} \cdot z^{-1} \cdot Z\left[G_{LCL}(s)\right]. \tag{19}$$

The magnitude Mag and the phase φ of G_{open} can be obtained as

$$\begin{cases} Mag = 20\lg\left|\dfrac{2L_1}{T_s\left(1+z^{-1}\right)}Z\left[G_{LCL}\right]\right| \\ \varphi = \varphi\left(\dfrac{1}{1+z^{-1}}\right) + \varphi\left(z^{-1}\right) + \varphi\left(G_{LCL}\right) \end{cases}. \tag{20}$$

According to the Nyquist stability criterion in open-loop bode diagrams, the phase should avoid any $(2j\pm1)\pi$ crossing

around resonance peak, which can be expressed as

$$\begin{cases} (2j-1)\times 180^\circ < \varphi(f_1) < (2j+1)\times 180^\circ \\ (2j-1)\times 180^\circ < \varphi(f_2) < (2j+1)\times 180^\circ \end{cases}, \quad (21)$$

where j is an integer. From (20), $\varphi(f_1)$ and $\varphi(f_2)$ can be expressed as

$$\begin{cases} \varphi(f_1) = 90^\circ + \varphi\left[\left(1+z^{-1}\right)^{-1}\right] + \varphi\left(z^{-1}\right) - \varphi_{PM} \\ \varphi(f_2) = -90^\circ + \varphi\left[\left(1+z^{-1}\right)^{-1}\right] + \varphi\left(z^{-1}\right) - \varphi_{PM} \end{cases}, \quad (22)$$

where $\varphi\left[\left(1+z^{-1}\right)^{-1}\right] \in [0, 90^\circ]$, and φ_{PM} is the phase margin.

The stable region for the CCF loop under PDBAM control can be derived from (21) and (22). When φ_{PM} =0, the maximum stable region can be obtained, which is f_{res} <0.5f_s. In order to enhance the reliability of the practical system, φ_{PM} is set as 30° to overcome parameter mismatches and nonlinearities in the system. Therefore, the stable region can be expressed as:

$$f_{res} < \frac{f_s}{3}, \quad (23)$$

The stable region provides guidelines for the configuration of system parameters, such as switching frequency and LCL filter parameters, and proper parameter configuration can enhance system robustness against uncertain grid variation. Fig.9 shows the control block diagram of CCF loop.

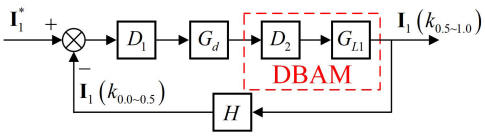

FIGURE 9. Control Block Diagram of the CCF loop.

In Fig.9, G_{L1} is the transfer function of converter-side inductors in the proposed DBAM. From (8), the discrete transfer function $D_2(z)G_{L1}(z)$ of DBAM can be written as

$$D_2(z)G_{L1}(z) = \frac{T_s\left(1+z^{-1}\right)}{2L_1\left(1-z^{-1}\right)}. \quad (24)$$

As mentioned in Section III-A, the system contains a unit time delay z^{-1} in the feedback path due to the oversampling process continuing for a whole control period. So, the transfer function of feedback path $H(z)$ can be expressed as

$$H(z) = z^{-1}. \quad (25)$$

Thus, the closed-loop transfer function of the CCF loop Φ(z) can be obtained as

$$\Phi(z) = \frac{D_1(z)\,G_d(z)\,D_2(z)\,G_{L1}(z)}{1+H(z)\,D_1(z)\,G_d(z)\,D_2(z)\,G_{L1}(z)} = z^{-1}. \quad (26)$$

From (26), PDBAM control can theoretically achieve the deadbeat control effect, which is consistent with the principle of deadbeat control.

Overall, the control schematic of the PCS under PDBAM control is shown in Fig.10.

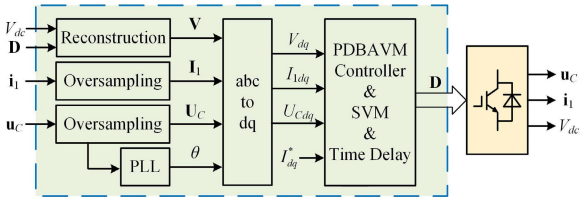

FIGURE 10. Control schematic of PCS.

C. COMPARISON OF EXISTING METHODS

In this section, the system's stability of conventional PI control, conventional deadbeat control, and the improved PI control applied in [21] are compared.

The transfer function $D_{PI}(z)$ for conventional digital PI control can be given by

$$D_{PI}(z) = K_P + T_s K_I \frac{1}{1-z^{-1}}, \quad (27)$$

From (3), The transfer function $D_{DB}(z)$ for conventional deadbeat control can be expressed as

$$D_{DB}(z) = \frac{L_1}{T_s}, \quad (28)$$

From (27) and (28), conventional deadbeat control can be considered as a specific PI control.

When the conventional control model is adopted in PI control, the average process does not exist, so $H(z) = 1$ and $D_2(z) = 1$ in Fig.7. In this case, the control period is equal to T_s; therefore, the control delay is T_s and PWM delay is $0.5T_s$, which means time delay of the system is $1.5T_s$. Hence, the open-loop transfer function $G_{open-PI}$ of PI control can be given by

$$G_{open-PI}(z) = D_{PI}(z)\cdot Z\left(e^{-s1.5T_s}\right)\cdot Z\left[G_{LCL}(s)\right], \quad (29)$$

To ensure the stability of the system, (21) needs to be satisfied according to the Nyquist stability criterion. When the system adopts the parameters shown in Table 1, (22) can be expressed as

$$\begin{cases} \varphi(f_1) = 90^\circ + \varphi_{PI} + \varphi\left(e^{-s1.5T_s}\right) \\ \in [-172.15^\circ, -82.15^\circ] \\ \varphi(f_2) = -90^\circ + \varphi_{PI} + \varphi\left(e^{-s1.5T_s}\right) \\ \in [-352.15^\circ, -262.15^\circ] \end{cases}, \quad (30)$$

where φ_{PI} is the phase of PI control, and $\varphi_{PI} \in$[−90°,0]. For conventional deadbeat control, (22) can be expressed as

$$\begin{cases} \varphi(f_1) = 90^\circ + \varphi_{DB} + \varphi\left(e^{-s1.5T_s}\right) = -82.15^\circ \\ \varphi(f_2) = -90^\circ + \varphi_{DB} + \varphi\left(e^{-s1.5T_s}\right) = -262.15^\circ \end{cases}, \quad (31)$$

where φ_{DB} is the phase of deadbeat control, deadbeat control has negligible influence on the phase characteristic.

From (30) and (31), the phase of $G_{open-PI}$ will cross $-180°$ around the resonance peak. Thus, the system is unstable when conventional PI control and deadbeat are applied.

In [21], sampling point shifting method is introduced to improve the phase characteristic of PI control. Generally, the default sampling point in PI control is set at the start of switching period to obtain the most computing resource of controller for control strategy. For time-delay reduction purpose, sampling point is typically shifted at the middle/end of switching period to avoid switching noise and maintain relatively small harmonics in the three-phase system. When the sampling point is shifted in the middle of switching period, the time delay of the system can be reduced to T_s, so (22) can be expressed as

$$\begin{cases} \varphi(f_1) = 90° + \varphi_{PI} + \varphi\left(e^{-sT_s}\right) \\ \in [-114.77°, -24.77°] \\ \varphi(f_2) = -90° + \varphi_{PI} + \varphi\left(e^{-sT_s}\right) \\ \in [-294.77°, -204.77°] \end{cases}, \tag{32}$$

At this point, the system is still unstable. When the sampling point is shifted at the end of switching period, the time delay of the system can be reduced to $0.5T_s$, then (22) can be rewritten as

$$\begin{cases} \varphi(f_1) = 90° + \varphi_{PI} + \varphi\left(e^{-s0.5T_s}\right) \\ \in [-57.38°, 32.62°] \\ \varphi(f_2) = -90° + \varphi_{PI} + \varphi\left(e^{-s0.5T_s}\right) \\ \in [-237.38°, -147.38°] \end{cases}, \tag{33}$$

From (33), with appropriate PI control parameters, the system can be stable with considerable phase margin in theory. However, because controller takes non-zero time to execute the control strategy, shifting sampling point at the end of switching period cannot be achieved in practical implementation. Consequently, the middle of the switching period is preferred for sampling point shifting in practical implementation. Thus, under the parameters in Table 1, PI control with sampling point shifting method cannot maintain system stability.

TABLE 1. Units for magnetic properties parameters of PCS.

Parameters	Value
Power Rating	500 kW
PCC line voltage (RMS)	400 V
Line frequency	50 Hz
DC-link voltage	600 V~850 V
Switching frequency	3 kHz
Converter-side inductor	100 μH
Filter capacitor	1200 μF
Grid-side inductor	30 μH
Resonance frequency	956 Hz

IV. SIMULATION AND EXPERIMENT RESULTS

The effectiveness and reliability of the PDBAM control method have been verified by simulation and experiment. The system parameters of the PCS are shown in Table 1, where the LCL filter design is based on reasonable resonance frequency according to (23), tolerable voltage drop across the inductors, and tolerable power factor decrease caused by the capacitor.

A. SIMULATION RESULTS

To verify the effectiveness and feasibility of the PDBAM control, a BESS was built in Matlab/Simulink, where the sampling frequency was 30 times the switching frequency.

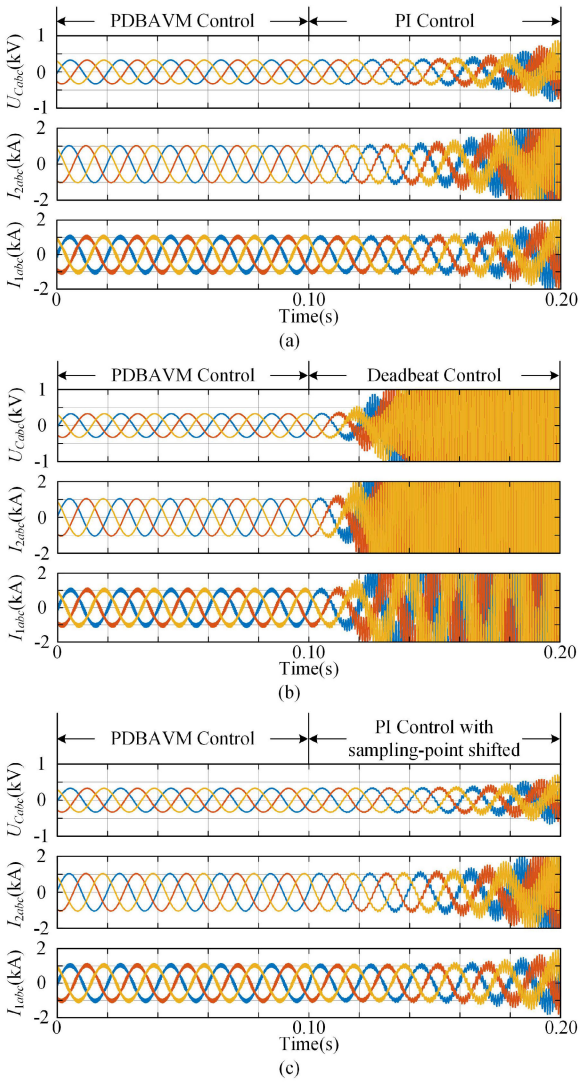

FIGURE 11. Simulation results of steady-state performance of the system under PDBAM control and (a) conventional PI control; (b) deadbeat control; (c) PI control with sampling point shifting in [21].

1) STABILITY

To verify the effectiveness of PDBAM control for the system's stability, the steady-state performance for PDBAM control and the existing control presented in section III.C,

including conventional PI control, deadbeat control, and PI control with sampling point shifting in [21], were compared, as shown in Fig.11. The PI parameters were tuned according to symmetrical optimum [33], [34], which can be given by $K_P = (L_1 + L_2)\cdot(3T_s)^{-1}$ and $K_I = 9T_s$. According to section III-C, sampling point was set in the middle of switching period.

From Fig.11, the system under PDBAM control operated stably, while the system suffered from resonance issues of *LCL* filter under PI control and deadbeat. By comparing the waveforms of the existing control, the resonance amplitude mainly depended on the gain of controller; the time-delay reduction provided by sampling point shifting could slightly alleviate resonance issues, but it was unable to maintain the stability of the system. Besides, the conventional deadbeat control was impractical because of serious resonance issues; to ensure the safety of the experiment, the conventional deadbeat control was only tested in Matlab/Simulink, but not in laboratory experiments.

It was clear that, to overcome LCL resonance, additional damping terms were necessary for PI control and deadbeat control, while PDBAM control was a better choice. Therefore, the PDBAM control effectively enhanced stability of the system.

2) BIDIRECTIONAL-POWER-FLOW CAPABILITY AND DYNAMIC PERFORMANCE

Bidirectional power flow was one of the essential functions of BESS. Generally, the grid codes required BESS to smoothly transition between inverter(discharging) mode and rectifier(charging) mode within 100 ms, which required high dynamic performance of the current control. In this section, the inverter/rectifier mode switching tests were simulated, as shown in Fig.12.

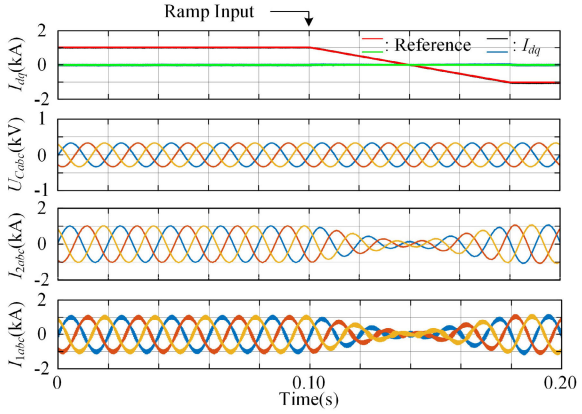

FIGURE 12. Simulation results of bidirectional-power-flow capability of the system.

For the sake of system security, ramp inputs were typically applied in the reverse process, as shown in Fig.12; the converter switched smoothly from inverter mode to rectifier mode under the ramp inputs of 1 pu to -1 pu during times 0.1∼0.18 s. The results showed that the output current tracked the reference quickly, and there was no overshoot or transient oscillation while the system remained stable in the dynamic process simultaneously.

Therefore, the simulation results confirmed the bidirectional-power-flow capability and dynamic performance of PDBAM control and further verified the effectiveness of PDBAM control for maintaining the system's stability in the dynamic processes.

3) ROBUSTNESS

In the practical BESS, the PCS was commonly connected to the grid through a series of transformers, and the uncertain leakage inductance of transformers was one of the main components of grid-side inductance, which depended on the grid conditions. The varying grid inductance affected the resonance frequency of the LCL filter and led to parameter mismatches in the control system, which further degraded the system's stability since the control algorithm was typically designed for the nominal parameters.

Assume actual grid inductance $L_2' = K_L \cdot L_2$, where K_L was the mismatch factor. So, (23) could be rewritten as

$$\sqrt{(L_1 + K_L L_2)\cdot(K_L L_1 L_2 C)^{-1}} < \frac{2\pi \cdot f_s}{3}. \tag{34}$$

According to the nominal parameters given in Table 1, the stable region for the mismatch factor could be given by

$$K_L > 0.892. \tag{35}$$

From (35), the worst case would happen when the actual grid inductance varied to the minimum value, and we should ensure that the minimum value of grid inductor was greater than 0.892 times the nominal value to ensure the stability of the system.

Related tests for grid inductance variation were simulated to verify the robustness of PDBAM control against grid inductance variation. Fig.13(a), (b), and (c) showed the output current waves of CCF loop(I_{1abc}) under different K_L of 0.9, 1.0, and 1.17, respectively, where the corresponding grid

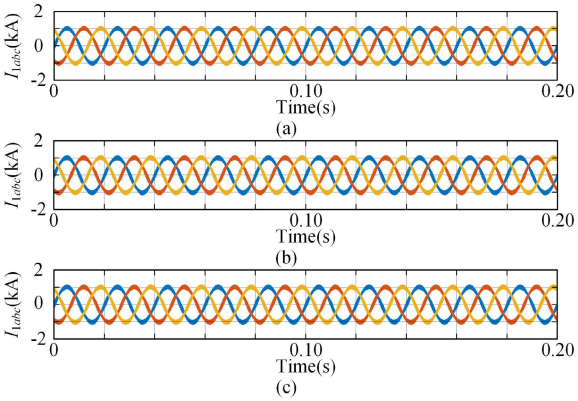

FIGURE 13. Simulation results of converter-side current under different grid inductance. (a) $L_2 = 27\ \mu$H. (b) $L_2 = 30\ \mu$H. (b) $L_2 = 35\mu$H.

inductance was 27 μH, 30 μH, and 35 μH respectively. Note that the stability of system under different mismatch factor K_L was analyzed in this section, and the corresponding harmonic performance of system would be analyzed in the section IV.B.3.

As shown in Fig.13(a), (b), and (c), the system operated stably under the different grid inductance(27 μH, 30 μH, and 35 μH, respectively) without resonance issues. Hence, the simulation results confirmed the robustness of PDBAM control and the effectiveness of the stable region derived in (23) and (35).

B. EXPERIMENTAL RESULTS

The proposed control method was verified in a 500kW PCS prototype. As shown in Fig.14, the prototype included a controller, three-phase bidirectional AC/DC converter, LC filter, variable inductors, and grid-connected transformer, where the grid-side inductance consisted of the inductance of variable inductors and the leakage inductance of transformer. The system parameters were given in Table 1.

IGBTs are selected as the switching devices of the prototype. A DSP(TMS320F28335) was used as the CPU of the prototype. The prototype used hall-effect current probes (ES1000C), and the bandwidth of probes, 100 kHz, is greater than the highest significant sine-wave-frequency component in the waveform's spectrum. Sampling is achieved via direct memory access(DMA) in conjunction with the analog-to-digital converter(ADC) built into the DSP, which does not require the CPU to participate in control transfer, thereby significantly improving the utilization efficiency of the CPU. The DMA allows the ADC sampling frequency to be set to 30 times the switching frequency($n = 30$), effectively supporting the proposed control.

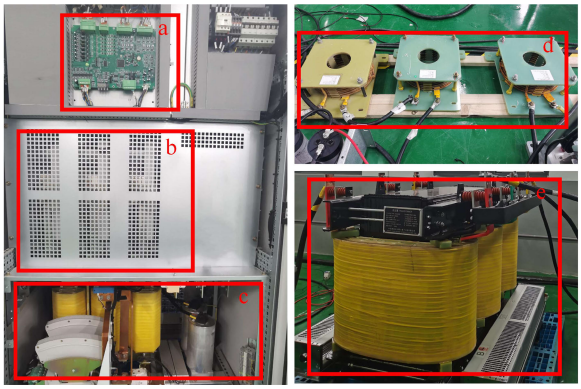

FIGURE 14. Experimental prototype. (a) Controller. (b) Three-phase bidirectional AC/DC converter. (c) LC Filter. (d) Variable inductors. (e) Grid-connected transformer.

1) STABILITY

Fig.15(a) confirmed the stability of PCS under PDBAM control.

From Fig.15(b) and (c), compared with conventional PI control and PI control with sampling point shifting in [21],

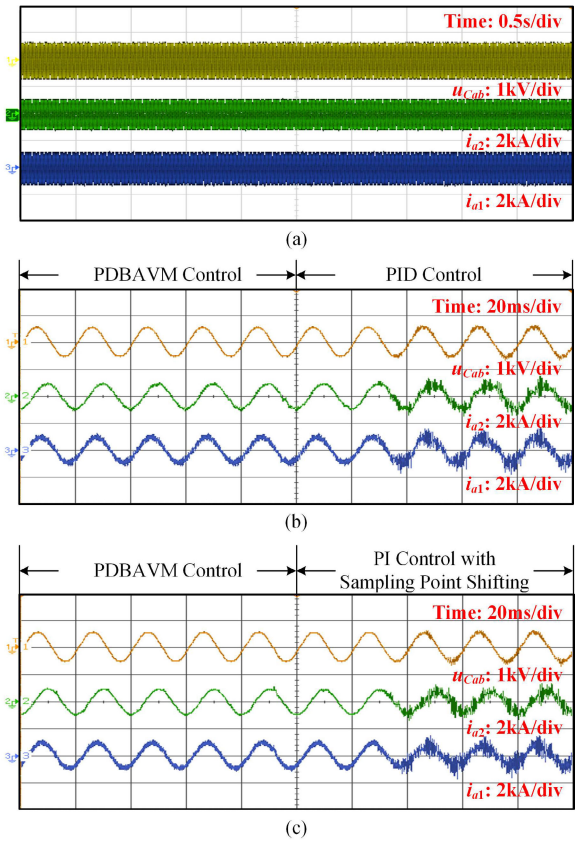

FIGURE 15. Experimental results of steady-state performance of the system under (a)PDBAM control, (b) compared with conventional PI control, and (c) PI control with sampling point shifting in [21].

PDBAM control could ensure the stable operation of PCS without introducing additional passive or active damping methods. The PDBAM control overcame the resonance issue caused by LCL filter, enhancing the system's stability.

2) BIDIRECTIONAL-POWER-FLOW CAPABILITY AND DYNAMIC PERFORMANCE

Fig.16 confirmed the bidirectional-power-flow capability and dynamic performance of PCS under PDBAM control. The system switched from the rated discharging state to the rated charging state, and the reference was the same as the ramp inputs in Section IV.A.2. From Fig.16, the captured results showed that the output could track the reference stably within

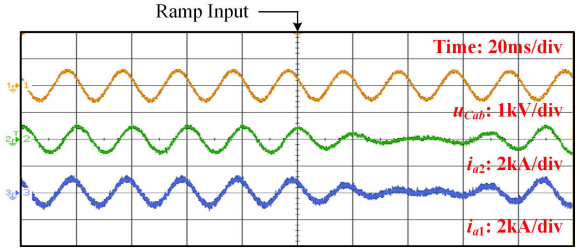

FIGURE 16. Experimental results of bidirectional-power-flow capability of the system.

100 ms, and there is no transient oscillation in the dynamic process. Therefore, the bidirectional-power-flow capability and dynamic performance of the PCS complied with the grid code.

3) ROBUSTNESS

Fig.17, Fig.18, and Fig.19 confirmed the robustness of PDBAM control against grid inductance variation. In this experiment, the grid inductance variation was implemented by adjusting the variable inductors. Refer to section IV-A.3, under the different grid-side inductance of 27 μH, 30 μH, and 35 μH, respectively, the corresponding resonant frequency of the LCL filter was 996 Hz, 956 Hz, and 902 Hz, respectively. From Fig.17(a), Fig.18(a), and Fig.19(a), the output current I_2 of PCS remained stable under the variable grid inductance. From Fig.17(b), Fig.18(b), and Fig.19(b), harmonic components of I_2 under the different grid inductance could be classified into two parts, one related to switching frequency (3 kHz) and the other related to resonant frequency. The different grid inductances directly affected the distributions of harmonic components related to resonant frequency. At the same time, grid inductors with higher inductance provided better total harmonic distortion(THD) performance of the output current.

The experimental results verified the effectiveness of the stable region derived in (23) and (35) and the robustness of PDBAM control.

In brief, the experimental results were consistent with the simulation results. Simulation results and experimental results verified the effectiveness and reliability of the proposed PDBAM control method.

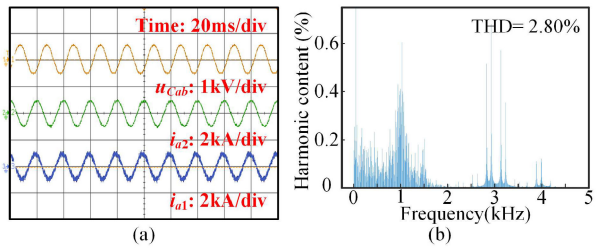

FIGURE 17. Experimental results of robustness with $L_2 = 27$ μH. (a) Waveforms. (b) Harmonic content of the grid-side current.

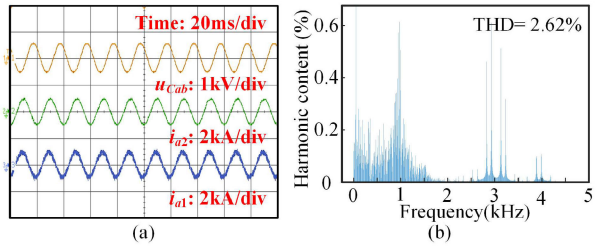

FIGURE 18. Experimental results of robustness with $L_2 = 30$ μH. (a) Waveforms. (b) Harmonic content of the grid-side current.

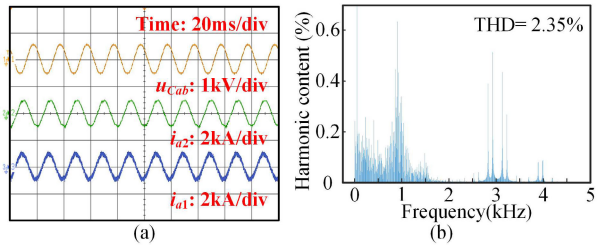

FIGURE 19. Experimental results of robustness with $L_2 = 35$ μH. (a) Waveforms. (b) Harmonic content of the grid-side current.

V. CONCLUSION

This study establishes a deadbeat average model(DBAM) for the CCF loop and develops a predictive deadbeat average model(PDBAM) control method for the PCS with *LCL* filter., which is taken as the research carrier in this paper. The proposed PDBAM control method has the following advantages:

1) Using the oversampling technique, we developed a DBAM for the CCF loop with a clear physical meaning, ingeniously transforming conventional single-point sampling control into multi-point average control, which can describe the actual plants accurately.

2) By incorporating predictive control combined with double-updated PWM method, the time delay of the CCF loop was minimized, which overcame the resonance issue of the LCL filters and improved the system's stability.

3) The stable region of the PDBAM control method was deduced, which provides guidelines for the system parameter configuration of the PCS.

APPENDIX A

Table 2. presents comparisons of control model, control effect, and features according to [21], [23], and [25] and the proposed method.

APPENDIX B

If a sufficient number of samples is available, the left-hand side of (7) can be rewritten as

$$\frac{1}{n}\sum_{m=0}^{n} L_1\left[\mathbf{i}_{1m}\left(k+1\right)-\mathbf{i}_{1m}\left(k\right)\right]=\frac{L_1}{T_s}\left[\mathbf{I}_1\left(k+1\right)-\mathbf{I}_1\left(k\right)\right], \tag{B1}$$

where $\mathbf{I}$ is the average current array in a control period.

The summation of $\mathbf{u}_C$ on the right-hand side of (7) can be rewritten as

$$\frac{1}{n}\sum_{m=0}^{n}\int_{(k+\frac{m}{n})T_s}^{(k+1+\frac{m}{n})T_s}\mathbf{u}_{Cm}\left(t\right)dt=\frac{\mathbf{U}_C\left(k+1\right)+\mathbf{U}_C\left(k\right)}{2}, \tag{B2}$$

where $\mathbf{U}_C$ is the average voltage array in a control period.

The summation of $\mathbf{v}$ on the right-hand side of (7) can be reconstructed by

$$\frac{1}{n}\sum_{m=0}^{n}\int_{(k+\frac{m}{n})T_s}^{(k+1+\frac{m}{n})T_s}\mathbf{v}_m\left(t\right)dt=\frac{1}{n}\sum_{m=0}^{n}V_{dc}\cdot\mathbf{D}_m, \tag{B3}$$

TABLE 2. Comparison of several time-delay elimination methods.

Literature	Time-delay elimination method	Control model	Control effect	Features
[21]	Sampling point shifting method	Regular-sampling-based model	Adjusted time-delay reduction(up to control delay)	Noise-sensitive; Limited by computing resources and sampling aliasing.
[23]	Improved deadbeat control	Regular-sampling-based model	Time-delay compensation for integer multiples of the control period	Model-based; Noise-sensitive.
[25]	Improved linear predictor	Regular-sampling-based model	Time-delay compensation for the control period(verified in [25])	Model-free; Parameter tuning is required for prediction accuracy and system stability.
This paper	Deadbeat control combined with multi-updated PWM	Oversampling-based model	Time-delay compensation for control delay and PWM delay.	Model-based; With enhanced anti-interference; Applying average states control;

From Fig.2, $\mathbf{S}_m$ and $\mathbf{D}_m$ will vary according to the position of the mth sampling point. When $d_a(k) < d_a(k+1)$, d_{am} can be expressed as

$$d_{am} = \begin{cases} d_a(k), 0 < \dfrac{m_s}{n} < \dfrac{1-d_a(k+1)}{2} \\ \dfrac{1+d_a(k)}{2} - \dfrac{m}{n}, \dfrac{1-d_a(k)}{2} < \dfrac{m_s}{n} < \dfrac{1-d_a(k+1)}{2} \\ \dfrac{d_a(k)+d_a(k+1)}{2}, \dfrac{1-d_a(k+1)}{2} < \dfrac{m}{n} < \dfrac{1+d_a(k)}{2} \\ d_a(k+1) + \dfrac{1-d_a(k)}{2} - \dfrac{m}{n}, \dfrac{1+d_a(k)}{2} < \dfrac{m}{n} \\ < \dfrac{1+d_a(k+1)}{2} \\ d_a(k+1), \dfrac{1+d_a(k+1)}{2} < \dfrac{m}{n} < 1 \end{cases} \tag{B4}$$

The values of d_{am} can also be derived using the same method for $d_a(k) \geq d_a(k+1)$. The summation of d_a can be given by

$$\frac{1}{n}\sum_{m=0}^{n} d_{am} = \frac{d_a(k)+d_a(k+1)}{2}. \tag{B5}$$

Due to the superimposability of the circuit states, the derivation in (B5) is valid for the effect of **S/D** on $\mathbf{i}_1$. So, the summation of $\mathbf{v}$ can be obtained as

$$\begin{aligned} \frac{1}{n}\sum_{m=0}^{n} V_{dc}\cdot\mathbf{D}_m &= V_{dc}\frac{\mathbf{D}(k)+\mathbf{D}(k+1)}{2} \\ &= \frac{\mathbf{V}(k+1)+\mathbf{V}(k)}{2}. \end{aligned} \tag{B6}$$

If a sufficient number of samples is available, the right-hand side of (7) can be rewritten as

$$\begin{aligned} &\frac{1}{n}\sum_{m=0}^{n}\int_{(k+\frac{m}{n})T_s}^{(k+1+\frac{m}{n})T_s} [\mathbf{v}_m(t) - \mathbf{u}_{Cm}(t)]\,dt \\ &= \frac{\mathbf{V}(k+1)+\mathbf{V}(k)}{2} - \frac{\mathbf{U}_C(k+1)+\mathbf{U}_C(k)}{2}. \end{aligned} \tag{B7}$$

Thus, from (B1) and (B7), (7) can be simplified as

$$\begin{aligned} \frac{L_1}{T_s}[\mathbf{I}_1(k+1) - \mathbf{I}_1(k)] &= \frac{\mathbf{V}(k+1)+\mathbf{V}(k)}{2} \\ &- \frac{\mathbf{U}_C(k+1)+\mathbf{U}_C(k)}{2}. \end{aligned} \tag{B8}$$

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