

Received 8 November 2023, accepted 2 December 2023, date of publication 5 December 2023, date of current version 13 December 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3340023

RESEARCH ARTICLE

275 GHz Quadrature Receivers for THz-Band 6G Indoor Network in 130-nm SiGe Technology

JEONG-MOON SONG¹, (Student Member, IEEE), VAN-SON TRINH¹, (Member, IEEE), SOOYEON KIM², (Member, IEEE), AND JUNG-DONG PARK¹, (Senior Member, IEEE)

¹Division of Electronics and Electrical Engineering, Dongguk University, Seoul 04620, Republic of Korea

²Electronics and Telecommunications Research Institute, Daejeon 34129, Republic of Korea

Corresponding author: Jung-Dong Park (jdpark@dongguk.edu)

This work was supported by the Electronics and Telecommunications Research Institute (ETRI) through the Korean Government, Study on 3-D Communication Technology for Hyper-Connectivity under Grant 23ZH1100.

ABSTRACT We report two 275-GHz quadrature receivers (Rx's) with mixer-first and LNA-first architectures in a 130-nm SiGe BiCMOS process. Both quadrature Rx's contain I and Q mixers implemented with a modified Gilbert-cell mixer with swapped RF and local oscillation (LO) ports to downconvert the RF signal at 260–290 GHz to the I and Q intermediate frequency (IF) bands at 0.1–30GHz. For a cost-effective solution, a compact 260GHz quadrature LO chain is integrated with a compact frequency tripler with an E-band driving amplifier (DA), a 260-GHz DA, and a differential hybrid coupler to generate the quadrature LO signals for I and Q mixers. Comprised of a push-push doubler cascaded with a single-balanced mixer, the frequency tripler was employed to isolate the LO harmonic leakages from the IF band. A wideband IF amplifier was used for an aimed conversion gain higher than 20 dB in each channel. In the measurement, the implemented mixer-first and LNA-first Rx's achieved a minimum single-sideband (SSB) noise figure (NF) of 22.3 and 21 dB, a peak gain of 21.4 and 27.5 dB with an IF bandwidth of 30 GHz. The amplitude and phase imbalances between the I and Q channels of the mixer-first Rx were measured around 1 dB and 4°. The fabricated mixer-first and LNA-first chips occupy a whole area of 1.418 and 2.030 mm², and consume a DC power of 434 and 490 mW, respectively.

INDEX TERMS 6G, IQ receiver, SiGe, terahertz.

I. INTRODUCTION

The sub-terahertz band is considered a promising solution for the 6th generation wireless communication networks (6G), applicable in various sectors such as ultra-high-definition video transmission, seamless remote robotic control, automatic production, and surgical video transmission. During the 2019 World Radiocommunication Conference (WRC-19), the 300 GHz band (275-296 GHz) was allocated for land mobile and fixed services. Along with the IEEE Standard 802.15.3d which defines the physical layer around 300 GHz, these allocations have significantly influenced the development of various Terahertz (THz) transceivers [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], standalone transmitters [14], [15], and receiver designs [16], [17], [18], [19],

The associate editor coordinating the review of this manuscript and approving it for publication was Mauro Fadda¹.

[20], [21] within this frequency range. Wireless communication links have proposed achieving data transmission speeds of over 100 Gb/s using SiGe technology [5], [7], [8], [9] while CMOS transceivers achieved data rates of 80 Gb/s by employing double-rate techniques to increase the operating frequency [6].

Recently, sub-THz transceivers at the 300GHz band also present a potential solution for the optical-to-electronic interface of future indoor wireline networks [1], [2]. The proposed 6G indoor wireline network presents a high operating bandwidth interface utilizing analog radio-over-fiber (RoF) technology to fully exploit the advantages of sub-terahertz frequencies. To support a cost-effective THz receiver solution for a recently proposed 6G indoor wireline network, our work presents integrated 275GHz quadrature receivers in 130nm SiGe BiCMOS technology which offers a nominal f_T/f_{max} of 350/450 GHz.

Two receiver architectures have been implemented, one is the mixer-first, and the other is the low noise amplifier (LNA)-first receiver. The designed SiGe THz receivers downconvert the target RF signal (260-290 GHz) to the intermediate frequency (IF) band (0-30 GHz) in two orthogonal I and Q channels. To achieve an efficient quadrature local oscillation (LO) generation at 260 GHz, a differential branchline coupler, a 260 GHz driving amplifier (DA), and a frequency tripler combined with an E-band DA were integrated as the LO chain with a compact form factor in the quadrature receiver chips.

The remaining parts of this paper are structured as follows: Section II describes detailed designs of the core blocks in the integrated sub-Terahertz receiver. In Section III, experimental results are presented which demonstrate the validity of the implemented THz receivers, followed by the conclusion in Section IV.

II. 260GHz INTEGRATED RECEIVERS

The block diagram of the proposed sub-THz quadrature receivers is presented in Fig. 1. The mixer-first architecture with a fundamental LO driver can improve the conversion gain and NF of the receiver chain owing to the enhanced mixer performance under the limited RF performance ($f_{RF} > f_{max}/2$) of the active device [21]. Alternatively, placing a low-noise amplifier (LNA) at the beginning of the receiver chain, followed by mixers, can improve the NF and obtain a higher signal-to-noise ratio (SNR), enabling higher data transmission rates [19].

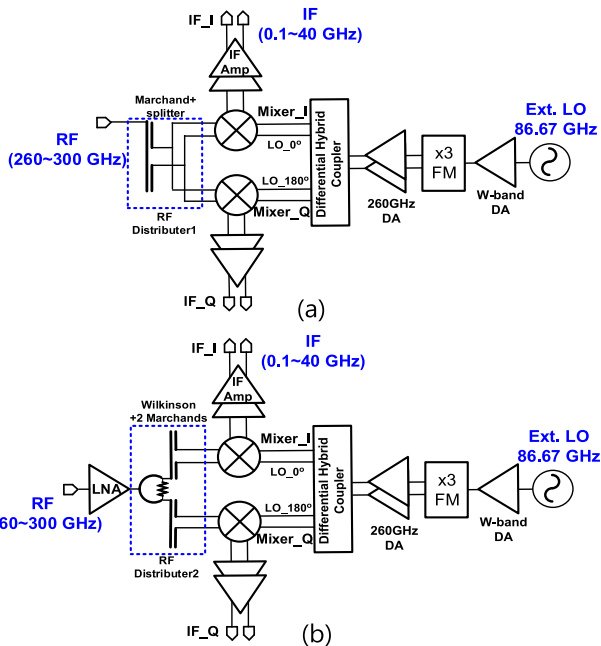


FIGURE 1. Block diagram of the mixer-first quadrature receiver (Rx1) (a) and the LNA-first quadrature receiver (Rx2).

In this work, both receivers are designed to down-convert a modulated signal (260~290 GHz) from a single-ended

RF input port into I and Q IF signals (0.1~30GHz) with a differential output. While the mixer-first receiver (Rx1) converts the single-ended signal into the differential one and distributes it directly to the RF ports of the I and Q mixers with RF Distributer1 using a single Marchand balun followed by a power splitter, the RF input signal of the LNA-first receiver (Rx2) is amplified first by the 275 GHz LNA. Then, the amplified RF signal is evenly distributed to the RFports of the I and Q mixers using the RF Distributer2 with a Wilkinson power divider followed by two Marchand baluns. A compact quadrature LO chain is integrated into the receivers for a cost-effective design. The 275 GHz RF signal is mixed with 260 GHz LO signals at I and Q mixers, generating I and Q IF signals. The down-converted IF signals are amplified by the wide-band IF amplifiers to drive external DSP blocks.

The integrated LO chain takes an 86.67 GHz sinusoidal signal from the external signal generator and provides a 260 GHz quadrature signal to the LO ports of the I and Q mixers. The 260GHz LO chain consists of the frequency tripler combined with an E-band driving amplifier (DA), and two single-ended 260GHz DAs to provide the required LO power to the mixers. The quadrature signals are generated by the differential hybrid coupler at the end of the LO chain.

A. 275 GHz LOW NOISE AMPLIFIER

A 275 GHz low noise amplifier (LNA) is employed at the front end to maximize gain and bandwidth improvement for noise figure (NF) enhancement in the receiver. Figure 2 shows the schematic of the designed LNA. The LNA is composed of six unit cells, each consisting of a common-emitter amplifier, cascaded to achieve the desired gain. Impedance matching in each stage is accomplished using microstrip transmission lines (MSTLs) and series-matching capacitors. The simulated S-parameters of the LNA are shown in Fig. 3. The designed 275 GHz LNA achieves a maximum gain of 8 dB, a 3 dB gain bandwidth of 56GHz (245~301 GHz), and the NF between 14.2 dB and 16.5 dB in simulation. It is noteworthy that the output of the LNA does not include the matching network. Instead, the input impedance of the RF distributor was designed close to the conjugate of the LNA output. Thus, the resulting return loss between LNA output and RF distributor input is better than 10 dB. Figure 4 presents the simulated large-signal results of the designed six-stage LNA and it shows an input third-order intercept point (IIP3) of 14.22 dBm with 31.6 mA of DC current consumption at 1.6 V supply.

B. RF SIGNAL DISTRIBUTOR

To provide a differential RF signal to I and Q mixers of the mixer-first receiver (Rx1), a compact-size RF distributor using a Marchand balun followed by an RF power divider was employed [21]. The simulated insertion loss is around 2 dB while the isolation between I and Q RF ports is about 11dB at 275 GHz. For the LNA first receiver (Rx2), a new RF signal distributor was implemented using a Wilkinson divider

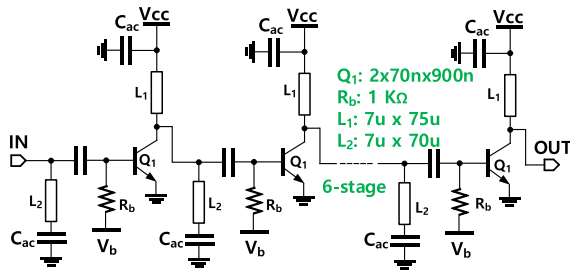


FIGURE 2. Schematic of the 275 GHz LNA.

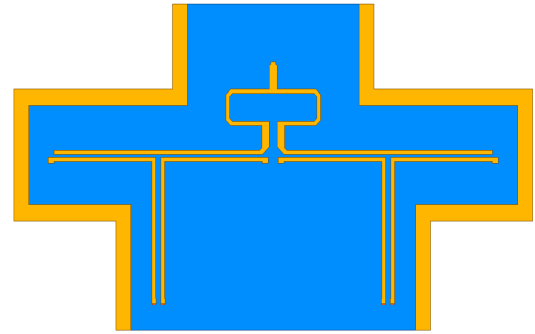


FIGURE 5. 3-D structures of the 275GHz RF signal distributor.

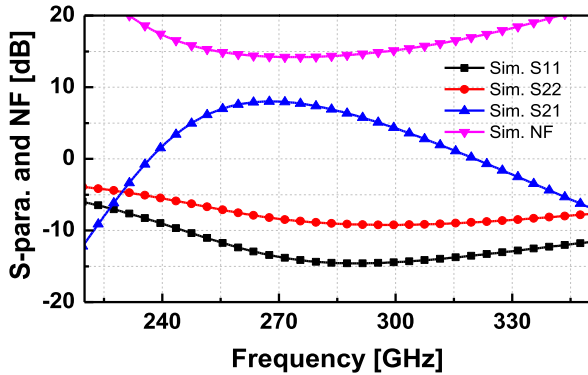


FIGURE 3. Simulated S-parameters and noise figure (NF) of the designed 275 GHz LNA.

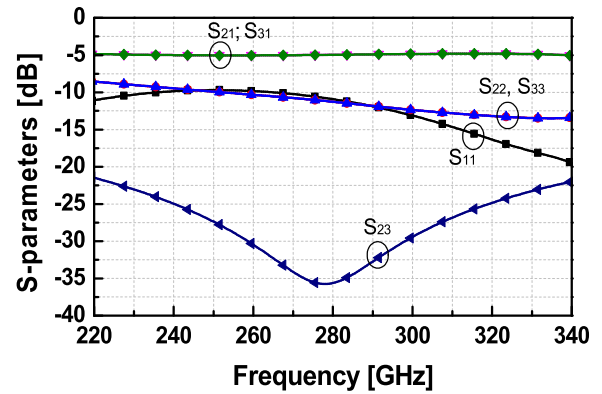


FIGURE 6. Simulated S-parameters of the designed RF signal distributor.

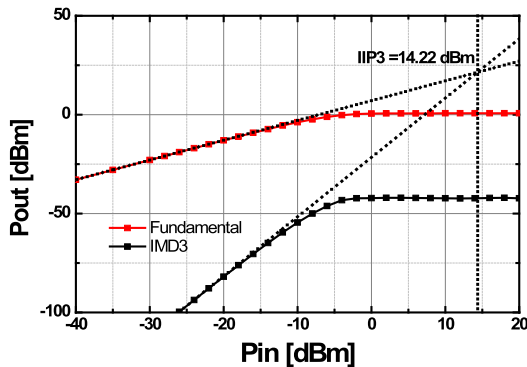


FIGURE 4. Simulated large signal result of designed 275GHz LNA.

followed by two Marchand baluns to achieve improved isolation between I and Q RF ports in trade-off with the area occupancy. Figure 5 shows the 3D electromagnetic (EM) model of the RF signal distributor implemented in HFSS. The realized RF signal distributor of the Rx2 achieves an intrinsic insertion loss of less than 2 dB between 260 GHz and 300 GHz with a return loss better than 10 dB at the input and output ports. The isolation between the I and Q RF ports is larger than 25 dB as shown in Fig.6.

C. DOWN CONVERSION MIXER

To achieve broad bandwidth performance, improved operational efficiency, and enhanced isolation between the LO and RF signals, an active double-balanced mixer structure

was chosen for the frequency down-conversion mixer in the quadrature receiver. The receivers utilize a modified Gilbert-cell mixer as I and Q mixers to improve the noise figure (NF) and the conversion gain by avoiding the effects of the parasitic capacitances at the common nodes [21]. The output current of the BJT-based Gilbert cell is given by

$$\Delta I = I_{tail} \left[\tanh \left(\frac{V_{RF}}{2V_T} \right) \right] \left[\tanh \left(\frac{V_{LO}}{2V_T} \right) \right] \quad (1)$$

Thus, there is no theoretical difference in the conversion gain by swapping RF and LO ports in the mixed output current. In this design, a Gilbert-cell mixer with swapped LO and RF ports was introduced to achieve better NF performance than the conventional one. As shown in Fig.6, the Gilbert-cell mixer with swapped LO and RF ports does not see C_p at the common node as each differential pair connected with RF+/RF- is fully activated in differential mode during each half cycle of the LO signal. Thus, it does not suffer from the gain degradation from C_p . In contrast, the gain degradation of the conventional Gilbert-cell mixer caused by C_p at the common emitter node is estimated by

$$\frac{A_{v_conv}}{A_{v_swap}} = \frac{g_{m1,2}}{\sqrt{\omega^2 C_p^2 + g_{m1,2}^2}} \quad (2)$$

Thus, the input-referred noise of the proposed mixer must be less degraded as frequency increases for a given C_p at the

emitter node of the differential pair owing to the complete differential operation during each half period of LO.

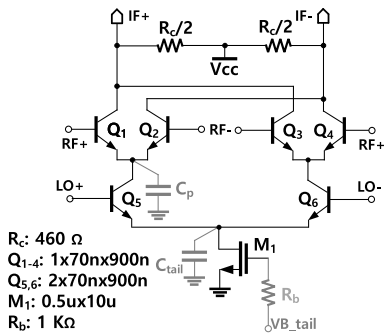


FIGURE 7. Schematic of the modified Gilbert-cell mixer [21].

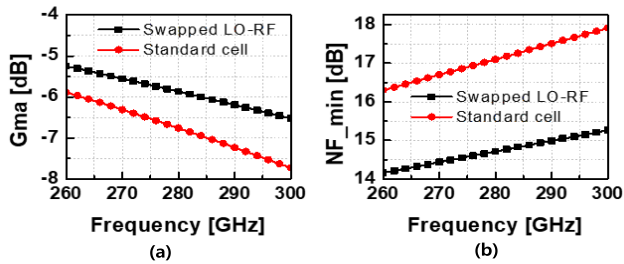


FIGURE 8. Simulated (a) G_{ma} and (b) minimum NF (NF_{min}) of the standard Gilbert-cell mixer and the modified version with swapped RF-LO ports at $P_{LO} = 0$ dBm.

Figure 7 illustrates the schematic of the designed frequency down-conversion mixer. The modified Gilbert-cell mixer with the absence of the input impedance matching inductor at the RF port was compared with a conventional Gilbert-cell mixer to observe the maximum available gain (G_{ma}) and minimum NF (NF_{min}) of each mixer with $P_{LO} = 0$ dBm as presented in Fig. 8. In the simulation, the swapped mixer achieved around 2.3-dB less NF and 0.8-dB more gain than the values of the conventional mixer.

D. BROADBAND IF AMPLIFIER

Figure 9 depicts the schematics of the designed broadband IF amplifier (IF AMP). To achieve a wideband operation, we employed the inductive peaking technique. Inductors and resistors were serially connected to serve as a wideband load. In this design, spiral inductors were used to provide relatively large inductance to compensate for parasitic capacitance while keeping a small physical size with a low quality(Q) factor.

To achieve broadband characteristics, a staggered matching technique was also applied by adjusting the resistance values of the load in each stage to slightly offset the center frequencies of the peaking load at each stage. Figure 10 shows the simulated voltage gain, output reflection coefficient(Γ_{out}), and group delay of the IF AMP. The peak gain of IF AMP is 35 dB at 40 GHz. It is noteworthy that the

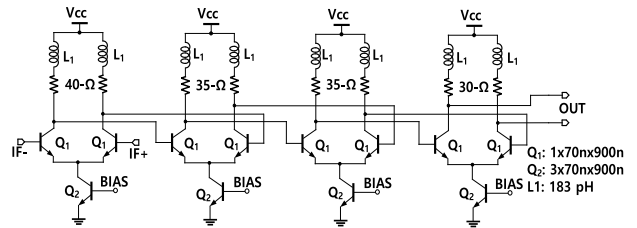


FIGURE 9. Schematic of the broadband IF amplifier.

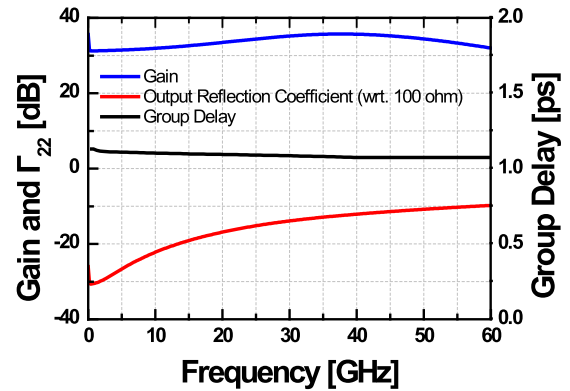


FIGURE 10. Simulated voltage gain, output reflection coefficient (Γ_{out}), and the group delay of the broadband IF AMP under the down-conversion operation with the co-designed mixer ($f_{LO} = 259$ GHz).

IF AMP was co-designed to provide lower gain in the lower frequency range to compensate for the gain variation with the IF band considering the conversion gain of the mixer is relatively higher in the lower frequency band. The simulated result shows about 4% of the group delay variation between 1GHz and 40GHz of the IF band. Figure 11 presents the simulated large signal characteristic of the designed broadband IF amplifier with the conjugate-matched source at 25 GHz. The 1 dB compression point ($OP1dB$) of the IF amplifier is about -12.3 dBm. The designed IF amplifier consumes $I_{cc} = 40$ mA with $V_b = 1$ V and $V_{cc} = 2.3$ V.

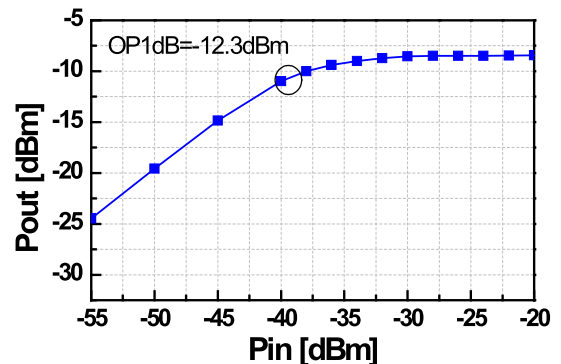


FIGURE 11. Simulated output power (P_{out}) versus input power (P_{in}) of the IF AMP with the conjugate-matched source at 25-GHz.

E. 260GHz QUADRATURE LO CHAIN

To demonstrate a cost-effective quadrature receiver solution, we integrated an LO chain in each receiver chip. Figure 12 illustrates the configuration of the LO chain. The E-band

sinusoidal signal (86.67 GHz) from an external signal generator is converted to a 260 GHz signal using a frequency tripler.

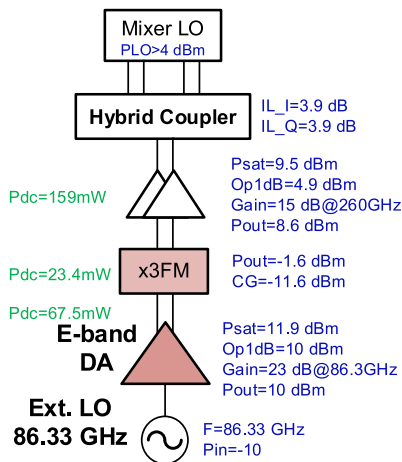


FIGURE 12. Power budget of the designed 260GHz LO chain.

A differential hybrid coupler is used to produce the in-phase (I) and quadrature (Q) LO signals for the down-conversion of the double-balanced mixers with an insertion loss of less than 1 dB. A 260 GHz DA provides around +4.7 dBm of LO power to the LO ports of the I and Q double-balanced mixers. The designed frequency tripler consists of a push-push doubler (PPD) followed by a single-balanced mixer as presented in Fig. 13. An E-band push-pull driving amplifier (DA) was co-designed to drive the PPD and the single-ended mixer simultaneously using a relatively small LO input power (~ -10 dBm). Under the bias condition of $V_{cc2} = 2.6$ V and $V_{b2} = 1.7$ V, it consumes $I_{cc2} = 9$ mA and $I_{b2} = 17.3$ uA. Since we employed the tripler in the LO chain with an input frequency of 86.67GHz, unwanted harmonic leakages from the LO chain may not contaminate the IF band (0-30GHz).

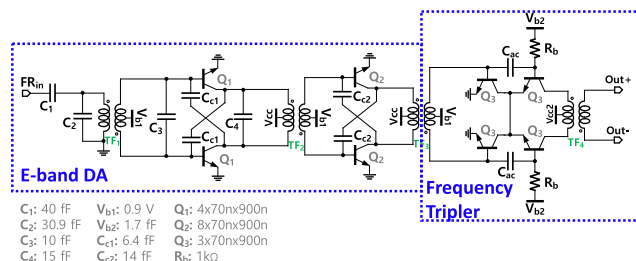


FIGURE 13. Schematic of the E-band DA cascaded with the tripler.

The peak gain of the E-band DA is 26.2 dB at 80 GHz. The OP1dB of the E-band DA at 86.6 GHz is 11.3 dBm, achieving a maximum output power of 12.3 dBm and a maximum power-added efficiency of 19.5%. The designed E-band DA consumes a DC of 42.2 mA at $V_{bb1} = 0.9$ V and $V_{cc1} = 1.6$ V supply. The integrated harmonic balance

(HB) simulation results of the frequency tripler with E-band DA are shown in Fig. 14. The tripler generates a differential signal of -1.7 dBm (-4.7 dBm in each single-ended output) at 260 GHz from -10 dBm input power of the E-band signal source at 86.67 GHz.

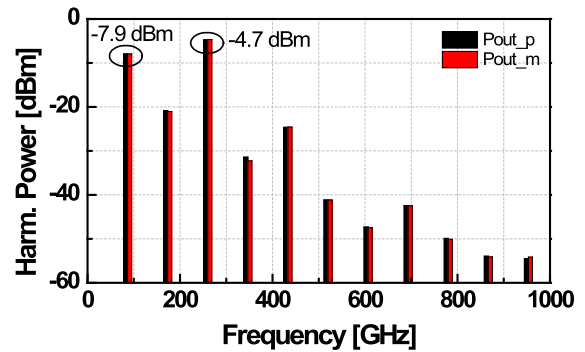


FIGURE 14. HB simulation results of the the frequency tripler combined with the E-band driving amplifier.

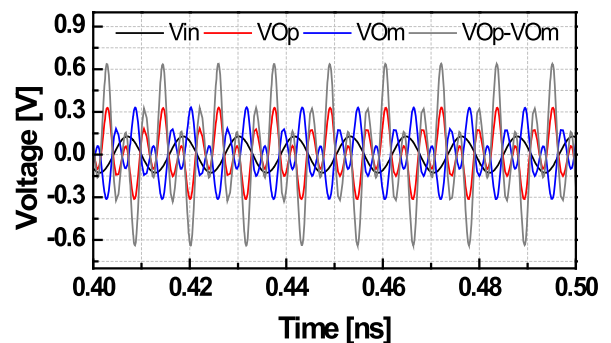


FIGURE 15. Transient simulation results of the frequency tripler combined with the E-band driving amplifier.

Figure 15 illustrates the transient simulation results of the tripler combined with the E-band DA. Two 260GHz DAs are used for a wanted LO power generation to drive the balanced hybrid coupler. The schematic of the designed 260 GHz DA is shown in Fig. 16. The final stage of the DA utilizes a larger HBT compared with the preceding stages. The schematic configuration of the LO DA is identical to the 275GHz LNA, composed of the cascaded 10-unit cells to provide the optimal LO power level from the external E-band signal. Operating in the wide range of 240-270 GHz, the DA exhibits a good gain characteristic, allowing it to operate at different LO frequencies in case the down-converted IF signal is within the IF band (0-30GHz).

The simulation results of the S-parameters of the 260 GHz DA are presented in Fig. 17. The peak gain of the 260 GHz DA in the LO chain is 18 dB at 240 GHz. Figure 18 shows the large signal simulation results of the 260 GHz DA. The simulated OP1dB of DA is approximately +4.3 dBm at 260 GHz with a DC current consumption of 99.3 mA at $V_{bb} = 0.93$ V and $V_{cc} = 1.6$ V supply. The simulation results of output power versus frequency of the 260 GHz DA are given in

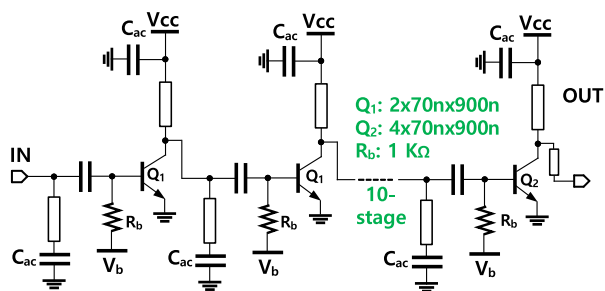


FIGURE 16. Schematic of 260GHz DA in the LO chain.

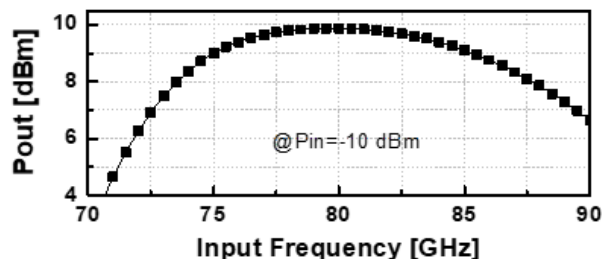


FIGURE 19. Simulated P_{out} of the 260GHz DA versus W-band input frequency of the 260GHz LO chain.

Fig. 19. The designed DA exhibits a gain of over 10 dB in the 214–282 GHz range. The LO chain can provide 4.7 dBm of quadrature LO signals to the LO ports of each mixer when the input LO signal is -10 dBm at 86.67GHz. \

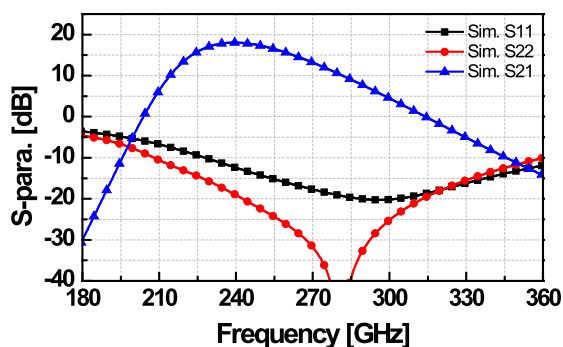


FIGURE 17. Simulated S-Parameters of the 260GHz DA.

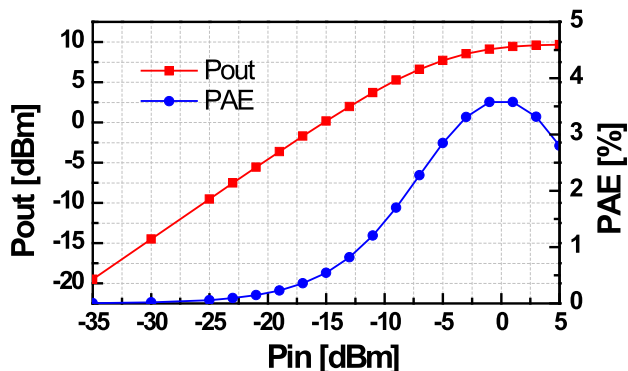
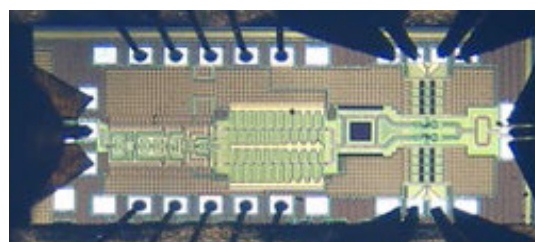


FIGURE 18. Simulated output power (P_{out}) and PAE of the 260GHz Driving Amplifier versus input power (P_{in}) at 260 GHz.

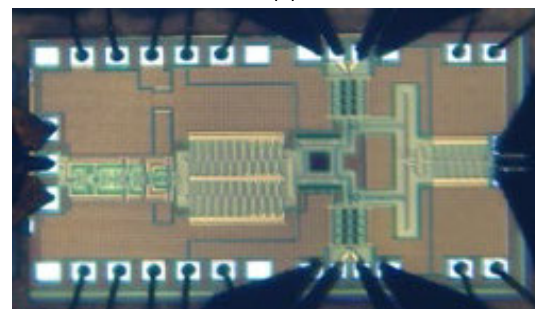
III. MEASUREMENTS RESULTS

Figure 20 shows the chip photograph of the implemented sub-THz receiver. The implemented mixer-first receiver (Rx1) consumes a DC power of 438 mW while the LNA-first receiver (Rx2) dissipates 490 mW in the measurements. The power gain of the implemented receivers was measured using a continuous-wave (CW) measurement setup. Figure 21 illustrates the setup for the gain measurements of the receiver. The RF signal was generated from the up-conversion mixer (VDI

SGX 3.4), while the 86.67GHz of the LO signal was provided from the external frequency multiplier and the signal generator (Agilent 83623B). The output power of the RF and LO signals was characterized using the Erickson power meter (VDI PM-5).



(a)



(b)

FIGURE 20. Chip photographs of the integrated 275GHz quadrature receivers under the measurements: (a) Mixer-first Rx (chip size: 1842 $\mu\text{m} \times 770 \mu\text{m}$) (b) and LNA-first Rx (chip size: 2010 $\mu\text{m} \times 1010 \mu\text{m}$).

The down-converted IF signal was measured using a spectrum analyzer (Agilent E4407B). The connection losses at IF and RF were measured and calibrated to measure the receiver gain. The simulated and measured conversion gains of the I/Q channels for the implemented receivers (Rx1 and Rx2) are shown in Fig. 22. In the measurements, both Rx1 and Rx2 exhibited a conversion gain similar to the simulations and achieved 1dB and 0.7dB of gain errors between I and Q channels for Rx1 and Rx2, respectively. The Rx1 achieved a peak gain of 21.4 dB with a bandwidth of 30 GHz, and the gain variation was within 3.1 dB of its peak value up to 290 GHz. The Rx2 achieved a peak gain of 27.5 dB and exhibited gain variations of 2.8 dB in the same bandwidth.

TABLE 1. Comparison with previously reported sub-THz receivers.

Ref.	This work		[3]	[4]	[5]	[6]	[16]	[17]
	Rx1	Rx2						
Tech	130nm SiGe	130nm SiGe	130nm SiGe HBT	130nm SiGe bi_CMOS	130nm SiGe	40nm CMOS	40nm CMOS	65nm CMOS
Frequency (GHz)	275	275	240	240	230	265	290	240
Conversion Gain (dB)	21.4	27.5	28	10.5	8	-	-19	25
IF BW (GHz)	30*(40**)	30*(40**)	13	17	26	20	26.5	14 [†]
SSB NF (dB)	22.3	20.1	15	15	14	22.9 (mean over 20GHz)	27	15
P _{DC} (mW)	438	490	-	866	450	897	650	260
Chip size	Rx : 1.418mm ²	Rx : 2.030mm ²	Rx : 1.522mm ²	Rx : 1.568mm ²	-	TRX : 11.05mm ²	RX : 3.15mm ²	RX : 2mm ²

*MEASURED BANDWIDTH **ESTIMATED BANDWIDTH [†]DOUBLE SIDE BAND

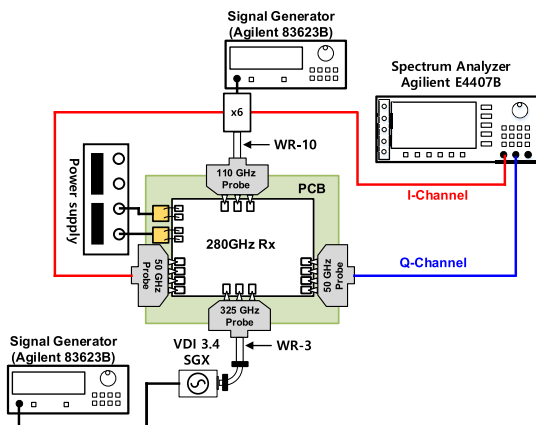


FIGURE 21. Measurement setup for gain measurement of the 275GHz receiver with continuous wave signals.

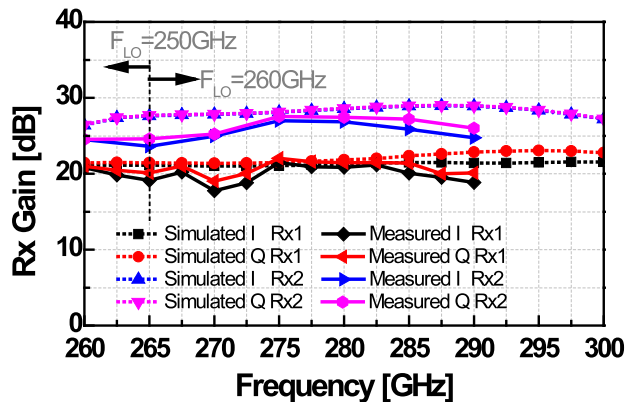


FIGURE 22. Measured and simulated receiver gain of the Rx1 and Rx2.

The noise figure (NF) of the receiver was evaluated using the gain method by measuring the noise floor level at the

IF output. The calibrated single sideband (SSB) NF of the Rx1 is around 23 dB with a minimum value of 22.3 dB at an intermediate frequency (IF) of 10 GHz. The LNA-first receiver (Rx2) has an NF of 21 dB, with a minimum value of 20.1 dB at an IF frequency of 10 GHz as shown in Fig. 23. The measured Rx2 had more NF degradation compared to Rx1 which must be mainly due to the gain reduction in the integrated LNA.

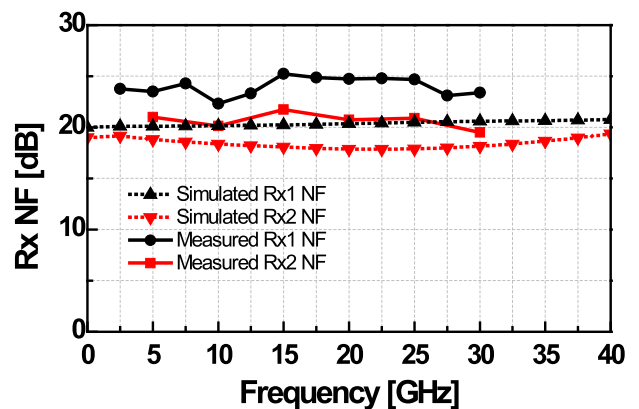


FIGURE 23. Measured and simulated results of SSB noise figure (NF) of the Rx1 and Rx2.

To measure the phase imbalance between I and Q channels, the two IF outputs were monitored using a 10-GHz digital oscilloscope (Keysight UXR0104A), and the phase difference versus RF frequency was extracted using embedded software in the scope. The phase imbalance between I and Q channels was measured to be about 4° up within 30 GHz for Rx1, which corresponds well with the simulation as

shown in Fig. 24. Due to the more balanced structure of the RF distributor with a Wilkinson followed by two Marchand baluns, the LNA-first receiver shows an improved I and Q phase balance. Based on the measured I and Q amplitude and phase imbalances, the image rejection ratio (IRR) of Rx1 is calculated as shown in Fig. 25. The calculated IRR of the receiver was approximately 27 dB, with a maximum value of 34.2 dB at an RF frequency of 260 GHz. Therefore, it is expected that the implemented receivers can handle up to 30GHz of the IF bandwidth which means more than 100Gb/s of 16QAM is feasible for the proposed indoor fiber network. The performance of the receiver is summarized in Table 1 and compared with recently published receiver designs operating in similar frequency bands.

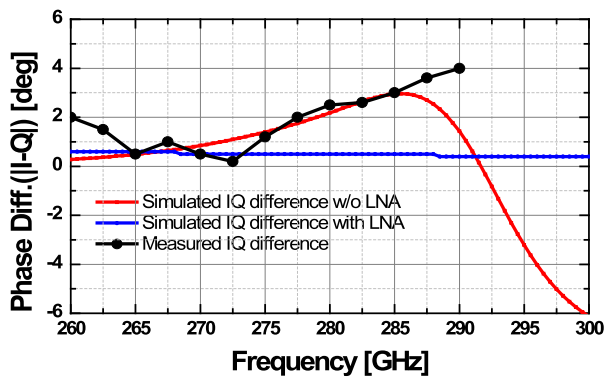


FIGURE 24. Comparison between measured and simulated phase errors.

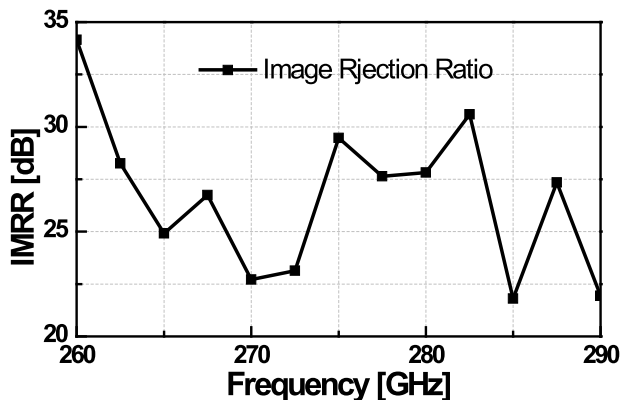


FIGURE 25. Image rejection ratio (IRR) of the Rx1 based on the amplitude and phase mismatch measurement.

Consequently, we verified that both architectures offer distinct advantages and trade-offs in designing an integrated sub-THz receiver. The LNA-first receiver consumed 13% more power dissipation and 43% increased area occupancy compared to the mixer-first architecture, which resulted in an improved 1.3 dB of the receiver NF. Since the designed 275GHz LNA consumed 8.43mW/stage of extra power with about 1 dB/stage of more power gain, its stage can be carefully selected to satisfy a desired receiver NF under the trade-off with bandwidth, power dissipation, and chip size.

IV. CONCLUSION

In this paper, we report two 275 GHz quadrature receivers with an IF bandwidth higher than 30GHz both in the mixer-first and LNA-first architectures integrated with a 260 GHz LO chain in 130-nm SiGe BiCMOS technology. This work aims to provide a cost-effective sub-THz receiver solution for the recently proposed optical-to-electronic interface of future indoor wireline networks [1], [2] in a commercial silicon technology. By integrating a compact LO chain that consists of a differential hybrid coupler, a 260 GHz driving amplifier, and a frequency tripler combined with an E-band driver, the measured mixer-first and LNA-first quadrature receivers achieved with more than 30GHz of IF bandwidth with amplitude and phase error less than 1 dB and 4° , which is expected to support more than 100Gb/s of 16QAM network. The implemented 275 GHz receivers will be successfully applicable for future indoor wireline networks for 6G wireless communications.

REFERENCES

- [1] S.-R. Moon, E.-S. Kim, M. Sung, H. Y. Rha, E. S. Lee, I.-M. Lee, K. H. Park, J. K. Lee, and S.-H. Cho, "6G indoor network enabled by photonics- and electronics-based sub-THz technology," *J. Lightw. Technol.*, vol. 40, no. 2, pp. 499–510, Jan. 15, 2022.
- [2] M. Sung, S. Kim, E.-S. Kim, S.-R. Moon, M. Kim, I.-M. Lee, K. H. Park, J. Ki Lee, and S.-H. Cho, "Design of RoF-based fiber-wireless system for THz-band 6G indoor network," in *Proc. Eur. Conf. Opt. Commun. (ECOC)*, Basel, Switzerland, Sep. 2022, pp. 1–4.
- [3] N. Sarmah, P. R. Vazquez, J. Grzyb, W. Foerster, B. Heinemann, and U. R. Pfeiffer, "A wideband fully integrated SiGe chipset for high data rate communication at 240 GHz," in *Proc. 11th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Oct. 2016, pp. 181–184, doi: 10.1109/EuMIC.2016.7777520.
- [4] N. Sarmah, J. Grzyb, K. Statnikov, S. Malz, P. R. Vazquez, W. Foerster, B. Heinemann, and U. R. Pfeiffer, "A fully integrated 240-GHz direct-conversion quadrature transmitter and receiver chipset in SiGe technology," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 2, pp. 562–574, Feb. 2016, doi: 10.1109/TMTT.2015.2504930.
- [5] P. Rodríguez-Vázquez, J. Grzyb, B. Heinemann, and U. R. Pfeiffer, "A 16-QAM 100-Gb/s 1-m wireless link with an EVM of 17% at 230 GHz in a SiGe technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 29, no. 4, pp. 297–299, Apr. 2019, doi: 10.1109/LMWC.2019.2899487.
- [6] S. Lee, S. Hara, T. Yoshida, S. Amakawa, R. Dong, A. Kasamatsu, J. Sato, and M. Fujishima, "An 80-Gb/s 300-GHz-band single-chip CMOS transceiver," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3577–3588, Dec. 2019, doi: 10.1109/JSSC.2019.2944855.
- [7] M. H. Eissa, N. Maletic, E. Grass, R. Kraemer, D. Kissinger, and A. Malignaggi, "100 Gbps 0.8-m wireless link based on fully integrated 240 GHz IQ transmitter and receiver," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Aug. 2020, pp. 627–630.
- [8] J. Grzyb, P. Rodríguez-Vázquez, S. Malz, M. Andree, and U. R. Pfeiffer, "A SiGe HBT 215–240 GHz DCA IQ TX/RX chipset with built-in test of USB/LSB RF asymmetry for 100+ Gb/s data rates," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 3, pp. 1696–1714, Mar. 2022.
- [9] P. Rodríguez-Vázquez, J. Grzyb, B. Heinemann, and U. R. Pfeiffer, "A QPSK 110-Gb/s polarization-diversity MIMO wireless link with a 220–255 GHz tunable LO in a SiGe HBT technology," *IEEE Trans. Microw. Theory Techn.*, vol. 68, no. 9, pp. 3834–3851, Sep. 2020.
- [10] I. Abdo, T. Fujimura, T. Miura, K. K. Tokgoz, H. Hamada, H. Nosaka, A. Shirane, and K. Okada, "A 300 GHz wireless transceiver in 65 nm CMOS for IEEE802.15.3d using push-push subharmonic mixer," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Aug. 2020, pp. 623–626.
- [11] M. H. Eissa, A. Malignaggi, R. Wang, M. Elkhoully, K. Schmalz, A. C. Ulusoy, and D. Kissinger, "Wideband 240-GHz transmitter and receiver in BiCMOS technology with 25-Gbit/s data rate," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2532–2542, Sep. 2018.

- [12] Y. Wang, B. Yu, Y. Ye, C.-N. Chen, Q. J. Gu, and H. Wang, "A G-band on-off-keying low-power transmitter and receiver for interconnect systems in 65-nm CMOS," *IEEE Trans. THz Sci. Technol.*, vol. 10, no. 2, pp. 118–132, Mar. 2020.
- [13] K. Schmalz, N. Rothbart, A. Glöck, M. H. Eissa, T. Mausolf, E. Turkmen, S. B. Yilmaz, and H.-W. Hübers, "Dual-band transmitter and receiver with bowtie-antenna in 0.13 μm SiGe BiCMOS for gas spectroscopy at 222–270 GHz," *IEEE Access*, vol. 9, pp. 124805–124816, 2021.
- [14] J. Yu, J. Chen, P. Zhou, Z. Li, H. Li, P. Yan, D. Hou, and W. Hong, "A 300-GHz transmitter front end with -4.1 -dBm peak output power for sub-THz communication using 130-nm SiGe BiCMOS technology," *IEEE Trans. Microw. Theory Techn.*, vol. 69, no. 11, pp. 4925–4936, Nov. 2021.
- [15] B. Hadidian, F. Khoeni, S. M. H. Naghavi, A. Cathelin, and E. Afshari, "A 220-GHz energy-efficient high-data-rate wireless ASK transmitter array," *IEEE J. Solid-State Circuits*, vol. 57, no. 6, pp. 1623–1634, Jun. 2022.
- [16] S. Hara, K. Katayama, K. Takano, R. Dong, I. Watanabe, N. Sekine, A. Kasamatsu, T. Yoshida, S. Amakawa, and M. Fujishima, "A 32 Gbit/s 16 QAM CMOS receiver in 300 GHz band," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Honolulu, HI, USA, Jun. 2017, pp. 1703–1706, doi: 10.1109/MWSYM.2017.8058969.
- [17] S. V. Thyagarajan, S. Kang, and A. M. Niknejad, "A 240 GHz fully integrated wideband QPSK receiver in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 50, no. 10, pp. 2268–2280, Oct. 2015, doi: 10.1109/JSSC.2015.2467216.
- [18] U. Alakusu, M. S. Dadash, S. Shopov, P. Chevalier, A. Cathelin, and S. P. Voinigescu, "A 210–284-GHz I-Q receiver with on-chip VCO and divider chain," *IEEE Microw. Wireless Compon. Lett.*, vol. 30, no. 1, pp. 50–53, Jan. 2020.
- [19] M. Elkhouly, Y. Mao, S. Glisic, C. Meliani, F. Ellinger, and J. C. Scheytt, "A 240 GHz direct conversion IQ receiver in 0.13 μm SiGe BiCMOS technology," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2013, pp. 305–308.
- [20] P. R. Vazquez, J. Grzyb, N. Sarmah, B. Heinemann, and U. R. Pfeiffer, "A 219–266 GHz fully-integrated direct-conversion IQ receiver module in a SiGe HBT technology," in *Proc. 12th Eur. Microw. Integr. Circuits Conf. (EuMIC)*, Oct. 2017, pp. 261–264.
- [21] V.-S. Trinh, J.-M. Song, and J.-D. Park, "A 260–300-GHz mixer-first IQ receiver with fundamental LO driver in 130-nm SiGe process," *IEEE Microw. Wireless Technol. Lett.*, vol. 33, no. 4, pp. 435–438, Apr. 2023.



JEONG-MOON SONG (Student Member, IEEE) received the B.S. degree in electrical and electronics engineering and the M.S. degree from Dongguk University, Seoul, South Korea, in 2019 and 2021, respectively, where he is currently pursuing the Ph.D. degree in electronics and electrical engineering.

His research interest includes RF integrated circuits.



VAN-SON TRINH (Member, IEEE) received the Bachelor of Science degree from the Hanoi University of Science and Technology (HUST), Hanoi, Vietnam, in 2015, and the Ph.D. degree in electronics and electrical engineering from Dongguk University, Seoul, South Korea, in 2022.

His current research interests include various analog and RF integrated circuits.



SOOYEON KIM (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Korea University, Seoul, South Korea, in 2007, 2009, and 2020, respectively. From 2009 to 2012, she was a Member of the Technical Staff with the Korea Astronomy and Space Science Institute. Since 2020, she has been with the Electronics and Telecommunication Research Institute, Daejeon. Her research interests include microwave and millimeter-wave

integrated circuits and systems.



JUNG-DONG PARK (Senior Member, IEEE) received the B.S. degree from Dongguk University, Seoul, South Korea, in 1998, the M.S. degree from the Gwangju Institute of Science and Technology (GIST), Gwangju, South Korea, in 2000, and the Ph.D. degree in EECS from the University of California at Berkeley, in 2012.

From 2000 to 2002, he was with the Institute for Advanced Engineering (IAE), Yongin, South Korea, where he was involved in the design of 35-GHz radar/radiometer transceivers. From 2002 to 2007, he was a Senior Researcher with the Agency for Defense Development (ADD), Daejeon, South Korea, where he was responsible for the development of millimeter-wave (mmW) passive/active sensors and related mmW modules. From 2007 to 2012, he was with the Berkeley Wireless Research Center (BWRC), where he was involved on silicon-based RF/millimeter-wave/terahertz circuits and systems. From 2012 to 2015, he was with Qualcomm Inc., San Jose, CA, USA, where he designed various RF/analog integrated circuits. He is currently an Associate Professor with the Division of Electronics and Electrical Engineering, Dongguk University. His research interests include wireless communications, remote sensors, microwave electronics, analog, RF, mixed-signal, and millimeter-wave circuits. He was a recipient of the 2017 Most Frequently Cited Papers Award as a Lead Author from 2010 to 2016 at the 2017 IEEE Symposium on VLSI Circuits held in Kyoto, Japan.

• • •