RESEARCH ARTICLE

A 2.4/5 GHz Dual-Band Low-Noise and Highly Linear Receiver With a New Power-Efficient Feedforward OPAMP for WiFi-6 Applications

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ABSTRACT This paper presents a 2.4/5 GHz dual-band low-noise and highly linear receiver (RX) for IEEE 802.11a/b/g/n/ac/ax applications. The RX employs an RF front-end architecture composing a balun-low-noise transconductance amplifier, current-mode passive mixers, and transimpedance amplifiers (TIAs) to achieve compactness, low noise, and high linearity. A novel power-efficient feedforward operational amplifier architecture was also implemented in the TIA design to achieve the target RX error vector magnitude (EVM) of less than -35 dB with modulation and coding scheme 11 and 1024 quadrature amplitude modulation. Fabricated in a 22-nm SOI CMOS process, the RX achieved noise figures of 2.1/4.2 dB, in-band input-referred third-order intercept points of $-11.8/-7.5$ dBm, EVMs of $-46.4/-44.6$ dB for the 2.4/5 GHz bands, respectively. It drew a bias current of 21 mA from a nominal supply voltage of 0.8 V. The active die area was 0.65 mm^2.

INDEX TERMS Dual-band, error vector magnitude, feedforward operational amplifier, power-efficient, receiver, transimpedance amplifier, WiFi 6, WLAN, 802.11ax.

I. INTRODUCTION

The state-of-the-art technologies of the fourth industrial revolution, such as the Internet of Things, smart factories, virtual/augmented reality, remote offices, and cloud computing require smart devices with very high data throughput and low latency for wireless connection. Accordingly, WiFi standards are continuously developed from 802.11ac to 802.11ax and 802.11be to satisfy these demands and ensure high performance. A receiver (RX) error vector magnitude

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(EVM) of -35 dB or less and channel bandwidth (CHBW) of 160 MHz must be ensured for modulation and coding scheme 11 (MCS11) 1024 quadrature amplitude modulation (QAM), to support 802.11ax [1], [2], [3], [4], [5]. An additional margin is required when considering the multipath fading environment. Therefore, the primary factors affecting the RX performance, such as circuit thermal noise, linearity, in-phase/quadrature (*I/Q*) gain and phase errors (i.e. image rejection ratio), local oscillator (LO) integrated phase noise, and in-band spurs must be significantly enhanced compared with those in 802.11ac [1], [2], [3], [4], [5]. Furthermore, to meet the target EVM floor requirement of MCS11, each
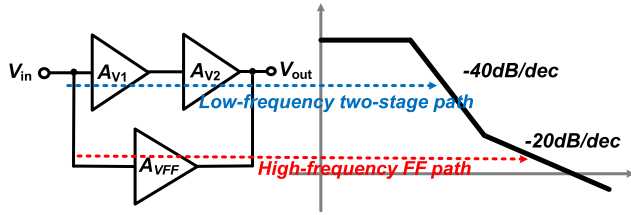
FIGURE 1. Block diagram and Bode plot of conventional two-stage FF OPAMP.

circuit block impairment contributing to the EVM should be 15 dB lower than the target EVM.

The current-driven passive mixer architecture has recently been used for high-performance receiving systems owing to its highly linear operation [1], [2], [3], [4], [5], [6], [7]. In this architecture, the overall performance (e.g., noise, linearity) of the RX signal path largely depends on the stage after the mixer, i.e., a transimpedance amplifier (TIA). Particularly, the TIA requires a high-performance operational amplifier (OPAMP) with a large voltage gain at the passband frequency range and large unity-gain frequency to support the CHBW of 160 MHz. In addition, the OPAMP should employ a power-efficient topology to reduce the RX power consumption.

This study proposes a 2.4/5 GHz dual-band low-noise and highly linear RX with a novel power-efficient feedforward (FF) OPAMP for IEEE 802.11a/b/g/n/ac/ax applications. The proposed WiFi RX employs an RF front-end architecture comprising a balun-low-noise transconductance amplifier (LNTA), current-mode passive mixers, and TIAs to achieve a small die size, low noise, and high linearity. This RF front-end architecture can achieve high linearity because the low input impedance of the TIA limits voltage swings at the mixer input and output. In addition, a new power-efficient FF OPAMP architecture is proposed and adopted in the TIA design to achieve low noise and high linearity for the RX chain. Section II describes the proposed power-efficient FF OPAMP architecture. Section III elaborates on the circuit implementation of the dual-band WiFi-6 RX. The experimental results are discussed in Section IV. The concluding remarks are presented in Section V.

II. NEW POWER-EFFICIENT FF OPAMP TOPOLOGY FOR THE HIGH-PERFORMANCE TIA

The FF OPAMP architecture reported in [8], [9], [10], and [11] is widely used for high-speed operation owing to its wide bandwidth and large voltage gain. The FF OPAMP phase can be compensated by a left-half-plane zero generated by the FF path without the Miller capacitance. Fig. 1 shows a simplified signal-path block diagram of the conventional FF OPAMP [8]. The FF and two-stage amplifier paths are observed on the –20 and –40 dB/dec lines at the Bode plot, respectively; consequently, the FF and the two-stage amplifier paths determine the characteristics of high and low frequencies, respectively. Fig. 2 shows the block diagrams of the conventional two-stage FF OPAMP topologies introduced in the previous
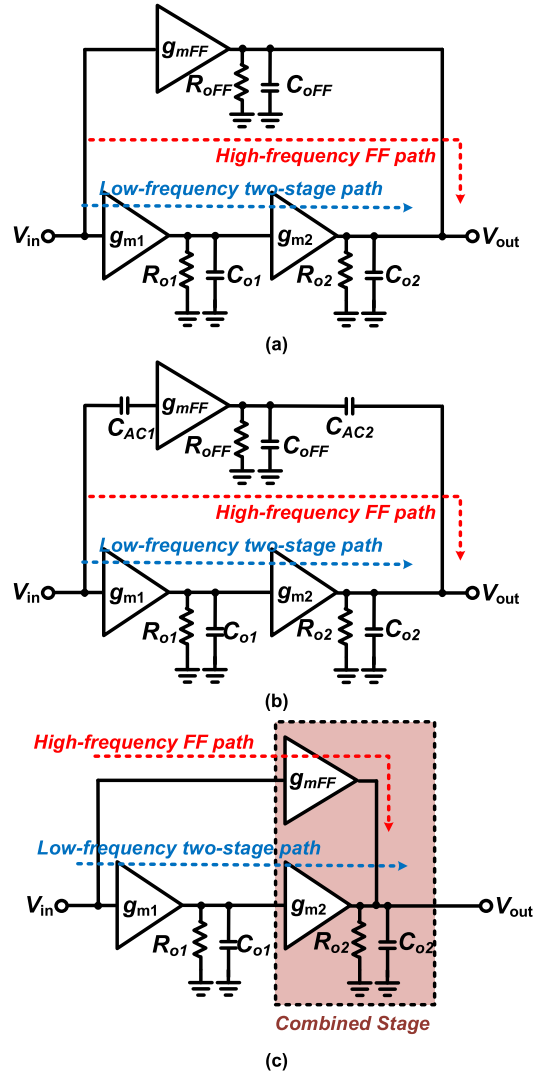

FIGURE 2. Block diagrams of conventional two-stage FF OPAMP topologies: (a) basic FF OPAMP topology (Version 1) [8] (b) modified FF OPAMP topology with ac coupling capacitors and current-reused g_{mFF} (Version 2) [9] (c) modified FF OPAMP topology with combined stage (Version 3) [11].

state-of-the-art. The basic two-stage FF OPAMP topology shown in Fig. 2(a) has the following transfer function:

$$H(s) \cong -\frac{(A_{V1}A_{V2} + A_{VFF})(1 + A_{VFF}s/(A_{V1}A_{V2} + A_{VFF})\omega_{p1})}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})},$$

(1)

where $A_{V1} = g_{m1}R_{o1}$, $A_{V2} = g_{m2}(R_{o2}||R_{oFF})$, and $A_{VFF} = g_{mFF}(R_{o2}||R_{oFF})$. $R_{o1,2,FF}$ and $C_{o1,2,FF}$ are the total resistance and capacitance at the output nodes of each stage, respectively. The dc gain, poles, and zero of the basic two-stage FF OPAMP topology (Version 1) are given by (2)–(5).

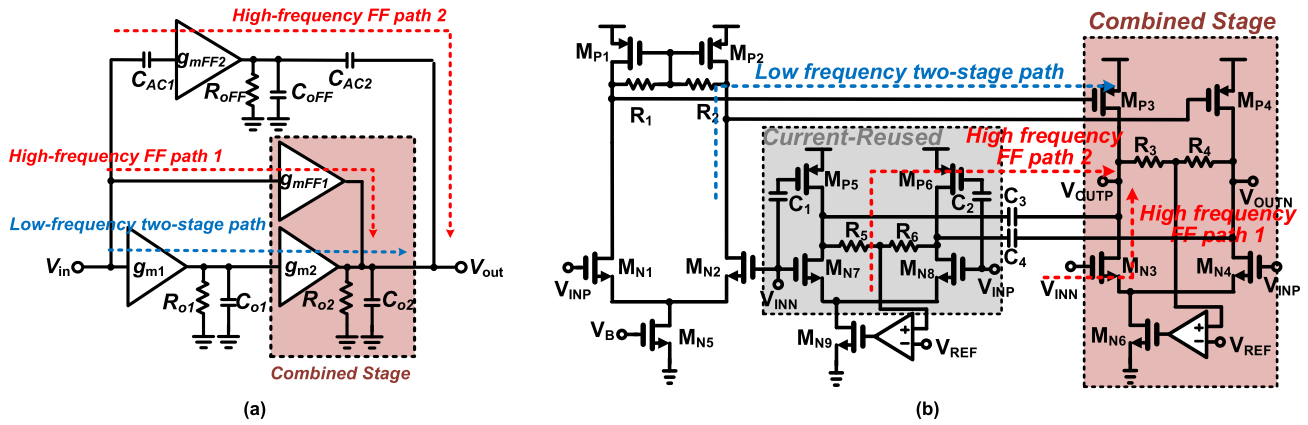$$A_{dc,Ver1} = -(A_{V1}A_{V2} + A_{VFF}) \approx -g_{m1}R_{o1}g_{m2}(R_{o2}||R_{oFF})$$

(2)

FIGURE 3. Proposed power-efficient FF OPAMP (Version 4): (a) block diagram (b) simplified schematic.
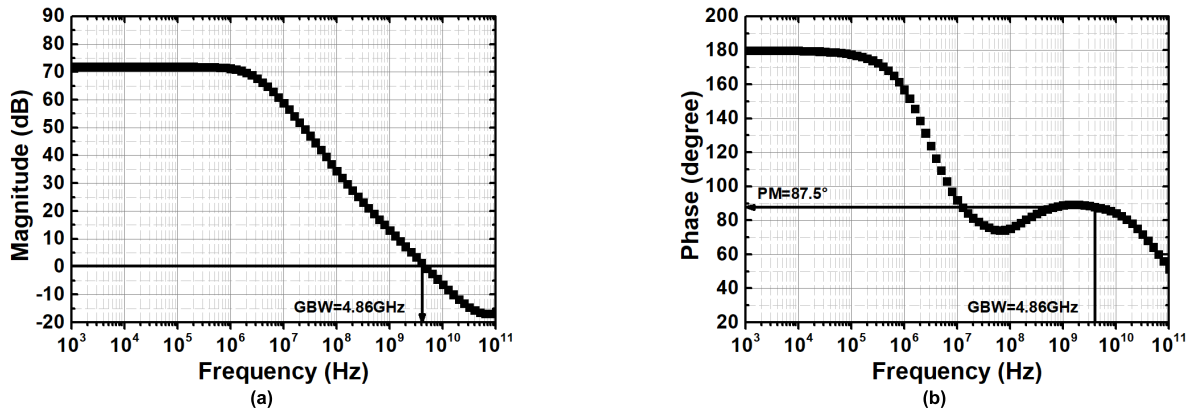

FIGURE 4. Simulated frequency response of the proposed FF OPAMP (a) magnitude (b) phase.

$$\omega_{p1,Ver1} = \frac{1}{R_{o1}C_{o1}} \quad (3)$$

$$\omega_{p2,Ver1} = \frac{1}{(R_{o2}||R_{oFF})(C_{o2} + C_{oFF})} \quad (4)$$

$$\omega_{z,Ver1} = \omega_{p1,Ver1}\left(1 + \frac{g_{m1}R_{o1}g_{m2}}{g_{mFF}}\right). \quad (5)$$

According to (2), the dc gain of the basic FF OPAMP is reduced owing to the parallel connection of R_{o2} and R_{oFF}. The dc gain is significantly reduced when the R_{oFF} value is comparable to or lower than R_{o2}. According to (5), a large g_{mFF} is necessary to move the $\omega_{z,Ver1}$ below unity-gain frequency (ω_t). Thus, realizing the phase compensation for sufficient phase margin requires a large current consumption. Accordingly, modified FF OPAMP topologies were introduced to address the two issues of the dc gain degradation and large current consumption of the FF stage [9], [10], [11]. The modified two-stage FF OPAMP topology employing ac coupling capacitors and current-reused g_{mFF} (Version 2), shown in Fig. 2(b), was introduced in [9]. The ac coupling capacitor, C_{AC2}, decouples the parallel connection of R_{o2} and R_{oFF} at dc. A current-reused CMOS (PMOS/NMOS) FF stage was also adopted to improve the power efficiency of the FF stage.

An ac coupling capacitor, C_{AC1}, was used to bias PMOS and NMOS transistors separately. The dc gain, poles, and zero of the modified two-stage FF OPAMP topology (Version 2) are given by (6)–(9).

$$A_{dc,Ver2} = -(A_{V1}A_{V2} + A_{VFF}) \approx -g_{m1}R_{o1}g_{m2}R_{o2} \quad (6)$$

$$\omega_{p1,Ver2} = \frac{1}{R_{o1}C_{o1}} \quad (7)$$

$$\omega_{p2,Ver2} \approx \frac{1}{(R_{o2}||R_{oFF})(C_{o2} + C_{oFF})} \quad (8)$$

$$\omega_{z,Ver2} = \omega_{p1,Ver2}\left(1 + \frac{g_{m1}R_{o1}g_{m2}}{g_{mFF}}\right). \quad (9)$$

The dc gain is improved, as shown in (6). The effective value of g_{mFF} of the current-reused CMOS FF stage is increased. That is, the current consumption required for the same g_{mFF} with the basic FF OPAMP topology (Version 1) is reduced. A modified FF OPAMP topology with a combined stage (Version 3), shown in Fig. 2(c), was also introduced to address the two issues [10], [11]. The modified topology of Version 3 combines a high-frequency FF path with the second stage of the low-frequency two-stage amplifier path. In this configuration, the load of the second stage of the
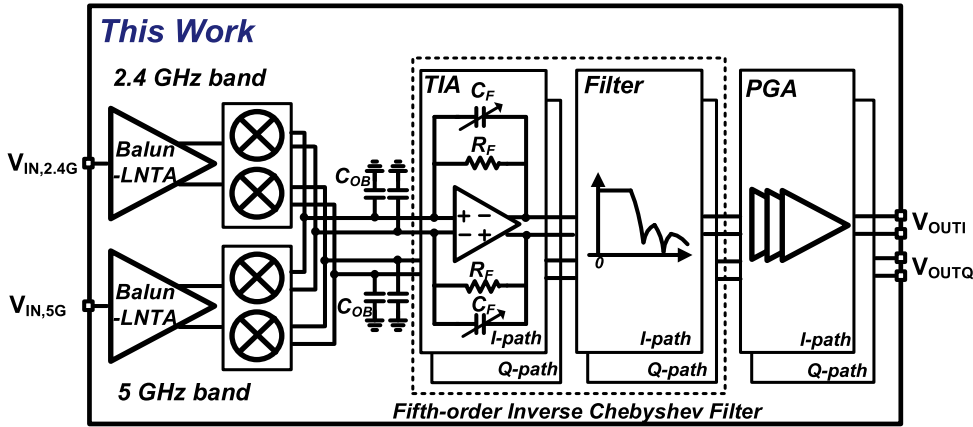
FIGURE 5. Block diagram of the proposed dual-band WiFi-6 receiver.

low-frequency two-stage amplifier acts as the G_m-stage of the high-frequency FF path, resulting in several advantages. First, the FF stage does not reduce the dc gain. Second, the combined stage improves power efficiency. In addition, the Version 3 topology effectively reduces the occurrence of internal poles and zeros caused by parasitic elements, limiting the bandwidth. The dc gain, poles, and zero of the modified two-stage FF OPAMP topology (Version 3) are given by (10)–(13).

$$A_{dc,Ver3} = -(A_{V1}A_{V2} + A_{VFF}) \approx -g_{m1}R_{o1}g_{m2}R_{o2} \quad (10)$$

$$\omega_{p1,Ver3} = \frac{1}{R_{o1}C_{o1}} \quad (11)$$

$$\omega_{p2,Ver3} \approx \frac{1}{R_{o2}C_{o2}} \quad (12)$$

$$\omega_{z,Ver3} = \omega_{p1,Ver3}\left(1 + \frac{g_{m1}R_{o1}g_{m2}}{g_{mFF}}\right). \quad (13)$$

This topology also improves dc gain, as shown in (10). According to (12), the total resistance increases, and the total capacitance decreases in the output node. Thus, $\omega_{p2,Ver3}$ is expected to be similar to $\omega_{p2,Ver1}$ and $\omega_{p2,Ver2}$.

A new FF OPAMP topology, shown in Fig. 3, is proposed. It comprises two high-frequency FF paths to further enhance power efficiency. The proposed FF OPAMP combines the key ideas of the previous modified FF OPAMP topologies. The additional high-frequency FF path with ac coupling capacitors C_{AC1} and C_{AC2} is employed in the modified FF OPAMP topology (Version 3) to further increase the effective g_m of the FF path, as shown in Fig. 3(a). C_{AC2} isolates the effect of the second FF path from the main low-frequency two-stage path at a low frequency; this prevents the gain reduction of the two-stage path caused by the second FF path. C_{AC2} gradually shortens the circuit with the increased operating frequency. The dc gain, poles, and zero of the proposed two-stage FF OPAMP topology (Version 4) are given by (14)–(17).

$$A_{dc,Ver4} = -(A_{V1}A_{V2} + A_{VFF}) \approx -g_{m1}R_{o1}g_{m2}R_{o2} \quad (14)$$

$$\omega_{p1,Ver4} = \frac{1}{R_{o1}C_{o1}} \quad (15)$$

$$\omega_{p2,Ver4} \approx \frac{1}{(R_{o2}||R_{oFF})(C_{o2} + C_{oFF})} \quad (16)$$

$$\omega_{z,Ver4} = \omega_{p1,Ver4}\left(1 + \frac{g_{m1}R_{o1}g_{m2}}{(g_{mFF1} + g_{mFF2})}\right). \quad (17)$$

According to (17), the effective g_{mFF} increases to $g_{mFF1} + g_{mFF2}$. Fig. 3(b) shows a schematic of the proposed power-efficient FF OPAMP topology (Version 4). A current-reuse inverter-type amplifier was used to realize the G_m-stage of the second FF path (g_{mFF2}) to improve the current efficiency. $C_{3,4}$ functions as C_{AC2} to prevent dc gain reduction. The proposed FF OPAMP topology presents a larger effective g_m for the FF path than the modified FF OPAMP topologies (Versions 2 and 3) for the same current consumption, demonstrating the improvement in the phase margin. Generally, the power required to obtain a similar phase margin, dc gain, and high-frequency characteristics is reduced. The first and second stages used local and global common-mode feedback (CMFB) loops, respectively, to maintain the output common-mode voltage. The second FF stage also used a global CMFB loop. Fig. 4 shows the simulated frequency response of the proposed FF OPAMP. The simulated dc gain was 71.8 dB. The unity-gain frequency with a 0.1 pF loading effect of the following stage was 4.86 GHz, with an 87.5° phase margin. The voltage gains were 58.8, 51.9, 44.6, and 37 dB at 10, 20, 40, and 80 MHz, respectively. Therefore, the proposed FF OPAMP has sufficient voltage gain at the operating frequencies.

III. DUAL-BAND WIFI-6 RECEIVER

This section describes a circuit implementation of the 2.4/5 GHz dual-band low-noise and highly linear RX with a power-efficient FF OPAMP for IEEE 802.11a/b/g/n/ac/ax applications. Fig. 5 shows a simplified block diagram of the proposed RX. It comprises the 2.4/5 GHz balun-LNTAs, *I/Q* double-balanced current-mode passive mixers with 25% duty-cycle *I/Q* LO signals, *I/Q* TIAs, *I/Q*
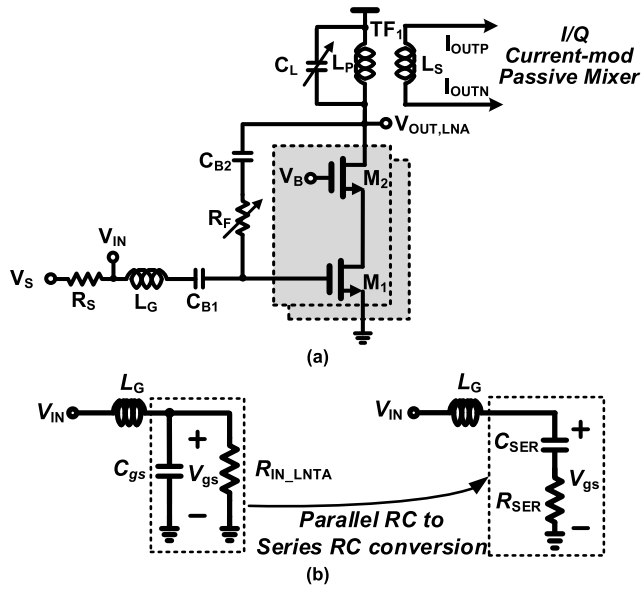
FIGURE 6. Schematic of the Q-boosted resistive-feedback balun-LNTA.

FIGURE 7. Schematic of the current-mode passive mixer with TIA.

FIGURE 8. Schematic of the fifth-order Inverse Chebyshev LPF.

fourth-order inverse Chebyshev active-RC low-pass filters (LPFs), and *I/Q* OPAMP-based programmable gain amplifiers (PGAs). C_{OB} suppresses the voltage swing of the out-of-band (OB) interferer on the RF and baseband sides of the mixer-switching transistors to improve the overall RX linearity [12], [13].

A. BALUN-LNTA
The 2.4/5 GHz balun-LNTAs employ a *Q*-boosted resistive feedback low-noise amplifier (RFLNA) topology with a series *RLC* input-matching network, as shown in Fig. 6 [14]. A 1:1 transformer, TF1, converts a single-ended voltage signal, $V_{OUT,LNA}$, into differential current signals, I_{OUTP} and I_{OUTN}. These current signals flowed into the double-balanced current-mode passive mixers with *I/Q* TIAs. The R_F provides the real part of the balun-LNTA input impedance. The balun-LNTA uses L_G to exploit the gain-boosting characteristics of an inductor-degenerated common-source LNA (L-CSLNA). The left subfigure of Fig. 6(b) shows a simplified diagram of the input-matching network of the balun-LNTA. The input impedance of the balun-LNTA R_{IN_LNTA} is expressed as

$$R_{IN\_LNTA} = \frac{R_F + R_{oLNTA}}{(1 + g_{m1}R_{oLNTA})}, \quad (18)$$

where R_{oLNTA} is $Q_L\omega L_P // g_{m2}r_{o2}r_{o1} // R_{IN\_MIXER}$ at the operating frequency. Q_L and R_{IN_MIXER} represent the quality factor of L_P and input impedance of the mixer, respectively. The right subfigure of Fig. 6(b) shows the equivalent input-matching network, converted through parallel *RC*-to-series *RC* conversion with a narrow frequency band of interest. Thus, the balun-LNTA performs input power matching with a series *RLC* network. The overall g_m of the balun-LNTA is effectively improved by $\sqrt{1 + Q_{SER}^2}$, where Q_{SER} is $\omega_o L_G/R_{SER}$ for an operational frequency of ω_o [14], [15].
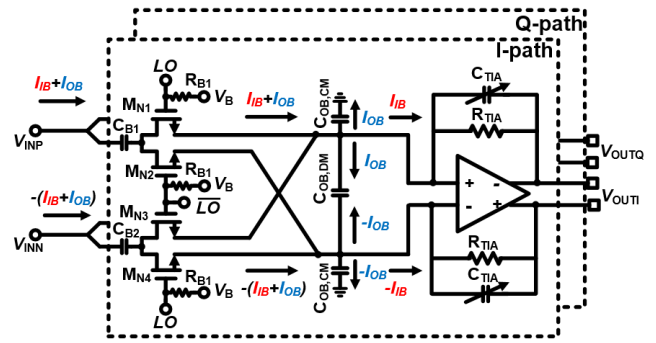
C_{SER} and R_{SER} are expressed as follows:

$$C_{SER} = C_{gs}\left(1 + \frac{1}{Q_{SER}^2}\right), \quad (19)$$

$$R_{SER} = \frac{R_F + R_{oLNTA}}{(1 + g_{m1}R_{oLNTA})\left(1 + Q_{SER}^2\right)}. \quad (20)$$

When the L_G and C_{SER} values are set to resonate at the operating band, the input impedance of the balun-LNTA is obtained as R_{SER}, which must be equal to the source resistance, R_S. Therefore, the overall voltage gain of the RFLNA from V_S to $V_{OUT,LNA}$ is given as

$$A_{V,RFLNA} = -\frac{\sqrt{1 + Q_{SER}^2}}{2}\left(g_{m1} - \frac{1}{R_F}\right)(R_{oLNTA}||R_F). \quad (21)$$

When $g_{m1}R_F \gg 1$, and $R_F \gg R_{oLNTA}$, $A_{V,RFLNA}$ can be approximated as

$$A_{V,RFLNA} \approx -\frac{\sqrt{1 + Q_{SER}^2}}{2}g_{m1}R_{oLNTA}. \quad (22)$$

The proposed RFLNA obtains a large voltage gain, similar to that of the L-CSLNA, while simultaneously removing the large on-chip spiral inductors at the source of M_1. A resistor bank for R_F and G_m-cells comprising main and cascode transistors are digitally controlled for LNA gain control. In addition, C_L can be digitally tuned to adjust the center frequency of the *LC* load according to the operating band
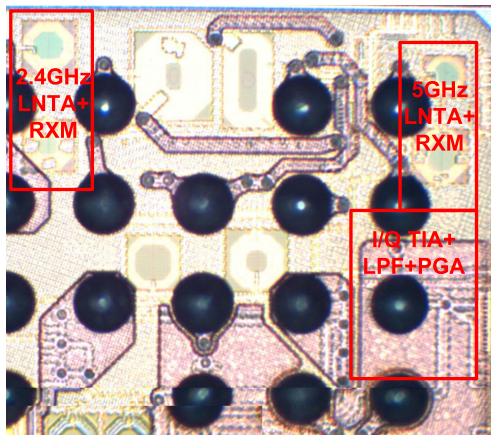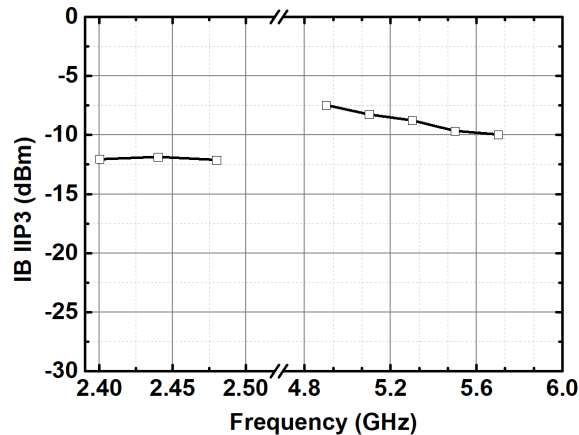
FIGURE 9. Chip microphotograph.
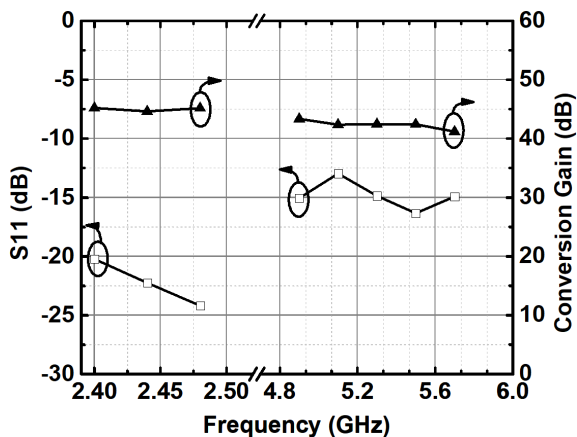

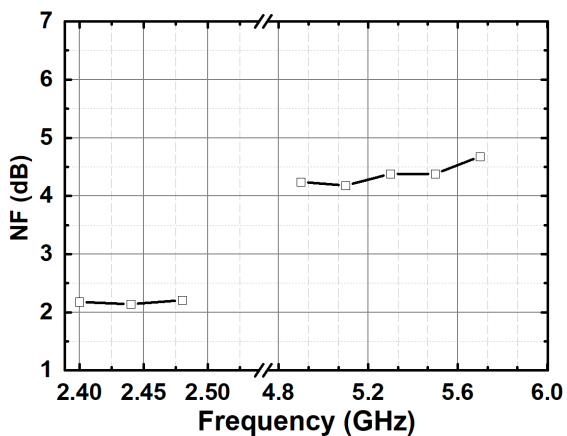**FIGURE 10.** Measured S_{11} and conversion gain.

FIGURE 11. Measured NF.

B. CURRENT-MODE PASSIVE MIXER WITH TIA

The required linearity is achieved using double-balanced current-mode passive mixers with the TIA shown in Fig. 7 while maintaining the low impedances at the input and output of the mixer. The passive mixer also improves the

FIGURE 12. Measured IB IIP3.

FIGURE 13. Measured IF frequency response versus filter bandwidth.

flicker noise performance owing to the absence of dc current. The ac-coupling capacitors (C_{B1} and C_{B2}) in front of the mixer-switching transistors perform high-pass filtering and reject the second-order intermodulation distortions generated by the preceding balun-LNTA. The I/Q mixers are driven by 25% duty-cycle quadrature LO signals provided by the divider and inverter-type LO buffers. The subsequent OPAMP-based TIA performs current-to-voltage conversion and eliminates the OB blockers and interfering signals. The OPAMP is the most important block because it determines the overall TIA performance, including the noise, linearity, and input impedance levels. Fig. 3 shows the proposed FF OPAMP with two high-frequency FF paths, adopted for the TIA to support an 80 MHz CHBW and achieve high linearity. The designed FF OPAMP can obtain a high voltage gain (even at high frequencies) and high unity-gain frequency for a given power consumption. As shown in Fig. 7, $C_{OB,DM}$ and $C_{OB,CM}$ are used to eliminate the differential-mode and common-mode OB interferers and blockers on the RF and baseband sides of the mixer-switching transistors to improve the overall RX linearity.
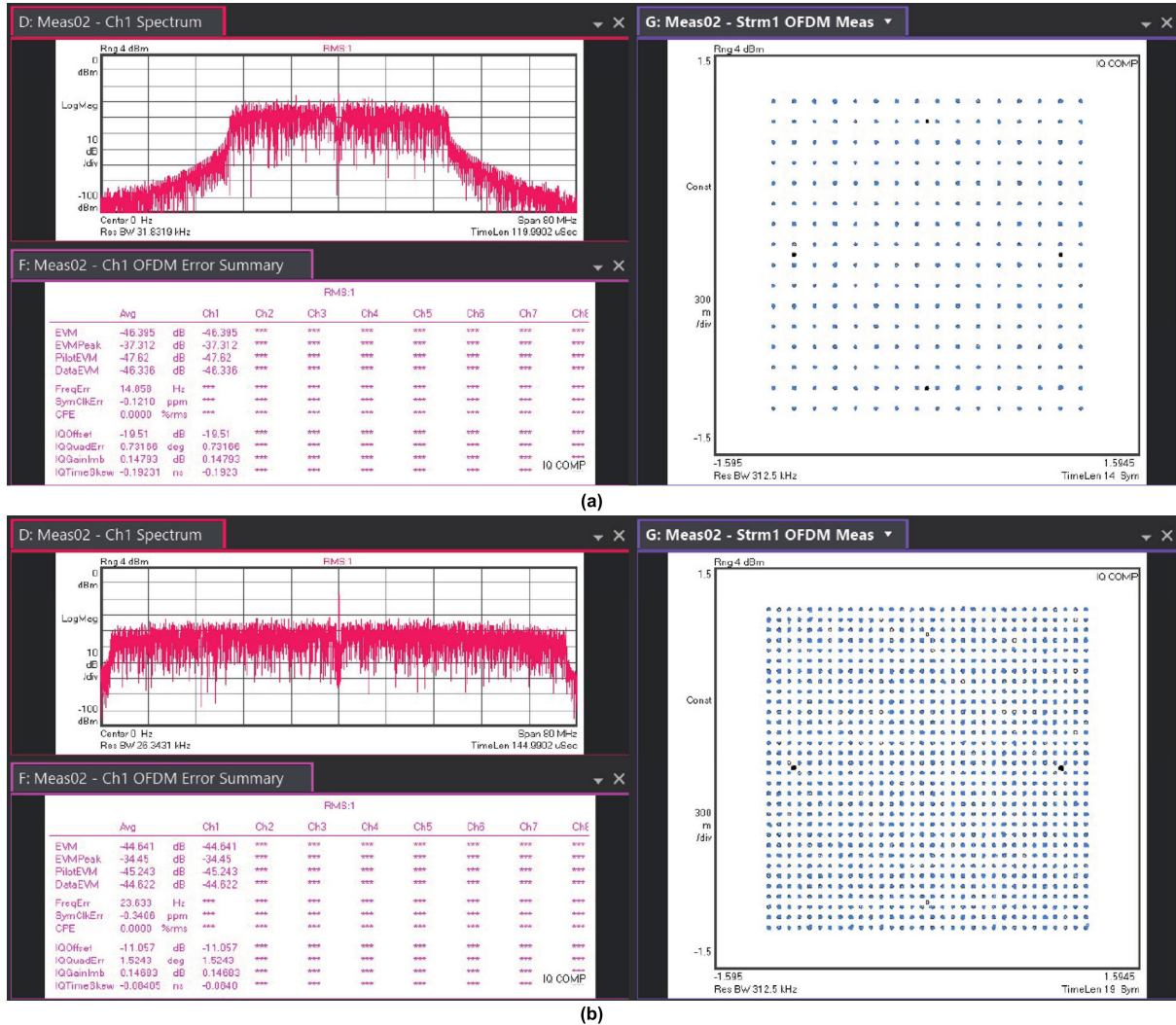
FIGURE 14. Measured EVMs and constellations: (a) 2.4 GHz band (MCS10 256QAM, CHBW = 40 MHz) (b) 5 GHz band (MCS11 1024QAM, CHBW = 80 MHz).

C. BASEBAND ANALOG CIRCUITS

As shown in Fig. 8, an active-RC LPF with the preceding TIA implements a fifth-order inverse Chebyshev LPF. It can provide an adjacent channel rejection ratio (ACRR) of more than 35 dB. The 3 dB filter bandwidth can be tuned to 10, 20, and 40 MHz based on the WiFi channel bandwidth. A three-stage OPAMP-based PGA is used to provide a 42 dB maximum voltage gain with a 60 dB dynamic range and 1 dB gain step.

IV. EXPERIMENTAL RESULTS

The dual-band WiFi-6 RX was fabricated using 22-nm silicon on insulator complementary metal-oxide semiconductor (SOI CMOS) technology. Fig. 9 shows a microphotograph of the chip. The RX has an active die area of 0.65 mm^2 including 2.4/5 GHz LNTAs/RXMs and I/Q TIAs/LPFs/PGAs. The 2.4/5 GHz RX, excluding the LO circuits, drew a current of 21/20.5 mA from a nominal supply voltage of 0.8 V. The current consumptions of the 2.4/5 GHz balun-LNTA, I/Q

TIAs, I/Q active-RC LPFs, and three-stage PGAs were 4/3.5, 3, 8, and 6 mA, respectively. A grounded 50-Ω coplanar waveguide was applied on an assembled printed circuit board to perform the measurements. The differential LO signals at $2f_{LO}$ were supplied from the off-chip through a commercial balun.

Fig. 10 shows the measured S_{11} and conversion gain of the RX when the baseband analog circuits have a 0 dB gain code. The implemented RX achieved a measured S_{11} of less than −10 dB and a conversion gain of 42–45 dB. Fig. 11 showed the measured double side-band (DSB) NFs versus the operating RF frequencies. The RX achieves minimum NFs of 2.1/4.2 dB at the 2.4/5 GHz bands, respectively. The RX in-band (IB) input-referred third-order intercept points (IIP3) were also characterized by adjacent and alternate channels. The two-tone test conditions of the IB IIP3 for 2.4 GHz band and 20 MHz CHBW were $f_1 = f_{LO} + 20$ MHz, $f_2 = f_{LO} + 41$ MHz, $p_{f1} = −60$ dBm, and $p_{f2} = −44$ dBm. The two-tone test conditions of the IB IIP3 for the 5 GHz

TABLE 1. Measured performance summaries and comparisons.

Reference		[1] ISSCC 2020	[2] ISSCC 2018	[3] RFIC 2018	[4] RFIC 2023	[5] JSSC 2017	This work
Supported WiFi Standard		802.11 a/b/g/n/ac/ax	802.11 a/b/g/n/ac/ax	802.11 a/b/g/n/ac/ax	802.11 a/b/g/n/ac/ax/be	802.11 a/b/g/n/ac	802.11 a/b/g/n/ac/ax
Technology		CMOS 55nm	CMOS 28nm	CMOS 28nm	CMOS 55nm	CMOS 40nm	SOI CMOS 22nm
RX NF (dB)	2.4G	4.2	2.9	3.7	3.5	2.9	2.1
	5G	4.8	3.2	3.8	4.5	4.5	4.2
IB IIP3 (dBm)	2.4G	NA†	NA	NA	NA	NA	-11.8
	5G	NA	NA	NA	NA	NA	-7.5
P_{dc} [mW]	2.4G	322	354 (4SS*+1LO)	NA	254 (1SS)	179 (2SS)	16.8 (1SS RX only)
	5G	420 (4SS+1LO)	447 (4SS+2LO)	NA	359 (1SS)	243 (2SS)	16.4 (1SS RX only)
Area (mm²)		22.9 (4SS)	12 (4SS)	11.7 (2SS+BT+FM)	3.74 (1SS)	8.6 (2SS+BT)	0.65 (1SS RX only)

†NA = not available *spatial stream

band and 80 MHz CHBW were $f_1 = f_{LO} + 80$ MHz, $f_2 = f_{LO} + 161$ MHz, $p_{f1} = -57$ dBm, and $p_{f2} = -41$ dBm. The two-tone test conditions are derived from the frequencies and powers of the adjacent and alternate adjacent channels. The obtained maximum IB IIP3s were –11.8/–7.5 dBm for the 2.4/5 GHz bands, respectively, as shown in Fig. 12. Fig. 13 shows the measured baseband frequency responses for different filter bandwidth modes. The proposed RX can support three bandwidth modes of 10/20/40 MHz. Fig. 14 shows the measured RX EVMs, received spectrums, and constellations for the 2.4/5 GHz bands. MCS10 256QAM/40 MHz CHBW and MCS11 1024QAM/80 MHz CHBW signals were used for the 2.4/5 GHz bands, respectively. The measured RF input power was −50 dBm for both bands. The obtained minimum RX EVMs were –46.4/–44.6 dB for the 2.4/5 GHz bands, respectively. The measured RX EVMs for the 2.4/5 GHz bands were much less than the target EVM of −35 dB. Table 1 presents a comparison of the performance of the proposed RX with those of other reported WiFi RXs. The implemented RX obtained similar or better noise performance compared to other WiFi RXs

V. CONCLUSION

A 2.4/5 GHz dual-band low-noise and highly linear RX for IEEE 802.11a/b/g/n/ac/ax applications was designed and implemented in a 22-nm SOI CMOS process. A new power-efficient FF OPAMP architecture was proposed to achieve a broadband, low-noise, and highly linear TIA. The proposed RX obtained a maximum conversion gain of 85 dB with a dynamic range of 120 dB, a gain step of 1 dB, and an ACRR of more than 35 dB. It also achieved NFs of 2.1/4.2 dB and IB IIP3s of −11.8/−7.5 dBm for the 2.4/5 GHz bands, respectively.

REFERENCES

[1] E. Ru, W. Li, Z. Deng, E. Rostami, P. Wu, K. Chang, Y. Chuang, C. Lai, Y. Chen, T. Peng, T. Tsai, H. Liu, C. Chiu, B. Huang, Y. Wang, J. Zhan, and O. Shanna, "A 4 × 4 dual-band dual-concurrent WiFi 802.11ax transceiver with integrated LNA, PA and T/R switch achieving +20 dBm 1024-QAM MCS11 pout and −43 dB EVM floor in 55 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 178–179.

[2] S. Kawai et al., "An 802.11ax 4 × 4 spectrum-efficient WLAN AP transceiver SoC supporting 1024 QAM with frequency-dependent IQ calibration and integrated interference analyzer," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 442–444.

[3] C. Wu et al., "A 28 nm CMOS wireless connectivity combo IC with a reconfigurable 2 × 2 MIMO WiFi supporting 80+80 MHz 256-QAM, and BT 5.0," in *Proc. IEEE RFIC*, Jun. 2018, pp. 300–303.

[4] T. Chen, M. Liu, P. Wu, W. Hong, T. Liang, W. Chao, P. Chang, Y. Chou, C. Chen, S. Liu, C. Huang, H. Ting, M. Hsu, Y. Wang, C. Hung, Y. Hsueh, E. Lu, and Y. Chung, "A Wi-Fi tri-band switchable transceiver with 57.9 fs-RMS-jitter frequency synthesizer, achieving −42.6 dB EVM floor for EHT320 4096-QAM MCS13 signal," in *Proc. IEEE RFIC*, Jun. 2023, pp. 181–184.

[5] S. Yan, L. Ye, R. Kulkarni, E. Myers, H. Shih, H. Wu, S. Saberi, D. Kadia, D. Ozis, L. Zhou, E. Middleton, and J. Tham, "An 802.11a/b/g/n/ac WLAN transceiver for 2 × 2 MIMO and simultaneous dual-band operation with +29 dBm P_{sat} integrated power amplifiers," *IEEE J. Solid-State Circuits*, vol. 52, no. 7, pp. 1798–1813, Jul. 2017.

[6] J. Han and K. Kwon, "I/Q balance-enhanced wideband receiver front-end for 2G/3G/4G/5G NR cellular applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 6, pp. 1881–1891, Jun. 2020.

[7] J. Han and K. Kwon, "RF receiver front-end employing IIP2-enhanced 25% duty-cycle quadrature passive mixer for advanced cellular applications," *IEEE Access*, vol. 8, pp. 8166–8177, 2020.

[8] J. Harrison and N. Weste, "A 500 MHz CMOS anti-alias filter using feedforward op-amps with local common-mode feedback," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2003, pp. 132–133.

[9] H. Jung, D. R. Utomo, S.-K. Han, J. Kim, and S.-G. Lee, "An 80 MHz bandwidth and 26.8 dBm OOB IIP3 transimpedance amplifier with improved nested feedforward compensation and multi-order filtering," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 10, pp. 3410–3421, Oct. 2020.

[10] K. Kwon, "A 40 M-1000 MHz 77.2-dB spurious free dynamic range CMOS RF variable gain amplifier for digital TV tuner ICs," *Int. J. Circuit Theory Appl.*, vol. 43, no. 7, pp. 875–886, Jul. 2015.

[11] D. Shin, K. Lee, and K. Kwon, "A blocker-tolerant receiver front end employing dual-band N-path balun-LNA for 5G new radio cellular applications," *IEEE Trans. Microw. Theory Techn.*, vol. 70, no. 3, pp. 1715–1724, Mar. 2022.

[12] K. Kwon and J. Han, "A 2G/3G/4G SAW-less receiver front-end adopting switchable front-end architecture," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 8, pp. 1716–1723, Aug. 2014.

[13] J. Deguchi, D. Miyashita, Y. Ogasawara, G. Takemura, M. Iwanaga, K. Sami, R. Ito, J. Wadatsumi, Y. Tsuda, S. Oda, S. Kawaguchi, N. Itoh, and M. Hamada, "A fully integrated 2 × 1 dual-band direct-conversion mobile Wimax transceiver with dual-mode fractional divider and noise-shaping transimpedance amplifier in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2774–2784, Dec. 2010.

[14] S. Joo, T.-Y. Choi, and B. Jung, "A 2.4-GHz resistive feedback LNA in 0.13-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3019–3029, Nov. 2009.

[15] B. Razavi, *RF Microelectronics*. Upper Saddle River, NJ: Prentice-Hall, 1998.

[16] R. Schaumann and M. Valkenburg, *Design of Analog Filters*. Oxford, U.K.: Oxford Univ. Press, 2001.

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