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RESEARCH ARTICLE

CMOS Variable-Gain Low-Noise Amplifier Adopting Transformer-Based Noise Cancelling Technique for 5G NR FR2 Applications

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ABSTRACT This study presents a complementary metal–oxide–semiconductor (CMOS) variable-gain low-noise amplifier (VGLNA) employing a transformer-based noise cancelling technique, applicable for fifth-generation new radio frequency range 2 communication. In the proposed design, gain controllability is realized by combining the in-phase main and current-steering path signals through a transformer load whose coupling coefficient is less than unity. Additionally, the noise contribution from cascode devices can be diminished through a transformer-based noise cancelling technique in low-gain modes. Consequently, an enhanced noise performance is achieved as the gain of the VGLNA is lowered. The proposed design is fabricated in a 65-nm CMOS process. At 28 GHz, the implemented VGLNA attains gains and noise figures of 12.1 to 2.7 dB and 3.55 to 4.3 dB, respectively. The design draws a bias current of 10.6 mA with a 1 V nominal supply and occupies a die size of 0.13 mm2, excluding bonding pads.

INDEX TERMS Complementary metal–oxide–semiconductor (CMOS), current-steering, fifth-generation (5G) new radio (NR), frequency range 2 (FR2), low-noise amplifier (LNA), noise cancelling, transformer, variable-gain amplifier (VGA).

I. INTRODUCTION

Millimeter wave (mmWave) frequency bands have recently gained increasing attention, particularly for fifth-generation (5G) new radio (NR) wireless communication owing to their abundant spectrum for high data-rates. In addition, beamforming technology has been widely adopted for mmWave 5G NR transceivers to achieve enhanced throughput and directivity performance and overcome high path losses in signal propagation through a phased-array architecture [1], [2], [3], [4]. Fig. 1(a) shows the block diagram of a conventional multi-element phased-array radio frequency (RF) front-end receiver, which comprises low-noise amplifiers (LNAs), variable-gain amplifiers (VGAs), and phase shifters (PSs). To precisely steer each beam with different weights, VGAs along with PSs are typically utilized to attenuate gain errors in accordance with phase changes and reduce side lobes. However, owing to the deteriorated noise performance of the VGA in low-gain modes, LNAs are in high demand in the preceding stages, which is undesirable for cost-effective and compact designs.

Previous studies have proposed various gain control (GC) approaches and demonstrated VGA designs in the mmWave frequency bands [5], [6], [7], [8], [9], [10], [11], [12],

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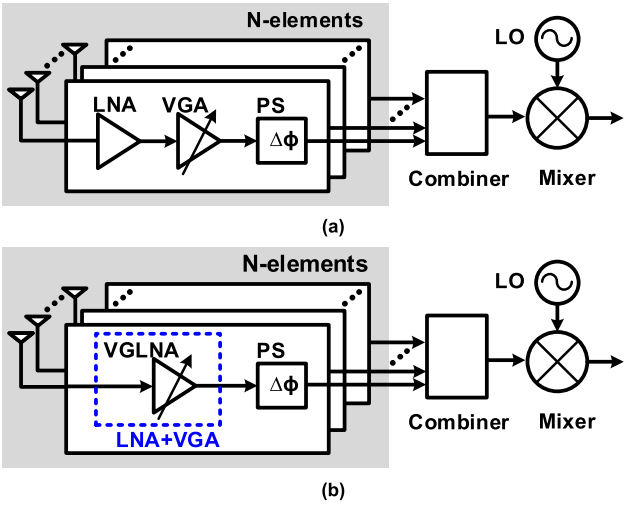

FIGURE 1. Block diagrams of (a) conventional and (b) LNA_VGA merged phase array architectures.

[13], [14], [15], [16], [17]. In [5], [6], [7], [8], and [9], straightforward gain control methods that simply tune the resistive/inductive impedance at the load or an attenuator between stages through control signals were presented. Using these methods, a relatively large gain control range (GCR) with fine steps can be readily obtained. Alternatively, a current-steering technique has been widely applied to attain gain controllability [10], [11], [12], [13], [14], [15]. The on–off controlled current-steering cascode devices adjust the amount of RF signal current flowing to the output load and supply. A lower gain is achieved as a larger RF current is wasted to AC ground. Reference [16] also introduced a gain reduction method by selectively combining in-phase and out-of-phase RF signals with low phase variation. In the aforementioned approaches, gain control can be performed in either analog or digital manner. However, the noise performance of VGAs can be significantly degraded with decreasing gain, primarily owing to additive on–off control devices and their inherent parasitic components. This limitation eventually prevents the VGA from performing the role of an LNA. The variable-gain LNA (VGLNA) in [17] employed a tunable coupling coefficient (k) transformer to change the output matching condition to ensure that the gain could be varied with a relatively small noise figure (NF) degradation. However, an extra LNA is utilized as the first stage in the design and its GCR is also limited by the design complexity of the tunable coupling coefficient of the transformer.

In this study, a complementary metal-oxide-semiconductor (CMOS) VGLNA adopting a transformer-based noise cancelling technique is presented, which facilitates a development of cost-effective and compact phased-array architectures (Fig. 1(b)). In the proposed design, gain controllability is primarily achieved by combining the in-phase main and current-steering path signals through a transformer load. In addition, the noise contribution from cascode devices can be reduced in low-gain modes owing to partial noise

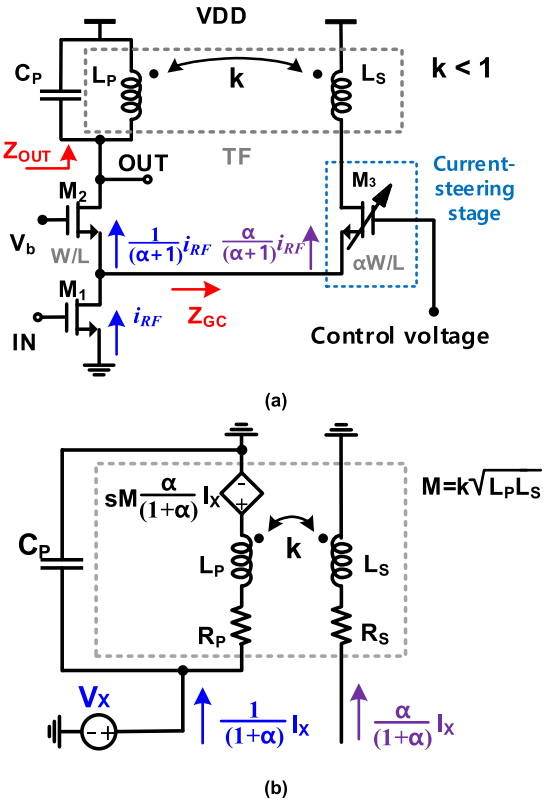

FIGURE 2. (a) Simplified circuit diagram of the proposed VGLNA adopting noise cancelling technique and (b) equivalent circuit model of the transformer load.

cancelling through the utilized transformer. The proposed design is fabricated with a 65 nm CMOS technology and targeted to support the n257 and n261 bands of the 5G NR frequency range 2 (FR2), (i.e., 26.5–29.5 GHz). The remainder of this paper is organized as follows. In Section II, the basic operation of the proposed VGLNA is discussed and analyzed, focusing on gain controllability and noise cancellation properties. Section III describes the circuit implementation of the design VGLNA in detail. The Measurement results of implement design are demonstrated in section IV. Finally, Section V presents the concluding remarks.

II. PROPOSED VARIABLE-GAIN LOW-NOISE AMPLIFIER WITH TRANSFORMER-BASED NOISE CANCELLING TECHNIQUE

Fig. 2(a) shows a simplified circuit diagram of the proposed VGLNA that adopts the transformer-based noise cancelling technique. The design fundamentally follows the common-source cascode amplifier configuration (M_{1-2}), which separately incorporates the main and current-steering stages for gain control. In this design, ordinary current-steering cascode gain control devices (M_3) are used whereas a transformer (TF) is additionally utilized between the loads of the two stages. Therefore, the primary and secondary coils of the transformer are placed as loads for the main and current-steering stages, respectively. This implies that the RF signal current flowing into the

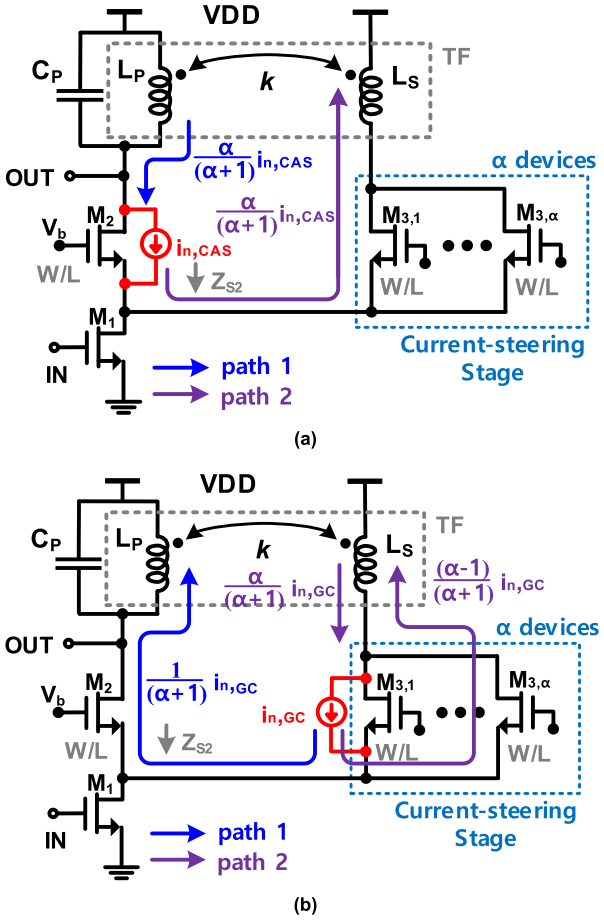

FIGURE 3. Noise cancelling mechanisms for (a) cascode device (M2) at the main path and (b) gain control devices (M3,1-3, α) at the current-steering path.

current-steering stage can be coupled back to the main stage and combined with the in-phase main signal. This is distinct from the conventional current-steering technique, which wastes the RF signal to supply (AC ground) for gain reduction.

A. GAIN CONTROL

In the proposed design, the VGLNA accomplishes gain controllability, primarily through the coupling coefficient of the transformer, which is less than unity ($k < 1$). Although the in-phase main and transformer-induced signals are integrated at the output, a larger steered RF signal current leads to a lower combined gain owing to the smaller induced signal to the output load. As depicted in Fig. 2(a), the input transconductance device (M_1) converts the input signal into an RF current ($i_{RF} = g_{m1}V_{in}$), where g_{mX} is the transconductance of M_X. According to the on–off control of cascode device (M_3), RF currents separately flow into the main and current-steering stages, which are defined as $1/(1+\alpha) \cdot i_{RF}$ and $\alpha/(1+\alpha) \cdot i_{RF}$, in this analysis, respectively; here "α" denotes the size (width) ratio of the gain control device (M_3) ($\alpha W/L$) with respect to the cascode device (M_2) (W/L). To determine the overall gain of the amplifier, including the effect of the transformer, the load output impedance (Z_{OUT}) must be evaluated by considering the RF current flows in both the main and current-steering stages. According to the equivalent model of the transformer load, as shown in Fig. 2(b), Z_{OUT} can be calculated as follows.

$$Z_{OUT}(s) = \frac{V_X}{I_X/(1+\alpha)} = \frac{R_P + sL_P(1+\alpha k)}{1 + sR_PC_P + s^2L_PC_P} \quad (1)$$

For simplicity, $L_P = L_S$ and $R_P = R_S$ are assumed where L_P/L_S and R_P/R_S denote the primary/secondary inductance and parasitic series resistance of the transformer, respectively. Therefore, mutual inductance (M) is simplified to $k{\cdot}L_P$. When Z_{OUT} is resonated with a shunt capacitor (C_P) at resonant frequency, ω_0 in the maximum (max)-gain mode ($\alpha = 0$), Z_{OUT} can be expressed as:

$$Z_{OUT}(j\omega_0) = \frac{L_P}{R_PC_P} + \alpha k\left(\frac{L_P}{R_PC_P} - R_P\right)$$
$$\cong \frac{L_P}{R_PC_P}(1+\alpha k),\ \omega_0 = \sqrt{\frac{L_P - R_P^2C_P}{L_P^2C_P}} \quad (2)$$

Assuming $L_P/R_PC_P \gg R_P$, Z_{OUT} can be further simplified. According to (2), the voltage gain (G) of the proposed VGLNA is expressed as

$$G = g_{m1}\frac{1}{1+\alpha}\frac{L_P}{R_PC_P}(1+\alpha k) = g_{m1}\frac{L_P}{R_PC_P}\frac{1+\alpha k}{1+\alpha} \quad (3)$$

Evidently from (3), the gain of the VGLNA can be varied as α increases for $k < 1$ (when $k = 1$ for an ideal transformer, no gain control occurs). This indicates that a smaller coupling coefficient, k entails a larger GCR, which can be adjusted through the transformer design. Moreover, to maximize the gain of the VGLNA, the values of C_P and R_P need to be minimized, even at the resonant frequency. This indicates that extra capacitor is not required in the secondary inductor.

B. NOISE CANCELLATION

As described above, the proposed VGLNA additionally offers noise cancellation property through the utilized transformer in low-gain modes. The concept of noise cancellation was previously introduced in [18], [19], [20], and [21]. Figs. 3(a) and 3(b) depict simplified circuit diagrams, showing the noise cancelling mechanisms of the channel noise, contributed from both cascode (M_2) and gain control devices ($M_{3,1-3,\alpha}$) at the main and current-steering stages, respectively. Herein, similar to the gain analysis, the $\alpha W/L$ size of gain control device is assumed in the current-steering stage with α number of identical devices (W/L). In general, the noise contribution from the cascode device is not critical owing to the high impedance (Z_{S2}) condition, seen from the source terminal of M_2 (max-gain mode in this design). However, in the low-gain modes, all/part of gain control devices ($M_{3,1-3,\alpha}$) are switched-on for RF current steering; thereby, the impedance of Z_{S2} is lowered correspondingly. This ultimately increases the noise contribution from the both cascode and gain control devices to the output significantly. For the noise analysis of M_2 in the low-gain modes,

shown in Fig. 3(a), the part of noise current ($i_{n,CAS}$) appears directly at the output load through path 1, which is determined by $\alpha/(\alpha+1)\cdot i_{n,CAS}$ with $g_{m2} = g_{m3}$. By contrast, the same amount of noise current can also flow into the secondary coils of the transformer via gain control devices (path 2) and be coupled to the output in the opposite phase. Consequently, the partial noise cancellation is achieved from the proposed design. The total noise voltage that appears at the output through paths 1 and 2 can be calculated by

$$v_{n,OUT}\big|_{M2} = -\frac{R_P + sL_P(1-k)}{1 + sR_PC_P + s^2L_PC_P} \cdot \frac{\alpha}{1+\alpha} i_{n,CAS} \quad (4)$$

Assuming $L_P/R_PC_P \gg R_P$ with sufficiently small k value and a resonant condition of ω_0 from (2), the approximated noise power expression given by M_2 can be determined as follows:

$$\overline{v_{n,OUT}^2}\Big|_{M2} \cong \frac{L_P^2(1-k)^2}{R_P^2C_P^2} \cdot \frac{\alpha^2}{(1+\alpha)^2} \overline{i_{n,CAS}^2} \quad (5)$$

As seen from (5), the output noise from M_2 can be reduced with $0 < k < 1$ as α increases. Perfect noise cancellation is attained for an ideal transformer with $k = 1$. The condition of $k = 0$ also corresponds to a noise contribution from the cascode device without the transformer-based noise cancellation technique. Similarly, the noise from gain control devices ($M_{3,1-3,\alpha}$) can be partially cancelled through the proposed design. Consider the noise current, $i_{n,GC}$ for one of the gain control devices ($M_{3,1}$) switched-on (Fig. 3(b)). Owing to α number of devices, excluding $M_{3,1}$, a noise current of $1/(\alpha+1)\cdot i_{n,GC}$ appears at the output through path 1. Moreover, the noise current flowing into the secondary coil of the transformer is determined by $[(\alpha-1)/(\alpha+1)-\alpha/(\alpha+1)]\cdot i_{n,GC}$ (path 2). Therefore, the combined noise voltage at the output can also be calculated as

$$v_{n,OUT}\big|_{M3,1} = \frac{R_P + sL_P(1-k)}{1 + sR_PC_P + s^2L_PC_P} \cdot \frac{1}{1+\alpha} i_{n,GC} \quad (6)$$

Considering the α number of gain control devices switched-on with identical assumptions as in (2) and (5), the approximated noise power given by $M_{3,1-3,\alpha}$ can be expressed as

$$\overline{v_{n,OUT}^2}\Big|_{M3,1-\alpha} \cong \frac{L_P^2(1-k)^2}{R_P^2C_P^2} \cdot \frac{\alpha}{(1+\alpha)^2} \overline{i_{n,GC}^2} \quad (7)$$

Similar to (5), the larger k of the transformer ensures less noise contribution from gain control devices in the low-gain modes. According to (3), (5), and (7), the overall noise factor (F) of the proposed VGLNA can be evaluated by assuming a perfect matching condition at the input, which is

$$\begin{aligned} F &\cong 1 + EF|_{M1} + EF|_{M2} + EF|_{M3,1-\alpha} \\ &\cong 1 + \frac{4\gamma}{g_{m1}R_S} + \frac{4\gamma g_{m2}(1-k)^2\alpha^2}{g_{m1}^2R_S(1+\alpha k)^2} + \frac{4\gamma g_{m2}(1-k)^2\alpha}{g_{m1}^2R_S(1+\alpha k)^2} \end{aligned} \quad (8)$$

where EF and γ denote the excess noise factor (indicating the noise contribution of each component) and excess noise coefficient of devices, respectively. As noticed from (8), in the absence of a load transformer ($k = 0$), the noise factor or NF is degraded significantly as α increases. By contrast, the added transformer between the main and current-steering stages mitigates NF degradation with the factor of$[(1-k)/(1+\alpha k)]^2$. Using (3) and (8), the voltage gains and NFs with respect to α and k were simulated and depicted in Figs. 4(a) and 4(b), respectively. As can be seen in Fig. 4, a lower gain is obtained as more gain control devices are switched-on (larger α). Further, a smaller k value increases the GCR of the VGLNA, thus indicating that fewer steered in-phase RF currents are induced in the output. Similarly, although NF is degraded as α increases, the amount of NF degradation can be diminished with the effect of k owing to noise cancellation effect.

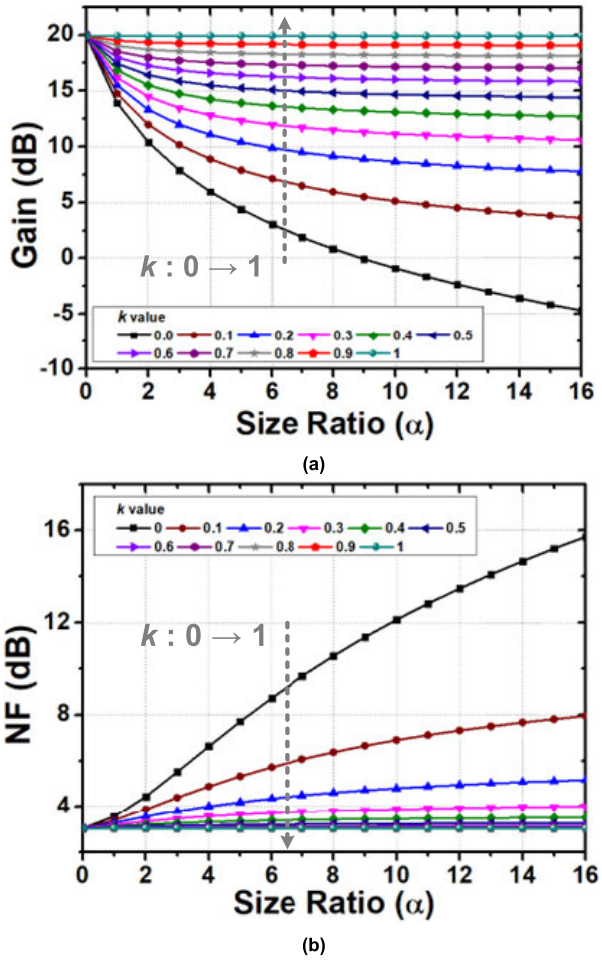

FIGURE 4. Calculated (a) gains and (b) NFs based on α and k (g_{m1} = 31 mS, g_{m2} = 4 mS, L_P = 160 pH, C_P = 200 fF, and Q_P = 12).

III. CIRCUIT IMPLEMENTATION

A detailed schematic of the implemented VGLNA is depicted in Fig. 5, which comprises a current-steering common-source amplifier stage with a transformer load and an output buffer stage. Herein, the four current-steering gain control

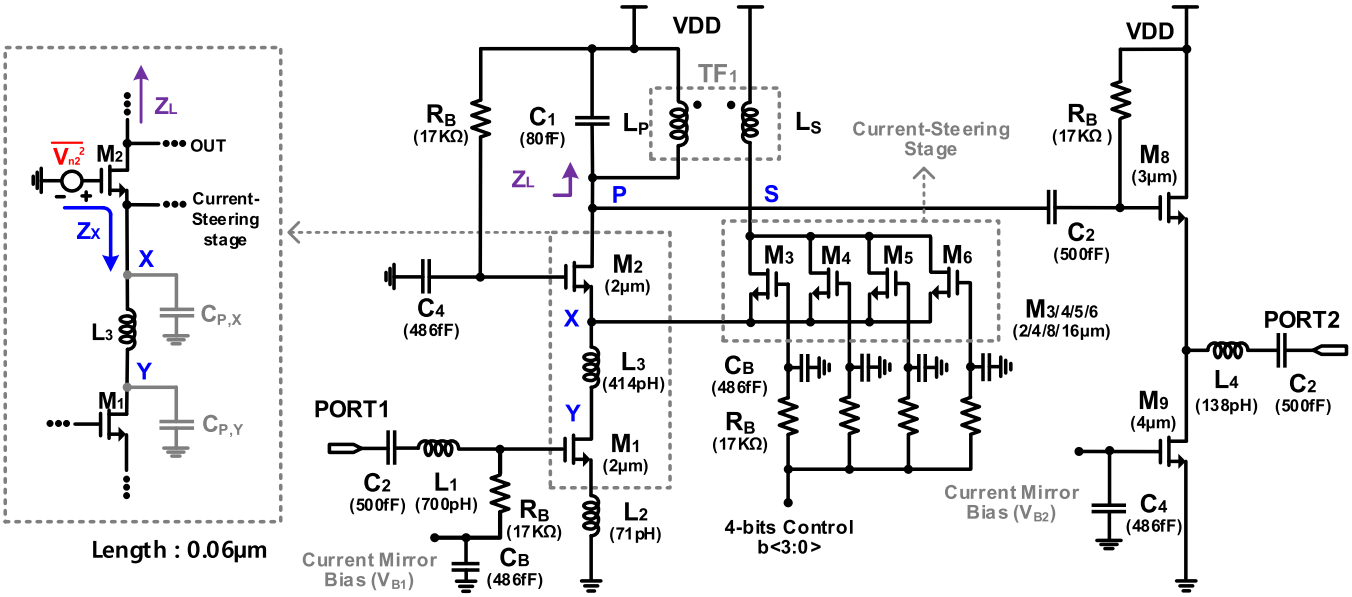

FIGURE 5. Schematic of the proposed variable gain low-noise amplifier adopting the transformer-based noise cancelling technique.

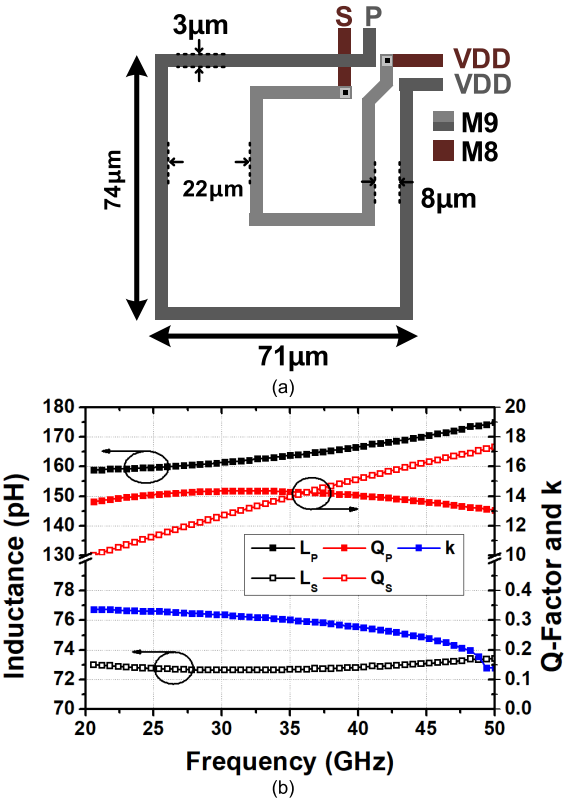

FIGURE 6. (a) layout and (b) simulation results of the implemented transformer design.

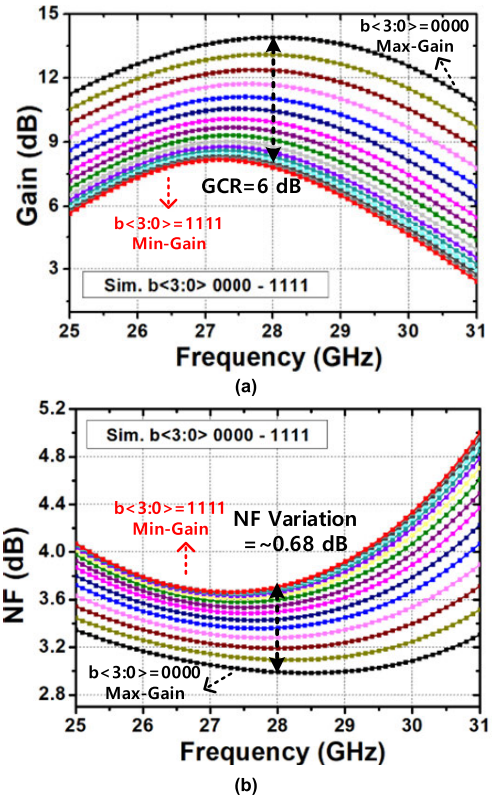

FIGURE 7. Simulation results of the implemented design adopting transformer-based noise cancelling technique: (a) gain and (b) noise figure.

devices (M_{3-6}) are utilized in parallel, which are managed by a binary-weighted four-bits control (b<3:0>). Input matching is performed using a conventional source degeneration inductor (L_2) and a series inductor (L_1) to achieve simultaneous power and noise matching conditions at operating frequency. In addition, the series inductor, L_3 is included as an inter-stage matching between the transconductance (M_1) and cascode (M_{2-6}) devices to further improve the

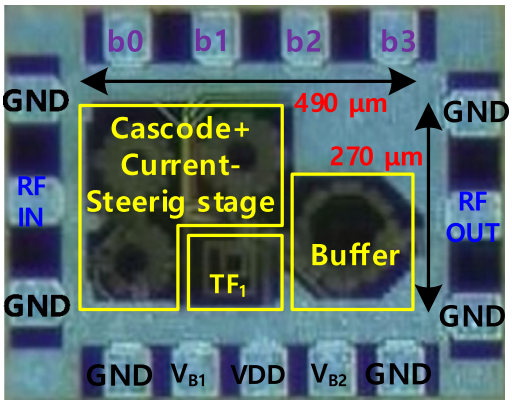

FIGURE 8. Chip microphotographs of the implemented VGLNA.

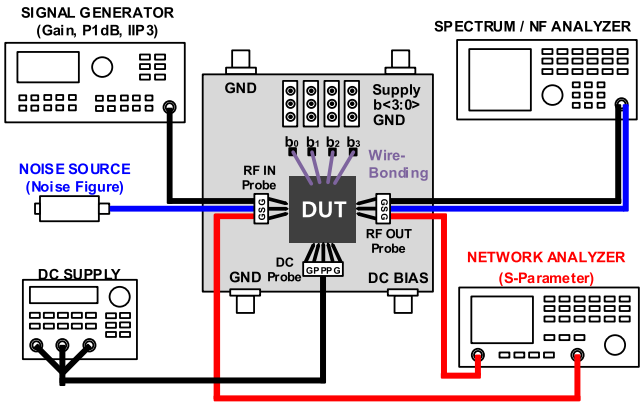

FIGURE 9. Measurement setup for characterization of the implemented VGLNA.

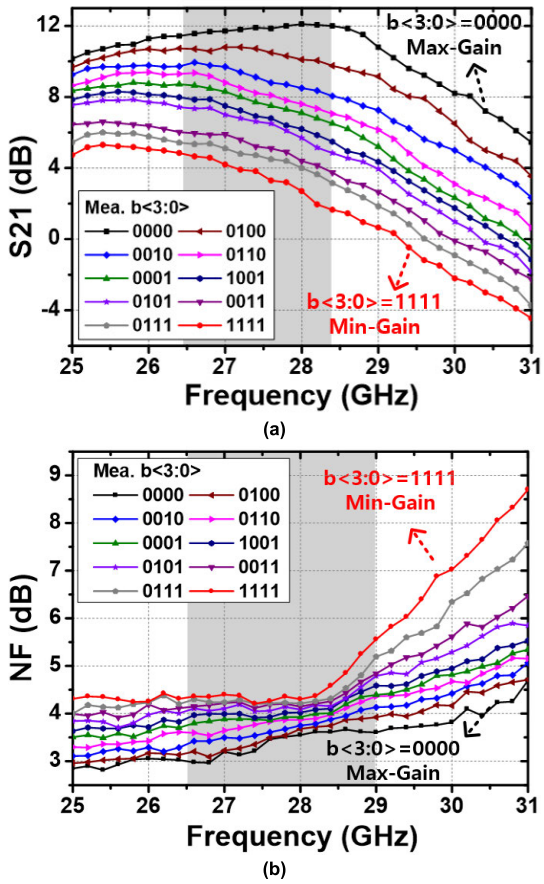

FIGURE 10. Measured (a) gains and (b) NFs with different gain settings.

gain and NF performance [22], [23], [24]. In reality, the noise contribution from the cascode device is considerable, particularly in the mmWave frequency bands, owing to the parasitic capacitance at the source node of

M_{2-6}. As shown in Fig. 5, the impedance (Z_X) looking into L_3 and the drain of M_1 at node X is evaluated as

$$Z_X(s) \cong \frac{1}{sC_{P,X}} || \left(sL_3 + r_{01} || \frac{1}{sC_{P,Y}} \right) \tag{9}$$

where $C_{P,X}$ and $C_{P,Y}$ denote the parasitic capacitances at nodes X and Y, respectively; and r_{o1} is the output impedance of M_1. Once the value of L_3 is determined to resonate with parasitic capacitive component at the operating frequency, Z_X can be maximized such that the noise contribution of M_2 can be minimal even in the max- gain mode. Herein, the transformer utilized at the load of the main and current-steering paths is designed and optimized with careful consideration of GCR and noise cancelling effect through electromagnetic (EM) simulations. Fig. 6 shows the layout and related simulation results for the designed load transformer (TF_1). The simulated values of the primary/secondary inductances and quality-factors (Q-factors) in the 28 GHz band are approximately 160.8/72.7 pH and 14.3/12.2, respectively. The coupling coefficient, k of approximately 0.3 is selected based on the GCR and level of NF degradation. The load capacitor (C_1) of 80 fF is also selected to realize the optimum resonance conditions according to the EM simulation results. In the second stage, the source-follower output buffer stage, which provides a solid output matching characteristic, is employed for test purposes. A series inductor (L_4) at the output further improves output matching by compensating for the output parasitic capacitance. Fig. 7 shows the simulated voltage gains and NFs of the designed amplifier with different control-bit settings. Evidently from Fig. 7, the simulated gain and NF in the max-gain mode are 13.9 dB and 2.9 dB, respectively. Moreover, a GCR of 6 dB and NF degradation of 0.68 dB are attained at the given design. Excluding the buffer stage, the NF variation between max- and minimum (min)-gain modes is reduced without the noise contribution from the buffer. All required EM simulations in this study were performed using the Cadence EMX tool.

IV. EXPERIMENTAL RESULTS

To validate the gain controllability and noise cancelling properties of the proposed design, a mmWave VGLNA employing the transformer was fabricated using a 65 nm CMOS process. Fig. 8 shows a chip microphotograph of the manufactured design, which occupies an active die size of 0.13 mm2 (0.49 mm × 0.27 mm), excluding bond pads. The design consumes a current of 10.6 mA with a nominal supply of 1 V.

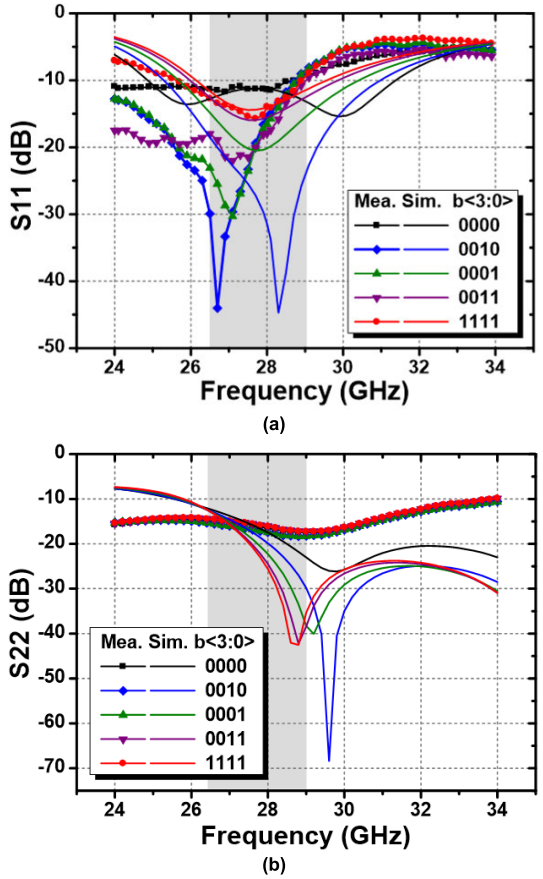

FIGURE 11. Measured and simulated (a) S11s and (b) S22s with different gain settings.

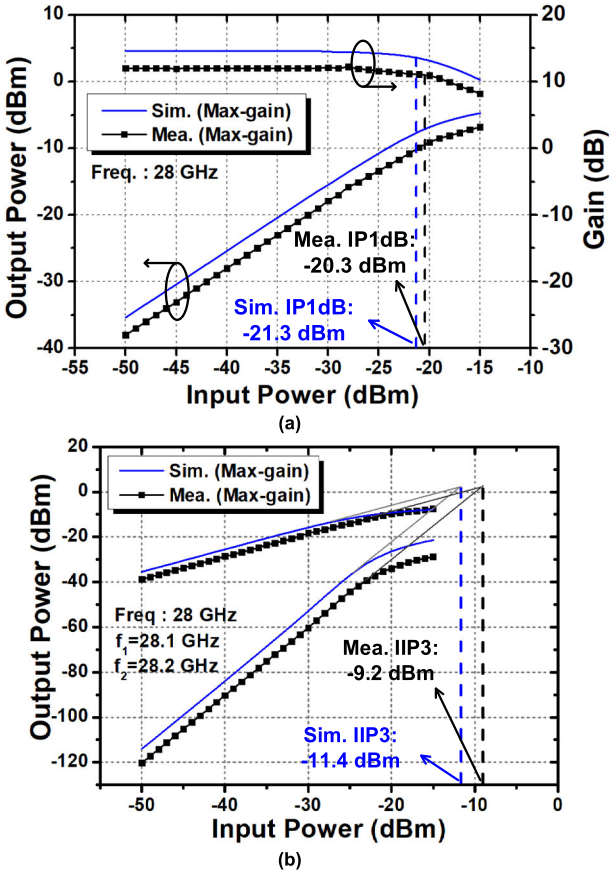

FIGURE 12. Measured and simulated (a) P1dB with an in-band tone of f_{IB} (f_{IB}=28GHz) and (b) IIP3 with two tones of f_1 and f_2 (f_1=28.1GHz and f_2=28.2GHz) in the max-gain mode.

For the characterization, signal path measurements were conducted at the input and output ports via on-wafer ground-signal-ground (GSG) RF probes, primarily for the center frequency of 28 GHz, which is targeted to n257 and n261 bands of 5G NR FR2 (26.5–29.5 GHz). The bias voltages, power, and ground for the design were supplied via a ground-power-ground (GPPPG) probe to diminish parasitic effects. The four-bits gain control voltages (b<3:0>) were separately applied from a printed circuit board through a wire bonding. Fig. 9 illustrates the measurement setup for performance evaluation of the implemented design. Fig. 10 shows the measured gains and NFs for 10 representative four-bits control settings. The obtained max- and min-gains at 28 GHz are approximately 12.1 dB and 2.7 dB respectively, which indicates a GCR of 9.4 dB. The corresponding NFs range from 3.55 to 4.3 dB. The lower coupling coefficient of the implemented transformer within the design may cause a slightly larger GCR and NF degradation, compared with the simulation results in Fig. 7. The measured and simulated input S11s and output S22s with different gain settings are also shown in Fig. 11. Owing to the limited reverse isolation at the input and output ports, matching conditions are relatively varied with different gain modes; however, observed S11s and S22s were less than –10 dB at the operating frequency of 25.7–29 GHz for all measured gain modes. In addition, to verify linearity performance of the design, an input 1-dB compression point (IP1dB) and input-referred third-order intercept point (IIP3) were measured in the max-gain mode which requires the most stringent requirements. Fig. 12 shows the measured and simulated IP1dBs and IIP3s with an in-band (IB) tone of f_{IB} ($f_{IB} = 28$ GHz) and two tones of f_1 and f_2 ($f_1 = 28.1$ GHz and $f_2 = 28.2$ GHz). The measured IP1dB and IIP3 are –20.5 dBm and –9.25 dBm at the max-gain, respectively. Moreover, it is noted that as the gain of the design is back-off, the linearity performance is improved correspondingly. The design draws a current of 10.6 mA (4.2 mA for the amplifier and 6.4 mA for the buffer) with a nominal supply of 1 V. Finally, the performance metrics of the proposed and other state-of-the-art VGA designs are summarized and compared in Table 1. In addition, the overall performances of the implemented VGAs for a given gain, GCR, NF, power, area, and linearity performance are evaluated using figure-of-merits (FOMs), which are defined as [28] and [29]

$$FOM_1 = \frac{Gain_{\max}[dB] \cdot GCR[dB]}{Power[mW] \cdot A[mm^2](NF[lin] - 1)} \quad (10)$$

$$FOM_2 = \frac{Gain_{\max}[abs] \cdot BW[GHz] \cdot IIP3[mW]}{Power[mW] \cdot A[mm^2] \cdot (NF[lin] - 1)} \quad (11)$$

TABLE 1. Comparison and Summary of Performance.

Ref.	Process (CMOS)	Gain Control Topology	Freq (GHz)	Gain (dB)	GCR (dB)	NF (dB)	Power (mW)	IP1dB* (dBm)	IIP3* (dBm)	Supply (V)	Chip Area (mm^2)	FOM_1 / FOM_2
[5]	65-nm	Resistive/inductive load control	30–34.5	20.8–10.2	10.6	3.71–4	16.5	–20.4	–10.8††	1.2	0.20	49.5 / 0.92
[13]	40-nm	Current-steering control	56–65	6.67–1.02	5.65	5.13–5.84	12.1	NA	–7.66	1.1	0.63**	2.2 / 0.19
[15]	65-nm	Current-steering control	17–26	18.5–4.5	14	4.1–7.5	67.2	NA	NA	1.2	0.19	12.9 / NA
[16]	65-nm	In- and out-of-phase signal control	20–43	14.5–(–7)	21.5	5.5–8.2	30.8	–16.5	–6.9††	1.1	0.34	11.7 / 0.93
[17]	65-nm	Transformer coupling-coefficient control	28†	18.2–12	6.2	3.9–4.1	9.8	–15	–5.4††	1	0.16	49.5 / NA
[25]	55-nm	Current-steering control	6.5–12	20.7–3.6	17.1	3.26*	75	–12.2	–2.6††	NA	0.98	4.3 / 0.4
[26]	40-nm	Digitally-assisted inductive load control	60†	19.8–6.5	13.3	5.98–7.54	18	–29.5	–19	1.1	0.22**	22.4 / 0.1
[27]	65-nm	NA	55-64	12.8	NA	3.6	8.8	–18.8	-9.2††	1	0.33**	NA / 1.26
This work	**65-nm**	**Current-steering with noise cancellation**	**25.7–29**	**12.1–2.7**	**9.4**	**3.6–4.3**	**10.6**	**–20.5**	**–9.2**	**1**	**0.13**	**63.9 / 0.9**

* At maximum-gain. ** Including pads. † Center frequency. †† Estimated IIP3 from IP1dB. § NA: Not Available.

where A represents a chip size, either including or excluding pads. As indicated in Table 1, the proposed VGLNA exhibits estimated FOM_1 and FOM_2 values of 63.9 and 0.9, respectively, which are better or comparable to those of other state-of-art VGA designs in the max-gain mode.

V. CONCLUSION

This study proposed and demonstrated a fully integrated CMOS VGLNA design that employs a transformer-based noise cancelling technique and its related analysis. The proposed design offers promising RF gain controllability with enhanced noise-reduction performance in low-gain mode. The implemented VGLNA is well-applicable for next-generation 5G NR multi-element phased-array receiver solutions, thereby offering low-cost and compact designs.

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