RESEARCH ARTICLE

A New PWM Operational Scheme for MicroLED Displays Using Inverter and Dynamic SWEEP Signal Slope for Low Gray Level Expression

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ABSTRACT In this paper, we present a novel pulse width modulation (PWM) operational scheme for micro-light-emitting-diode (μLED) displays using inverter and dynamic SWEEP signal slope. In the proposed PWM operational scheme, the slope of the SWEEP signal steepens as the gray level decreases. This adjustable SWEEP signal slope further shortens the falling time compared to the inverter-only strategy, leading to an exceptional capability to express extremely low gray levels. We implement the proposed scheme with a low-temperature poly-Si oxide (LTPO) thin-film transistor (TFT) pixel circuit and verify the operation through HSPICE based on measured TFT data. The simulation results show that the proposed scheme can significantly shorten the falling time to under 1 μs level. The gray level of 14 G is accurately expressed without wavelength shift or pulse distortion, achieving a falling time of 0.21 μs. In addition, we also verify the compensation accuracy of the pixel circuit, and the results indicate that the proposed pixel circuit can reliably compensate for TFT variations.

INDEX TERMS MicroLED, LTPO, TFT, pixel circuit, PWM, inverter, falling time, low gray level.

I. INTRODUCTION

The micro-light-emitting-diode (μLED) displays can achieve higher resolution, lower power consumption, and enhanced temperature stability compared to OLED displays [1], [2], [3], [4]. In particular, μLEDs utilize inorganic materials in their emissive layer, so they can be free from burn-in issues [5], [6], [7]. However, the wavelength of μLED's light can shift depending on its current density, resulting in color distortion [8], [9], [10]. Therefore, pulse width modulation (PWM) driving, which adjusts the emission period with a constant current to express gray levels, must be applied to μLED displays [5], [11], [12], [13], [14].

When implementing PWM driving with a pixel circuit, a ramp signal called SWEEP is commonly used to control

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the switching of the driving thin-film transistor (DRT) in the PWM part. The switching of DRT in the PWM part directly affects the operation of DRT in the constant current generation (CCG) part, causing the CCG part to cease supplying current to the μLED. However, this SWEEP signal-based approach inherently exhibits a falling time of several hundred microseconds until the current ceases to flow, since DRT in the PWM part does not function as an ideal switch and the SWEEP signal also has a certain slope [12].

This falling time of several hundred microseconds poses a critical limitation to grayscale expression, especially for low gray levels where the emission period is shorter than the falling time. Generally, approximately at 60 to 90 gray levels (G), the peak current starts to reduce, and the falling time decreases with a deteriorated current waveform [14], [15], [16]. These results indicate that the operation does not proceed as intended. Therefore, reducing the falling time
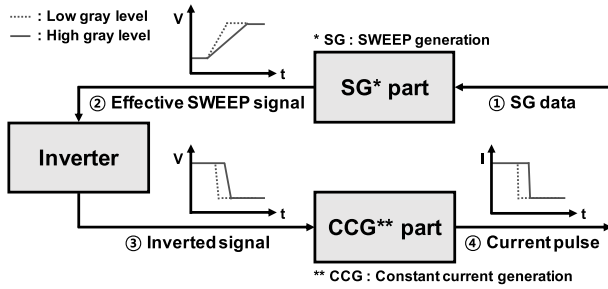
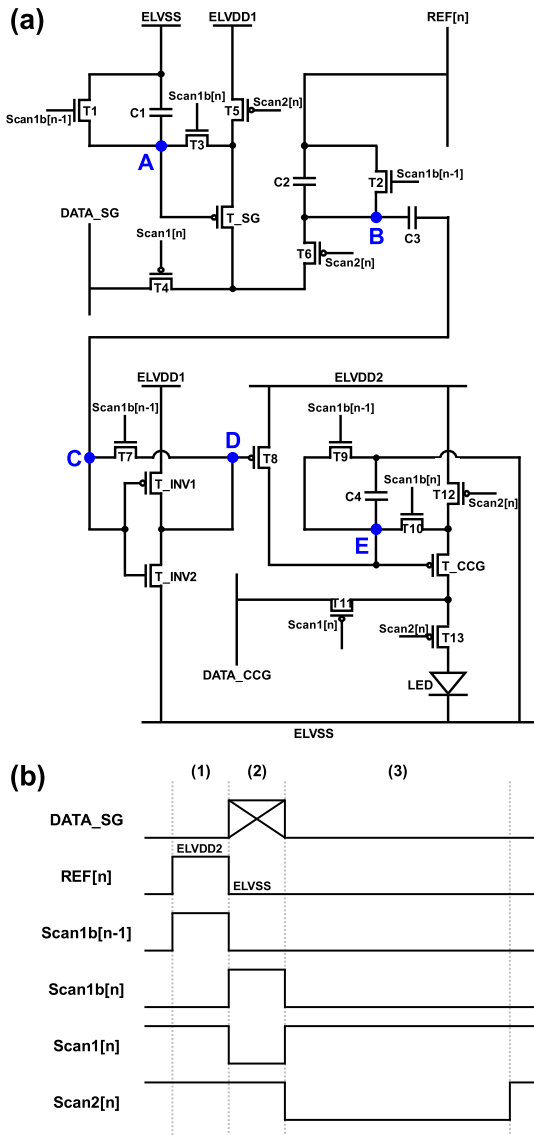**FIGURE 1.** Block diagram of the proposed PWM operational scheme using inverter and dynamic SWEEP signal slope.

FIGURE 2. (a) 17T4C LTPO pixel circuit structure and (b) signal timing diagram to implement the proposed PWM operational scheme.

TABLE 1. Operational conditions of the proposed circuit.

Circuit Operating Conditions			
ELVDD1	10 V	T1-T11	3 μm/3 μm
ELVDD2	7.2 V	T12, T_CCG	24 μm/3 μm
ELVSS	-2 V	T13	12 μm/3 μm
V_{GH} / V_{GL}	12 V / -9 V	T_SG	3 μm/24 μm
V_{H_REF} / V_{L_REF}	7.2 V / -2 V	T_INV1, T_INV2	3 μm/3 μm
V_{DATA_CCG}	1.8 V	C1, C3, C4	400 fF
V_{DATA_SG}	2 V ~ 10 V	C2	1 pF

time is significantly shortened. However, even when the inverter is employed, we have confirmed that the limitation imposed by the falling time still exists for expressing gray levels below 37 G. Consequently, we have concluded that an improved PWM operational scheme, which adjusts the slope of the SWEEP signal itself based on the gray level, must be additionally applied for the accurate expression of extremely low gray levels.

In this paper, we propose a novel PWM operational scheme for μLED displays using inverter and dynamic SWEEP signal slope. The proposed scheme can dynamically adjust the slope of the SWEEP signal itself depending on the gray level. We utilize our previously suggested SWEEP generation method using linear charging of a capacitor [19], [20] to adjust the slope of the SWEEP signal. This scheme can significantly shorten the falling time since the slope of the SWEEP signal steepens as the gray level becomes lower [12]. We introduce low temperature poly-Si oxide (LTPO) thin-film transistor (TFT) pixel circuit to implement the proposed PWM operational scheme. Since the suggested circuit is based on the LTPO technology, it can take advantage of both the high current driving capability of low-temperature poly-Si (LTPS) TFTs and the low off current of amorphous In-Ga-Zn-oxide (a-IGZO) TFTs. In addition, the LTPO technology enables the implementation of a high-performance inverter with better efficiency compared to using either n-type or p-type TFT alone. We verified the circuit operation through HSPICE and confirmed its capability to express gray levels down to 14 G range.

II. PROPOSED PWM OPERATIONAL SCHEME

Fig. 1 shows the block diagram of the proposed PWM operational scheme using inverter and dynamic SWEEP signal slope, conceptually demonstrating the functions and operation sequence of each part. The 17T4C LTPO pixel circuit structure and signal timing diagram to implement the proposed scheme are shown in Fig. 2. The pixel circuit is structured with three main parts: the sweep generation (SG) part, inverter, and CCG part. The SG part and inverter, which consist of T1-T7, T_SG, T_INV1, T_INV2, and C1-C3, function as a conventional PWM part that adjusts the emission period. The CCG part consists of T8-T13, T_CCG, and C4, and supplies a constant current to μLED. Meanwhile, the switching TFTs connected to the storage capacitors,

emerges as the most crucial challenge for reliable grayscale expression in μLED displays.

Recently, an inverter has been adopted in the PWM part to shorten falling time [17], [18]. When the SWEEP signal passes through the inverter, its slope steepens, so the falling
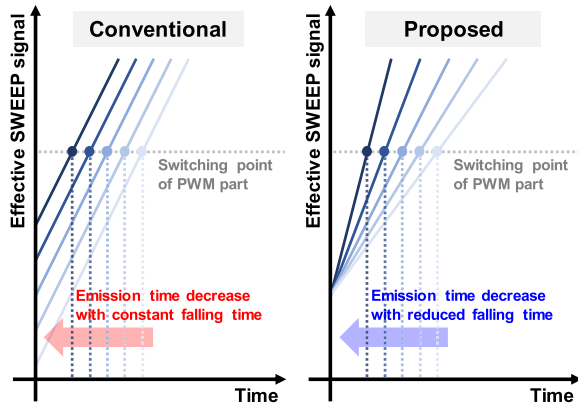
FIGURE 3. The conceptual schematic of the conventional and proposed PWM operational schemes.

T1-T3, T7, T9, and T10, utilize a-IGZO TFTs, while other TFTs utilize LTPS TFTs. Detailed operational conditions about the dimensions of TFTs, capacitance of the capacitors, and operating voltage are specified in Table 1. In this study, we employed two DC power sources, ELVDD1 and ELVDD2, whose voltage difference is 2.8 V, to ensure a stable turn-off state for T8 during the emission period of μLED.

The operation of the suggested pixel circuit is divided into three stages: (1) initialization and inverter compensation, (2) SG and CCG part compensation, and (3) emission. The operational principles are described as follows:

(1) Initialization and inverter compensation stage: The Scan1b[n-1] signal is set to a high level, so T1, T2, T7, and T9 are turned on. Then, the voltage at nodes A and E is reset to ELVSS, and the voltage at node B is reset to ELVDD2, the high level of the REF[n] signal. Additionally, as the input node of the inverter, node C, and its output node, node D, are connected through T7, the switching threshold (V_m) of the inverter, defined at $V_C = V_D$, is sensed at both nodes.

(2) SG and CCG part compensation stage: The Scan1b[n-1] and Scan1[n] signals are set to a low level, and the Scan1b[n] signal is set to a high level. Consequently, T1, T2, T7, and T9 are turned off, and T3, T4, T10, and T11 are turned on. As current flows through C1 and C4, the voltage at nodes A and E increases to $V_{DATA\_SG}[n] - V_{TH\_SG}$ and $V_{DATA\_CCG} - V_{TH\_CCG}$, respectively. Here, V_{TH_SG} and V_{TH_CCG} represent the threshold voltage of T_SG and T_CCG, respectively. Meanwhile, the REF[n] signal is set to a low level, ELVSS, so the voltage at nodes B and C decreases to ELVSS and V_m + ELVSS – ELVDD2, respectively. Then, T_INV1 is turned on and the voltage at node D becomes ELVDD1. As a result, T8 remains in the off-state throughout this stage.

(3) Emission stage: The Scan1b[n] and Scan2[n] signals are set to a low level, and the Scan1[n] signal is set to a high level. Consequently, T3, T4, T10, and T11 are turned off, and T5, T6, T12, and T13 are turned on.

As the current of T_SG flows through C2, the voltage at node B linearly rises over time, functioning as a conventional SWEEP signal. At the same time, the voltage at node C also rises along with node B voltage by charge conservation. When the voltage at node B reaches ELVDD2 and the voltage at node C exceeds V_m, T_INV1 turns off and T_INV2 turns on. Then, the voltage at node D becomes ELVSS, causing T8 to turn on. Subsequently, the voltage at node E becomes ELVDD2. Hence, the source-to-gate voltage (V_{SG}) of T_CCG becomes smaller than its threshold voltage. As a result, T_CCG ceases supplying current to the μLED.

Fig. 3 compares the conventional and proposed PWM operational schemes. In the conventional operation scheme, the SWEEP signal applied to the PWM part maintains a constant slope while the starting voltage varies depending on the gray level. A higher starting point leads to a shorter emission period, yet the falling time remains unchanged due to the constant slope of the SWEEP signal. In contrast, the proposed operation scheme changes the slope of the SWEEP signal, so both the emission period and falling time can be varied according to the gray level. For example, as the current of T_SG increases, the voltage at node B rises more rapidly. This leads to a shorter emission period since the voltage at node C exceeds V_m more quickly. Additionally, the faster rise in node B voltage induces a swifter switching of the inverter output, contributing to a significant reduction in falling time. Therefore, by employing the proposed PWM operational scheme, a change in falling time depending on the gray level can be implemented. The effect of enhancing grayscale expression accuracy through adjustable falling time is especially noticeable at extremely low gray levels.

Meanwhile, the proposed PWM operational scheme offers a substantial advantage regarding the complexity of the peripheral circuit. The conventional PWM scheme uses an integrator or employs a highly dense staircase function to generate a SWEEP signal, demanding extra power sources and circuitry components in the peripheral circuit. The burden of the peripheral circuit can significantly increase with progressive emission, where separate SWEEP signals shifted by 1 H time are necessary for each horizontal line. However, the proposed PWM operational scheme generates a SWEEP signal within a pixel circuit and eliminates the need for the aforementioned extra elements. As a result, the complexity of the peripheral circuit would greatly decrease with our proposed PWM operational scheme.

On the other hand, despite the simplified peripheral circuit, the proposed scheme would consume higher power because each pixel generates a SWEEP signal individually. This power consumption can be optimized by reducing the size of C2 and lowering I_{SG}, but achieving low power consumption is still challenging with this scheme. The trade-off between power consumption and maximizing the capability to express extremely low gray levels should be carefully considered depending on the product specification. We expect
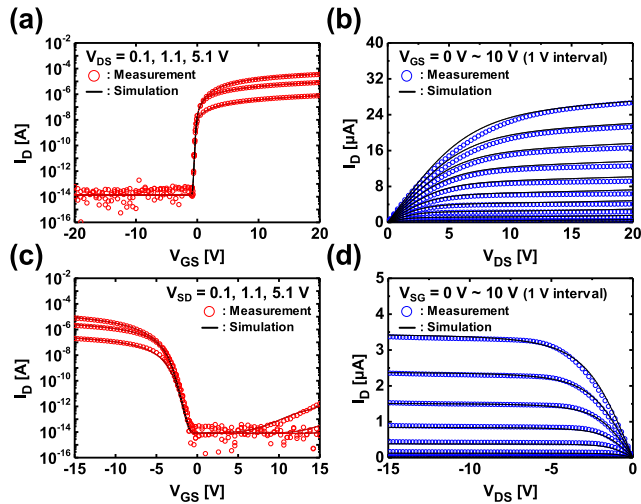
FIGURE 4. Measured and simulated (a) transfer characteristic, and (b) output curves of a-IGZO TFT with a size of 24 μm/21 μm, and measured and simulated (c) transfer characteristic, and (d) output curves of p-type LTPS TFT with a size of 30 μm/400 μm.

that the proposed PWM operational scheme will be highly applicable in large-sized displays that have a direct power source connection.

III. RESULTS AND DISCUSSION

We simulated the operation of the suggested μLED pixel circuit using HSPICE from Synopsys. For the reliable simulation, we developed a-IGZO and LTPS TFT model libraries based on the measured electrical properties. The measured threshold voltage (V_{TH}), mobility, and subthreshold swing (SS) of a-IGZO TFT were −0.46 V, 17.7 cm²/V·s, and 81.6 mV/dec, respectively. Similarly, for LTPS TFT, the values were −1.53 V, 80.1 cm²/V·s, and 396.6 mV/dec, respectively. The developed libraries exhibit high accuracy with a coefficient of determination (R2) over 0.9996, as shown in Fig. 4. Fig. 5 shows the simulated transient waveforms of the SWEEP signal and μLED current. The simulation is performed for a modular-type 480 × 270 resolution display panel with a refresh rate of 120 Hz, thus one horizontal time (H time) is set to 30.7 μs. It is important to note that the rise in node B voltage cannot exhibit perfect linearity, as the source-to-drain voltage (V_{SD}) of T_SG decreases over time. However, since T_SG is designed with an elongated channel length to maintain adequate saturation, the linearity remains almost ideal until the voltage at node C exceeds V_m, as shown in Fig. 5(a).

On the contrary, at extremely low gray levels below 20 G, where V_{DATA_SG} is very small, T_SG cannot operate in the saturation region during SWEEP generation. We anticipated that this operation in the linear region of T_SG could significantly degrade the linearity of the SWEEP signal. However, even for the SWEEP signal generated for extremely low gray levels, it exhibited decent linearity comparable to that observed at high gray levels until the voltage at node C exceeds V_m, as shown in Fig. 5(b). This result
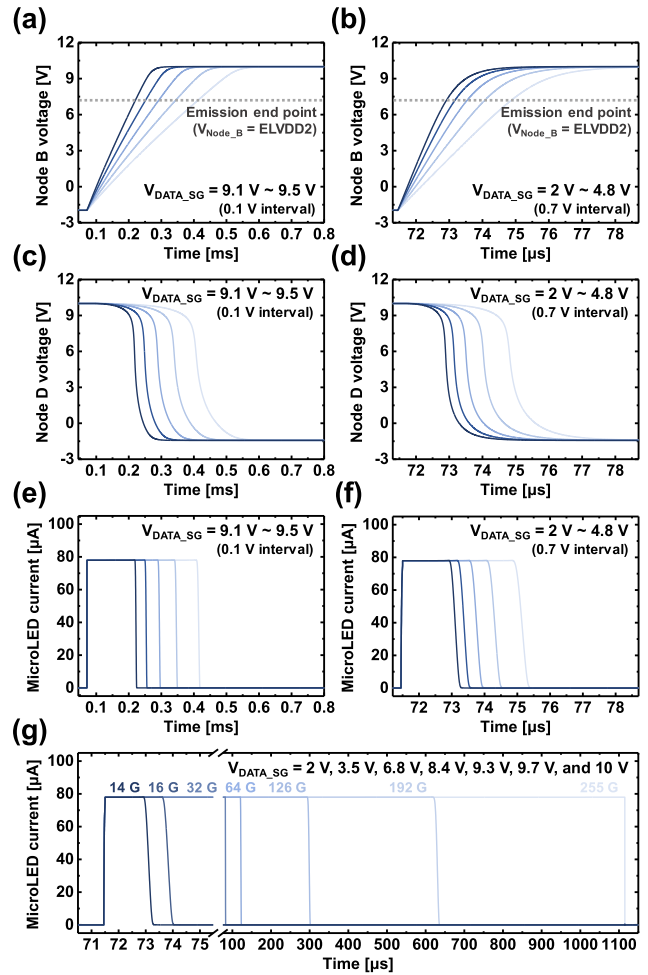
FIGURE 5. Simulated transient waveforms of the generated SWEEP signals at (a) high gray levels, and (b) extremely low gray levels, and corresponding operation curves of an inverter at (c) high gray levels, and (d) extremely low gray levels. Resulting μLED current at (e) high gray levels, (f) extremely low gray levels, and (g) all gray levels.

can be attributed to the short SWEEP generation period for extremely low gray levels. In Fig. 5(a) and (b), the emission end point, where the voltage at node B reaches ELVDD2 and inverter switches, is expressed as a dashed line.

The operation curves of an inverter when the SWEEP signals depicted in Fig. 5(a) and (b) are applied are shown in Fig. 5(c) and (d). The resulting current pulse waveforms flowing through the μLED are shown in Fig. 5(e), (f), and (g). In this study, the maximum emission period is set to thirty-four H time, approximately 1 ms. However, the maximum emission period can be extended up to 8.333 ms, an entire frame time of 120 Hz refresh rate, by expanding the V_{GL} period of the Scan2[n] signal and increasing V_{DATA_SG} up to 10.5 V. Under the operational condition with an emission period of 1 ms, the suggested pixel circuit could be applied to TV or indoor signage requiring luminance of several hundred nits. If the emission period is extended up to the entire frame time using the aforementioned method, the circuit could also be utilized for outdoor signage requiring
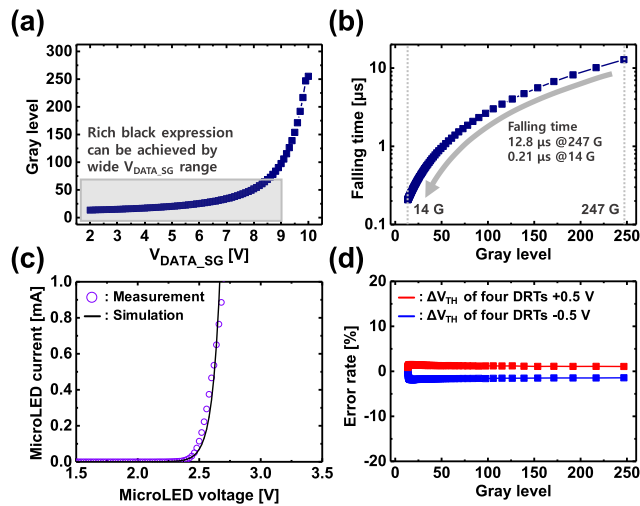
FIGURE 6. (a) Gray level according to V_{DATA_SG}, and (b) falling time according to gray level. (c) Measured and simulated current-voltage characteristic of μLED, and (d) compensated current error rates.

TABLE 2. Comparison of the proposed pixel circuit and other works.

	Inverter	SWEEP Signal	CCG part Compensation	Transition Time (μs)*
[12]	Not used	Needed	O	200**
[13]	Not used	Needed	O	200
[14]	Not used	Needed	O	300
[17]	1 Used	Needed	O	20
[18]	2 Used	Needed	X	3
Proposed	1 Used	Not needed	O	~ 0.21

* : Falling [12]-[17] or rising time [18] depending on PWM operation.
** : Estimated from the transient current waveform in the paper.

luminance of several thousand nits due to the increase in average brightness.

Fig. 6(a) shows the variation in gray levels corresponding to V_{DATA_SG}. As V_{DATA_SG} decreases, the current of T_SG rapidly increases in accordance with the transistor's current equation. Consequently, the gray level significantly changes in middle to high gray levels. In this study, the lowest data voltage difference between each gray level is approximately 3 mV, which exceeds one least significant bit (1 LSB) of a 10-bit digital-to-analog converter (DAC) [21], [22]. However, the rate of change is gradually reduced as the operation of T_SG shifts to the linear region. This characteristic enables the utilization of a broader data range for expressing low gray levels. Considering that conventional OLED displays tried to expand the data range for low gray levels to achieve deep and rich black expression [23], [24], the proposed pixel circuit is expected to offer significant advantages for the precise expression of low gray levels. Fig. 6(b) shows the falling time variation corresponding to V_{DATA_SG}. The falling time is calculated as the time between the 90% point and the 10% point of the peak current and is extracted approximately 12.8 μs at 247 G, and 0.21 μs at 14 G. If only the inverter had been employed without changing the slope of the SWEEP signal,

the falling time would remain around 12.8 μs, even for low gray levels. Consequently, it would be impossible to express gray levels below 34 G, given that the emission period at 34 G is about 12.5 μs. Therefore, in order to achieve the expression of extremely low gray levels down to the 14 G range, the proposed PWM operational scheme of changing the slope of the SWEEP signal must be applied.

Meanwhile, the mentioned lowest gray level, 14 G, can further decrease by modulating the operating voltage condition or increasing the emission period. If the operating voltage condition is adjusted in the direction of reducing ELVSS, V_{DATA_SG} range can be extended to even lower value, enabling the expression of lower gray levels. We have confirmed that the achievable lowest gray level can decrease to 11 G by reducing ELVSS to -6 V. Furthermore, if the total emission period is extended to 8 ms, the achievable lowest gray level even decreases to 4 G. Also, there is another approach to maximize the capability to express low gray levels. If the control signal applied to T12 and T13, related to the start point of emission, is separately applied and turned on a few microseconds after the Scan2[n] signal applied to T5 and T6, related to the start point of SWEEP generation, the emission start point can be customized to the desired timing. As a result, there is no need to significantly decrease V_{DATA_SG} to express extremely low gray levels. This approach effectively enables the expression of much lower gray levels with a minimized data range.

Fig. 6(c) shows the current-voltage characteristics of the μLED device used in the simulations. Fig. 6(d) shows the current errors when V_{TH} of T_SG, T_CCG, T_INV1, and T_INV2 are all shifted by ± 0.5 V. Although V_{TH} variations could differ depending on the TFT type, we aimed to verify the stability of the proposed circuit under conditions where both LTPS and IGZO TFTs experience substantial V_{TH} variations simultaneously. For this purpose, we applied an equivalent V_{TH} shift of 0.5 V to both types of TFTs. Even under the V_{TH} variation in these four TFTs, the current error rates remained below approximately 1.8%, confirming the reliable compensation capability of the proposed pixel circuit in addition to its outstanding performance in expressing low gray levels. The PWM operational scheme and accuracy of the proposed μLED pixel circuit are compared with that of other previously published papers in Table 2.

The papers [12], [13], and [14] propose μLED pixel circuits with the conventional PWM operational method. Their operations are highly effective but have a critical limitation of a very long falling time, approximately hundreds of microseconds. As a result, they cannot inherently express the mid to low gray levels, typically 80 G or less. To overcome such a long falling time, papers [17] and [18] employed an inverter. While the paper [17] introduces a pixel circuit based on an inverter, it still exhibits a falling time of about 20 μs. Consequently, it cannot express low gray levels below approximately 40 G. The paper [18] proposes a compact pixel circuit based on two inverters. However, in this circuit, the second inverter does not compensate

for V_m. Furthermore, although the pixel circuit in [18] utilizes two inverters, it still exhibits a current transition time of around 3 μs. Therefore, they cannot accurately express extremely low gray levels as the proposed circuit can.

Meanwhile, pixel circuits in papers [12], [13], [14], [17], and [18] require external input of SWEEP signals for PWM operation, so the peripheral circuits need to have extra power sources and circuitry components to generate SWEEP signals. The burden imposed by these additional elements significantly increases in progressive emission, where a separate SWEEP signal shifted by 1 H time is required for each horizontal line. Hence, pixel circuits in papers [14], [17], and [18] should consider the highly increased complexity of peripheral circuits for practical implementation. In contrast, the proposed PWM operational scheme generates a SWEEP signal within a pixel circuit. The proposed scheme can eliminate the need for external input of SWEEP signals, and substantially reduce the complexity of the peripheral circuits.

Our paper prioritizes introducing the new PWM circuit operation based on the inverter and the adjustable SWEEP signal slope to overcome the existing bottlenecks of the μLED pixel circuit, rather than proposing the compact pixel circuit. In addition, there is definite potential for further reducing the number of transistors by adopting other circuit structures in implementing the proposed scheme. Therefore, we did not primarily focus on the compactness of the circuit in this work.

IV. CONCLUSION

In this paper, we proposed a novel PWM operational scheme for μLED displays using inverter and dynamic SWEEP signal slope. In the proposed scheme, the slope of the SWEEP signal dynamically steepens as the gray level decreases. This adjustable SWEEP signal slope effectively complements the inverter-only strategy in reducing the falling time. We implemented the proposed scheme with an LTPO TFT pixel circuit, consisting of the SG part, inverter, and CCG part. The SG part and inverter together function as the conventional PWM part in previous μLED pixel circuits. The circuit operation was verified through HSPICE by Synopsys, and the results showed that the falling time was significantly shortened with the adoption of the dynamic SWEEP signal slope. Notably, an extremely low gray level of 14 G was accurately expressed with a falling time of 0.21 μs. Meanwhile, the compensation accuracy of the pixel circuit was also verified by shifting V_{TH} of T_SG, T_CCG, T_INV1, and T_INV2 by ± 0.5 V. The results indicate that current error rates remained below approximately 1.8%. Therefore, we expect that the proposed PWM operational scheme will be indispensable for next-generation μLED displays that demand exceptional low gray expression.

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REFERENCES

[1] Z. Y. Fan, J. Y. Lin, and H. X. Jiang, "III-nitride micro-emitter arrays: Development and applications," *J. Phys. D, Appl. Phys.*, vol. 41, no. 9, May 2008, Art. no. 094001, doi: 10.1088/0022-3727/41/9/094001.

[2] T. Wu, C.-W. Sher, Y. Lin, C.-F. Lee, S. Liang, Y. Lu, S.-W. Huang Chen, W. Guo, H.-C. Kuo, and Z. Chen, "Mini-LED and micro-LED: Promising candidates for the next generation display technology," *Appl. Sci.*, vol. 8, no. 9, p. 1557, Sep. 2018, doi: 10.3390/app8091557.

[3] H.-A. Ahn, S.-K. Hong, and O.-K. Kwon, "An active matrix micro-pixelated LED display driver for high luminance uniformity using resistance mismatch compensation method," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 65, no. 6, pp. 724–728, Jun. 2018, doi: 10.1109/TCSII.2018.2790412.

[4] C.-J. Chen, H.-C. Chen, J.-H. Liao, C.-J. Yu, and M.-C. Wu, "Fabrication and characterization of active-matrix 960 *times* 540 blue GaN-based micro-LED display," *IEEE J. Quantum Electron.*, vol. 55, no. 2, pp. 1–6, Apr. 2019, doi: 10.1109/jqe.2019.2900540.

[5] J.-H. Kim, S. Shin, K. Kang, C. Jung, Y. Jung, T. Shigeta, S.-Y. Park, H. S. Lee, J. Min, J. Oh, and Y.-S. Kim, "15-1: PWM pixel circuit with LTPS TFTs for micro-LED displays," *SID Symp. Dig. Tech. Papers*, vol. 50, no. 1, pp. 192–195, Jun. 2019, doi: 10.1002/sdtp.12887.

[6] J. Ok, Y. Yu, J.-Y. An, S. Na, W. Jang, H.-W. Lim, and J.-Y. Lee, "Distinguished paper: A multi-unit compensation for OLED burn-in in mobile displays," *SID Symp. Dig. Tech. Papers*, vol. 52, no. 1, pp. 165–168, May 2021, doi: 10.1002/sdtp.14637.

[7] J. Kim, J. Ko, J. Park, G. Jeong, H. Maeng, S. Park, and W. Choe, "35-4: A compensation algorithm for degradation in AMOLED displays," *SID Symp. Dig. Tech. Papers*, vol. 49, no. 1, pp. 445–448, May 2018, doi: 10.1002/sdtp.12596.

[8] Z. Gong, S. Jin, Y. Chen, J. McKendry, D. Massoubre, I. M. Watson, E. Gu, and M. D. Dawson, "Size-dependent light output, spectral shift, and self-heating of 400 nm InGaN light-emitting diodes," *J. Appl. Phys.*, vol. 107, no. 1, Jan. 2010, Art. no. 013103, doi: 10.1063/1.3276156.

[9] C.-C. Lin, Y.-H. Fang, M.-J. Kao, P.-K. Huang, F.-P. Chang, L.-C. Yang, and C.-I. Wu, "59-2: Invited paper: Ultra-fine pitch thin-film micro LED display for indoor applications," *SID Symp. Dig. Tech. Papers*, vol. 49, no. 1, pp. 782–785, May 2018, doi: 10.1002/sdtp.12373.

[10] D.-H. Kim, Y. S. Park, D. Kang, K.-K. Kim, T.-Y. Seong, and H. Amano, "Combined effects of V pits and chip size on the electrical and optical properties of green InGaN-based light-emitting diodes," *J. Alloys Compounds*, vol. 796, pp. 146–152, Aug. 2019, doi: 10.1016/j.jallcom.2019.05.070.

[11] C.-L. Lin, Y.-C. Chen, J.-H. Chang, Y.-S. Lin, S.-C. Chen, M.-H. Lee, and C.-Y. Chang, "AM mini-LED backlight driving circuit using PWM method with power-saving mechanism," *IEEE J. Electron Devices Soc.*, vol. 10, pp. 256–262, 2022, doi: 10.1109/JEDS.2022.3157935.

[12] P.-A. Zou, Y.-G. Xu, C. Liu, L.-R. Zhang, J.-H. Zhang, Y.-K. Yuan, W. Cai, S.-H. Han, L. Zhou, M. Xu, L. Wang, W.-J. Wu, and J.-B. Peng, "A new analog PWM pixel circuit with metal oxide TFTs for micro-LED displays," *IEEE Trans. Electron Devices*, vol. 69, no. 8, pp. 4306–4311, Aug. 2022, doi: 10.1109/TED.2022.3178363.

[13] J. Oh, J.-H. Kim, J. Lee, E. K. Jung, D. Oh, J. Min, H. Im, and Y.-S. Kim, "Pixel circuit with P-type low-temperature polycrystalline silicon thin-film transistor for micro light-emitting diode displays using pulse width modulation," *IEEE Electron Device Lett.*, vol. 42, no. 10, pp. 1496–1499, Oct. 2021, doi: 10.1109/LED.2021.3107152.

[14] E. K. Jung, S.-H. Ahn, S. Hong, H. Im, and Y.-S. Kim, "Micro light-emitting diode pixel circuit based on indium–gallium–zinc oxide thin-film transistors using pulse width modulation," *IEEE Electron Device Lett.*, vol. 44, no. 9, pp. 1484–1487, Sep. 2023, doi: 10.1109/led.2023.3297689.

[15] Y.-H. Hong, E. K. Jung, H. Im, and Y.-S. Kim, "Improvement of the low gray-level expression using hybrid pulse width modulation and pulse amplitude modulation driving method for a micro light-emitting diode pixel circuit," *J. Inf. Display*, vol. 23, no. 4, pp. 243–249, Oct. 2022, doi: 10.1080/15980316.2022.2084464.

[16] Y.-H. Hong, E. K. Jung, Y.-R. Jeong, H. Im, and Y.-S. Kim, "Micro light-emitting diode pixel circuit based on P-type low-temperature polycrystalline silicon thin-film transistor for mobile displays," *IEEE Trans. Electron Devices*, vol. 70, no. 9, pp. 4662–4668, Sep. 2023, doi: 10.1109/TED.2023.3296068.

[17] Y. Liu, S. Que, Z. Song, J. Fu, X. Zheng, C. Liao, X. Wang, L. Lu, and S. Zhang, ''38.2: An accurate and stable PWM pixel circuit based on LTPO TFTs for AM-micro-LED display,'' *SID Symp. Dig. Tech. Papers*, vol. 54, no. S1, pp. 242–245, Apr. 2023, doi: 10.1002/sdtp.16273.

[18] J. Kim, H. Lee, M. Jeong, J. Bae, C. Park, and J. Jang, ''Micro-LED pixel circuit using low-temperature poly-Si oxide TFTs with fast rise and fall times of pulse width modulation for low gray expression,'' *IEEE Electron Device Lett.*, vol. 44, no. 9, pp. 1448–1451, Sep. 2023, doi: 10.1109/led.2023.3299958.

[19] K.-S. Kang, J.-H. Park, C. Park, and S.-Y. Lee, ''A new line-by-line SWEEP signal generation method for PWM driving microLED TFT pixel circuit,'' *SID Symp. Dig. Tech. Papers*, vol. 54, no. 1, pp. 70–73, Jun. 2023, doi: 10.1002/sdtp.16490.

[20] K.-S. Kang, J.-H. Park, C. Park, and S.-Y. Lee, ''A new compact progressive emission microLED pixel circuit with only three scan signals,'' in *Proc. 23rd Int. Meeting Inf. Display (IMID)*, Aug. 2023.

[21] C.-W. Lu, P.-Y. Yin, and M.-Y. Lin, ''A 10-bit two-stage R-DAC with isolating source followers for TFT-LCD and AMOLED column-driver ICs,'' *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 27, no. 2, pp. 326–336, Nov. 2018, doi: 10.1109/TVLSI.2018.2876638.

[22] C.-W. Lu and L.-C. Huang, ''A 10-bit LCD column driver with piecewise linear digital-to-analog converters,'' *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 371–378, 2008, doi: 10.1109/jssc.2007.914274.

[23] T. Nishiyama, K. Tanaka, K. Yamamoto, K. Yamamoto, S. Uchida, R. Yonebayashi, T. Miyamoto, M. Hosokawa, and H. Katoh, ''P-31: Pixel circuit with backgate feedback for deep and rich black expressions on light-emitting display,'' *SID Symp. Dig. Tech. Papers*, vol. 50, no. 1, pp. 1329–1332, Jun. 2019, doi: 10.1002/sdtp.13180.

[24] B. Liu, D. Ding, T. Zhou, and M. Zhang, ''P-53: A novel pixel circuit providing expanded input voltage range for OLEDoS microdisplays,'' *SID Symp. Dig. Tech. Papers*, vol. 48, no. 1, pp. 1438–1441, May 2017, doi: 10.1002/sdtp.11916.
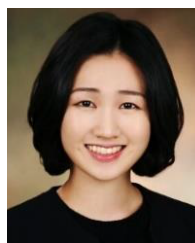
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