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RESEARCH ARTICLE

A Highly Resilient Fault Tolerant Topology of Single Phase Multilevel Inverter

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ABSTRACT Low reliability of the inverter is caused by high failure rates of semiconductor components and capacitors as well as high requirements for these components in the design of multilevel inverter topologies. The primary challenges in the reported fault-tolerant topology solutions include high component count, handling single and multiple switch faults, handling open and short switch failures on all fault locations, and achieving natural voltage balancing of the capacitors. This paper proposes a highly resilient fault-tolerant topology to accomplish the above challenges without compromising efficiency during faulty conditions. The acquired experimental results verify the proposed topology's robustness and efficacy. The proposed topology is evaluated by considering multiple instances of switch failures to encompass various fault locations and types. A comparison with the recently reported fault-tolerant MLI topologies verifies the superiority of the proposed topology.

INDEX TERMS Multilevel inverter, capacitor voltage balancing, single switch fault tolerance, multiple switch fault tolerance, reliability analysis.

I. INTRODUCTION

The high performance and efficiency of power electronic converters make them employed extensively in numerous applications, including adjustable drives, devices that interface solar and wind sources to the grid, electric vehicles, etc. [1]. The use of multilevel inverters (MLIs) effectively handles the voltage restriction imposed on traditional two-level inverters. Other benefits of MLI over its rivals include less dv/dt stress on the switches, more output voltage levels to increase power quality, high electromagnetic compatibility, and the elimination of filters [2]. However, to achieve all these benefits, switches and capacitors which are highly vulnerable to failure, are required in large numbers [3]. Hence, it is necessary to have a compromise between the quality of the output waveform and the topology's reliability. To address the aforementioned challenge, one option is to develop an MLI architecture with less device count. However, this sacrifices the inherent redundancy in the MLI architecture [4], [5] resulting in application false operation or outright shutdown under fault. As a result, research has focused on implementing fault-tolerant qualities into an MLI architecture with the lowest overall device count.

In [6] an early solution of adding fault-tolerant properties into an MLI topology has been proposed. As the middle voltage levels in [6] have inherent redundancy, the rated output power is produced even under faulty conditions. However, the design provides a derated output for the failure on the outermost switches. Another downside is that when a failure occurs on a switch that is closer to the DC-link terminals, the capacitor voltage balancing is lost.

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Additionally, a high device count increases the system's cost and complexity.

The traditional flying capacitor (FC) topology is modified in [7] to ensure successful operation in faulty conditions. FC's traditional voltage ratios are forced to non-traditional ratios to maintain the same number of voltage levels as the pre-fault condition. To perform capacitor voltage balancing, the available redundancy for intermediate voltage vectors is used. However, each FC has a bidirectional switch connected in series, which contributes to power losses under normal conditions. Furthermore, silicon-controlled rectifiers (SCR) are kept in parallel with the semiconductor switches, increasing the system's cost.

In the context of the three-level NPC design mentioned in reference [8], a supplementary three-level FC leg operates as a redundant component. This extra leg averts the occurrence of faults in any of the existing legs within the NPC converter. Additionally, it maintains a stable neutral point during normal operations, effectively eradicating low-frequency oscillations within the neutral point. To ensure the desired functionality, it's important to incorporate press-back technology in the inner switches of the NPC legs. This technology guarantees a swift transition to a short circuit state if an open circuit fault arises.

A three-level FC leg serves as a redundant leg to the three-level NPC design in [8]. The added leg avoids the faulty condition in one or more of the legs in the NPC converter and offers a rigid neutral point during normal conditions, hence eliminating low-frequency oscillations. However, it is essential for the inner switches within the Neutral-Point-Clamped (NPC) legs to incorporate press-back technology. This technology guarantees the swift transition to a short circuit state in case an open circuit fault occurs. The fault-tolerant capabilities of a multilayer active clamped (MAC) inverter is investigated in [9]. For a single device defect, the proposed approach can withstand both open and short switch failure. This property is accomplished as a result of the topology's intrinsic redundancy. The topology necessitates 'n-1' DC sources for a 'n' level inverter, which is a significant disadvantage, as is the requirement for a large number of switches. In addition, the architecture provides derated output voltage in the event of a fault on the peripheral switches. The developed fault-tolerant topologies of active NPC (ANPC) and T-type inverters is explored in [10] and [11]. No redundant leg is introduced to the usual three-level topologies in either of these articles. Both these are designed to tolerate faults on neutral path switches. However, the only derated output voltage is accessible for failure on half-bridge switches. Furthermore, the solutions in [10] and [11] are only applicable to a three-phase system.

Modular multilevel converters (MMC) offer the potential to attain fault-tolerant characteristics. Within each arm of MMCs, there exist redundant sub-modules that have the flexibility to be either active or inactive during regular operations as reported in [12] and [13]. Nonetheless, it's important to acknowledge that MMCs require a substantial quantity of devices, thereby introducing intricacy and increased expenses into the system, as indicated by reference [14]. Additionally, a robust fault-tolerant design for MMCs should effectively manage challenges related to circulating current, energy distribution equilibrium, and the balancing of capacitor voltages, as highlighted in [15], [16], and [17].

A network of relays has been employed to make a typical CHB inverter fault-tolerant [18]. After reconfiguration, the remaining healthy switches must endure a greater blocking voltage, necessitating switch oversizing. This drawback has been addressed in [19]. However, the topology outlined in [19] requires the incorporation of a load-side Cascaded H-Bridge (CHB) bridge to generate polarity, but this approach lacks fault resilience. The fundamental disadvantage of fault-tolerant topologies based on CHB is the need for multiple isolated DC power sources.

In [20], a solution is presented wherein all voltage sources except for one are substituted with capacitors. Nevertheless, when facing faulty circumstances, the works reported in [18] and [19] encounter difficulty in achieving equilibrium among capacitor voltages. Similarly, both [18] and [19] demonstrate an inability to maintain output power subsequent to a second fault occurrence. Addressing this challenge, [21] introduces an alternative fault-tolerant architecture based on the Cascaded H-Bridge (CHB) topology, featuring an equivalent count of switches in both the principal and redundant leg. Furthermore, the inclusion of redundant leg switches in a healthy state increased the power loss of the architecture. Due to the high number of levels in the output voltage waveform, the fault-tolerant MLI reported in [22] provides good output quality. However, under faulty conditions, this approach provides a derated output voltage. The primary drawbacks of [22] are the need for two isolated DC sources and high-blocking voltage switches. The topology reported in [23] balances the energy between the voltage sources and can withstand a fault without requiring a spare leg. The centre-tapped transformer, which allows the topology to regain the output power capability under problematic circumstances, is sacrificed in order to exclude the redundant leg. Only if the semiconductor switches are used in place of the clamping diodes will the inner switches in the NPC leg be able to tolerate fault. Additionally, the topology cannot tolerate numerous switch failures. The topology reported in [24] has a similar construction to the topology in [23]. Six switches constitute a redundant leg that is designed to withstand a fault on any switch in the primary topology. The proposed topology in [24] stands out because it can maintain pre-fault output power in faulty conditions with no increase in capacitor voltage ripple. The major drawback of this is that three active switches are used to replace the faulty switch, which results in a reduced output. An alternate approach utilizing a redundant leg, as discussed in [25], demonstrates the capability to withstand open and short switch failures,

along with the flexibility to manage fault occurrences across various locations within the primary inverter.

Based on the location of the faulty cell it is either replaced by a single switch or two switches from the redundant leg. However, regardless of the fault location, the proposed architecture in this study employed a single switch from the redundant leg. The solution in [25] requires two isolated DC sources and further, it is not multiple switch fault tolerant. According to the above explanation, the aforementioned topologies have one or more of the following challenges:

1. Derated output voltage under faulty conditions.
2. Capacitor voltage unbalancing under faulty conditions.
3. High device count.
4. Utilization of bidirectional switches.
5. Requirement of press-back technology in the semiconductor switches.
6. Requirement of more than one isolated DC source.
7. Oversizing of the switches.
8. Inner switches of the NPC leg are fault tolerant only if the clamping diodes are replaced by the switches.
9. High number of conducting switches under both healthy and faulty conditions.
10. Intolerance to multiple switch failure on both legs of the inverter.

Based on the above analysis, a novel fault-tolerant MLI topology is proposed in this paper, which can deliver rated output power and voltage under single and multiple switch failures, respectively. In contrast to the documented studies, the suggested configuration demands just a solitary DC source and a minimal quantity of switches (both in total and those actively engaged) within the redundant leg. The short circuit (SC) failure is handled by employing fast-acting fuses which blows open the arm containing faulty switch and thus, converts an SC failure into an OC one. The proposed topology can operate with single and multiple switch faults and with faults on all switches of main inverter topology. Further, no bidirectional switches are used in the proposed topology. If achieving only the rated output voltage is the goal, the inner switches within the Neutral-Point-Clamped (NPC) leg remain fault tolerant without necessitating the replacement of clamping diodes with semiconductor switches. Furthermore, the proposed topology inherently ensures capacitor voltage balance in both normal and faulty conditions. The experimental results obtained serve to validate the practicality and viability of the suggested inverter design.

The paper is organized as follows: the proposed topology is described in Section II followed by the validation through experimental results in Section III. The comparison of the proposed topology with recently reported topologies is presented in Section IV followed by conclusion in Section V.

II. OPERATION OF THE PROPOSED TOPOLOGY

Figure 1 illustrates the schematic diagram of the fault-tolerant topology proposed in this study. This topology consists of a primary inverter alongside a redundant leg. The primary inverter combines a traditional three-level Neutral-Point-Clamped (NPC) configuration with a traditional three-level Flying Capacitor (FC) setup. The redundant leg takes the form of a three-level structure following the conventional design of a Cascaded H-Bridge (CHB) inverter.

To begin, the operational principle of the primary inverter is examined, providing insight into its functionality. Subsequently, the analysis extends to evaluating how the inclusion of the redundant leg influences the overall performance of the proposed topology. The study also delves into the consequences of faults occurring at different locations, specifically their impact on intrinsic capacitor voltage equilibrium and the pre-fault output capacity. The investigation then turns to assessing the performance of both the primary inverter and the redundant leg. This comprehensive examination covers various aspects of their operation and effectiveness.

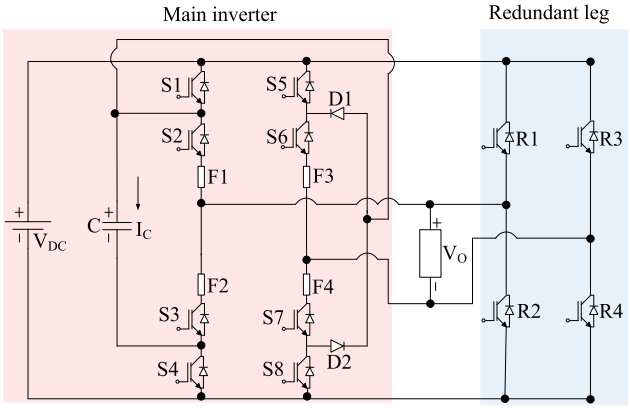

FIGURE 1. Circuit diagram of proposed fault-tolerant MLI.

A. OPERATING PRINCIPLE OF THE MAIN INVERTER TOPOLOGY

The switching strategy of main inverter topology and impact on FC voltage for positive capacitor current direction are summarized in Table 1. Under healthy operation, the main inverter produces an output voltage waveform with five levels. The zero voltage level (V5) has two redundant paths for its generation which are named as V5seq, 1 and V5seq, 2 (see Table 1). The voltage levels, V2 and V4, have a single path for generating $+V_{DC}$ and $-V_{DC}$ voltage level respectively. As observed from Table 1, voltage state of FC has no impact during the generation of V2, V4, and V5 voltage levels.

V1 and V3 voltage levels are termed as middle voltage levels, which are responsible for generating the voltage level which is in the middle of zero and $\pm V_{DC}$ voltage level. Both the "V1" and "V3" voltage level have two paths which have opposite impacts on the state of FC voltage. One of the simplest conventional ways of achieving inherent capacitor voltage balancing is by choosing V1seq, 1 and V3seq, 2 voltage sequences since it would lead to FC charging

TABLE 1. Switching strategy of the main inverter.

Level	Sequence	Load Voltage	Turn 'ON' switches	Effect on flying capacitor $i_c > 0$
Middle voltage level (V1)	$V1_{seq,1}$	V_{DC}-C_V	S1,S3,S7,S8	↑
	$V1_{seq,2}$	C_V	S2,S4,S7,S8	↓
High voltage level (V2)	$V2$	V_{DC}	S1,S2,S7,S8	–
Middle voltage level (V3)	$V3_{seq,1}$	-(V_{DC}-C_V)	S2,S4,S5,S6	↑
	$V3_{seq,2}$	-C_V	S1,S3,S5,S6	↓
High voltage level (V4)	$V4$	-V_{DC}	S3,S4,S5,S6	–
Zero voltage level (V5)	$V5_{seq,1}$	0V	S1,S2,S5,S6	–
	$V5_{seq,2}$	0V	S3,S4,S7,S8	–

Note: Charging and discharging phenomena affecting the flying capacitor in the context of positive capacitor current ($i_c > 0$, as depicted in Fig. 1), utilizing the subsequent notation:
'↑' Charging of the FC
'↓' Discharging of the FC
'–' No effect on FC

and discharging respectively in the positive and negative half of the fundamental cycle. Similarly, V1seq, 2 and V3seq, 1 could be used to attain inherent capacitor voltage balancing. Due to equal charging and discharging of the FC across each fundamental period, inherent capacitor voltage balancing is thus accomplished [26]. It is important to note that throughout the entire study, the middle voltage levels under pre-fault conditions are generated using V1seq, 2 and V3seq, 1. The severity of a fault in an MLI topology is determined by the fault type and its location. Table 2 illustrates a scenario in which an Open-Circuit (OC) failure is examined for each switch within the primary inverter. In the case of an OC failure occurring on switch S1, the voltage level 'V5' will be produced utilizing the value V5seq,2.

TABLE 2. Characteristics offered at various fault locations for the main inverter topology.

Faulty Devices	Output voltage level status					1*	2*
	V1	V2	V3	V4	V5		
S1	√	×	√	√	√	√	×
S2	√	×	√	√	√	√	×
S3	√	√	√	×	√	√	×
S4	√	√	√	×	√	√	×
S5	√	√	√	×	√	√	×
S6	√	√	×	×	√	√	×
S7	×	×	√	√	√	×	×
S8	×	×	√	√	√	×	×
1*= Natural capacitor voltage balancing property							
2*=Post-fault output power=Pre-fault output power							

The voltage level V1seq, 2 can independently generate the 'V1' voltage level. Maintaining inherent capacitor voltage equilibrium is still possible by utilizing the V3seq, 1 voltage level, as previously explained. However, in post-fault situations, the inability to generate the 'V2' voltage level leads to a reduction in the output voltage. This examination extends to OC failures on the remaining switches, with the results tabulated in Table 2. The data presented in the table indicates that the primary inverter has the capacity to achieve partial inherent capacitor voltage balancing for certain fault locations. However, in the scenario where an Open-Circuit (OC) fault arises on any of its switches, the primary inverter is unable to achieve the full pre-fault output power rating.

B. OPERATING PRINCIPLE OF THE PROPOSED TOPOLOGY

The addition of a typical three-level CHB leg to the main inverter topology resolves the main inverter's failure to accomplish inherent capacitor voltage balancing and pre-fault output power under faulty situations. In this regard, a CHB leg is connected to the load terminals as the redundant leg.

The inclusion of the redundant leg ensures that the following properties are incorporated into the main inverter topology:

- Single switch fault tolerance, with equivalent post-fault and pre-fault voltage waveforms.
- Multiple switch fault tolerance, with equal post-fault and pre-fault output voltage.
- Inherent capacitor voltage balancing under all scenarios.
- High reliability.

From Fig.1, it can be observed that the redundant leg architecture is very straightforward. A conventional three-level CHB leg is placed across the load terminals. Switch R1 from the redundant leg provides the alternate path to join the positive terminal of the DC supply with the positive load terminal. Similarly, the rest of the switches corresponding to the CHB leg architecture can be interpreted. The generation of high voltage levels 'V2' and 'V4' do not require any flying capacitor participation. Hence, under single or multiple switch failures, the high voltage levels can be easily generated by the activation of such redundant leg switches which correspond to the main inverter faulty switches. For example, a fault on switch S3 or S4 or both requires the activation of switch R2 from the redundant leg. 'V4' voltage level, which was earlier generated using switches S3, S4, S5, and S6, can now be generated using R2, S5, and S6 switches. Hence, it does not matter whether the proposed topology encounters a single or multiple switch failure, it will inevitably generate a three level output voltage waveform which has the same pre-fault voltage rating.

One thing to be noted is that the architecture of the redundant CHB leg does not have any direct electrical connection with the FC terminals. Hence, the middle voltage levels which require FC for their generation can only be generated through the available inherent redundancy, i.e. using either V1seq, 1 and V3seq, 2 or V1seq, 2 and V3seq, 1. This fact results in a minor difference in the output voltage waveform under single and multiple switch failure. For a better understanding of this fact, let us assume that

a single switch failure has occurred on switch S5 which requires the activation of switch R3 from the redundant leg. High voltage level 'V2' does not require switch S5 for its generation whereas 'V4' voltage level can now be generated by the combination of switches S3, S4, and R3 to produce −VDC voltage level. Zero voltage level can be generated using V5seq, 2. Middle voltage levels should be generated using V1seq, 1 and V3seq, 2 since V3seq, 1 cannot be generated. Hence, under the switch S5 failure situation, the proposed topology is capable of generating an equivalent pre-fault voltage waveform, and the same can be extended and applied for any single switch failure condition.

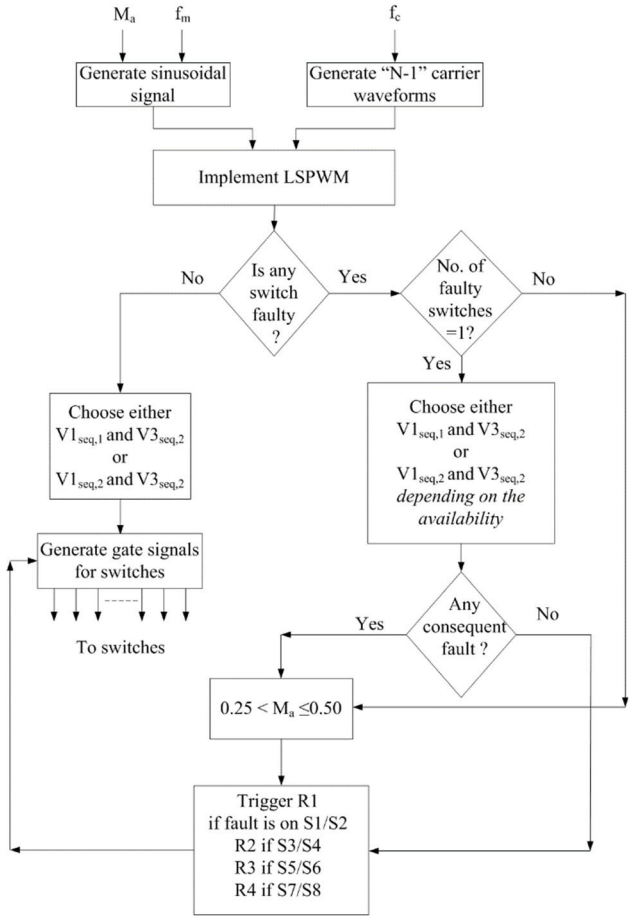

FIGURE 2. Flowchart depicting various switching strategies under different scenarios.

Now, let us assume that under healthy conditions, V1seq, 2 and V3seq, 1 are utilized to generate the middle voltage levels. The case study of switch S5 failure requires the activation of switch R3 and utilizing V1seq, 1 and V3seq, 2 as mentioned before. Considering a subsequent failure of switch S6, it implies that the middle voltage level V3seq, 2 cannot be generated (see Table 1). Hence, the utilization of the only V1seq, 1 middle voltage level would fully charge the capacitor to VDC. To avoid this situation, the modulation index post multiple switch failure is required to be updated so that the proposed topology generates a symmetrical three level output voltage waveform with the pre-fault output voltage rating. The acceptable range of modulation index value under multiple switch failure lies between 0.25 and 0.50. Whether the proposed topology is working under healthy, single switch or multiple switch failure condition, the flowchart of the switching scheme defines the rules based on the above discussion and is schematically represented in Fig.2. First, the modulation index (Ma) value, modulating frequency (fm), and carrier frequency (fc) are defined. Modulation index (Ma) value is chosen to be one for pre-fault conditions in order to achieve the maximum fundamental component in the output voltage waveform [22]. Then, the level shift pulse width modulation (LS-PWM) scheme is applied to generate the gating pulses. Fault detection is considered to be out of the scope of this paper. Hence, the decision making process which informs the controlling scheme of the faulty switch is already known. If there is no faulty switch present, then the controlling scheme ensures inherent capacitor voltage balancing before providing the gate pulses to the switches. Upon the occurrence of a fault on a single switch, the first step is to ensure capacitor voltage balancing. If there is any consequent fault, then the modulation index value is updated, else the redundant leg switches are triggered to deliver the output.

If multiple switch failures have occurred simultaneously, then there is no need for a capacitor voltage balancing step since a three-level output voltage waveform will be generated. Thus, the only requirement under multiple switch failure is the post-fault modulation index update with the activation of redundant leg switches. Table 3 emphasizes the impact of a solitary switch failure on the main inverter switches within the proposed topology. Unlike the findings in Table 2, the incorporation of the redundant leg yields a comparable pre-fault output voltage waveform characterized by inherent capacitor voltage balancing. Importantly, the suggested architecture is capable of achieving the pre-fault output voltage rating even when facing multiple switch faults denoted by 'm', where 'm' ranges from 2 to 'M' (with M = 8, representing the total number of main inverter switches).

TABLE 3. Characteristics offered at various fault locations for the proposed topology.

Faulty Devices	Output voltage level status					1*	2*
	V1	V2	V3	V4	V5		
S1	√	√	√	√	√	√	√
S2	√	√	√	√	√	√	√
S3	√	√	√	√	√	√	√
S4	√	√	√	√	√	√	√
S5	√	√	√	√	√	√	√
S6	√	√	√	√	√	√	√
S7	√	√	√	√	√	√	√
S8	√	√	√	√	√	√	√
1*= Natural capacitor voltage balancing property							
2*=Post-fault output power=Pre-fault output power							

III. SIMULATION AND EXPERIMENTAL ANALYSIS

The feasibility and robustness of the proposed topology are carried out in Simulink environment and verified through the obtained experimental results. The system parameters used for simulation and experimental study are listed as follows: Input voltage source (V_{DC}) = 25V, C = 1200μF, Switching frequency (fsw) = 5 kHz, and output load with R = 20Ω, and L = 20mH. The proposed topology is studied under the healthy condition and various fault locations. Under both OC and SC failure, two cases of failure are studied. In the first fault situation, a single switch is considered to be faulty which is followed by another single switch failure. This study covers the single switch fault tolerance of the proposed topology. In the second situation, two switches are considered to develop fault simultaneously. The OC failure situation on a particular switch is emulated by the removal of gate pulses whereas the SC failure situation are emulated by constant application of gate pulses. The paper is focused only on the architectural aspects of the proposed MLI topology and the switching scheme reconfiguration under faulty conditions. Hence, it is assumed that under short circuit failure, the fuse corresponding to the faulty switch will blow open if current of high magnitude flows for a sufficient time. This transforms an SC failure into an OC failure. In the obtained results, an instance of OC failure is represented by OCI, instance of SC failure is represented by SCI, and instance of switching scheme reconfiguration to activate the appropriate redundant leg switches is represented by RI. For the obtained experimental results, output voltage and capacitor voltage waveform are scaled at 10V/div whereas the output current waveform is scaled at 10A/ div.

A. OPEN CIRCUIT FAULT ANALYSIS

1) OC ON SWITCH S3, FOLLOWED BY OC ON SWITCH S6

In all healthy scenarios, the intermediate voltage levels 'V1' and 'V3' are generated using V1seq,2 and V3seq,1, respectively. The switching sequences V1seq,2 and V3seq,1 facilitate discharging and charging of the capacitor during the positive and negative segments of the fundamental cycle, respectively. A thorough examination of Table 1 uncovers that an Open-Circuit (OC) failure involving switch S3 leads to the absence of the 'V4' voltage level generation. This, in turn, leads to a reduction in the amplitude of the load current during the negative phase of the fundamental cycle (as depicted in Fig. 3(a)). Given that the same load current traverses through the Flying Capacitor (FC) during the V3seq,1 switching sequence, the decreased current magnitude through the FC during the negative phase culminates in the loss of inherent capacitor voltage equilibrium.

The Reconfiguration Instance (RI) signifies the activation of switch R2 through the redundant leg. At the RI point (occurring at t = 0.26 seconds), the capability to generate the 'V4' voltage level is restored, leading to the topology reverting to its pre-fault behavior. An Open-Circuit (OC) failure is then introduced on switch S6 at t = 0.32 seconds.

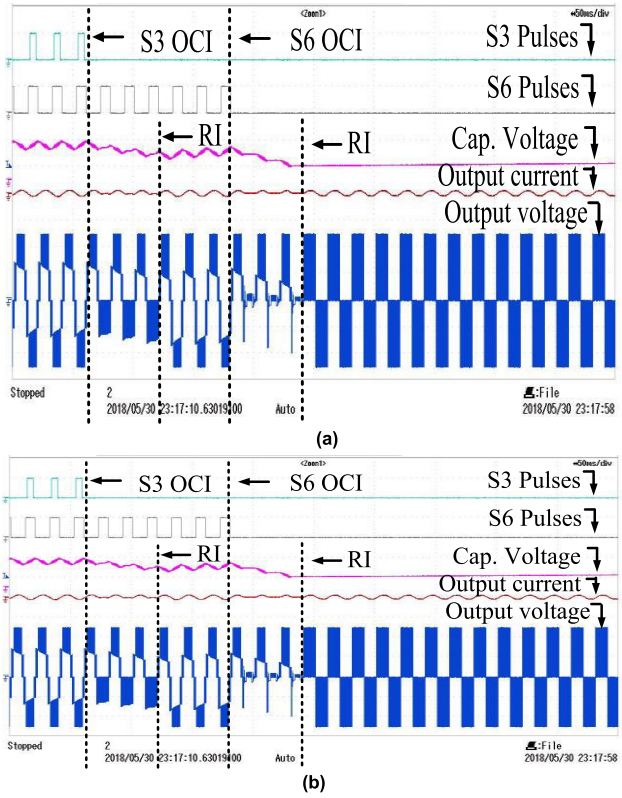

FIGURE 3. Waveforms under switch S3 and S6 OC failure (a) Simulation (b) Experimental.

Post the OC failure in the primary inverter, neither the 'V3' nor 'V4' voltage levels can be generated. Consequently, the load current experiences a reduction, ultimately causing a complete discharge of the Flying Capacitor (FC). Switch R3 is triggered during the RI (at t = 0.38 seconds), resulting in the restoration of the 'V4' voltage level generation capacity. Despite the topology now functioning as a three-level inverter, it can still deliver the pre-fault output voltage rating to the load. Figure 3(b) visually displays the experimental outcome under OC failures of switches S3 and S6, showcasing a perfect alignment with the simulation results.

2) OC ON SWITCH S3, S5, AND S8

In the presence of a simultaneous Open-Circuit (OC) failure on switches S3, S5, and S8 (observed at t = 0.20 seconds in Fig. 4(a)), it becomes impossible to generate all the voltage levels corresponding to the switching strategy outlined in Table 1. Additionally, the Flying Capacitor (FC) loses its charging and discharging pathways, resulting in the preservation of its voltage level. During the reconfiguration instance (occurring at t = 0.26 seconds), switches R2, R3, and R4 are activated through appropriate pulses. This reconfiguration leads to the formation of a three-level output voltage waveform, restoring the pre-fault output power rating. The experimental results for this scenario are presented in Fig. 4(b), and they closely align with the simulation results.

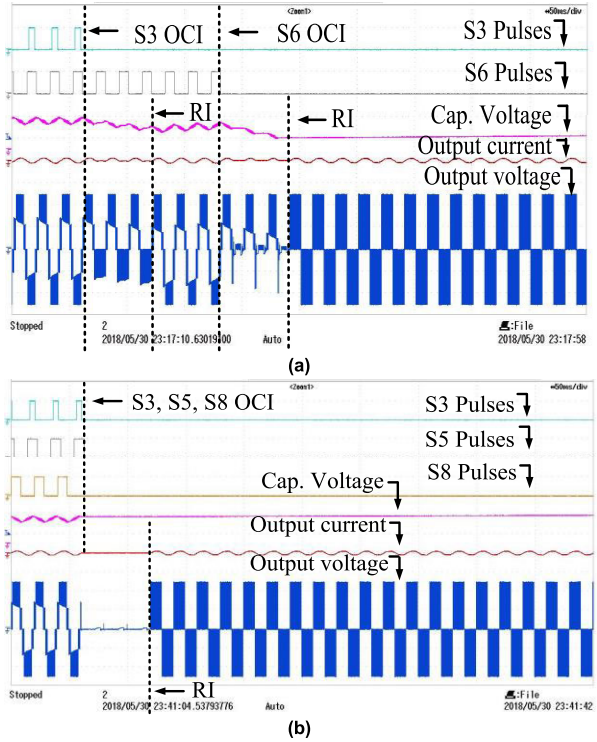

FIGURE 4. Waveforms under switch S3, S5 and S8 OC failure (a) Simulation (b) Experimental.

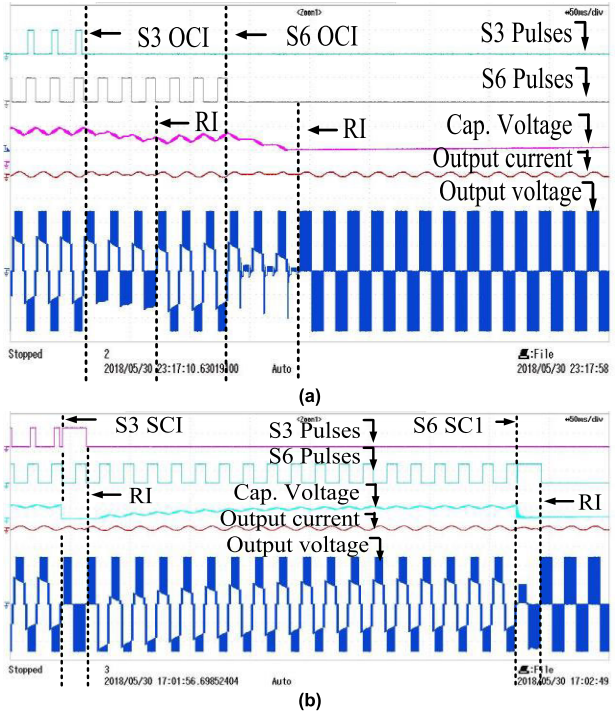

FIGURE 5. Waveforms under switch S3 and S6 SC failure (a) Simulation (b) Experimental.

B. SHORT CIRCUIT (SC) FAULT ANALYSIS

Unlike an OC failure, an SC failure does not interrupt the current flow through the failed switch. Under the SC failure on any switch, turning on of its complementary switch might lead to a short circuit path. Such as, an SC failure on switches S5 and S6 might result in short-circuiting of the voltage supply during the generation of 'V2' voltage level. Therefore, fuses F1∼F4 are added in each arm of the main inverter topology which ensures complete isolation of the faulty arm as in [8], and thus, after isolation, can be treated as an OC failure. In the following cases on short circuit failure, the fuse is considered to blow open at the reconfiguration instance (RI) and changes in the switching scheme are carried out simultaneously.

1) SC ON SWITCH S3, FOLLOWED BY SC FAILURE ON SWITCH S6

Under the healthy condition, voltage level 'V0' is generated using V5seq, 1. At the instance of SC failure on switch S3 (t = 0.20 sec in Fig.5(a)), FC gets instantaneously discharged to zero through the failed switch S3 and S2, which is turned on for 'V0' voltage level generation. Thus, the FC can no longer provide the middle voltage level generation. At the RI (t = 0.22 sec in Fig.5(a)), the corresponding fuse 'F2' is considered to blow open. This converts the SC failure into an OC one, which has been studied in the previous section. The activation of switch 'R2' results in the generation of 'V4' voltage level, following which the FC starts to naturally clamp at VDC/2 voltage level. Thus, an output voltage waveform comprising of five levels immediately starts generating. A consequent SC failure on switch S6 is considered at time t = 0.48 sec. At the instance of SC failure on switch S6, FC gets short-circuited again. At the RI (t = 0.50 sec in Fig.5(a)), the corresponding fuse 'F3' is considered to blow open. This again converts the short circuit into an open circuit failure situation, which has already been covered in the previous section. Thus, the activation of switch R3 results into a three-level output voltage generation which has the same peak to peak voltage magnitude when compared to the pre-fault one. Fig.5(b) shows the obtained experimental results under switch S3 and S6 SC failure, which are in a close match to the simulation results.

2) SC ON SWITCH S3, S5, AND S8

Under the healthy condition, the voltage level 'V0' is generated using the switches S1, S2, S5, and S6. At the instance of simultaneous SC failure on switches S3, S5, and S8 (see t = 0.20 sec in Fig.6(a)); all the voltage levels corresponding to the switching scheme defined in Table 1, cannot be generated. FC gets instantaneously discharged to zero through the failed switch S3 and S2, which is turned on for 'V0' voltage level generation. Thus, the FC can no longer provide the middle voltage level generation. At the RI (t = 0.26 sec in Fig.6(a)), the corresponding fuses 'F2', 'F3', and 'F4' are considered to blow open. This turns the SC failure into an OC failure, as discussed in the previous section. Switches R2, R3, R4 are triggered with appropriate pulses during the reconfiguration instance (t = 0.26 sec), forming a

three-level output voltage waveform with the pre-fault output power rating. Fig.6(b) shows the obtained experimental results under the considered case which matches closely with the simulation results.

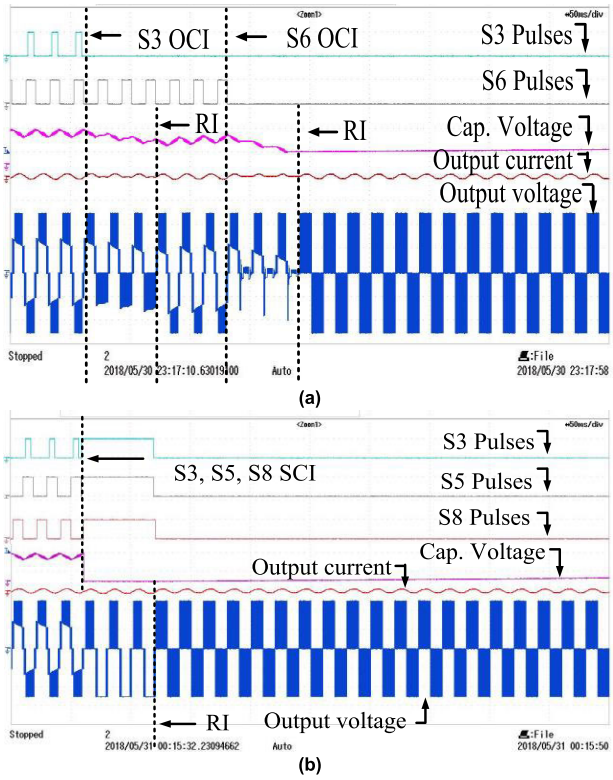

FIGURE 6. Waveforms under switch S3, S5 and S8 SC failure (a) Simulation (b) Experimental.

3) RATED OUTPUT POWER AND VOLTAGE

Under single switch failure conditions, the rated output power is preserved on account of the ability of the proposed MLI topology to regain pre-fault output voltage waveform. Whereas under multiple switch failure conditions, the number of output voltage levels decreases. With the decrease in the number of output voltage levels, the total harmonic distortion of the waveform increases, or the fundamental component of the output voltage decreases. This results in a decrease in the fundamental component of the output voltage current which leads to reduced output power. An important thing to be noted is that though the number of output voltage levels may change upon fault occurrence, its peak-to-peak magnitude remains the same. Thus, the pre-fault output voltage rating of the inverter is preserved under multiple switch failures. Hence, in conclusion, output power and voltage are preserved under single and multiple switch failures.

IV. DYNAMICS OF THE FUSE UNDER SHORT CIRCUIT BEHAVIOR

Implementation of fast acting fuses in a MLI topology protects the semiconductor switches from overload or faulted current [24], [25]; based on which all the simulation and hardware results for the proposed topology have been carried out. However, a finite time interval is required during which sufficient thermal energy is created by the transient surge currents to melt the fuse element. This effect is known as the melting integral of the fuse and is commonly referred to as the integral. Time-current curve characteristics in the datasheet of an electrical fuse depict the time required by a specific rated fuse to blow open for a particular value of fault current. This section aims at focusing on the dynamic response of the fuse under short circuit failure conditions. Input parameters considered for experimental study are: VDC = 25V, C = 1200 μF, fSW = 5 kHz and R = 20 ohm and L = 20 mH. Table 4 represents the severity on the main inverter topology under individual semiconductor switch short circuit failure. As can be seen from Table 4, complimentary switch pairs S2 & S3 and S6 & S7 are most severe in nature; hence short circuit failure on switches S3 and S6 are analyzed.

TABLE 4. Severity of short circuit failure.

Short Circuit Switch	Severity
S1 or S4	The capacitor voltage balancing is lost.
S2	Capacitor voltage balancing is lost if $V1_{seq,2}$ and $V3_{seq,1}$ are utilized. Short circuit of the capacitor if $V1_{seq,1}$ and $V3_{seq,2}$ are utilized.
S3	Capacitor voltage balancing is lost if $V1_{seq,1}$ and $V3_{seq,2}$ are utilized. Short circuit of the capacitor if $V1_{seq,2}$ and $V3_{seq,1}$ are utilized.
S5 or S8	No effect
S6 or S7	Short circuit path through DC voltage source. The capacitor voltage balance is lost.

Case 1 (Short Circuit Failure on Switch S3): In Table A, severity of a short circuit failure is defined in terms of magnitude of short circuit current. Hence, for short switch failure on switch S3, voltage sequences V1seq,1 and V3seq,2 are chosen for generating (VDC−CV) and (-VC) output voltage level respectively. Since the load current has a peak to peak magnitude of 2.5A, therefore a fuse of 5A rating is implemented under the case study [27]. The experimental results for switch S3 are shown in Fig.7. An observation of Fig.7 reveals that the flying capacitor discharges instantaneously as soon as the short circuit failure was introduced on switch S3. The short span of discharge was unable to melt the fuse. This result is verified by plotting switch S3 fault current values on the time-current characteristic of the fuse as shown in Fig.8. It can be observed that there is no intersection of the plotted fault current against the curve of 5A fuse; hence, it confirmed the inability of the fuse to melt and blow open.

Case 2 (Short circuit failure on switch S6): Unlike switch S3 where the short circuit current dies out quickly on account of instantaneous discharge of the capacitor, short circuit failure of switch S6 leads to high magnitude of fault current. The reason being is that the DC voltage source gets short

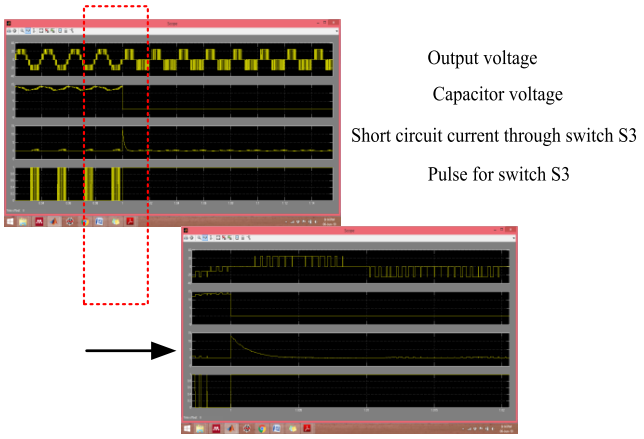

FIGURE 7. Experimental result under switch S3 short circuit failure.

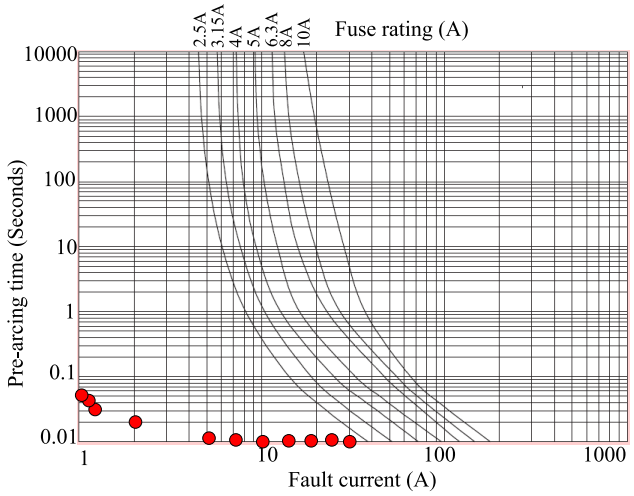

FIGURE 8. Fault current plotted on the time-current curve characteristic of the electrical fuse for short circuit on switch S3.

circuited periodically through S1, clamping diode, S6, S7, and S8 during the generation of +VDC output voltage level generation. Since the magnitude of fault current is too high and the available electrical fuses are of lower rating, a resistor is placed in series with switch S6 to analyze the dynamics of the fuse. The experimental results for switch S3 are shown in Fig. 9. In Fig. 9, the instance of short circuit failure on switch S6 is highlighted by the origin of high magnitude fault current which exists for a time interval of approximate 1.35 seconds. After the elapse of this period, the fuse has melted and successfully transformed the short circuit failure into an open circuit one. The pre-fault output voltage waveform is regained by activating switch R3 from the redundant leg. The clearing time of the fuse is verified by plotting switch S6 fault current values on the time-current characteristic of the fuse. An observation of Fig.10 reveals that for a fault current of 25A, the fuse datasheet reads a clearing time of 1.3 seconds which is very close to the recorded time for the experimental study. In a similar way, dynamics of the fuse corresponding to switch S3 can be also studied for short circuit failure if the flying capacitor is replaced by a stiff voltage source.

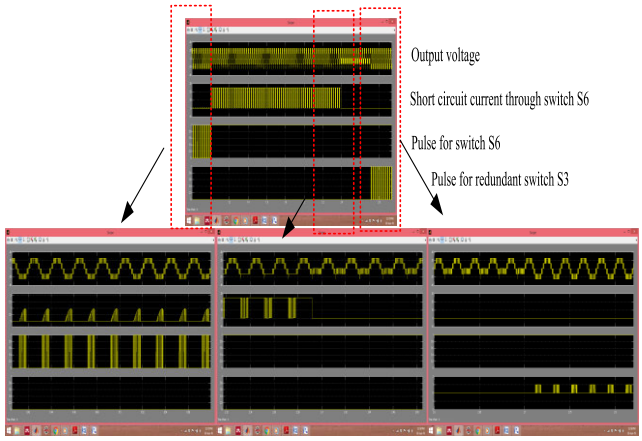

FIGURE 9. Experimental result under switch S3 short circuit failure.

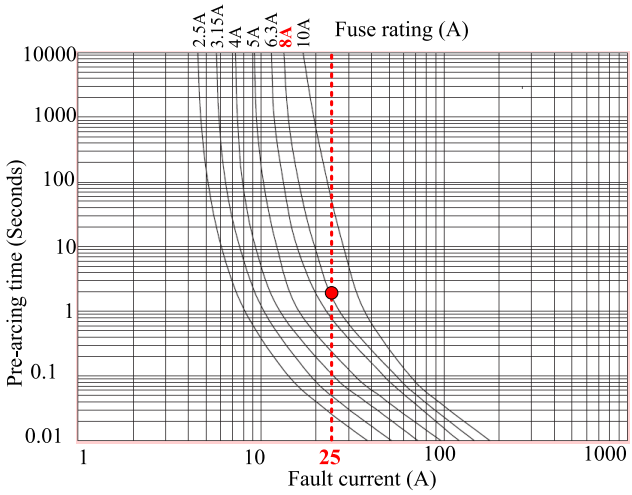

FIGURE 10. Fault current plotted on the time-current curve characteristic of the electrical fuse for short circuit on switch S6.

V. COMPREHENSIVE COMPARISON, EVALUATION, AND NOVELTY

A. EFFICIENCY COMPARISON

An important characteristic which determines the efficiency of an inverter is the number of semiconductor switches active at any given instant. Lesser the number of 'ON' semiconductor switches, higher will be the efficiency of the MLI and vice versa. In the proposed topology, four switches are always in active mode under healthy conditions (for e.g. see Fig.11(i)). Under single switch failure condition, the lost voltage level (/s) is (/are) generated by activating only one switch from the redundant leg, hence a total of three 'ON' switches are required (for e.g. see Fig.11(ii)). For multiple switch failure on two switches, a total of three (for e.g. see Fig.11(iii)) or two (for e.g. see Fig.11(iv)) switches are required to be turned 'ON' depending on the switch faulty location. In a similar way, the rest of the cases for multiple

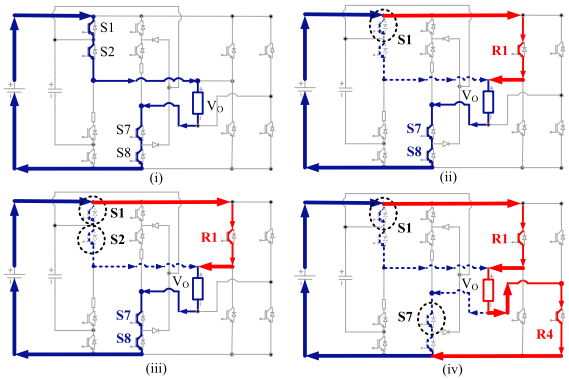

FIGURE 11. Schematic diagram representing active switches for the proposed topology under (i) Healthy condition (ii) Switch S1 faulty condition (iii) Switch S1 and S2 failure condition (iv) Switch S1 and S7 failure condition.

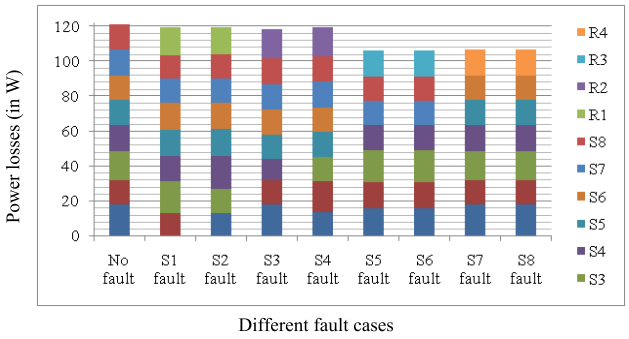

FIGURE 12. Power losses of the proposed topology under healthy and various single switch failure conditions.

switch failure (where number of faulty switches are more than two) can be considered. Due to the necessity of activating a maximum of three switches in faulty scenarios, a comparison of efficiency is performed between healthy and single switch failure conditions for the proposed topology. For efficiency evaluation, the FF600R06ME3 IGBT module [28] is selected, and the following parameter values are utilized: Input voltage VDC: 200V, load R = 20 ohms, and L = 20 mH. Reference [29] is referred for assessing power losses. Fig.12 illustrates the cumulative losses experienced by the proposed Modular Multilevel Inverter (MLI) topology in both normal and single switch failure scenarios. As anticipated, the efficiency of the proposed MLI proves higher in faulty conditions. This is due to the fact that only three switches are activated during a single switch failure, as opposed to the healthy state where four switches are utilized concurrently. The power loss result in Fig.12 proves that the incorporation of CHB as the redundant bridge to the main inverter topology results in higher efficiency under faulty conditions when compared to the healthy condition. This advantage has been achieved on account of lesser number of 'ON' switches under faulty conditions. Hence, the factor 'Number of ''ON'' switches' serves the purpose of efficiency comparison of the proposed MLI topology with the recently developed topologies for similar input and output conditions. In order to bring out an effective comparison with recently proposed single phase fault tolerance MLI topologies, the main inverter topology considered in this paper is chosen to be same for the topologies presented in [24] and [25]. Fig.13 compares the number of active switches for the proposed topology and the topologies presented in [24] and [25] for a particular voltage level generation. It can be observed that the proposed topology requires least number of active devices over the rest. Another advantage of utilizing CHB as the redundant leg is that the main inverter topology becomes fault tolerant to multiple switch faults on switches belonging to different legs. Fig.14 shows the schematic diagram where multiple switch fault occurrence is considered on the proposed topology and topologies presented in [24] and [25]. It can be observed from Fig.14(i) that the topology presented in [24] cannot tolerate multiple switch failure. Though the topology in [25] is capable of multiple switch fault tolerance (see Fig.14(ii)), however it requires more number of active switches in comparison to the proposed topology (see Fig.14(iii)). It is to be noted that for Fig.13 and Fig.14, solid and dotted line represents the current ability and inability to achieve a closed path respectively, whereas blue and red color line represents the current traversing through the main inverter and redundant leg switches respectively.

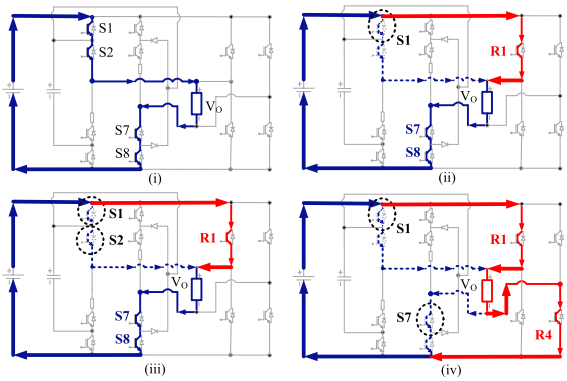

FIGURE 13. +VDC output voltage level generation under switch S1 faulty condition for (i) Topology in [24] (ii) Topology in [25] (iii) Proposed topology.

B. COMPONENT AND FUNCTIONALITY COMPARISON

A thorough comparison of the proposed topology with the most recent fault-tolerant topology is presented in Table 5. The topologies in [12], [18], and [19] are taken into consideration to deliver a five-level output voltage waveform in order to make an effective comparison. To calculate the overall blocking voltage, a VDC input voltage of 1.0 pu is taken into consideration. Topology in [23] requires a center tapped transformer to preserve the output power rating whereas the topologies proposed in [18] and [19] fail to preserve the output power after second fault occurrence. The proposed topology does not employ any bidirectional switch and has the minimum number of 'ON' state switches during faulty conditions. Also, the proposed topology has

the overall least device count. The proposed topology can tolerate both OC and SC failure on all fault locations. Thus, both quantitative and qualitative superiority of the proposed topology has been brought to limelight.

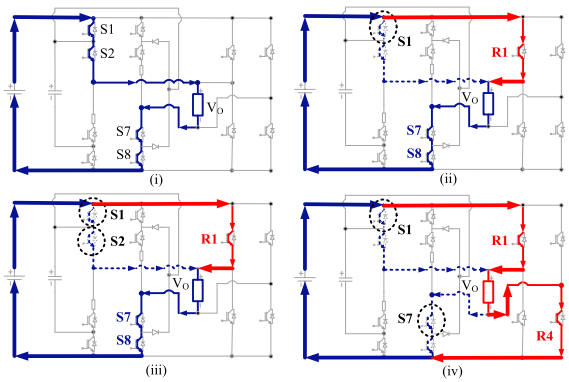

FIGURE 14. Multiple switch failure study (i) Topology in [24] (ii) Topology in [25] (iii) Proposed topology.

TABLE 5. Comparison with recent literature.

Parameter	Ref [12]	Ref [23]	Ref [24]	Ref [25]	Ref [18]	Ref [19]	Proposed
1*	1	2	1	2	2	2	1
2*	2	0	1	0	0	0	0
3*	8	0	0	0	0	0	1
4*	0	2	3	0	0	0	0
5*	10	4([1])	6	6	8([2])	16([2])	8
6*	4	3	3	4	4([2])	8([2])	4
7*	5	5	4	3	4([2])	8([2])	3
8*	7.0	8.5	9.0	10	8.0	15.0	8.0
9*	√	×	√	√	√	√	√
10*	√	√	√	√	√	√	√
11*	×	×	×	√	×	×	√
12*	×	×	×	√	×	×	√

1*= Number of voltage sources
2*= Number of DC sources
3*= Number of flying capacitors (FCs)
4*= Number of bidirectional switches
5*= Total number of switches in redundant leg
6*= Turn 'ON' switches before fault
7*= Turn 'ON' switches after fault
8*= Total blocking voltage
9*= Tolerant to single switch open failure
10*= Tolerant to single switch short failure
11*= Tolerant to multiple switch open failure
12*= Tolerant to multiple switch short failure
([1])= Centre-tapped transformer is also utilized alongside two bidirectional switches
([2])= Relay count

C. NOVELTY OF THE PROPOSED WORK

Though the architecture of the main inverter topology or the redundant leg is not novel, however, the choice of implementing CHB as the redundant bridge is novel. At first glance the contribution of the paper seems trivial based on the architectural terms of the proposed topology. However, the choice of CHB as the redundant bridge provides a generalized solution to five level conventional and recently proposed MLI topologies. A common characteristic of single phase five level MLI topologies (conventional CHB, flying capacitor, & neutral point clamped (NPC) inverter; standard five level active NPC (ANPC) [30], T-type [31], hybrid inverter topologies such as modified stacked [32], reduced five level ANPC [33], [34], or recently proposed fault tolerant MLI topologies [19], [21], [23], [24], [25], [35], [36]) is that all these topologies possess inherent redundancy for the generation of zero voltage and middle voltage levels (±VDC/2). This particular characteristic can be taken advantage of for achieving fault tolerant characteristics for all similar kind of topologies. Based on this, the main inverter in the present paper comprises of conventional three level FC and NPC leg. Under single switch failure, the inherent redundancy in the main inverter topology enables the generation of zero and middle voltage level, whereas the outer voltage levels (±VDC) are generated by activating appropriate switches from main inverter topology and redundant three level cascaded H-bridge. Thus, pre-fault rated power is delivered under single switch failure condition. Another characteristic of the redundant bridge is that it delivers rated output voltage under multiple switch failure. An important characteristic of choosing CHB is that the number of conducting devices is least under any faulty condition.

VI. CONCLUSION

This paper proposed a novel fault-tolerant five-level Modular Multilevel Inverter (MLI) topology by integrating conventional Flying Capacitor (FC), Neutral-Point-Clamped (NPC), and Cascaded H-Bridge (CHB) inverters. The core structure of the proposed topology comprises a combination of the three-level FC and NPC legs, while implementing a conventional three-level CHB inverter imparts fault-tolerant capabilities to the main inverter. The significant accomplishments of the proposed topology encompass its capacity to withstand single and multiple switch failures affecting pairs, triplets, or even quadruples of switches within the main inverter. It also demonstrated resilience against open and short switch failures, all the while maintaining output power and efficiency during faulty conditions. Through a comparative analysis, the proposed topology exhibited both quantitative and qualitative superiority over previously established fault-tolerant configurations. Experimental results substantiated the feasibility and robustness of the proposed topology.

REFERENCES

[1] W. Zhang, D. Xu, P. N. Enjeti, H. Li, J. T. Hawke, and H. S. Krishnamoorthy, "Survey on fault-tolerant techniques for power electronic converters," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6319–6331, Dec. 2014, doi: 10.1109/TPEL.2014.2304561.
[2] J. Rodriguez, J.-S. Lai, and F. Zheng Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002, doi: 10.1109/TIE.2002.801052.
[3] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1441–1451, May 2011, doi: 10.1109/TIA.2011.2124436.
[4] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: A review," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 135–151, Jan. 2016, doi: 10.1109/TPEL.2015.2405012.

[5] E. Babaei, S. Laali, and Z. Bayat, "A single-phase cascaded multilevel inverter based on a new basic unit with reduced number of power switches," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 922–929, Feb. 2015, doi: 10.1109/TIE.2014.2336601.

[6] A. Chen, L. Hu, L. Chen, Y. Deng, G. Yao, and X. He, "A multilevel converter topology with fault tolerant ability," in *Proc. 19th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2004, pp. 1610–1616, doi: 10.1109/APEC.2004.1296080.

[7] X. Kou, K. A. Corzine, and Y. L. Familiant, "A unique fault-tolerant design for flying capacitor multilevel inverter," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 979–987, Jul. 2004, doi: 10.1109/TPEL.2004.830037.

[8] S. Ceballos, J. Pou, E. Robles, I. Gabiola, J. Zaragoza, J. L. Villate, and D. Boroyevich, "Three-level converter topologies with switch breakdown fault-tolerance capability," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 982–995, Mar. 2008.

[9] J. Nicolas-Apruzzese, S. Busquets-Monge, J. Bordonau, S. Alepuz, and A. Calle-Prado, "Analysis of the fault-tolerance capacity of the multilevel active-clamped converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 4773–4783, Nov. 2013, doi: 10.1109/TIE.2012.2222856.

[10] J. Li, A. Q. Huang, Z. Liang, and S. Bhattacharya, "Analysis and design of active NPC (ANPC) inverters for fault-tolerant operation of high-power electrical drives," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 519–533, Feb. 2012, doi: 10.1109/TPEL.2011.2143430.

[11] U.-M. Choi, K.-B. Lee, and F. Blaabjerg, "Diagnosis and tolerant strategy of an open-switch fault for T-type three-level inverter systems," *IEEE Trans. Ind. Appl.*, vol. 50, no. 1, pp. 495–508, Jan. 2014, doi: 10.1109/TIA.2013.2269531.

[12] A. Ghazanfari and Y. A. I. Mohamed, "A resilient framework for fault-tolerant operation of modular multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2669–2678, May 2016, doi: 10.1109/TIE.2016.2516968.

[13] K. Li, L. Yuan, Z. Zhao, S. Lu, and Y. Zhang, "Fault-tolerant control of MMC with hot reserved submodules based on carrier phase shift modulation," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6778–6791, Sep. 2017.

[14] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Jan. 2015, doi: 10.1109/TPEL.2014.2309937.

[15] J. Pou, S. Ceballos, G. Konstantinou, V. G. Agelidis, R. Picas, and J. Zaragoza, "Circulating current injection methods based on instantaneous information for the modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 777–788, Feb. 2015, doi: 10.1109/TIE.2014.2336608.

[16] Z. Wang, A. Zhang, H. Zhang, and Z. Ren, "Control strategy for modular multilevel converters with redundant sub-modules using energy reallocation," *IEEE Trans. Power Del.*, vol. 32, no. 3, pp. 1556–1564, Jun. 2017, doi: 10.1109/TPWRD.2017.2670921.

[17] R. Darus, J. Pou, G. Konstantinou, S. Ceballos, R. Picas, and V. G. Agelidis, "A modified voltage balancing algorithm for the modular multilevel converter: Evaluation for staircase and phase-disposition PWM," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4119–4127, Aug. 2015, doi: 10.1109/TPEL.2014.2359005.

[18] M. M. Haji-Esmaeili, M. Naseri, H. Khoun-Jahan, and M. Abapour, "Fault-tolerant structure for cascaded H-bridge multilevel inverter and reliability evaluation," *IET Power Electron.*, vol. 10, no. 1, pp. 59–70, Jan. 2017, doi: 10.1049/iet-pel.2015.1025.

[19] H. K. Jahan, F. Panahandeh, M. Abapour, and S. Tohidi, "Reconfigurable multilevel inverter with fault-tolerant ability," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7880–7893, Sep. 2018, doi: 10.1109/TPEL.2017.2773611.

[20] H. Sepahvand, J. Liao, M. Ferdowsi, and K. A. Corzine, "Capacitor voltage regulation in single-DC-source cascaded H-bridge multilevel converters using phase-shift modulation," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3619–3626, Sep. 2013, doi: 10.1109/TIE.2012.2206335.

[21] V. V. S. Pradeep Kumar and B. G. Fernandes, "A fault-tolerant single-phase grid-connected inverter topology with enhanced reliability for solar PV applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 3, pp. 1254–1262, Sep. 2017, doi: 10.1109/JESTPE.2017.2687126.

[22] M. Jalhotra, L. Kumar, S. P. Gautam, and S. Gupta, "Development of fault-tolerant MLI topology," *IET Power Electron.*, vol. 11, no. 8, pp. 1416–1424, 2018.

[23] M. Rao. A and K. Sivakumar, "A fault-tolerant single-phase five-level inverter for grid-independent PV systems," *IEEE Trans. Ind. Electron.*, vol. 62, no. 12, pp. 7569–7577, Dec. 2015, doi: 10.1109/TIE.2015.2455523.

[24] S. P. Gautam, L. Kumar, S. Gupta, and N. Agrawal, "A single-phase five-level inverter topology with switch fault-tolerance capabilities," *IEEE Trans. Ind. Electron.*, vol. 64, no. 3, pp. 2004–2014, Mar. 2017, doi: 10.1109/TIE.2016.2626368.

[25] M. Aly, E. M. Ahmed, and M. Shoyama, "A new single-phase five-level inverter topology for single and multiple switches fault tolerance," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9198–9208, Nov. 2018, doi: 10.1109/TPEL.2018.2792146.

[26] S. P. Gautam, L. Kumar, and S. Gupta, "Single-phase multilevel inverter topologies with self-voltage balancing capabilities," *IET Power Electron.*, vol. 11, no. 5, pp. 844–855, May 2018, doi: 10.1049/iet-pel.2017.0401.

[27] S. P. Gautam, L. Kumar, S. Gupta, and A. H. Chander, "Reliability analysis of a novel fault tolerant multilevel inverter topology," in *Proc. 44th Annu. Conf. IEEE Ind. Electron. Soc.*, Oct. 2018, pp. 1460–1465, doi: 10.1109/IECON.2018.8592684.

[28] M. Jalhotra, S. P. Gautam, L. Kumar, and S. Gupta, "Single and multi switch fault tolerant topology of multi level inverter," in *Proc. Int. Conf. Power, Instrum., Control Comput. (PICC)*, Jan. 2018, pp. 1–6, doi: 10.1109/PICC.2018.8384814.

[29] M. Jalhotra, L. K. Sahu, S. P. Gautam, and S. Gupta, "Reliability and energy sharing analysis of a fault-tolerant multilevel inverter topology," *IET Power Electron.*, vol. 12, no. 4, pp. 759–768, Apr. 2019, doi: 10.1049/iet-pel.2018.5452.

[30] P. Barbosa, P. Steimer, J. Steinke, M. Winkelnkemper, and N. Celanovic, "Active-neutral-point-clamped (ANPC) multilevel converter technology," in *Proc. Eur. Conf. Power Electron. Appl.*, 2008, p. 10, doi: 10.1109/epe.2005.219713.

[31] G. E. Valderrama, G. V. Guzman, E. I. Pool-Mazun, P. R. Martinez-Rodriguez, M. J. Lopez-Sanchez, and J. M. S. Zuñiga, "A single-phase asymmetrical T-type five-level transformerless PV inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 1, pp. 140–150, Mar. 2018, doi: 10.1109/JESTPE.2017.2726989.

[32] A. Karthik and U. Loganathan, "A reduced component count five-level inverter topology for high reliability electric drives," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 725–732, Jan. 2020, doi: 10.1109/TPEL.2019.2913821.

[33] H. Wang, L. Kou, Y.-F. Liu, and P. C. Sen, "A seven-switch five-level active-neutral-point-clamped converter and its optimal modulation strategy," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5146–5161, Jul. 2017, doi: 10.1109/TPEL.2016.2614265.

[34] H. Wang, L. Kou, Y.-F. Liu, and P. C. Sen, "A new six-switch five-level active neutral point clamped inverter for PV applications," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6700–6715, Sep. 2017, doi: 10.1109/TPEL.2016.2623568.

[35] S. K. Maddugari, V. B. Borghate, S. Sabyasachi, and R. R. Karasani, "A fault tolerant cascaded multilevel inverter topology for open circuit faults in switches," in *Proc. IEEE Transp. Electrific. Conf. (ITEC-India)*, Dec. 2017, pp. 1–5, doi: 10.1109/ITEC-India.2017.8333861.

[36] S. K. Maddugari, V. B. Borghate, and S. Sabyasachi, "A reliable and efficient single-phase modular multilevel inverter topology," *Int. J. Circuit Theory Appl.*, vol. 47, no. 5, pp. 718–737, May 2019, doi: 10.1002/cta.2613.

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