IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 28 October 2023, accepted 22 November 2023, date of publication 24 November 2023,
date of current version 29 November 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3336767

RESEARCH ARTICLE

Hybrid Pulse-Width Modulation Strategy With Reduced High-Frequency Common-Mode Voltage to Lower RMS Motor Leakage Current for a Three-Level Neutral Point Clamped Converter

KHOA DANG PHAM, MON-VAN DOI, AND NHO-VAN NGUYEN, (Member, IEEE)
Faculty of Electrical and Electronics Engineering, Ho Chi Minh City University of Technology, Ho Chi Minh City 70000, Vietnam
Vietnam National University Ho Chi Minh City, Ho Chi Minh City 70000, Vietnam

Corresponding author: Nho-Van Nguyen (nvnho@hcmut.edu.vn)

This work was supported by the National Foundation for Science and Technology Development under Grant 103.99-2019.369.

ABSTRACT Due to the capacitive nature of Common-mode impedance, high-frequency Common-mode voltage due to high switching frequency leads to an increase in RMS leakage current, which, in turn, causes higher power loss, Electromagnetic Interferences, and deteriorated harmonic distortion in the three-level Neutral-Point-Clamped converter. Recently-proposed pulse-width modulation type 1 with reduced Common-mode-voltage magnitudes, zero average Common-mode-voltage, and improved harmonic distortion has been presented for the three-level Neutral-Point-Clamped converter. However, the high-frequency Common-mode voltage could be further mitigated by reducing the number of CMV variations. Therefore, this article presents a hybrid pulse-width modulation scheme featuring reduced Common-mode-voltage magnitudes and variations, zero average Common-mode-voltage, and improved harmonic distortion. The Common-mode-voltage variation reduction is realized by re-arranging the order of the switching states in the recently-proposed scheme in a carrier period. The resulting modified sequences type 1 suffer simultaneous switchings between two phase-legs, hence leading to Common-mode-voltage spike due to deadtime. Hence, another type of modified sequences (type 2) is utilized with the modified sequences type 1 and the information of three-phase currents, hence the term ''hybrid''. Results under Volt-per-Hertz-2.2KW-rated induction motor with different loading conditions in the Three-Level Neutral-Point-Clamped Converters indicate that at rated frequency of 50Hz, the proposed scheme leads to a noticeable decrease in RMS leakage current while producing similar-to-better harmonic distortion at the expense of slight reduction of the efficiency of a converter as opposed to the recently-proposed Reduced-Common-mode-voltage Pulse-width modulation type 1 with improved switching loss and Phase-Opposition-Disposition-Sinusoidal Pulse-width modulation.

INDEX TERMS Common-mode voltage, leakage current, neutral point clamped inverter, pulse-width modulation strategy.

ABBREVIATIONS

3L-NPCs	Three-Level Neutral-Point-Clamped Converters.
3L-SVD	Three-Level Space Vector Diagram.
CM	Common-Mode.
CMV	Common-Mode Voltage.
EMIs	Electromagnetics Interferences.
NP	Neutral Point.
HRCMV-CMC	Hybrid Reduced-Common Mode Voltage with Reduced High-Frequency Common-Mode Voltage.
M-RCMV1	Modified Reduced-Common Mode Voltage Pulse-Width Modulation Type 1.

The associate editor coordinating the review of this manuscript and approving it for publication was Zhilei Yao.

M-RCMV2	Modified Reduced-Common Mode Voltage Pulse-Width Modulation Type 2.
M-RCMV3	Modified Reduced-Common Mode Voltage Pulse-Width Modulation Type 3.
POD-SPWM	Phase Opposition Disposition Sinusoidal Pulse-Width Modulation.
PWM	Pulse-Width Modulation.
RCMV1	Reduced-Common Mode Voltage Pulse-Width Modulation Type 1.
RCMV1-SLO	Reduced-Common Mode Voltage Pulse-Width Modulation Type 1 with Improved Switching Loss.
V/f	Volt-per-Hertz.
ZCMV-PWMs	Zero-Common Mode Voltage Pulse-Width Modulation Schemes.

I. INTRODUCTION

Multilevel converters have found themselves in practical motor-drive applications owing to several advantages such as superior output harmonic distortion, lower voltage stress, lesser Electromagnetic Interferences (EMIs), and a large number of redundant switching states in comparison to traditional two-level converters [1], [2]. Three-level Neutral-Point-Clamped converters (3L-NPCs), as shown in Fig. 1, are one of the most popular multilevel topologies [2]. The three-level Neutral-Point-Clamped converters (3L-NPCs) are usually either fed with a single DC source or two isolated ones [3]. The single DC source requires Neutral-Point (NP) voltage balancing control, which can be achieved by hardware solutions [4], [5] or software (modulation schemes) [6], [7], [8], [9], [10]. An alternative practical approach to the Neutral Point (NP) voltage balancing is the use of two separate DC sources, which can be realized by the 12-pulse diode-bridge rectifier, hence the Neutral Point (NP) voltage being balanced [3]. And such a configuration is used in high-power applications and is considered in this article. Without the consideration of Neutral Point (NP) voltage balancing control, the modulation schemes derived for the mentioned configuration place emphasis on the reduction of Common-mode voltage (CMV), leakage current, and output harmonic distortion.

Despite the aforementioned merits of multilevel converters, Common-mode voltage (CMV) still exists, albeit being reduced in magnitude as opposed to two-level counterparts [1], [2], [3], [4], [5], [6], [7], [8], [9], [10]. Large-magnitude-and-high-frequency Common-mode voltage (CMV) gives rise to shaft voltage and bearing current, thereby reducing the service lifetime of motors [11], [12], [13], [14]. In addition, in medium-voltage applications, large magnitudes of Common-mode voltage (CMV) lead to the destruction of motor winding insulation [15]. Hence, the Common-mode voltage (CMV) magnitudes should be reduced for proper operation in motor-drive applications. Moreover, as for the high-frequency Common-mode voltage (CMV), the reduction of which can be achieved by reducing the Common-mode voltage variations. Research literature indicates that the high-frequency Common-mode voltage (CMV) induces leakage current flowing out of the motor frame, into the ground via motor parasitic capacitance, thus incurring power losses, EMIs, and deterioration of harmonic distortion [11], [12], [13], [14], [16]. Therefore, both large magnitudes and high frequency of Common-mode voltage (CMV) must be suppressed to keep the adverse effects of CMV at bay.

Aside from the large magnitudes and high frequency of Common-mode voltage (CMV), the low-frequency components of CMV also contribute to difficulty in Common-mode (CM) filter design [17], heated Common-mode (CM) inductors [17], low-frequency mechanical vibrations [18]. Therefore, the concept of zero average Common-mode voltage (CMV) has been introduced in [17] to suppress the low-frequency components of Common-mode voltage (CMV). In practice, long cables connected between an inverter and a motor further exacerbates the negative issues relating to high-frequency and low-frequency components of Common-mode voltage (CMV) [19], [20].

Several modulation schemes have been put forward to eliminate the Common-mode voltage (CMV) magnitudes, namely Zero-CMV-magnitude pulse-width modulation schemes (ZCMV-PWMs) [21], [22], [23], [24]. Even though the Common-mode voltage (CMV) magnitudes are eliminated, the common drawbacks of these modulation schemes are inferior output harmonic distortion [21], [22], [23] and Common-mode voltage (CMV) spikes [24], [25]. The poor output harmonic distortion is due to the utilization of distant voltage vectors [21], [22], [23]. Meanwhile, the Common-mode voltage (CMV) spikes occur owing to the simultaneous switching commutations of two phase-legs [24], [25]. As a result, most research works focus on these two issues. In [21], [22], and [23], research works attempt to lower output harmonic distortion by either utilizing the redundancy of switching patterns [21] or modifying the switching sequence [22], [23] with the help of Harmonic Distortion Factor [26]. Nevertheless, due to the nature of use of distant voltage vectors, the output harmonic distortion given by [21], [22], and [23] is still significantly higher than the conventional Sinusoidal PWM, which makes use of three nearest voltage vectors [3]. It is also worth noting that the focus of research works in [21], [22], and [23] is on the improvement of output harmonic distortion while leaving the Common-mode voltage (CMV) spikes undealt with. Hence, the Common-mode voltage (CMV) spikes still occur in [21], [22], and [23]. As a result, the research work in [24] has been proposed to reduce the Common-mode voltage (CMV) spikes. Even though the Common-mode voltage (CMV) spikes are effectively reduced, the inferior output harmonic distortion in still remains [24].

To extend the linear modulation range in Zero-CMV-magnitude pulse-width modulation schemes (ZCMV-PWMs) [21], [22], [23], [24], another group of pulse-width modulation (PWM) schemes featuring reduced Common-mode voltage (CMV) magnitudes and constant Common-mode voltage (CMV) has been suggested to suppress the high-frequency

components of Common-mode voltage (CMV) [27], [28], [29], [30]. In these modulation schemes, the CMV magnitudes are constant over a carrier period, hence the term constant CMV as mentioned in [27], [28], [29], and [30]. Even though the high-frequency components of Common-mode voltage (CMV) are effectively suppressed, the low-frequency ones due to the non-zero average Common-mode voltage (CMV) occurs, thereby leading to the Common-mode voltage (CMV)-related issues owing to low-frequency components of Common-mode voltage (CMV). Moreover, in order to maintain per-carrier equipotential of Common-mode voltage (CMV), remote voltage vectors are used, thus causing inferior output harmonic distortion [27], [28], [29], [30]. Similar to the Zero-CMV-magnitude pulse-width modulation schemes (ZCMV-PWMs) [21], [22], [23], [24], simultaneous switching commutations in any two phase-legs also occur, hence giving rise to the Common-mode voltage (CMV) spikes [27], [28], [29], [30].

In order to avoid the inferior output harmonic distortion and the Common-mode voltage (CMV) spikes while still being able to mitigate the adverse effects of Common-mode voltage (CMV), another group of pulse-width modulation (PWM) schemes featuring reduced Common-mode voltage (CMV) magnitudes and zero average Common-mode voltage (CMV) has been utilized [31], [32], [33]. One notable pulse-width modulation (PWM) scheme in this category is the conventional Phase Opposition Disposition Sinusoidal PWM (POD-SPWM) [31]. Recently, a novel modulation scheme, namely RCMV1, which possesses reduced CMV magnitudes, zero average CMV, and even lower output harmonic distortion than POD-SPWM, has been proposed in [32]. Moreover, an improved version of RCMV1, namely RCMV1-SLO, has been introduced to reduce the extra switchings, thereby optimizing switching loss while inheriting all the positive features of RCMV1 [33].

Nevertheless, despite the reduced Common-mode voltage (CMV) magnitudes and the suppression of low-frequency components of Common-mode voltage (CMV), the high-frequency Common-mode voltage (CMV) have remained untouched. The high-frequency Common-mode voltage (CMV) can be mitigated by reducing the CMV variations. As shall be demonstrated in the later section, the number of variations in Common-mode voltage (CMV) values is 6 times per carrier period in RCMV1 [32], and RCMV1-SLO [33], thereby contributing to bearing current and leakage current. With the increase in switching frequency enabled by the wide-bandgap switching devices [34], [35], [36], high-frequency Common-mode voltage (CMV) further aggravates the Common-mode voltage (CMV)-related issues. Therefore, this article presents a hybrid pulse-width modulation strategy possessing reduced Common-mode voltage (CMV) magnitudes, lowered Common-mode voltage (CMV) variations, zero average Common-mode voltage (CMV), and improved output harmonic distortion, namely HRCMV-CMC. This scheme is based on the modified version of the previously

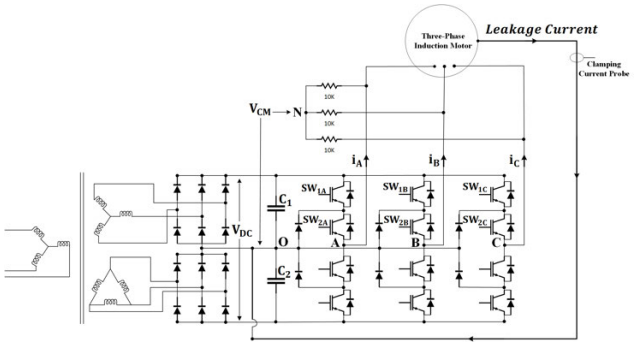


FIGURE 1. A 3L-NPC fed with 12-pulse diode-bridge rectifier for a three-phase induction motor load.

presented one (RCMV1) [32], hence the term M-RCMV1. Specifically, the order of switching states in a carrier period is rearranged to achieve the reduction of CMV variations. The term ''hybrid'' comes from the fact that the utilization of both M-RCMV1 and another modified scheme (M-RCMV2) are required to avoid the CMV spikes based on the information of phase currents. It is worth noting that M-RCMV1 takes precedence over M-RCMV2 due to having better output harmonic distortion in the case that both sequences are capable of compensating for the deadtime to avoid CMV spikes.

The main contributions of HRCMV-CMC are summarized as follows:

(1) HRCMV-CMC features reduced high-frequency Common-mode voltage while yielding lowered Common-mode voltage magnitudes, zero average CMV, and improved output harmonic distortion in comparison to RCMV1-SLO and POD-SPWM. The reduced high-frequency Common-mode voltage, which is achieved by lowering the CMV variations, leads to a deduction in RMS leakage current.

(2) HRCMV-CMC involves the use of either M-RCMV1 or M-RCMV2 in combination with the three-phase currents to achieve the reduction of CMV variations and avoid CMV spikes due to deadtime effect. The choice of either M-RCMV1 or M-RCMV2 depends on the information of phase currents to avoid CMV spikes with M-RCMV1 taking precedence over M-RCMV2 due to having better output harmonic distortion.

(3) Thorough simulated and experimental analyses of CMV, leakage current, harmonic distortion, and switching loss/efficiency are demonstrated to confirm the effectiveness of HRCMV-CMC over RCMV1-SLO and POD-SPWM under the balanced three-phase R-L load and V/f induction motor with different loading conditions.

The rest of article is organized as follows. Section II briefly reviews the previously presented schemes. The modifications of which are then proposed to reduce CMV variations. Deadtime analysis is shortly presented, leading up to the proposed hybrid pulse-width modulation (PWM) scheme, namely HRCMV-CMC. Section III demonstrates in-depth simulated and experimental analyses of CMV, leakage current,

harmonic distortion, and switching loss for HRCMV-CMC, RCMV1-SLO, and POD-SPWM. Section IV concludes the article with some remarks.

II. PROPOSED HYBRID REDUCED-CMV PWM SCHEME WITH REDUCED HIGH-FREQUENCY CMV (HRCMV-CMC)

A. PREVIOUSLY PROPOSED SCHEME [32]

This subsection briefly describes the previously presented strategy to set the scene for the subsequent sections. To facilitate the description, Eq. (1) – (11) are shown below.

The instantaneous pole voltages V_{AO}, V_{BO}, and V_{CO} are defined as follows.

$$\begin{cases} V_{AO} = (S_{1A} + S_{2A}) \times \dfrac{V_{DC}}{2} - \dfrac{V_{DC}}{2} \\ \quad = V_{AN} \times \dfrac{V_{DC}}{2} - \dfrac{V_{DC}}{2} \\ V_{BO} = (S_{1B} + S_{2B}) \times \dfrac{V_{DC}}{2} - \dfrac{V_{DC}}{2} \\ \quad = V_{BN} \times \dfrac{V_{DC}}{2} - \dfrac{V_{DC}}{2} \\ V_{CO} = (S_{1C} + S_{2C}) \times \dfrac{V_{DC}}{2} - \dfrac{V_{DC}}{2} \\ \quad = V_{CN} \times \dfrac{V_{DC}}{2} - \dfrac{V_{DC}}{2} \end{cases} \tag{1}$$

where: V_{AN}, V_{BN}, and V_{CN} are normalized instantaneous three-level switching voltages, taking a value of 2, 1, or 0. V_{dc} is the total DC-link voltage of the 3L-NPC. S_{1A} and S_{2A} are the switching states of SW_{1A} and SW_{2A}, assuming a value of 0 or 1. Similarly, S_{1B} and S_{2B} are the switching states of SW_{1B} and SW_{2B}. S_{1C} and S_{2C} are the switching states of SW_{1C} and SW_{2C}.

In the 3L-NPC, there are constraints, specifically $S_{1A} \leq S_{2A}$, $S_{1B} \leq S_{2B}$, $S_{1C} \leq S_{2C}$.

The normalized instantaneous three-level switching voltages V_{AN}, V_{BN}, and V_{CN} can also be decomposed into 2 components as follows.

$$\begin{cases} V_{AN} = L_A + s_A \\ V_{BN} = L_B + s_B \\ V_{CN} = L_C + s_C \end{cases} \tag{2}$$

where: L_A, L_B, and L_C are the normalized base voltages, taking a value of 0 or 1 in the 3L-NPC. s_A, s_B, and s_C are the normalized instantaneous two-level switching voltages, taking a value of 0 or 1.

The instantaneous CMV can be defined as follows.

$$\begin{aligned} V_{CM} &= \frac{(V_{AO} + V_{BO} + V_{CO})}{3} \\ &= \frac{(V_{AN} + V_{BN} + V_{CN} - 3) \times V_{DC}}{6} \end{aligned} \tag{3}$$

The normalized average three-level switching voltages v'_{Aref}, v'_{Bref}, and v'_{Cref} are defined as follows.

$$\begin{cases} v'_{Aref} = v_{Aref} + v_{off} = \dfrac{2 \times m}{\sqrt{3}} \times \cos(\omega t) + v_{off} \\ v'_{Bref} = v_{Bref} + v_{off} = \dfrac{2 \times m}{\sqrt{3}} \times \cos\left(\omega t - \dfrac{2\pi}{3}\right) + v_{off} \\ v'_{Cref} = v_{Cref} + v_{off} = \dfrac{2 \times m}{\sqrt{3}} \times \cos\left(\omega t + \dfrac{2\pi}{3}\right) + v_{off} \end{cases} \tag{4}$$

where: v_{Aref}, v_{Bref}, and v_{Cref} are the normalized average reference load voltages. v_{off} is the normalized offset voltage. m is the modulation index.

The average CMV can be defined as follows.

$$v_{CM} = \frac{\left(v'_{Aref} + v'_{Bref} + v'_{Cref}\right)}{3} = \frac{(3 \times v_{off} - 3) \times V_{DC}}{6} \tag{5}$$

Since $v_{Aref} + v_{Bref} + v_{Cref} = 0$. Hence, under the zero average CMV condition, v_{off} is equal to 1 in the 3L-NPC. Hence, Eq. (4) can be re-written as:

$$\begin{cases} v'_{Aref} = \dfrac{2 \times m}{\sqrt{3}} \times \cos(\omega t) + 1 \\ v'_{Bref} = \dfrac{2 \times m}{\sqrt{3}} \times \cos\left(\omega t - \dfrac{2\pi}{3}\right) + 1 \\ v'_{Cref} = \dfrac{2 \times m}{\sqrt{3}} \times \cos\left(\omega t + \dfrac{2\pi}{3}\right) + 1 \end{cases} \tag{6}$$

The modulation index is defined as follows.

$$m = \frac{V_{1m}}{\frac{1}{\sqrt{3}} \times V_{DC}} \tag{7}$$

where: V_{1m} is the fundamental magnitude of the phase voltages. Under the zero average CMV condition, m falls into the range of $0 \leq m \leq \sqrt{3}/2$.

The normalized average three-level switching voltages v'_{Aref}, v'_{Bref}, and v'_{Cref} can also be decomposed into two components as follows.

$$\begin{cases} v'_{Aref} = L_A + \xi_A \\ v'_{Bref} = L_B + \xi_B \\ v'_{Cref} = L_C + \xi_C \end{cases} \tag{8}$$

where: L_A, L_B, and L_C are the normalized base voltages, taking a value of 0 or 1 in the 3L-NPC. ξ_A, ξ_B, and ξ_C are the normalized average two-level switching voltages. They are calculated as follows.

$$\begin{cases} L_A = floor\left(v'_{Aref}\right) \\ L_B = floor\left(v'_{Bref}\right) \\ L_C = floor\left(v'_{Cref}\right) \end{cases} \tag{9}$$

$$\begin{cases} \xi_A = v'_{Aref} - L_A \\ \xi_B = v'_{Bref} - L_B \\ \xi_C = v'_{Cref} - L_C \end{cases} \tag{10}$$

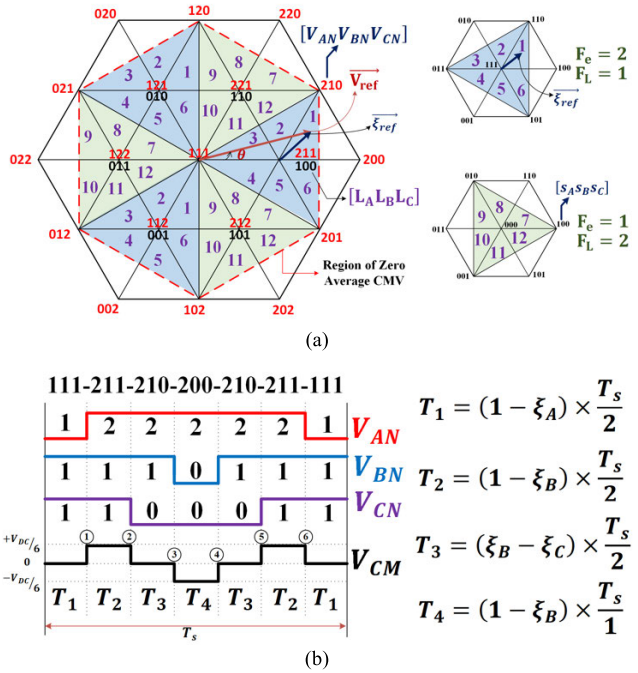


FIGURE 2. (a) A 3L-SVD with the constitution of two types of two-level Space Vector Diagram (b) Per-carrier switching sequence of RCMV1 for the synthesis of $\overrightarrow{V_{ref}}$ at the location 1(100).

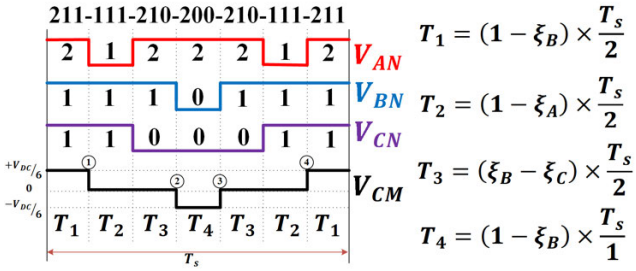


FIGURE 3. Modified switching sequence of RCMV1 with reduced CMV variations (M-RCMV1).

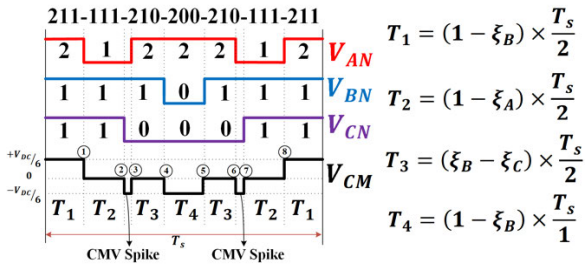


FIGURE 4. CMV spikes due to deadtime effect in M-RCMV1 for $i_A \times i_C > 0$.

TABLE 1. Identification of sub-regions via relation of average two-level active switching voltages and base voltages.

F_L=$L_A + L_B + L_C$	Relation of ξ_A, ξ_B, ξ_C	Sub-regions
1	$\xi_A \geq \xi_B \geq \xi_C$	1
	$\xi_B \geq \xi_A \geq \xi_C$	2
	$\xi_B \geq \xi_C \geq \xi_A$	3
	$\xi_C \geq \xi_B \geq \xi_A$	4
	$\xi_C \geq \xi_A \geq \xi_B$	5
	$\xi_A \geq \xi_C \geq \xi_B$	6
2	$\xi_A \geq \xi_B \geq \xi_C$	7
	$\xi_B \geq \xi_A \geq \xi_C$	8
	$\xi_B \geq \xi_C \geq \xi_A$	9
	$\xi_C \geq \xi_B \geq \xi_A$	10
	$\xi_C \geq \xi_A \geq \xi_B$	11
	$\xi_A \geq \xi_C \geq \xi_B$	12

The total normalized average two-level switching voltage (F_e) and the total normalized base voltage (F_L) are defined as follows.

$$\begin{cases} F_e = \xi_A + \xi_B + \xi_C \\ F_L = L_A + L_B + L_C \end{cases} \tag{11}$$

The total base voltage (F_L) and total average two-level switching voltage (F_e) divide 3L-SVD into two distinct regions, namely $F_e = 2$ ($F_L = 1$) and $F_e = 1$ ($F_L = 2$).

The sub-regions are designated from (1) to (6) for $F_e = 2$ ($F_L = 1$) and from (7) to (12) for $F_e = 1$ ($F_L = 2$).

These sub-regions can be identified via the relation of the normalized average two-level switching voltages, specifically ξ_A, ξ_B, and ξ_C, as shown in Table. 1.

The location of $\overrightarrow{V_{ref}}$ can be then identified by such relation and the base voltages. As shown in Fig. 2 and Table. 1, the position of $\overrightarrow{V_{ref}}$ can be located by $\xi_A \geq \xi_B \geq \xi_C$ and $L_AL_BL_C = 100$, or abbreviated as 1(100) from this point forward.

RCMV1 has been proposed in [32]. The features of which consist of lowered CMV magnitudes, zero average CMV, and improved output harmonic distortion. The per-carrier switching sequence of RCMV1 is shown in Fig. 2(b) to synthesize $\overrightarrow{V_{ref}}$ at 1(100). As can be observed in Fig. 2(b), despite achieving reduced CMV magnitudes and zero average CMV, RCMV1 still possesses the high number of CMV variations. Specifically, the number of variations in CMV values is 6 times per-carrier period. Due to the capacitive nature of CM impedance in motors [37], [38], the high number of CMV variations leads to motor leakage current, resulting in increased power loss, EMIs, deteriorated output harmonic distortion, and nuisance tripping of circuit breakers [11], [12], [13], [14]. Therefore, the next section discusses the proposed scheme to lower the CMV variations.

B. PROPOSED HYBRID SCHEME (HRCMV-CMC)

To lower the CMV variations while maintaining reduced CMV magnitudes, zero average CMV, and enhanced output harmonic distortion, the order of the switching states in RCVM1 as shown in Fig. 2(b) are rearranged. Specifically, the switching states, which generate zero CMV magnitude, are grouped together such that the number of variations in CMV values is reduced from 6 to 4. And the newly modified switching pattern is termed M-RCVM1 and shown in Fig. 3.

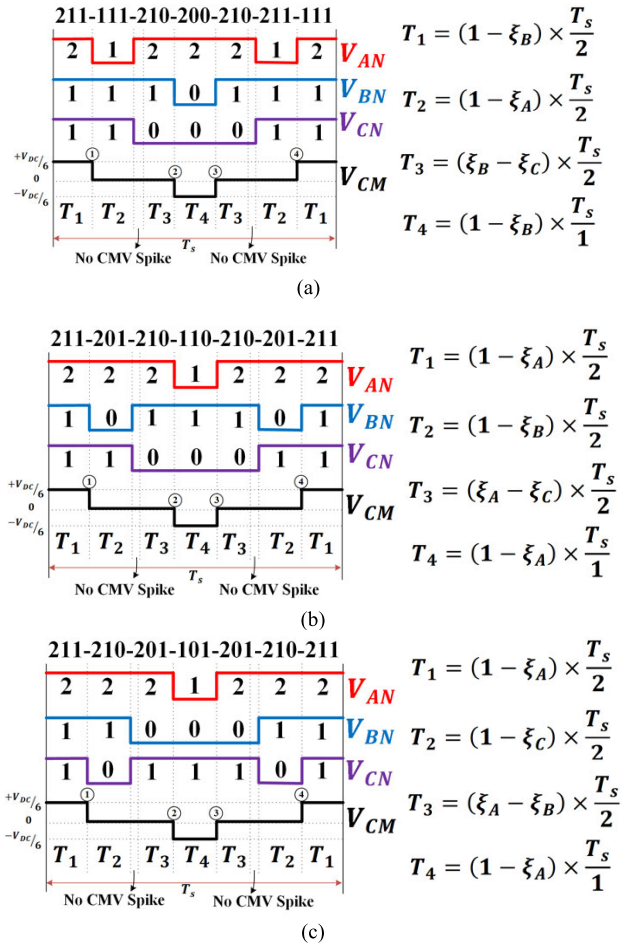


FIGURE 5. CMV spikes due to deadtime effect in (a) Modified switching sequence type 1 (M-RCMV1) for $i_A \times i_C \leq 0$ (b) Modified switching sequence type 2 (M-RCMV2) for $i_B \times i_C \leq 0$ and (c) Modified switching sequence type 3 (M-RCMV3) for $i_B \times i_C \leq 0$.

Under the capacitive characteristics of motor CM impedance [37], [38], the reduced CMV variations in the modified switching pattern is expected to lower motor leakage current. However, due to the deadtime implemented in practical applications to avoid shoot-through, simultaneous switching commutations, which occur between phase A and C, as can be observed in Fig. 3, give rise to CMV spike, thereby rendering the reduction of CMV variations less effective [16], [21], [22], [23], [24], [25].

The analysis of deadtime effect on CMV spikes has been presented in detail in [24] and [25]. Therefore, it shall be briefly summarized as follows. In 3L-NPCs, to avoid CMV spikes, two phase-legs, which experience simultaneous switching commutations, must have opposite phase current directions, i.e., $i_x \times i_y \leq 0$, where the subscripts x and y refer to the two phase-legs x and y respectively having simultaneous switching commutations. The positive current direction in this article is defined as the one flowing from the inverter to motor, as illustrated in Fig. 1, whereas the negative one is the one flowing from the motor to inverter.

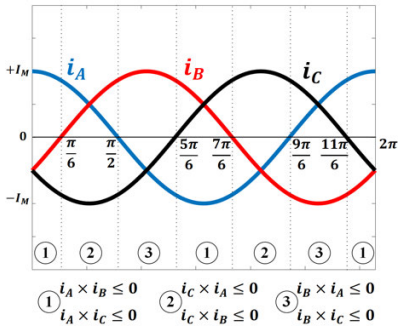


FIGURE 6. Phase current directions over the course of fundamental period.

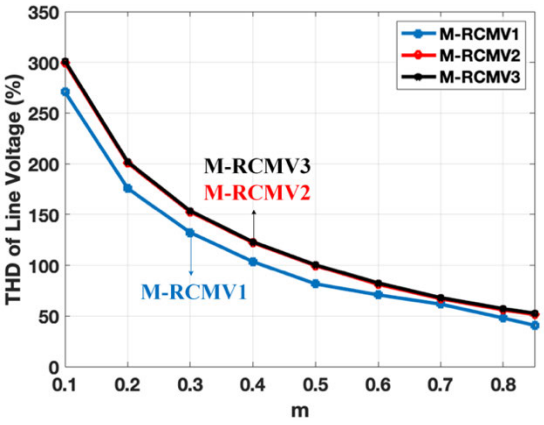


FIGURE 7. Simulated THD of Line voltage of M-RCMV1, M-RCMV2, M-RCMV3 with respect to modulation index under PF = 0.85 and other parameters tabulated in Table. 4.

The modified per-carrier switching sequence M-RCMV1 is re-illustrated with the deadtime being taken into account for $i_A \times i_C > 0$ and $i_A \times i_C \leq 0$, as demonstrated in Fig. 4 and 5(a) respectively.

As can be observed in Fig. 4 and 5(a), the per-carrier switching sequence of M-RCMV1 for the synthesis of $\overrightarrow{V_{ref}}$ at 1(100) can avoid the CMV spikes as the two phase-legs, i.e., phase A and C, which experience coinciding switching commutations, exhibit opposite phase current directions or $i_A \times i_C \leq 0$.

Under the condition of steady-state balanced three-phase currents ($i_a + i_b + i_c = 0$), there always exist two pairs of two phase-legs in which phase current directions are opposite. And they are designated from 1 to 3, as illustrated in Fig. 6. For instance, in region 1, the two pairs of two phase-legs having opposite phase current directions are (A, B) and (A, C). And other regions are also similar. Therefore, to avoid the CMV spikes under arbitrary power factor conditions, as the reference vector $\overrightarrow{V_{ref}}$ is at a specific location in the 3L-SVD, there must exist two per-carrier switching sequences, which are capable of synthesizing the reference vector at the same location. And they each possess a different pair of phase legs having simultaneous switching commutations.

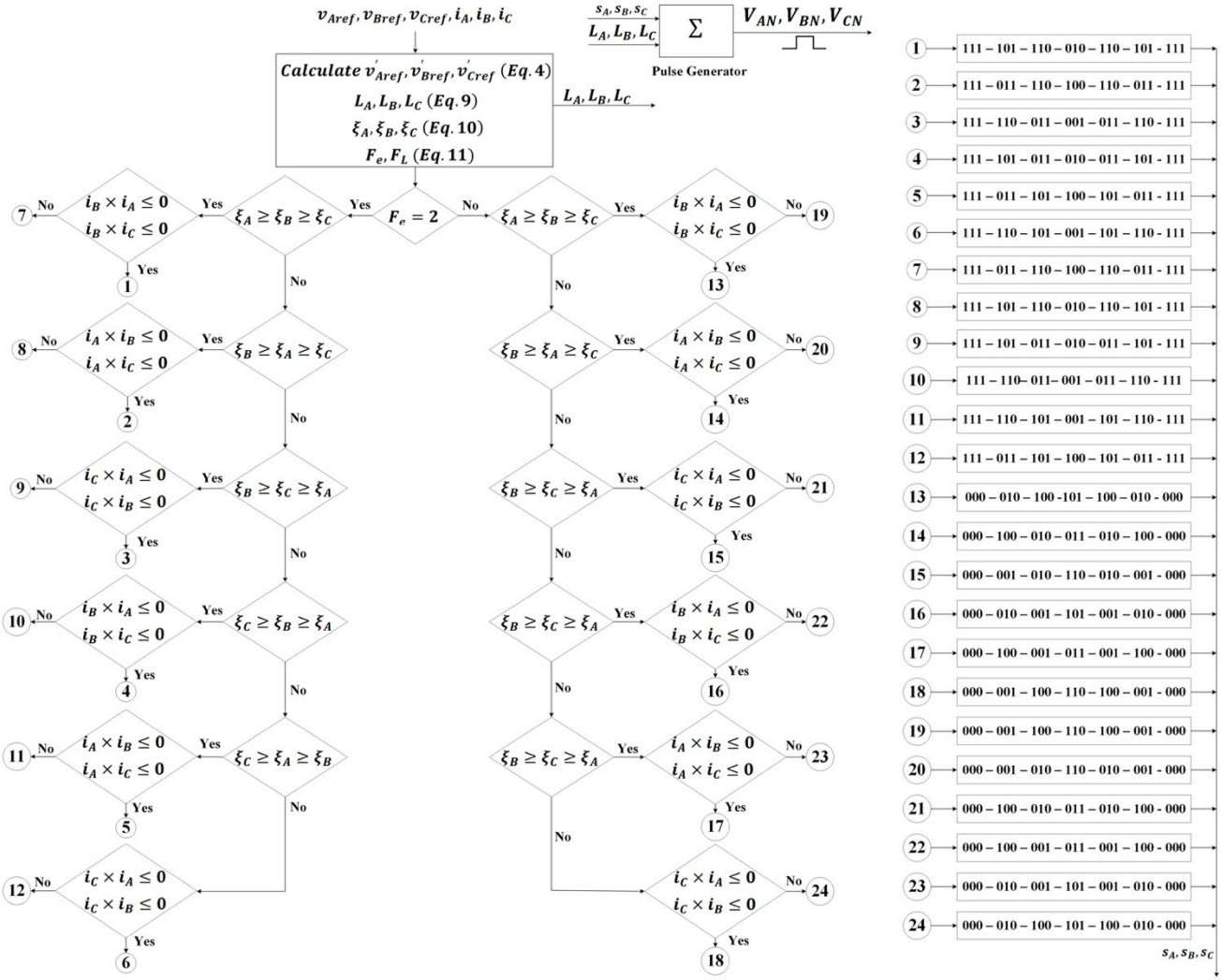


FIGURE 8. Flowchart of the proposed HRCMV-CMC.

TABLE 2. Simulated THD of line voltage of M-RCMV1, M-RCMV2, and M-RCMV3 with respect to modulation index PF = 0.85 and other parameters tabulated in Table. 4.

m	THD of Line Voltage (%)		
	M-RCMV1	M-RCVM2	M-RCMV3
0.1	270.81	299.73	301.29
0.3	132.71	152.63	152.92
0.6	71.77	81.16	82.55
0.85	41.60	51.48	52.68

TABLE 3. Deadtime compensation with M-RCMV1 and M-RCMV2 as $\overrightarrow{V_{ref}}$ is at 1(100).

	3 Regions of Phase Current Polarity		
	$i_b \times i_a \leq 0$ $i_b \times i_c \leq 0$	$i_a \times i_b \leq 0$ $i_a \times i_c \leq 0$	$i_c \times i_a \leq 0$ $i_c \times i_b \leq 0$
Choice of Sequence	M-RCMV2	M-RCMV1	M-RCMV1

To explain this in detail, let's take $\overrightarrow{V_{ref}}$ at 1(100) as an example. As illustrated in Fig. 5(a), the per-carrier switching sequence of M-RCMV1 is used to synthesize $\overrightarrow{V_{ref}}$ at the location 1(100) in the 3L-SVD, comprising a pair of two phase-legs A and C having simultaneous switching commutations. Hence, another switching sequence, which is also able to synthesize $\overrightarrow{V_{ref}}$ at 1(100) and exhibits simultaneous switching commutations of two phase-legs, i.e., either (A, B) or (B, C), are required to compensate for the deadtime under arbitrary power factor conditions. Fortunately, as presented in [30], besides the per-carrier switching sequence, as shown in Fig. 5(a) for the synthesis of $\overrightarrow{V_{ref}}$, there are also two other per-carrier switching sequences, namely RCMV2 and RCMV3, also featuring reduced CMV magnitudes, zero average CMV. The modifications of which are demonstrated in Fig. 5(b) and 5(c) and are termed M-RCMV2 and M-RCMV3 respectively. As can be seen in Fig. 5(b) and (5c), the per-carrier switching sequences in both M-RCMV2 and M-RCMV3 have simultaneous switching commutations

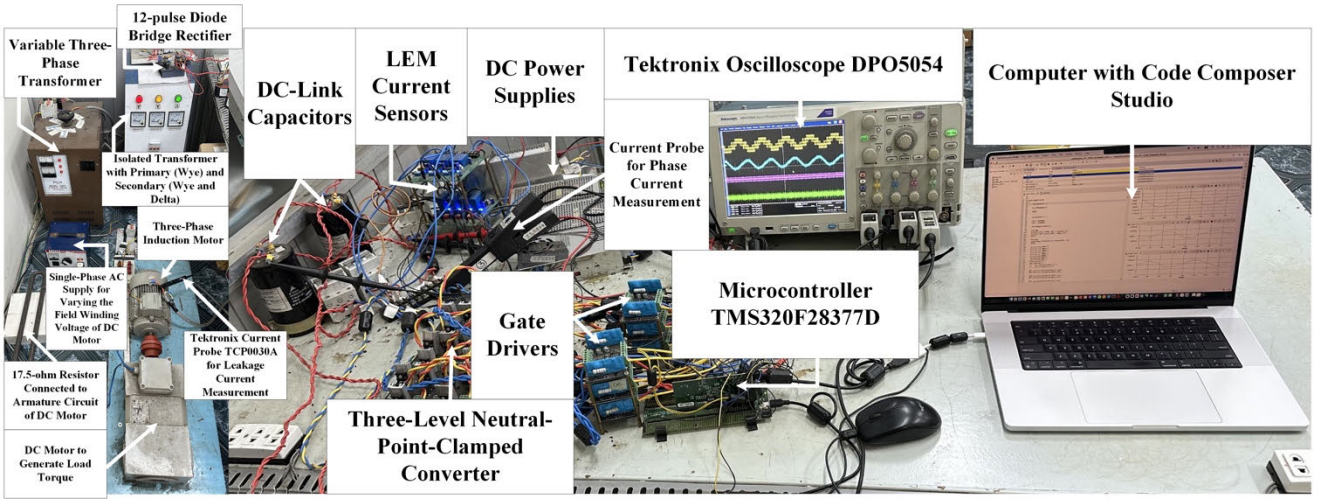


FIGURE 9. A snapshot of the experimental setup used for the analysis of the proposed schemes (HRCMV-CMC), the previously proposed scheme (RCMV1-SLO), and POD-SPWM.

occurring at phase legs B and C for the synthesis of $\overrightarrow{V_{ref}}$ at 1(100). Therefore, in combination with M-RCMV1, either M-RCMV2 or M-RCMV3 is required to avoid the CMV spikes.

As investigated in detail via simulation and experimental results, RCMV1 gives the best output harmonic distortion, which is followed by RCMV2, and then RCMV3. Hence, M-RCMV1 and M-RCMV2 are expected to produce better output harmonic distortion accordingly. To confirm the harmonic distortion given by M-RCMV1, M-RCMV2, and M-RCMV3, simulated Total Harmonic Distortion (THD) of Line Voltage with respect modulation index, which is conducted under Power Factor of 0.85 and other parameters as shown in Table. 4, are demonstrated in Fig. 7 and Table. 2. Based on these results, M-RCMV1 and M-RCMV2 produce better output harmonic distortion than M-RCMV3. As a result, M-RCMV1 and M-RCMV2 are selected to avoid the CMV spikes and to optimize output harmonic distortion. It is worth noting that the requirement of avoiding the CMV spikes takes precedence over that of optimized output harmonic distortion. In the case that both M-RCMV1 and M-RCMV2 are able to avoid the CMV spikes, M-RCMV1 will be selected due to having better harmonic distortion than M-RCMV2. For example, Table. 3 illustrates the use of switching sequences of M-RCMV1 and M-RCMV2, as shown in Fig. 5(a) and 5(b) respectively, to avoid the CMV spikes as the reference vector $\overrightarrow{V_{ref}}$ is at 1(100).

To completely demonstrate the use of M-RCMV1 and M-RCMV2 to avoid the CMV spikes for other locations which $\overrightarrow{V_{ref}}$ is in, the flowchart in Fig. 8 is shown. The use of both M-RCMV1 and M-RCMV2 leads to Hybrid PWM scheme and is termed HRCMV-CMC in this article.

III. VERIFICATIONS

Both simulation and experiment are conducted to thoroughly investigate the CMV performance, leakage current, and harmonic distortion, as well as switching loss and efficiency for HRCMV-CMC, RCMV1-SLO, and POD-SPWM.

It is worth noting that RCMV1-SLO is an improved version of RCMV1, which inherits all the positive features of RCMV1 in addition to optimized switching loss. Hence, it is selected to provide an up-to-date comparison with the proposed scheme.

TABLE 4. Parameters of simulation and experiment.

Parameters	Values	
	Simulation	Experiment
Rated Apparent Power of Inverter	S = 3.0KVA	S = 3.0KVA
Total DC-Link Voltage	$V_{DC} = 360V$	$V_{DC} = 360V$
DC-Link Capacitance	$C_1 = C_2 = 4700\mu F$	$C_1 = C_2 = 4700\mu F$
Fundamental Frequency	$f_m = 50Hz$	Varied, V/f
Carrier Frequency	$f_{cr} = 5KHz$	$f_{cr} = 5KHz$
Three-Phase R-L Load	R = 15.4Ω, L = 30mH (PF = 0.85) R = 3.62Ω, L = 56.5mH (PF = 0.2)	N/A
Three-Phase Induction Motor	N/A	2.2KW, 380V(Y)/220V(Δ), 4.7A(Y)/8.15A(Δ), PF = 0.85, R_s=3Ω, L_m= 0.2496H, R_r=2.2844Ω, L_{ls}=L_{lr}=0.0137H, open-loop V/f control, delta-connected
DC Motor	N/A	2.2KW, V_A = 260V, I_A = 9.6A, V_F = 200V, I_F = 0.5A
Deadtime	$2\mu s$	$2\mu s$
Microcontroller	N/A	TMS320F28377D
Simulation Platform	PLECS	N/A

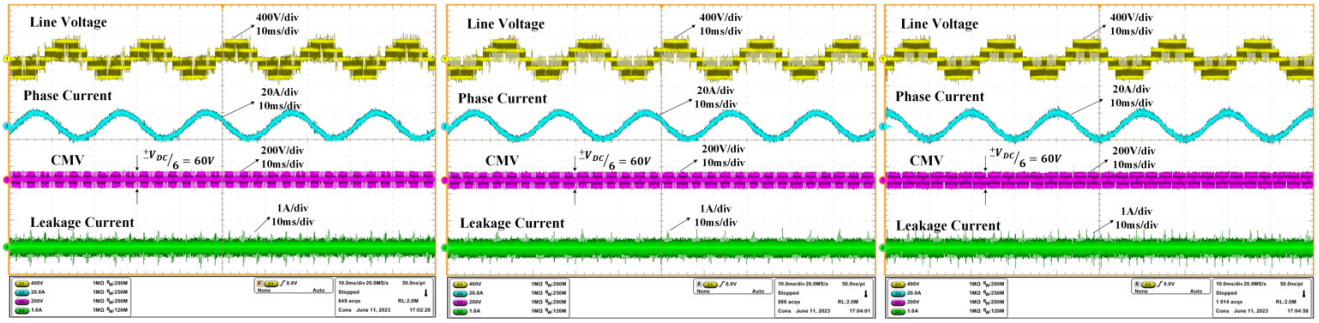


FIGURE 10. Experimental waveforms of line voltage, phase current, CMV, and leakage current over 5 cycles of the fundamental period of 20ms for (a) HRCMV-CMC (b) RCMV1-SLO and (c) POD-SPWM under full load (f_m = 50Hz (m = 0.866), PF = 0.85).

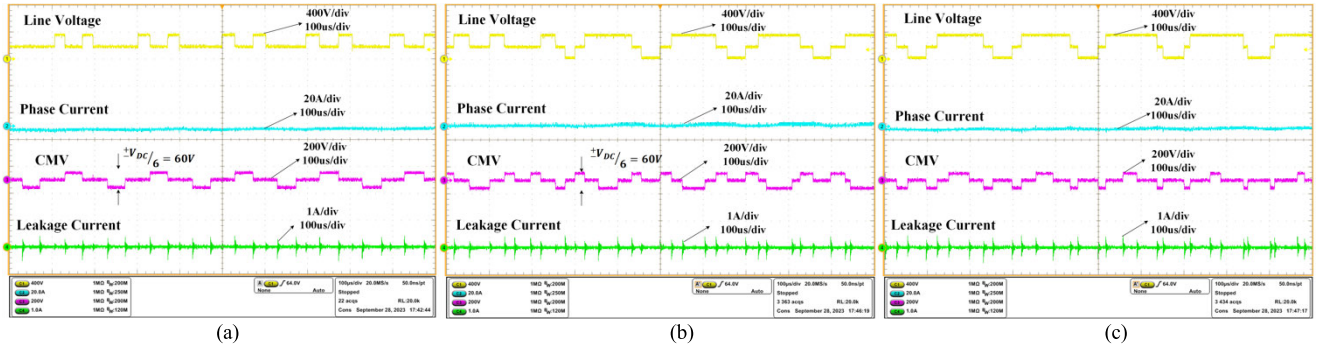


FIGURE 11. Experimental waveforms of line voltage, phase current, CMV, and leakage current over 5 cycles of the carrier period of 200μs for (a) HRCMV-CMC (b) RCMV1-SLO and (c) POD-SPWM under full load (f_m = 50Hz (m = 0.866), PF = 0.85).

A 2.2KW-rated three-phase induction motor is operated under open-loop V/F control, whose shaft is coupled with that of a DC motor for the purpose of generating load torque.

The load torque is created by varying the field winding voltage of the DC motor. Hence, the performance of the proposed scheme can be analyzed under different loading conditions.

Meanwhile, the armature circuit is formed a closed-loop circuit by hooking up with an external resistor of 17.5Ω.

All PWM schemes are coded in the Code Composer Studio and loaded into the microcontroller TMS320F28377D from Texas Instruments.

The experimental setup, which is used to conduct the comparative analyses of the proposed scheme (HRCMV-CMC), the previously proposed scheme (RCMV1-SLO), and POD-SPWM in terms of CMV, leakage current, and output harmonic distortion, is shown in Fig. 9.

The experimental waveforms of line voltage, phase current, CMV, and leakage current are illustrated in Fig. 9(a), (b), and (c) over 5 cycles of the fundamental period of 20ms for HRCMV-CMC, RCMV1-SLO, and POD-SPWM respectively under full load (f_m = 50Hz (m = 0.866), PF = 0.85).

To clearly distinguish the reduction of CMV variations in the proposed scheme over the other two PWM strategies, the experimental waveforms over 5 cycles of the carrier period of 200μs are shown in Fig. 10.

A. CMV ANALYSIS

The CMV is normally measured between the neutral point of the induction motor and that of the DC-link voltage (O). However, since the induction is delta-connected, in order to access to the neutral point of the induction motor, three Y-connected resistors, which have a resistance value of 10KΩ each, are connected in parallel with the induction motor, as shown in Fig. 1. The neutral point of these three resistors is denoted as (N). Hence, the CMV is measured between the point (N) and (O) of the DC-link voltage. The Tektronix differential probe THDP0200 with the bandwidth of 200MHz [42] is used to measure the CMV. The Tektronix oscilloscope DPO5054 [44] with the bandwidth of 500MHz and up-to-5GS/s real-time sample rate is then used to capture the figures and data of the CMV waveforms.

The macroscopic and microscopic views of simulated CMV waveforms are shown in Fig. 12(a), (b), and (c) for HRCMV-CMC, RCMV1-SLO, and POD-SPWM respectively at m = 0.866, PF = 0.85. Likewise, the experimental CMV waveforms are also shown in Fig. 13(a), (b), and (c) for HRCMV-CMC, RCMV1-SLO, and POD-SPWM respectively at f_m = 50Hz (m = 0.866), PF = 0.85.

As can be observed in Fig. 12 and 13, all PWM strategies achieve reduced CMV magnitudes, i.e., $\pm V_{DC}/6$ or $\pm 60V$. Moreover, the condition of zero average CMV is also maintained for all modulation schemes.

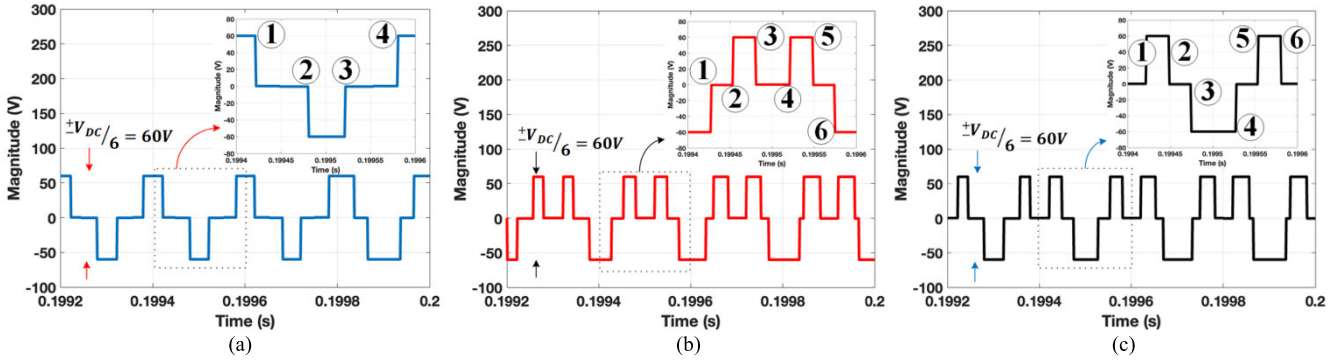


FIGURE 12. Macroscopic and microscopic views of simulated CMV waveforms of (a) HRCMV-CMC (b) RCMV1-SLO and (c) POD-SPWM at m = 0.866, PF = 0.85.

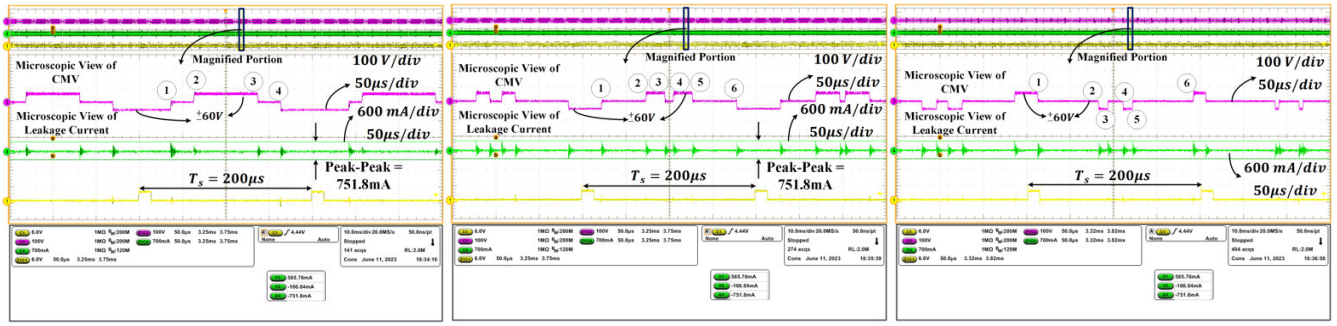


FIGURE 13. Macroscopic and microscopic views of experimental CMV waveforms (top trace, pink) and leakage current (bottom trace, green) of (a) HRCMV-CMC (b) RCMV1-SLO and (c) POD-SPWM under full load (f_m = 50Hz (m = 0.866), PF = 0.85).

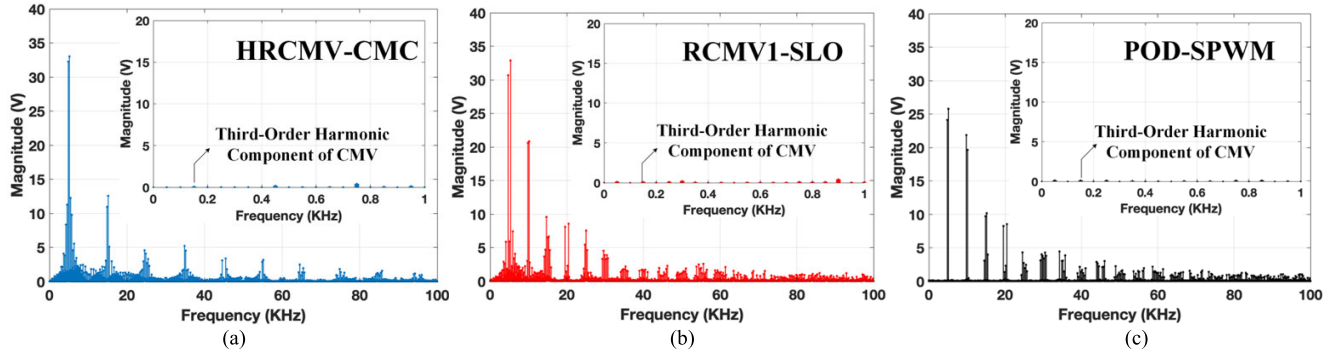


FIGURE 14. Simulated frequency spectra of CMV of (a) HRCMV-CMC (b) RCMV1-SLO and (c) POD-SPWM at m = 0.866, PF = 0.85.

As can be observed in Fig. 14 and 15, the frequency spectra of CMV of HRCMV-CMC, RCMV1-SLO, and POD-SPWM confirms that the third-order CMV components of fundamental frequency (f = 150Hz) and its multiples are virtually zero, thus zero average CMV being achieved [17], [32], [33].

Moreover, the CMV variations are reduced in HRCMV-CMC as opposed to RCMV1-SLO and POD-SPWM. Specifically, the per-carrier number of variations in CMV values is 4 times for HRCMV-CMC in comparison to 6 times for RCMV1-SLO and POD-SPWM, as can be seen in the microscopic view of Fig. 11, 12, and 13.

The reduction of CMV variations in HRCMV-CMC is further analyzed and compared with other modulation schemes via the simulated and experimental frequency spectra of CMV at f_m = 50Hz (m = 0.866), as shown in Fig. 14 and 15 respectively.

As can be observed in Fig. 14 and 15, in comparison to RCMV1-SLO, the effect of reduction of CMV variations in HRCMV-CMC manifests itself in the attenuation of dominant CMV components at around even multiples of 5KHz, i.e., 10KHz, 20KHz, 30KHz, etc.

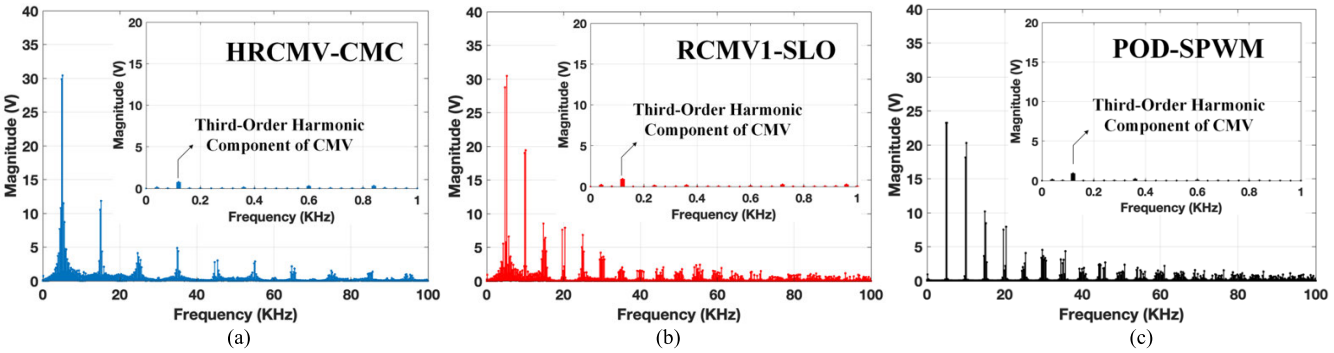


FIGURE 15. Experimental frequency spectra of CMV of (a) HRCMV-CMC (b) RCMV1-SLO and (c) POD-SPWM under full load (f_m = 50Hz (m = 0.866), PF = 0.85).

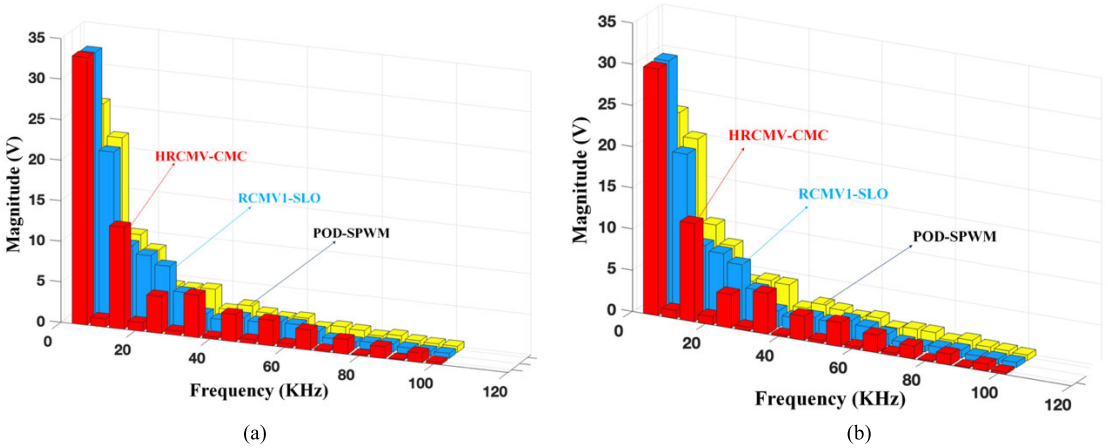


FIGURE 16. (a) Simulated magnitudes of dominant CMV components at around multiples of 5KHz for HRCMV-CMC, RCMV1-SLO, and POD-SPWM at m = 0.866, PF = 0.85 and (b) Experimental magnitudes of dominant CMV components at around multiples of 5KHz for HRCMV-CMC, RCMV1-SLO, and POD-SPWM under full load (f_m = 50Hz (m = 0.866), PF = 0.85).

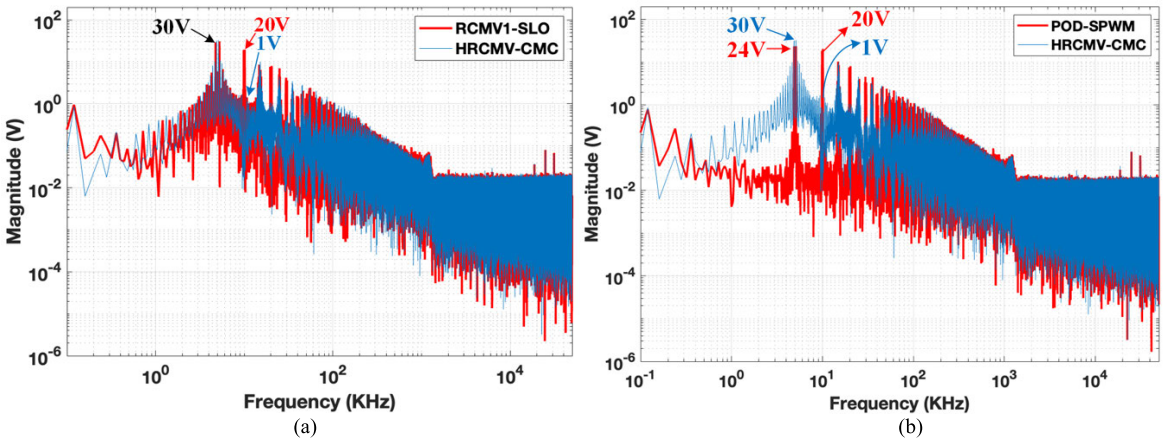


FIGURE 17. Experimental frequency spectra of the CMV waveforms with the frequency range extended to 50MHz for (a) HRCMV-CMC and RCMV1-SLO and (b) HRCMV-CMC and POD-SPWM under full load (f_m = 50Hz (m = 0.866), PF = 0.85).

Meanwhile, at around odd multiples of 5KHz, i.e., 5KHz, 15KHz, 25KHz, etc., the dominant CMV components are insignificantly different between HRCMV-CMC and RCMV1-SLO.

With regard to POD-SPWM, as can be observed in Fig. 14 and 15, HRCMV-CMC also gives noticeably lower dominant CMV components at around even multiples of 5KHz while it maintains relatively comparable

dominant CMV components at around odd multiples of 5KHz.

Hence, based on these results from the frequency spectra of CMV, high-frequency components of CMV at the even multiples of the carrier frequency in HRCMV-CMC are reduced in comparison to RCMV1-SLO and POD-SPWM. Therefore, HRCMV-CMC achieves reduced high-frequency CMV.

To further illustrate the attenuation of high-frequency CMV in HRCMV-CMC in comparison to RCMV1-SLO and POD-SPWM, the simulated and experimental magnitudes of dominant CMV components at around odd and even multiples of 5KHz are recorded and shown in Fig. 16(a) and 16(b) respectively for three modulation schemes.

For complete demonstration, the frequency range of the frequency spectra of CMV under three PWM schemes are extended to 50MHz, as shown in Fig. 17.

As can be seen in Fig. 17 over the frequency range of 0KHz – 100KHz, the proposed scheme (HRCMV-CMC) achieves a noticeable decrease in the CMV components at the even multiples of the carrier frequency ($f_{cr} = 5$KHz) while giving comparable CMV components at odd multiples of the carrier frequency.

Moreover, beyond 100KHz (100KHz – 50MHz), all three PWM schemes yield comparable CMV components.

B. LEAKAGE CURRENT

To provide a path for the flow of leakage current, the motor mental frame of the three-phase induction motor is connected to the neutral point of the DC-link voltage (O), as shown in Fig. 1. And the leakage current is measured via the highly accurate Tektronix Hall-based clamping current probe TCP0030A with the bandwidth of 120MHz [43] by clamping on the wire connecting between the Neutral Point (O) and the motor frame, as illustrated in Fig. 1 and 9. The Tektronix oscilloscope DPO5054 [44] with the bandwidth of 500MHz and up-to-5GS/s real-time sample rate is then used to capture the figures and data of the leakage current waveforms.

The macroscopic and microscopic waveforms of leakage current of three modulation schemes are shown in Fig. 11 and 13 respectively.

As can be observed in Fig. 11 and 13, the reduction of CMV variations in HRCMV-CMC does not lead to a reduction of peak-to-peak value of leakage current in comparison to RCMV1-SLO and POD-SPWM. In particular, they are 751.8mA, as indicated in Fig. 13.

As for the RMS values as shown in Table. 5, HRCMV-CMC yields an RMS value of leakage current of 48.72mA as opposed to 63.47mA and 63.31mA for RCMV1-SLO and POD-SPWM respectively under full load ($f_m = 50$Hz (m = 0.866), PF = 0.85).

For other PF values at $f_m = 50$Hz, the peak-to-peak and RMS values of three modulation schemes are tabulated in Table. 5. With regard to RCMV1-SLO and POD-SPWM, they both yield similar peak-to-peak and RMS values of leakage current, as can be seen in Table. 5 owing to having the same CMV magnitude ($\pm V_{DC}/6$) and CMV variations.

In addition, the frequency spectra of leakage current of HRCMV-CMC, RCMV1-SLO, and POD-SPWM under full load ($f_m = 50$Hz (m = 0.866), PF = 0.85) are shown in Fig. 18(a), (b), and (c) respectively.

Based on Fig. 18, what really stands out is the noticeable attenuation of dominant leakage current components at around even multiples of 5KHz, i.e., 10KHz, 20KHz, 30Khz, etc., in HRCMV-CMC in comparison to both RCMV1-SLO and POD-SPWM. This attenuation corresponds to the reduction of dominant CMV components also at around even multiples of 5KHz.

As for odd multiples of 5KHz, dominant leakage current components are relatively comparable for three modulation schemes.

To further demonstrate the reduction of dominant leakage current components at around even multiples of 5KHz in HRCMV-CMC over RCMV1-SLO and POD-SPWM, magnitudes of dominant leakage current components under full load ($f_m = 50$Hz (m = 0.866), PF = 0.85) are recorded and shown in Fig. 19.

For complete demonstration, the frequency range of the frequency spectra of leakage current under three PWM schemes are extended to 50MHz, as shown in Fig. 20.

As can be seen in Fig. 20 over the frequency range of 0KHz – 100KHz, the proposed scheme (HRCMV-CMC) achieves a noticeable decrease in the leakage current components at the even multiples of the carrier frequency ($f_{cr} = 5$KHz) while giving comparable leakage current components at odd multiples of the carrier frequency.

Moreover, beyond 100KHz (100KHz – 50MHz), all three PWM schemes yield comparable leakage current components.

C. HARMONIC DISTORTION ANALYSIS

The simulated harmonic distortion analyses of output current with respect to modulation index at three different power factors of 0.2, 0.6, and 0.85 are illustrated in Fig. 21(a), (b), and (c), respectively.

Likewise, the experimental harmonic distortion analyses of output current with respect to fundamental frequency at no load and power factor values of 0.6 and 0.85 are also demonstrated in Fig. 22(a), (b), and (c) respectively.

Based on the observation of these figures, the trend of output harmonic distortion given by HRCMV-CMC is that it produces better output harmonic distortion than that of RCMV1-SLO and POD-SPWM over a wide range of modulation index, i.e., $0.1 \leq m \leq 0.75$ in the simulation at low power factor and $10\text{Hz} \leq f_m \leq 44\text{Hz}$ in the experiment at no load.

Moreover, at power factors of 0.6 and 0.85, HRCMV-CMC yields similar-to-better output harmonic distortion than that of RCMV1-SLO and POD-SPWM at high range of modulation index, i.e., $0.55 \leq m \leq 0.866$ in the simulation and $34\text{Hz} \leq f_m \leq 50\text{Hz}$ in the experiment.

TABLE 5. Comparative analysis of peak-to-peak and RMS values of leakage current for various modulation schemes at f_m = 50Hz (m = 0.866).

PF	HRCMV-CMC				RCMV1-SLO		POD-SPWM	
	Peak-to-Peak (mA)	RMS (mA)	%Reduction of RMS Value compared with RCMV1-SLO	%Reduction of RMS Value compared with POD-SPWM	Peak-to-Peak (mA)	RMS (mA)	Peak-to-Peak (mA)	RMS (mA)
0.2 (no load)	751.8	52.12	21.87% (14.59mA)	22.06% (14.75mA)	751.8	66.71	751.8	66.87
0.4		53.89	19.24% (12.84mA)	19.4% (12.97mA)		66.73		66.86
0.6		54.79	16.47% (10.8mA)	16.68% (10.97mA)		65.59		65.76
0.85 (full load)		48.72	23.24% (14.75mA)	23.05% (14.59mA)		63.47		63.31

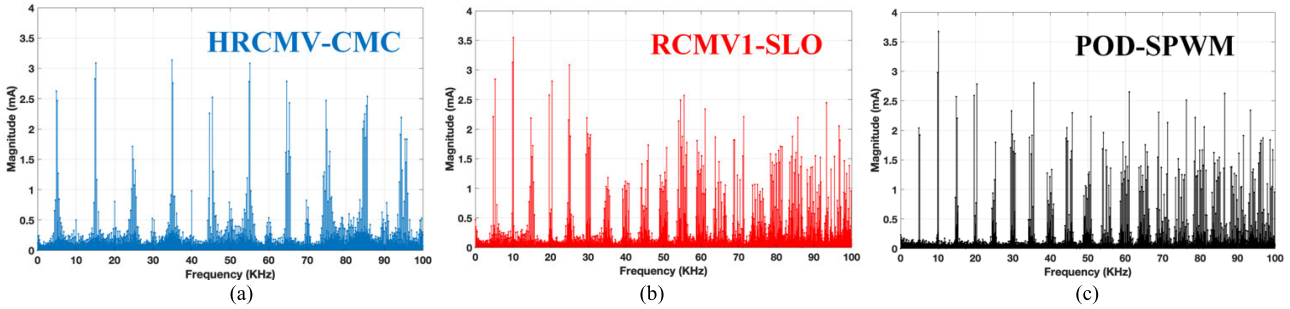


FIGURE 18. Experimental frequency spectra of leakage current of (a) HRCMV-CMC (b) RCMV1-SLO and (c) POD-SPWM under full load (f_m = 50Hz (m = 0.866), PF = 0.85.

TABLE 6. Overall performance evaluation at f_m = 50Hz (m = 0.866).

		When compared to RCMV1-SLO			When compared to POD-SPWM		
	PF	% Reduction RMS Leakage Current	Experimental THD of current	Efficiency	% Reduction RMS Leakage Current	Experimental THD of current	Efficiency
HRCMV-CMC	**0.2 (no load)**	21.87% (14.59mA) reduction	1.3% increase	0.16% reduction	22.06% (14.75mA) reduction	1.15% increase	0.18% reduction
	0.6	16.47% (10.8mA) reduction	Similar	0.049% reduction	16.68% (10.97mA) reduction	Similar	0.054% reduction
	0.85 (full load)	23.24% (14.75mA) reduction	Similar	0.03% reduction	23.05% (14.59mA) reduction	Similar	0.03% reduction

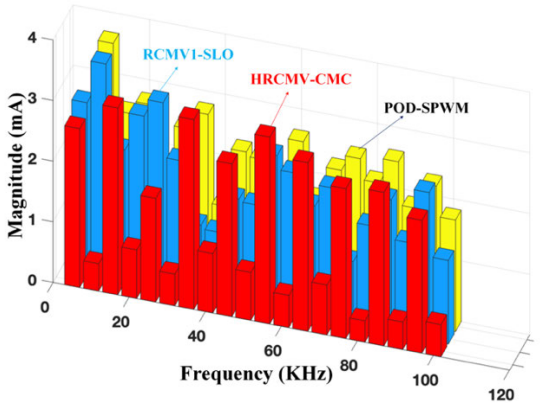


FIGURE 19. Dominant magnitudes of experimental leakage current components at around multiples of 5KHz under full load (f_m = 50Hz (m = 0.866), PF = 0.85).

D. SWITCHING LOSS AND EFFICIENCY ANALYSES

The switching loss analysis is conducted in PLECS Thermal Module for HRCMV-CMC, RCMV1-SLO, and POD-SPWM with respect to modulation index and power factor.

The switching power devices are IGB15N60T [39] and HFA15TB60 [40], which are used as Insulated Gate Bipolar Transistors (IGBTs) and clamping diodes respectively in the 3L-NPC.

The thermal characteristics of which can be downloaded from the manufacturer's website and imported into PLECS. Some prominent parameters of these two devices are listed in detail in [39] and [40].

As can be observed in Fig. 23, under different operating conditions, HRCMV-CMC produces higher switching loss than those of RCMV1-SLO and POD-SPWM. It is expected due to the fact that there are 8 switching commutations per carrier period in HRCMV-CMC as opposed to 6 in RCMV1-SLO and POD-SPWM.

The efficiency of converter with respect to output power is also estimated in PLECS Thermal Module [41] to further investigate the impact of switching loss on the converter efficiency.

The output power is varied by changing the Power Factor of the RL load. At m = 0.866 (f_m = 50Hz), the output power of 2.2KW corresponds to the power factor of 0.85. And this

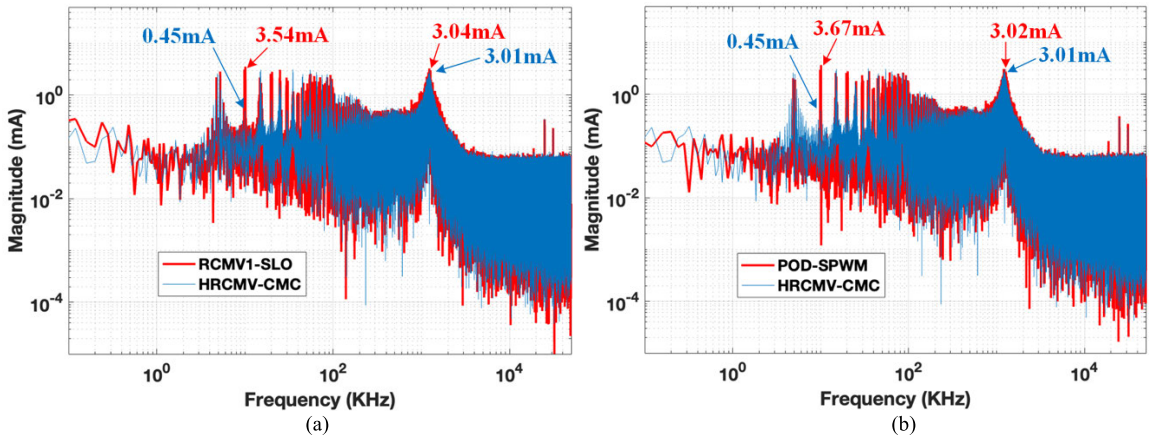


FIGURE 20. Experimental frequency spectra of the leakage current with the frequency range extended to 50MHz for (a) HRCMV-CMC and RCMV1-SLO and (b) HRCMV-CMC and POD-SPWM under full load (f_m = 50Hz (m = 0.866), PF = 0.85).

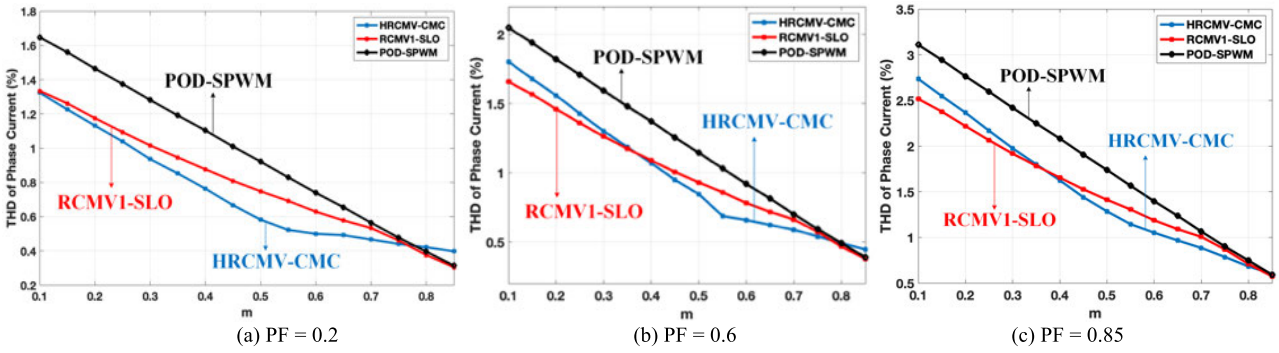


FIGURE 21. Simulated THD of phase current with respect to modulation index at (a) PF = 0.2 (b) PF = 0.6 and (c) PF = 0.85.

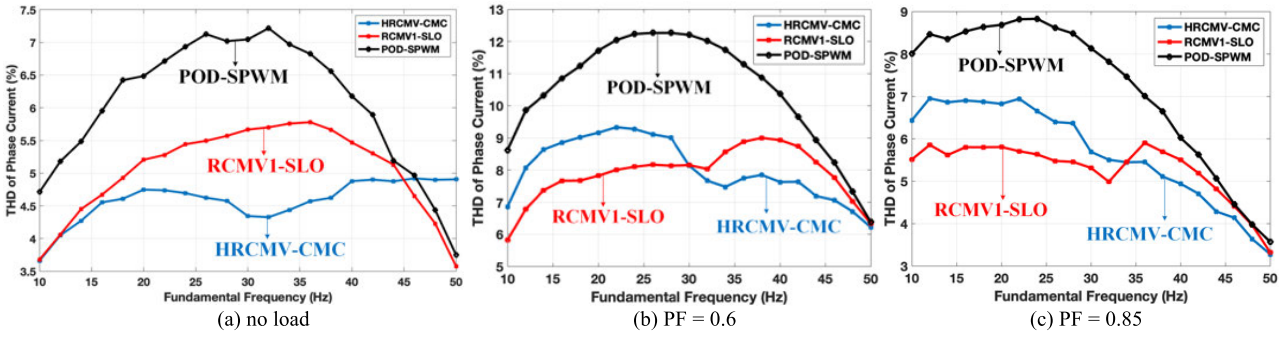


FIGURE 22. Experimental THDs of phase current with respect to fundamental frequency (a) under no-load (b) under load (PF = 0.6) and (c) under load (PF = 0.85) V/f induction motor for HRCMV-CMC, RCMV1-SLO, and POD-SPWM.

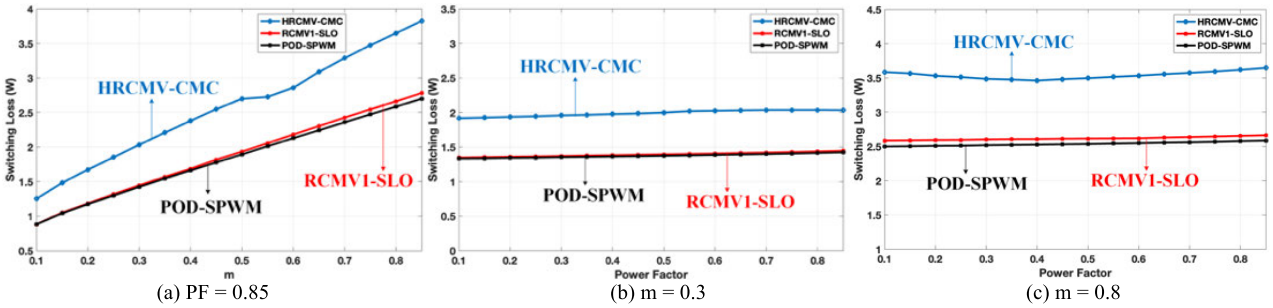
also correlates with the rated power of the induction motor under full load.

As can be seen in Fig. 24, higher switching loss incurred in HRCMV-CMC as opposed to RCMV1-SLO and POD-SPWM under PF = 0.85 only reduces the efficiency of the converter to a small extent.

Specifically, at the output power of 2200W (PF = 0.85), the estimated converter efficiency in HRCMV-CMC is 97.79% while they are 97.82% and 97.83% for RCMV1-SLO and POD-SPWM respectively. Meanwhile, at the output power of 535W (PF = 0.2), HRCMV-CMC gives an estimated efficiency of 90.25% in comparison to 90.41% and 90.43% for RCMV1-SLO and POD-SPWM respectively.

E. OVERALL PERFORMANCE EVALUATION

Table. 6 demonstrates the performance of HRCMV-CMC in comparison to RCMV1-SLO and POD-SPWM in terms of RMS leakage current, output harmonic distortion, and



(a) PF = 0.85 (b) m = 0.3 (c) m = 0.8

FIGURE 23. Comparative analyses of switching loss for HRCMV-CMC, RCMV1-SLO, and POD-SPWM at (a) PF = 0.85 with respect to modulation index (b) m = 0.3 with respect to power factor (c) m = 0.8 with respect to power factor.

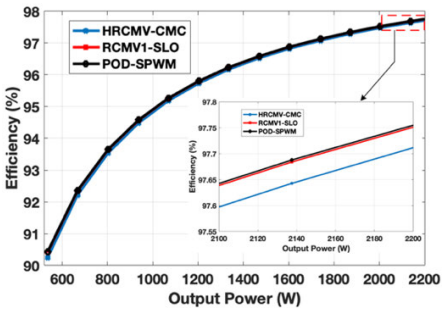


FIGURE 24. Estimated efficiency of the converter in PLECS Thermal Module at m = 0.866 (f_m = 50Hz).

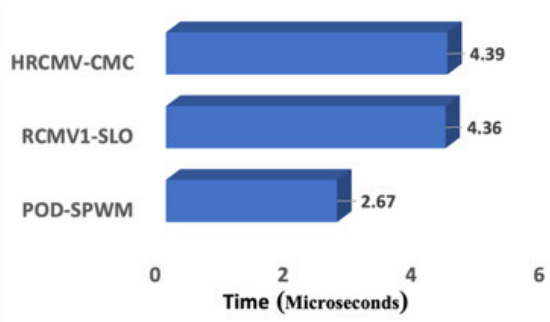


FIGURE 25. Code execution times of HRCMV-CMC, RCMV1-SLO, and POD-SPWM obtained from the Code Composer Studio.

efficiency at $f_m = 50$Hz (m = 0.866) for three different power factors of 0.2, 0.6 and 0.85.

Based on the results indicated in Table. 6, HRCMV-CMC consistently produces lower RMS leakage current than that of RCMV1-SLO and POD-SPWM for power factors of 0.2, 0.6, and 0.85 at $f_m = 50$Hz.

Specifically, at power factor of 0.85, f_m 50Hz under full load, HRCMV-CMC gives rise to more than 23% reduction of RMS leakage current as opposed to RCMV1-SLO and POD-SPWM.

Hence, taking both harmonic distortion and efficiency into account at $f_m = 50$Hz and power factor ranging from medium to high values, HRCMV-CMC gives the lowest RMS leakage current while producing comparable output harmonic distortion and slightly reducing the efficiency of the converter.

F. COMPUTATIONAL BURDEN

The code execution times of the proposed scheme (HRCMV-CMC), the previously proposed scheme (RCMV-SLO), and POD-SPWM are recorded in the Code Composer Studio from Texas Instrument. They are plotted in Fig. 25 in the form of bar chart.

As can be seen in Fig. 25, the traditional Phase Opposition Disposition Sinusoidal Pulse-width modulation (POD-SPWM) achieves the lowest code execution time, i.e., 2.67μs since it involves simple comparison between the three modulating signals with a carrier signal for generating the gating signals for power switching devices.

Meanwhile, both the proposed scheme (HRCMV-CMC) and the previously proposed scheme (RCMV1-SLO) yield comparable code execution times. In particular, they are 4.39μs and 4.36μs for HRCMV-CMC and RCMV1-SLO respectively.

IV. CONCLUSION

This article proposes a hybrid pulse-width modulation strategy, namely HRCMV-CMC, featuring reduced high-frequency CMV while producing lowered CMV magnitudes, zero average CMV, and improved harmonic distortion in comparison to RCMV1-SLO and POD-SPWM. The reduction of high-frequency CMV is achieved by reducing the CMV variations. This is realized by rearranging the order of switching states in a carrier period. The newly resulting switching sequences, namely M-RCMV1, possess simultaneous switching commutations of two phase-legs. Hence, deadtime is taken into account with the utilization of another type of switching sequences, i.e., M-RCMV2. The choice of two types of switching sequences is based on the information of phase currents to avoid the CMV spikes with M-RCMV1 having higher priority over M-RCMV2 due to having better harmonic distortion performance. With the reduction of both magnitude and high-frequency of CMV, as well as the CMV spikes, HRCMV-CMC leads to a significant reduction of RMS leakage current for different loading conditions at the rated frequency of 50Hz under V/f induction motor control in comparison RCMV1-SLO and POD-SPWM. In addition, HRCMV-CMC also leads to similar-to-better output harmonic distortion over a wide modulation range as opposed to

RCMV1-SLO and POD-SPWM. All the advantages offered by HRCMV-CMC come with the cost of slight reduction in the efficiency of the converter in comparison to RCMV1-SLO and POD-SPWM.

REFERENCES

[1] B. Wu and M. Narimani, "Two-level voltage source inverter," in *High-Power Converters and AC Drives*. USA: Wiley, 2017, pp. 93–117, doi: 10.1002/9781119156079.ch6.

[2] B. Wu and M. Narimani, "Diode-clamped multilevel inverters," in *High-Power Converters and AC Drives*. USA: Wiley, 2017, pp. 143–183, doi: 10.1002/9781119156079.ch8.

[3] B. Wu and M. Narimani, "Voltage source inverter fed drives," in *High-Power Converters and AC Drives*. USA: Wiley, 2017, pp. 287–308, doi: 10.1002/9781119156079.ch12.

[4] K. S. Kumar, K. Corzine, G. Mondal, K. Gopakumar, and S. De, "Neutral-point balancing of neutral-point-clamped three-level inverter with a front end switched rectifier DC source for the full modulation range," *IET Power Electron.*, vol. 2, no. 5, pp. 527–534, Sep. 2009.

[5] K. K. Tan, F. Gao, P. C. Loh, and F. Blaabjerg, "Enhanced buck–boost neutral-point-clamped inverters with simple capacitive-voltage balancing," *IEEE Trans. Ind. Appl.*, vol. 46, no. 3, pp. 1021–1033, May 2010.

[6] J.-S. Lee and K.-B. Lee, "New modulation techniques for a leakage current reduction and a neutral-point voltage balance in transformerless photovoltaic systems using a three-level inverter," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1720–1732, Apr. 2014, doi: 10.1109/TPEL.2013.2264954.

[7] U.-M. Choi, H.-H. Lee, and K.-B. Lee, "Simple neutral-point voltage control for three-level inverters using a discontinuous pulse width modulation," *IEEE Trans. Energy Convers.*, vol. 28, no. 2, pp. 434–443, Jun. 2013, doi: 10.1109/TEC.2013.2257786.

[8] F. Guo, T. Yang, A. M. Diab, S. S. Yeoh, S. Bozhko, and P. Wheeler, "An enhanced virtual space vector modulation scheme of three-level NPC converters for more-electric-aircraft applications," *IEEE Trans. Ind. Appl.*, vol. 57, no. 5, pp. 5239–5251, Sep. 2021, doi: 10.1109/TIA.2021.3085798.

[9] F. Guo, T. Yang, S. Bozhko, and P. Wheeler, "A novel virtual space vector modulation scheme for three-level NPC power converter with neutral-point voltage balancing and common-mode voltage reduction for electric starter/generator system in more-electric-aircraft," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Sep. 2019, pp. 1852–1858, doi: 10.1109/ECCE.2019.8913186.

[10] H.-H. Lee, U.-M. Choi, and K.-B. Lee, "Neutral-point voltage control for grid-connected three-level inverters using a discontinuous pulse width modulation," in *Proc. IEEE Vehicle Power Propuls. Conf.*, Oct. 2012, pp. 638–642, doi: 10.1109/VPPC.2012.6422641.

[11] J. M. Erdman, R. J. Kerkman, D. W. Schlegel, and G. L. Skibinski, "Effect of PWM inverters on AC motor bearing currents and shaft voltages," *IEEE Trans. Ind. Appl.*, vol. 32, no. 2, pp. 250–259, Apr. 1996, doi: 10.1109/28.491472.

[12] H. Abu-Rub, M. Malinowski, and K. Al-Haddad, "Common-mode voltage and bearing currents in PWM inverters: Causes, effects and prevention," in *Power Electronics for Renewable Energy Systems, Transportation and Industrial Applications*. USA: Wiley, 2014, pp. 664–694, doi: 10.1002/9781118755525.ch21.

[13] D. Busse, J. Erdman, R. J. Kerkman, D. Schlegel, and G. Skibinski, "Bearing currents and their relationship to PWM drives," *IEEE Trans. Power Electron.*, vol. 12, no. 2, pp. 243–252, Mar. 1997, doi: 10.1109/63.558735.

[14] Z. Zhang, Y. Hu, X. Chen, G. W. Jewell, and H. Li, "A review on conductive common-mode EMI suppression methods in inverter fed motor drives," *IEEE Access*, vol. 9, pp. 18345–18360, 2021, doi: 10.1109/ACCESS.2021.3054514.

[15] B. Wu and M. Narimani, "Transformerless MV drives," in *High-Power Converters and AC Drives*. USA: Wiley, 2017, pp. 417–445, doi: 10.1002/9781119156079.ch17.

[16] A. Janabi and B. Wang, "Hybrid SVPWM scheme to minimize the common-mode voltage frequency and amplitude in voltage source inverter drives," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1595–1610, Feb. 2019, doi: 10.1109/TPEL.2018.2834409.

[17] K. Tian, J. Wang, B. Wu, Z. Cheng, and N. R. Zargari, "A virtual space vector modulation technique for the reduction of common-mode voltages in both magnitude and third-order component," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 839–848, Jan. 2016, doi: 10.1109/TPEL.2015.2408812.

[18] J. Huang, Q. Liu, X. Wang, and K. Li, "A carrier-based modulation scheme to reduce the third harmonic component of common-mode voltage in a three-phase inverter under high DC voltage utilization," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 1931–1940, Mar. 2018, doi: 10.1109/TIE.2017.2745439.

[19] S. Reddy and B. Basavaraja, "Simulation and analysis of common mode voltage, bearing voltage and bearing current in two-level and three-level PWM inverter fed induction motor drive with long cable," in *Proc. Int. Conf. Power Adv. Control Eng. (ICPACE)*, Bengaluru, India, Aug. 2015, pp. 221–226, doi: 10.1109/icpace.2015.7274947.

[20] P. Xie, J. Lu, G. Chen, and H. Chen, "Influence of motor cable on common-mode currents in an inverter-fed motor drive system," *Frontiers Inf. Technol. Electron. Eng.*, vol. 19, pp. 273–284, Apr. 2018, doi: 10.1631/FITEE.1601518.

[21] T. T. Nguyen, N.-V. Nguyen, and N. R. Prasad, "Eliminated common-mode voltage pulsewidth modulation to reduce output current ripple for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5952–5966, Aug. 2016, doi: 10.1109/TPEL.2015.2489560.

[22] T. T. Nguyen, N.-V. Nguyen, and N. R. Prasad, "Novel eliminated common-mode voltage PWM sequences and an online algorithm to reduce current ripple for a three-level inverter," *IEEE Trans. Power Electron.*, vol. 32, no. 10, pp. 7482–7493, Oct. 2017, doi: 10.1109/TPEL.2016.2634009.

[23] T. T. Nguyen and N.-V. Nguyen, "An efficient four-state zero common-mode voltage PWM scheme with reduced current distortion for a three-level inverter," *IEEE Trans. Ind. Electron.*, vol. 65, no. 2, pp. 1021–1030, Feb. 2018, doi: 10.1109/TIE.2017.2733418.

[24] P. Khoa-Dang and N. Nho-Van, "Pulse-width modulation strategy for common mode voltage elimination with reduced common mode voltage spikes in multilevel inverters with extension to over-modulation mode," *J. Power Electron.*, vol. 19, no. 3, pp. 727–743, May 2019, doi: 10.6113/JPE.2019.19.3.727.

[25] X. Zhang, D. Boroyevich, R. Burgos, P. Mattavelli, and F. Wang, "Impact and compensation of dead time on common mode voltage elimination modulation for neutral-point-clamped three-phase inverters," in *Proc. IEEE ECCE Asia Downunder*, Melbourne, VIC, Australia, Jun. 2013, pp. 1016–1022, doi: 10.1109/ECCE-Asia.2013.6579232.

[26] C.-C. Hou, C.-C. Shih, P.-T. Cheng, and A. M. Hava, "Common-mode voltage reduction pulsewidth modulation techniques for three-phase grid-connected converters," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1971–1979, Apr. 2013, doi: 10.1109/TPEL.2012.2196712.

[27] M. C. Cavalcanti, K. C. de Oliveira, A. M. de Farias, F. A. S. Neves, G. M. S. Azevedo, and F. C. Camboim, "Modulation techniques to eliminate leakage currents in transformerless three-phase photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 57, no. 4, pp. 1360–1368, Apr. 2010, doi: 10.1109/TIE.2009.2029511.

[28] X. Guo, M. C. Cavalcanti, A. M. Farias, and J. M. Guerrero, "Single-carrier modulation for Neutral-Point-Clamped inverters in three-phase transformerless photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2635–2637, Jun. 2013, doi: 10.1109/TPEL.2012.2224138.

[29] X. Guo, B. Wei, T. Zhu, Z. Lu, L. Tan, X. Sun, and C. Zhang, "Leakage current suppression of three-phase flying capacitor PV inverter with new carrier modulation and logic function," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2127–2135, Mar. 2018, doi: 10.1109/TPEL.2017.2692753.

[30] T. Yu, W. Wan, and S. Duan, "A modulation method to eliminate leakage current and balance neutral-point voltage for three-level inverters in photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 70, no. 2, pp. 1635–1645, Feb. 2023, doi: 10.1109/TIE.2022.3161809.

[31] M. M. Renge and H. M. Suryawanshi, "Five-level diode clamped inverter to EliminateCommon mode voltage and reduce dv/dt inMedium voltage rating induction motor drives," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1598–1607, Jul. 2008, doi: 10.1109/TPEL.2008.925423.

[32] K. D. Pham and N. V. Nguyen, "A reduced common-mode-voltage pulsewidth modulation method with output harmonic distortion minimization for three-level neutral-point-clamped inverters," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 6944–6962, Jul. 2020, doi: 10.1109/TPEL.2019.2959984.

[33] K. D. Pham and N.-V. Nguyen, "Switching loss optimization for a pulsewidth modulation strategy with reduced CMV and improved output harmonic distortion for a three-level NPC converter," *IEEE Trans. Power Electron.*, vol. 37, no. 10, pp. 12118–12133, Oct. 2022, doi: 10.1109/TPEL.2022.3175898.

[34] N. Oswald, P. Anthony, N. McNeill, and B. H. Stark, "An experimental investigation of the tradeoff between switching losses and EMI generation with hard-switched all-Si, Si-siC, and all-siC device combinations," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2393–2407, May 2014, doi: 10.1109/TPEL.2013.2278919.
[35] Z. Zhang, F. Wang, L. M. Tolbert, B. J. Blalock, and D. J. Costinett, "Evaluation of switching performance of SiC devices in PWM inverter-fed induction motor drives," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5701–5711, Oct. 2015, doi: 10.1109/TPEL.2014.2375827.
[36] Y. Han, H. Lu, Y. Li, and J. Chai, "Analysis and suppression of shaft voltage in SiC-based inverter for electric vehicle applications," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6276–6285, Jul. 2019, doi: 10.1109/TPEL.2018.2873079.
[37] M. Schinkel, S. Weber, S. Guttowski, W. John, and H. Reichl, "Efficient HF modeling and model parameterization of induction machines for time and frequency domain simulations," in *Proc. 21st Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Dallas, TX, USA, Mar. 2006, p. 6, doi: 10.1109/apec.2006.1620689.
[38] O. Magdun and A. Binder, "High-frequency induction machine modeling for common mode current and bearing voltage calculation," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 1780–1790, May 2014, doi: 10.1109/TIA.2013.2284301.
[39] *Datasheet of IGBT15N60T*. Accessed: Jul. 13, 2023. [Online]. Available: https://www.infineon.com/cms/en/product/power/igbt/igbt-discretes/igb15n60t/
[40] *Datasheet of HFA15TB60*. Accessed: Jul. 13, 2023. [Online]. Available: https://www.infineon.com/cms/en/product/small-signal-transistors-diodes/diode/rectifier/switching-and-rectifier-diodes/hfa15tb60/
[41] *Introduction to Thermal Domain, PLECS Tutorial*. Accessed: Jul. 13, 2023. [Online]. Available: https://www.plexim.com/sites/default/files/tutorials_categorized/plecs/thermal_domain.pdf
[42] *Datasheet of Voltage Probe THDP0200*. Accessed: Jul. 13, 2023. [Online]. Available: https://www.tek.com/vn/datasheet/high-voltage-differential-probes
[43] *Datasheet of Current Probe TCP0030A*. Accessed: Jul. 13, 2023. [Online]. Available: https://www.tek.com/vn/datasheet/30-ac-dc-current-probe
[44] *Datasheet of Oscilloscope DPO5054*. Accessed: Jul. 13, 2023. [Online]. Available: https://www.tek.com/en/products/oscilloscopes/mso5000-dpo5000

KHOA DANG PHAM was born in Ho Chi Minh City, Vietnam, in 1990. He received the B.S. and M.S. degrees in electrical engineering from the Ho Chi Minh City University of Technology, Ho Chi Minh City, where he is currently pursuing the Ph.D. degree in electrical engineering. His current research interests include ac motor control, renewable energy, and PWM converters.

MON-VAN DOI received the M.S. degree in electrical engineering from the Ho Chi Minh University of Technology-VNUHCM, Ho Chi Minh City, Vietnam, in 2016, where he is currently pursuing the Ph.D. degree in electrical engineering. His current research interests include model predictive control and PWM control techniques for power converters, such as multilevel inverters, ac–ac matrix converter, and power converter applications in electric drives and power systems.

NHO-VAN NGUYEN (Member, IEEE) was born in Vietnam, in 1964. He received the M.S. and Ph.D. degrees in electrical engineering from the University of West Bohemia, Plzen, Czech Republic, in 1988 and 1991, respectively.

Since 1992, he has been with the Department of Electrical and Electronics Engineering, Ho Chi Minh City University of Technology, Vietnam, where he is currently an Associate Professor. He was with KAIST as a Postdoctoral Fellow for six months, in 2001, and a Visiting Professor for one year, from 2003 to 2004. His research interests include modeling and control of switching power active filters, and PWM techniques for power converters.