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RESEARCH ARTICLE

Integrated Multiport DC-DC and Multilevel Converters for Multiple Renewable Energy Source Integration

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ABSTRACT This research introduces an innovative converter system which has been developed to seamlessly incorporate multiple sources of renewable energy into both DC and AC grids. The integration of multiple energy sources is made possible through the utilization of a unique converter system that combines a multiport DC converter topology with a multilevel inverter topology, while maintaining a low component count and hence increased overall power density and efficiency for the proposed converter system. Unlike previous literature, where each energy source needs a separate DC converter and a two-level converter is used for DC to AC conversion, this converter system features buck-boost operation, superior power quality characteristics, and fewer components. The system suggests the implementation of a DC link voltage balancing technique that relies on an auxiliary circuit to achieve equilibrium in the voltage on the DC link, as a possible substitute to the more complicated control-based balancing scheme. The operational integrity of the converter system is assessed through rigorous numerical simulations and experimentally validated using OPAL-RT's OP5700 hardware-in-the-loop (HIL) implementation platform as well as an in-house experimental test setup.

INDEX TERMS DC-DC converter, dc link capacitor balancing, multiport converter, multilevel inverter.

I. INTRODUCTION

Lately, there has been a rising awareness regarding the finite nature of fossil energy sources and the harmful environmental effects linked with their utilization in response to the escalating global energy requirements and market conditions. Consequently, a strong focus has been exploring sustainable energy options [1], [2], [3]. Fuel cells, wind turbines, and photovoltaic (PV) systems have demonstrated their potential as viable options for delivering environmentally-friendly solutions [4], [5]. The rising acceptance and integration of renewable energy sources (RESs) are catalysing an important transformation in the landscape of electrical energy generation and utilization. This transition entails a fundamental shift from traditional centralized generation systems to more decentralized and distributed models [6], [7], [8], [9]. Future power systems are expected to rely heavily on distributed generation systems, which are primarily based on DC microgrids. DC microgrids have several advantages over AC microgrids, like the lack of issues with reactive power and synchronization. As a result, they are considered the backbone of future power systems [10], [11]. Nonetheless, AC power systems are widely prevalent in many traditional power systems, particularly in developing countries [12],

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[13]. Therefore, it remains crucial to convert power generated from renewable energy sources (RESs) from DC to AC [14].

Multilevel inverters (MLIs) have been gaining popularity as an efficient and effective solution for achieving high power DC to AC power conversion [15], [16], [17]. These inverters offer compelling advantages, for example, reduced total harmonic distortion (THD), minimal switching losses, negligible common-mode voltage (CMV), decreased compact filter components, electromagnetic interference, and enhanced thermal management capabilities, among various other benefits [18]. Compared to traditional two-level inverters, MLIs offer significant advantages, motivating researchers to develop new MLI topologies. Although numerous studies have proposed novel MLI topologies [19], [20], [21], conditioning the inputs of MLIs has remained challenging. This is due to the complex controllers required to maintain the desired output waveform, and the high voltage and current handling capabilities needed. Many current topologies operate under the assumption of constant DC inputs, which, while theoretically ideal, proves impractical in real-world scenarios due to the varying output voltages exhibited by most renewable energy sources (RESs) during their operation [22]. However, these challenges can be addressed using DC-DC converters [23], [24]. DC-DC converters can be used to condition the input voltage source for MLIs by stepping up or down the voltage to the required level [25]. This can be particularly useful when the input voltage source is not at the desired level, such as in RES applications where the input voltage from solar panels or wind turbines can vary [26].

Various attempts have been made to address the challenge of integrating RESs into the power grid, including proposing MLIs that can precondition the outputs of RESs before the conversion to AC takes place [27], [28], [29], [30], [31]. Nevertheless, the MLI configurations suggested in these studies have certain drawbacks. For example, these configurations may be limited to a single RES and can solely boost input voltage. To address these constraints, an alternative MLI design, as proposed in [31], integrates two RESs by employing two DC-DC converters connected in cascade configuration prior to the MLI stage. This integration allows for buck-boost functionality and facilitates the utilization of multiple inputs. However, this arrangement is not without its drawbacks, including a higher number of components, increased power losses, increased system costs, reduced power density, and efficiency.

Furthermore, other attempts were made to propose DC to AC converters comprising of integrated MLIs and DC-DC converters for RES integration in [32], [33], [34], [35], and [36]. However, these approaches also suffer from several limitations, such as the limitation on the number of RES inputs, number of phases and levels and the need for transformers for isolation, which result in bulky designs. More specifically, a family of multi-port modular multilevel converters is introduced in [35], interfacing one AC port with two DC ports with the help of low-frequency transformers. The reported topologies generate high voltage levels using either full-bridge or half-bridge cells. Modularity and wide applicability are their main features, besides the limitless reachable voltage level counts. However, they face challenges due to the large number of required capacitors and switches, influencing the reliability and complexity of the conversion system, in addition to the well-known related drawbacks of using transformers, including size and cost. On the other hand, the authors in [36] proposed a transformerless three-port bidirectional converter structured by connecting a DC-DC buck-boost stage with a T-type three-level inverter. The suggested converter eliminates the drawbacks associated with using transformers. However, it loses the modularity feature, restricting its suitability to low- and medium-voltage applications.

Moreover, integrating multiple RESs introduces the challenge of balancing the voltage across the DC link capacitors in MLIs. In certain cases, MLIs require multiple DC link capacitors connected in series to evenly distribute the DC link voltage among them. This is necessary to ensure proper operation and prevent voltage imbalances [22]. Hence, achieving voltage balance across these capacitors is crucial to preserve the integrity of output waveforms and ensure optimal power quality. However, attaining this balance entails the implementation of a sophisticated control system that can effectively regulate the voltage distribution among the capacitors [37]. This creates a unique opportunity to fill the gap by applying multiport converters in the integration of RESs to AC grid through MLIs, to achieve attractive features of low component count, high efficiency, low THD and higher power density.

The research presented in this paper introduces an innovative approach to tackle the mentioned challenges in RES integration. It involves the utilization of a multiport DC converter (MDC) as a means to integrate the RESs, resulting in reduced component count during the preprocessing stage. Consequently, this approach offers several benefits, including decreased costs, lower power losses, improved efficiency, and increased power density. Additionally, the research proposes the implementation of an auxiliary circuit to achieve a simplified DC link capacitor voltage balancing method, as opposed to the previously suggested control-based technique. The proposed configuration offers versatile capabilities, including buck-boost operation, as well as the ability to facilitate individual and simultaneous power transfer from multiple RESs. This flexibility allows for efficient energy management and optimized utilization of the available renewable energy sources. More specifically, the proposed converter system has the following novel features:

1) The number of input sources (RESs) can be arbitrarily increased.
2) It can transmit power from the inputs (RESs) to the DC and AC buses independently and simultaneously.
3) It can perform unidirectional buck and boost operations with a high voltage gain.
4) When an extra input is introduced, only one additional reverse blocking switch is needed to increase the number of inputs.

5) The DC converter section simply needs a single input single output (SISO) controller, such as the common double loop PI controller, and has a straightforward control strategy as detailed and proposed in [38].

Within this framework, the new converter system was analyzed for three input sources with equal and different input voltage levels, put through extensive simulations, and experimentally verified. Rigorous numerical verification and validation is performed, using a state-of-the-art hardware-in-the-loop (HIL) device to assess the performance and operation of the converter system. This advanced testing methodology ensures that the converter system operates reliably and accurately under various operating conditions, providing confidence in its functionality and effectiveness. The initial idea of the integrated converter system proposed in this work has been presented in [39]. In this paper, the detailed analysis and features are numerically verified, and results from experimental validation using the HIL test rig are presented. HIL verification has been proved to accurately and sufficiently prove the operation of power converters [40], [41], [42] and, as such is implemented in the verification of the proposed converter system. Other key features of the proposed integrated converters have been vigorously addressed in [22] and [42], the individual converters from which the integrated converter is derived. These features include efficiency, dynamic response to disturbances, component selection, and voltage and current stress. Since they have been sufficiently addressed, they are not included in this paper.

II. PROPOSED INTEGRATED CONVERTERS

Figure 1 illustrates the combined multiport DC and multilevel converter system, which incorporates a new multiport DC-DC converter (synthesized from the converter in [42]) highlighted in blue color. The system also features a DC bus output colored in purple and incorporates the multilevel inverter portion colored in green, previously introduced in [22], responsible for generating the AC output. The proposed configuration provides a high degree of flexibility, allowing for the seamless integration of diverse RESs with varying voltage levels into both the DC and AC links. The system enables independent or simultaneous connection of these energy sources, facilitating efficient power flow and utilization in a versatile manner.

A. MULTIPORT DC CONVERTER TOPOLOGY

The region highlighted in blue in Figure 1 showcases the proposed novel topology of a unidirectional multiport DC to DC converter (MDC). Within the DC converter section, there is a single inductor, two diodes, and $N + 1$ reverse-blocking transistors, where N represents the number of input ports in the multiport converter. In cases where the availability of reverse-blocking FETs is limited, a diode can be connected in series with a standard FET as an alternative solution. The distinctive advantages of the proposed MDC lie in its

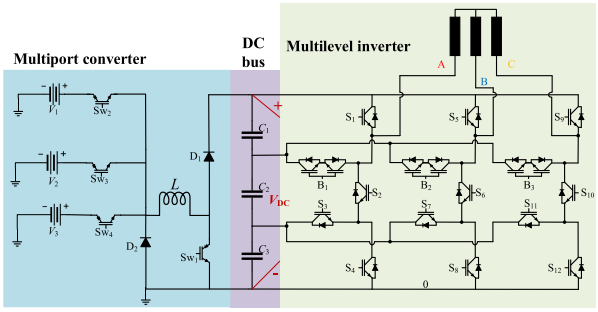

FIGURE 1. Schematic of the integrated multiport converters system.

departure from conventional MDC designs. Unlike traditional MDCs that necessitate N inductors for N input sources, the proposed MDC employs just one inductor to accommodate any number of input sources. This feature holds the potential for achieving higher power density in the proposed MDC. Additionally, the incorporation of an additional input port only requires the inclusion of a single extra reverse-blocking FET.

The MDC offers a diverse range of unidirectional modes, including four modes that allow simultaneous power flow from two or more sources (e.g., V_1 & V_2, V_2 & V_3, V_1 & V_3, V_1 & V_2 & V_3). Additionally, three modes enable independent power flow from each of the three sources (V_1 – V_3) to the DC link. Upon closer examination, the independent power flow from the sources exhibits similarities to the standard non-inverting buck-boost converter. In this mode, the switching period T_S is divided into two distinct periods: T_1 for inductor charging and T_2 for inductor discharging. The converter can operate in either the buck or boost mode in the independent power flow mode, depending on the duty ratio 'D' applied across the switches. Here, 'D' represents the ratio of the inductor charging time (T_1) to the total switching period ($D = T_1/T_S$). Consequently, the conventional equations [38], [42] that describe the relationship between input and output voltage in a basic buck-boost converter also apply to this converter for independent power flow from the respective inputs to the output, V_{DC}.

In the mode of simultaneous power transfer, as previously discussed, the operation of the MDC necessitates the concurrent supply of energy from two or more sources. In this paper, the MDC is examined in the context of three input sources, and the conduction modes during switching states and steady-state waveforms are illustrated in Figures 2 and 3, respectively. Within this mode, the inductor charging period denoted as T_1, is further subdivided into two or more subperiods, contingent upon the number of simultaneous input sources. Throughout the duration of T_1, switches S_{W1}, S_{W2}, S_{W3} and S_{W4} are turned ON. On the other hand, during the initial subdivision of T_1, the inductor voltage corresponds to the highest source voltage, denoted as V_1. Consequently, the inductor charges at a rate of V_1/L. Once the first subdivision period of T_1 concludes, S_{W2} is deactivated while S_{W3}, S_{W4} and S_{W1} remain activated. In the subsequent subdivision of

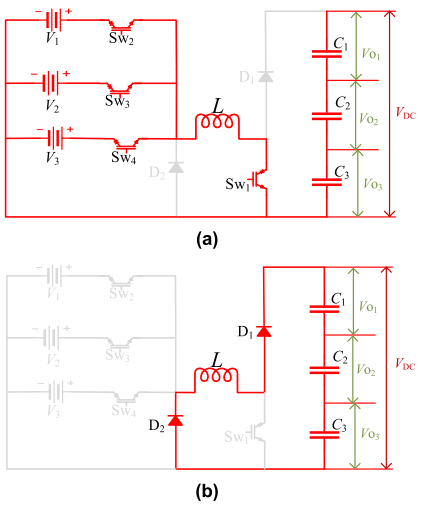

FIGURE 2. Path of current flow of the MDC in steady state CCM under simultaneous power transfer for inductor (a) charging and (b) discharging.

T_1, the inductor voltage transitions to V_2, and the inductor continues to charge at a slope of V_2/L. During the third subdivision of T_1, only switches S_{W1} and S_{W4} will remain in the ON state, resulting in the inductor voltage equaling V_3. Consequently, the inductor continues to charge at a rate of V_3/L. This sequential charging process follows a similar pattern for an MDC with more than three inputs, where the subdivisions occur in decreasing order of the input voltage magnitudes. Upon completion of the inductor charging period, all active switches ($S_{W1} - S_{W4}$) of the MDC transition to an OFF state, initiating the subsequent discharging period, denoted as T_2. Throughout T_2, the inductor (L) discharges through the capacitors ($C_1 - C_3$) to the DC bus via D_1 and D_2. As a result, the voltage across the inductor becomes $-V_o$, and the discharge occurs with a gradient of $-V_o/L$. The resulting voltage across the inductor from each source is determined by multiplying the effective ON-time of the source by its corresponding voltage magnitude. Illustrated in Figure 3, the effective voltage values are as follows: $D_{1eff}V_1$ for the first subdivision of the inductor charging period, $D_{2eff}V_2$ for the second subdivision, and $D_{3eff}V_3$ for the third subdivision.

To ensure efficient commutation of the switches during simultaneous power transfer, certain rules need to be followed to achieve the desired power transfer to the load. In the case of unequal voltages, if the input sources are arranged in ascending order of magnitudes ($V_1 > V_2 > \ldots > V_N$) for N input ports, the duty cycles of the switches (S_{W2}, S_{W3}, and S_{W4}) controlling the input sources must be set in a manner that satisfies $D_1 < D_2 < \ldots < D_N$, and vice versa. This arrangement ensures the proper coordination of the switches to facilitate simultaneous power transfer. For, $D_1 = D_{1eff}$, $D_2 = D_{1eff} + D_{2eff}, \ldots, D_N = D_{1eff} + D_{2eff} + \ldots + D_{Neff}$. But, in cases where the magnitudes of the input sources are equal ($V_1 = V_2 = \ldots = V_N$) for N input ports, the duty cycles of the PWM signals should be set such that $D_1 = D_2 = \ldots = D_N$ in order to achieve equal power delivery from all sources.

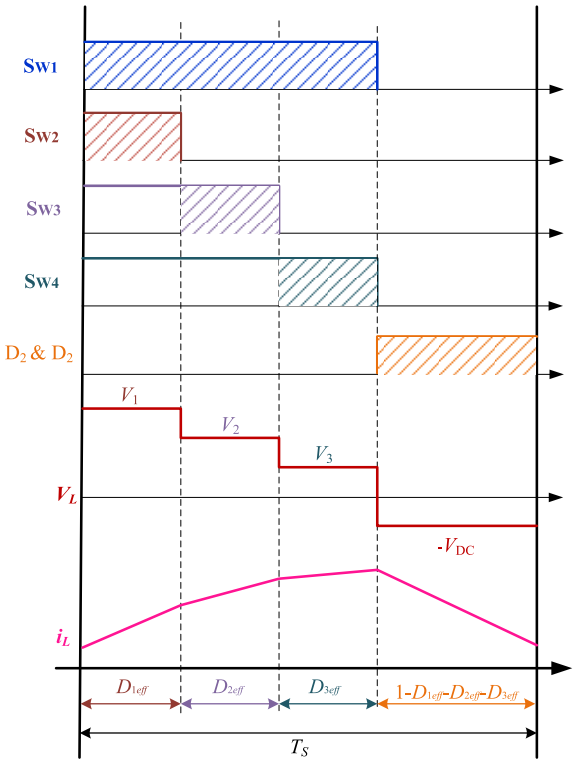

FIGURE 3. Steady state CCM waveforms of the MDC under simultaneous power transfer from the three sources to the dc link.

Then again, in cases where the desired power delivery from the sources is not equal, the values of $D_1, D_2, \ldots, D_N$ can be determined in increasing order of magnitude based on the respective sources. Additionally, by applying the principle of volt-second balance to the steady-state waveform depicted in Figure 3, the relationship between the input sources and the output voltage can be described by equation (1) for N input sources and by equations (1) and (2) specifically for the three-input configuration. In cases where the input sources have equal magnitudes, and the duty cycles are equal, the relationship between the input and output voltage can be expressed as equation (3). Yet, if the input sources have equal voltages but unequal duty cycles, the relationship between the input and output voltage can be described by equation (4), where V_{in} is the input voltage and D_{max} represents the maximum duty cycle among D_1 and D_2.

$$V_O = \frac{\sum_{i=1}^{N} \left(D_{(i)eff} V_i\right)}{1 - \sum_{i=1}^{N} D_{(i)eff}} \tag{1}$$

$$V_O = \frac{D_{1eff}V_1 + D_{2eff}V_2 + D_{3eff}V_3}{1 - D_{1eff} - D_{2eff} - D_{3eff}} \tag{2}$$

$$V_O = \frac{T_1}{T_2} V_{in} = \frac{D}{1 - D} V_{in} \tag{3}$$

$$V_o = \frac{D_{\max}}{1 - D_{\max}} V_{in} \tag{4}$$

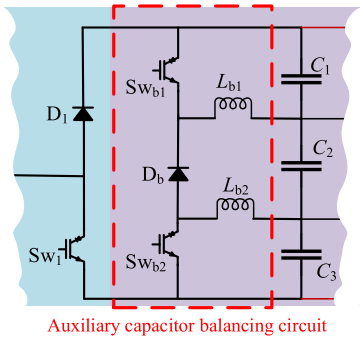

FIGURE 4. Schematic of the auxiliary circuit for capacitor balancing.

B. MULTILEVEL INVERTER TOPOLOGY

Figure 1 illustrates the MLI topology, which is indicated by the green shading. The MLI comprises of twelve unidirectional switches labelled as S_1 to S_{12}, along with three bidirectional switches identified as B_1 to B_3. In order to streamline the gate-drive circuits, a common-emitter structure is implemented to configure the bidirectional switches. The MLI topology utilizes three dc-link capacitors to establish the dc-link configuration. Through the control of the inverter switches, the topology is capable of producing four unipolar voltage levels: 0, E/3, 2E/3, and E, which correspond to the pole voltages V_{A0}, V_{B0}, and V_{C0}. By subtracting the adjacent pole voltages, the MLI can generate seven-level bipolar voltages in the line voltages V_{AB}, V_{BC}, and V_{CA}. For instance, the voltage V_{AB} is created by subtracting the value of V_{B0} from V_{A0}, resulting in a seven-level voltage comprising of -E, -2E/3, -E/3, 0, E/3, 2E/3, and E. The operational modes and modulation techniques of the MLI topology are thoroughly discussed in [22], providing comprehensive insights into its functionality.

C. CAPACITOR VOLTAGE BALANCING AND CONTROL STRATEGY

Figure 5 presents the high-level control structure of the proposed MDC, indicating the different controllers utilised for the different sections of the MDC. Also highlighted in the control structure is the capacitor balance control strategy for both the circuit- and control-based schemes. In four-level inverter topologies, it is not uncommon to encounter capacitor voltage imbalances. This occurs when three capacitors are linked in series, dividing the dc-link voltage into three equal portions, as depicted in Figure 1. A comprehensive approach to analyze and address the issue of capacitor voltage imbalance in four-level topologies was detailed in [37]. The proposed configuration results in unequal currents flowing through the three capacitors in the DC link, namely I_{C1}, I_{C2}, and I_{C3}. This current imbalance leads to a voltage disparity among the capacitors. Specifically, the current flowing through the middle capacitor, I_{C2}, is greater than the currents flowing through the other two capacitors, I_{C1} and I_{C3}, which are equal. As a result, there is an unequal discharge of energy among the capacitors C_1 and C_3 compared to C_2. Precisely,

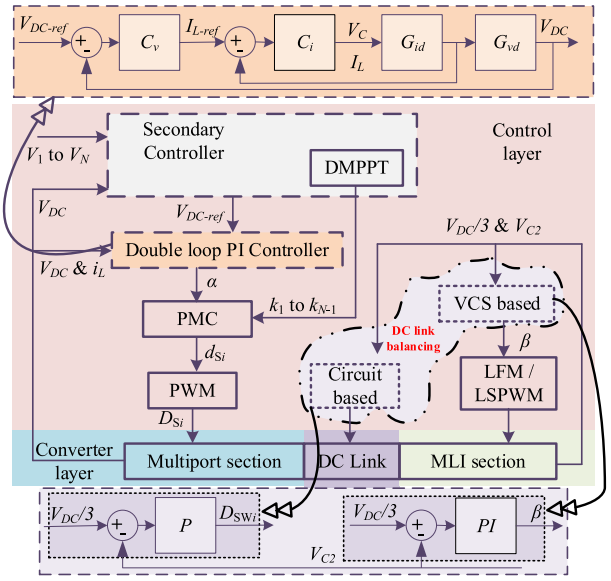

FIGURE 5. Control structure of the proposed MDC.

C_2 discharges more rapidly until reaching zero, while the full DC-link voltage V_{dc} is equally distributed between C_1 and C_3. This discrepancy in discharge causes an imbalance in the capacitor voltages, primarily due to the over-discharge of C_2. Hence, to achieve equilibrium among the capacitors, C_1 and C_3 can be balanced by regulating the voltage of C_2. Consequently, the three capacitor voltages, V_{C1}, V_{C2}, and V_{C3}, become equal when V_{C2} is regulated to $V_{dc}/3$. A control-based voltage balancing approach known as the variable-carrier scheme (VCS) is employed for this purpose in previous studies [22], [37], which relies on control-based methods. The VCS approach comprises three essential components: the generation block for modulation signals, the block for carrier signals, and a PI controller. These components work together to generate modulation signals with variable third-harmonic injection and fixed carrier signals. The purpose of this signal generation is to regulate the voltage of C_2, ensuring it remains at $V_{dc}/3$.

Nevertheless, in this implementation, a more straightforward approach is adopted by incorporating an auxiliary circuitry for capacitor balancing. This auxiliary capacitor balancing circuit, depicted in Figure 4, involves the utilization of two inductors (L_{b1}, L_{b2}) and three switches (a diode, D_b, and two MOSFETs, S_{Wb1}, S_{Wb2}). The operation of S_{Wb1} and S_{Wb2} is orchestrated using a common pulse signal. When these switches are activated, the two inductors are charged and subsequently discharged through D_b. This process ensures that the voltage of C_2 does not drop to zero. To achieve this, a proportional controller is employed, selected through a heuristic approach, which determines the duty cycle of S_{Wb1} and S_{Wb2}. The controller ensures that the voltage of C_2 is regulated to $V_{dc}/3$, while simultaneously maintaining the natural balance of C_1 and C_3 at $V_{dc}/3$. The use of a standard double-loop control strategy to regulate the

TABLE 1. Parameters used in system verification.

Parameter	Value	Unit
Inductor (L)	4	mH
Inductor (L_{b1}=L_{b2})	0.1	mH
Output capacitor (C_1=C_2=C_3)	9.4	mF
Voltage sources (V_1/V_2/V_3)	300/250/200	V
AC load ($R-L$)	8.1 / 12.5	Ω / mH

multiple RESs has been introduced and explained in [38]. The stress on the different components of the MDC has been analysed separately in [22] for the MLI section and [38] for the multiple RES section, these are the converters from which the proposed MDC is synthesized.

III. RESULTS

The validity of the suggested integrated converter system has been ascertained via numerical simulations and hardware-in-the-loop (HIL) implementation, utilizing the OPAL-RT's OP5700 device which is powered by a 64-bit virtex-7 FPGA. As depicted in Figure 6, the HIL and experimental setup employed for the validation process is presented, respectively, and the parameter values for each component utilized are shown in Table 1. Verification process was conducted under both open-loop and closed-loop conditions, and the outcomes were evaluated using numerical simulations, real-time HIL implementation and experimental verification. The key results of the verification process are included in this section.

The simulation results in Figure 7 showcase the performance of the MDC in an open-loop configuration when the input voltages are set as $V_1 = 300$ V, $V_2 = 250$ V, and $V_3 = 200$ V. The corresponding duty cycles applied to switches S_{W2} to S_{W4} are $D_1 = 20\%$, $D_2 = 40\%$ and $D_3 = 60\%$ (D_{SW2} to D_{SW4}), resulting in effective duty cycles of $D_{1eff} = D_{2eff} = D_{3eff} = 0.2$. In this scenario, the stress on the switches (V_{SW2} to V_{SW4}), inductor (V_L), and the current flowing through the switches (i_{SW2} to i_{SW4}), which also represent the input currents from the sources (i_{V1} to i_{V3}), are presented. Additionally, the voltage of the dc link (V_{DC}) and the voltages across the three capacitors (V_{C1} to V_{C3}) are also shown. The voltage of the dc link measures approximately 372 V and is evenly distributed across the three dc link capacitors, with each capacitor holding a voltage of around 124 V. The results obtained from the HIL implementation, as shown in Figure 8, align with the findings from the analytical simulation, confirming the accuracy and consistency of the system's performance. Additionally, the MLI stage operates using a level-shifted pulse width modulation (LS-PWM) scheme, which is extensively explained in [22]. Figures 9 and 10 showcase the outcomes of the simulation and HIL implementation of the MLI stage. In both cases, the MLI stage was configured to generate seven-level output voltages at a frequency of 50 Hz. It is noteworthy that the simulation and HIL results agree, providing further validation of the MLI's performance and functionality.

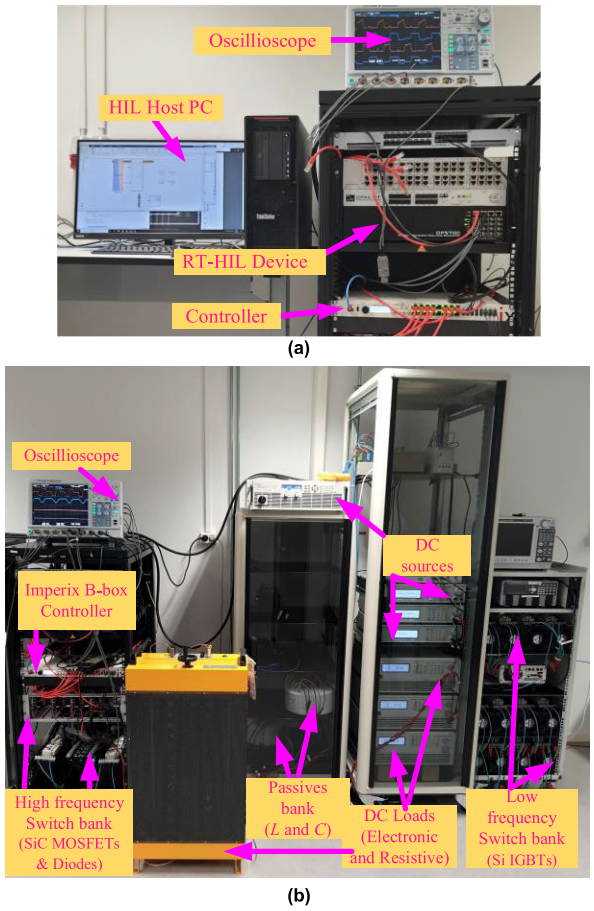

FIGURE 6. Integrated converter system validation on (a) in-house HIL platform and (b) the experimental validation platform.

In order to validate the voltage balancing across the dc link capacitors, both the control-based voltage balancing technique and the circuit-based voltage balancing were applied in both simulation and the HIL platform. The outcomes for each technique can be observed in Figures 11 and 12, respectively. These results serve to confirm the effectiveness of both voltage balancing approaches in maintaining a balanced voltage distribution across the dc link capacitors. The controller parameters of the control-based voltage balancing technique were determined using a heuristic approach, as detailed in [22]. As depicted in Figure 11 (a), the controller successfully maintains a stable steady state with the voltage across C_2, V_{C2}, regulated at approximately 124.8 V. Meanwhile, C_1 and C_3 exhibit natural balancing tendencies, distributing the remaining 247 V. It is worth noting that some oscillations are observed in the simulation results. Likewise, in the HIL implementation results shown in Figure 11 (b), the control-based voltage balancing technique successfully regulates V_{C2} to approximately 121 V. Meanwhile, C_1 and C_3 exhibit natural balancing tendencies, distributing the remaining 251 V. Oscillations are also observed in this scenario. On the other hand, the circuit-based capacitor balancing technique employs a basic proportional controller to regulate the active switches (Sw_{b1} and Sw_{b2}) of the

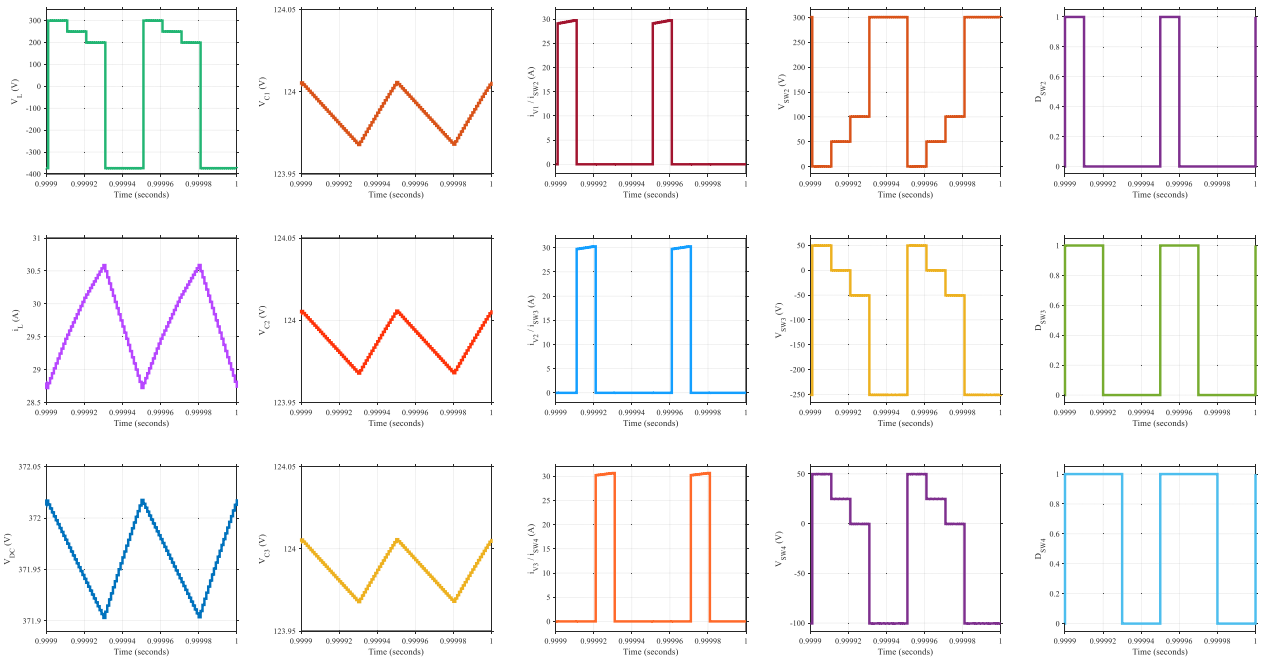

FIGURE 7. Open loop simulation results showing key waveforms of the MDC operation when $D_1 = 20\%$, $D_2 = 40\%$ and $D_3 = 60\%$.

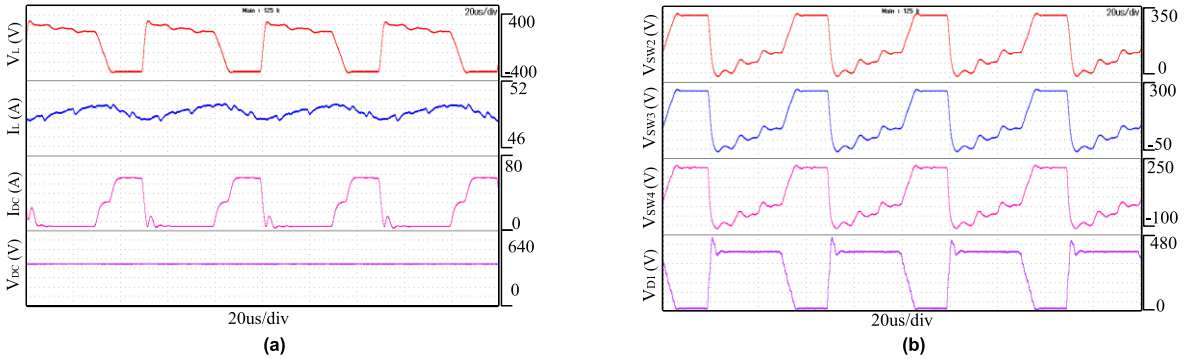

FIGURE 8. Open loop HIL implementation results showing key waveforms of the MDC operation when $D_1 = 20\%$, $D_2 = 40\%$ and $D_3 = 60\%$.

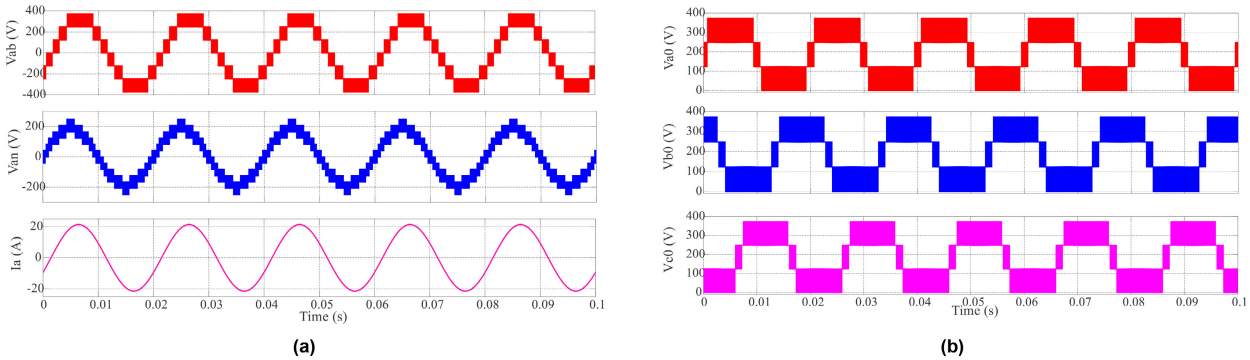

FIGURE 9. Simulation results of the MLI when the MDC duty is $D_1 = 20\%$, $D_2 = 40\%$ and $D_3 = 60\%$ showing (a) output current and voltage waveforms and (b) the pole voltages.

auxiliary capacitor balancing circuit. These switches operate with identical duty cycles, as determined heuristically. Figure 12 (a) presents the simulation outcome, demonstrating the successful achievement of capacitor voltage balancing through the implementation of the auxiliary circuit-based technique. Notably, this technique exhibits superior accuracy compared to the control-based technique shown in Figure 11 (a). V_{C2} is effectively regulated to approximately 124.1 V,

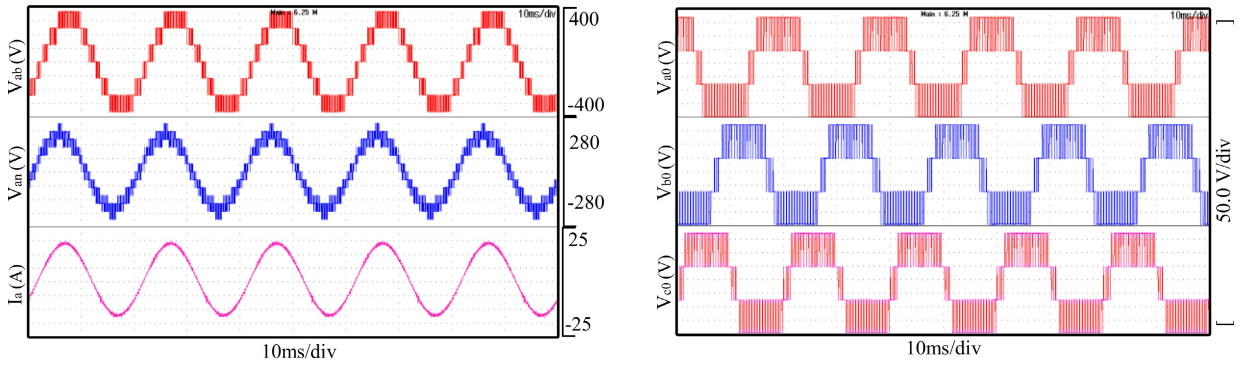

FIGURE 10. HIL implementation results of the MLI when the MDC duty is $D_1 = 20\%$, $D_2 = 40\%$ and $D_3 = 60\%$ showing (a) output current and voltage waveforms and (b) the pole voltages.

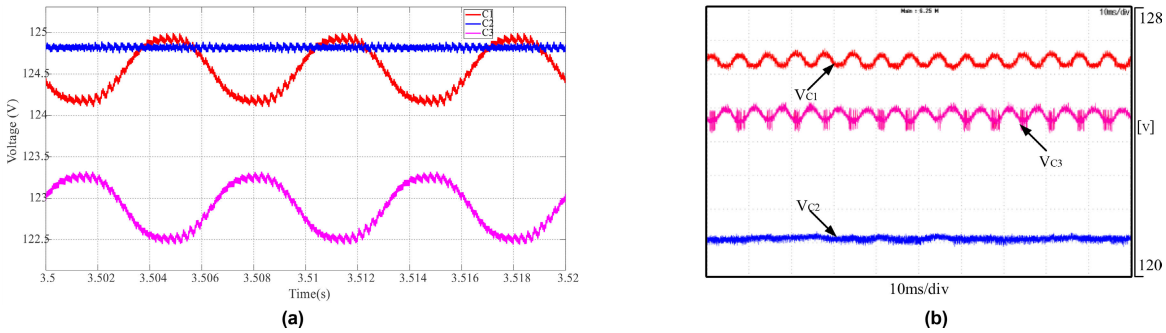

FIGURE 11. Control-based dc link capacitor voltage balancing showing (a) simulation and (b) HIL implementation results.

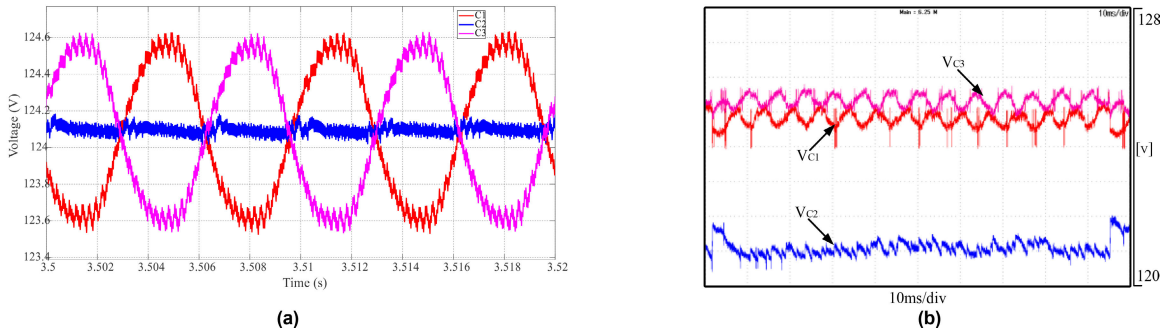

FIGURE 12. Auxiliary circuit-based dc link capacitor voltage balancing showing (a) simulation and (b) HIL implementation results.

while the remaining voltage of 248 V is equally distributed between C_1 and C_3. Oscillations, as observed earlier in Figure 11, are also present in this simulation. Additionally, Figure 12 (b) showcases the HIL implementation outcome, which aligns consistently with the simulation result depicted in Figure 12 (a). V_{C2} is effectively regulated to approximately 121 V, while the remaining voltage of 251 V is equally distributed between C_1 and C_3. Some oscillations are observed in this HIL implementation result as well. Comparing the HIL implementation results of the control-based technique displayed in Figure 11 (b) and the circuit-based technique illustrated in Figure 12 (b), it becomes evident that the latter achieves a more balanced distribution of the leftover voltage between C_1 and C_3 after V_{C2} is controlled to the required value. Moreover, the circuit-based approach necessitates additional components but demands less controller effort, whereas the control-based technique entails a complex controller without the need for extra components. Therefore, a trade-off between control complexity and component count must be carefully considered when deciding between these two techniques.

Furthermore, the closed-loop operation of the integrated converter system was implemented using the MDC, with the objective of regulating VDC to a target value of 400 V during the HIL implementation. The closed-loop strategy employed for MDCs, as detailed in [42], was adopted for this specific configuration. The PI control variables were heuristically chosen to attain the desired dynamic

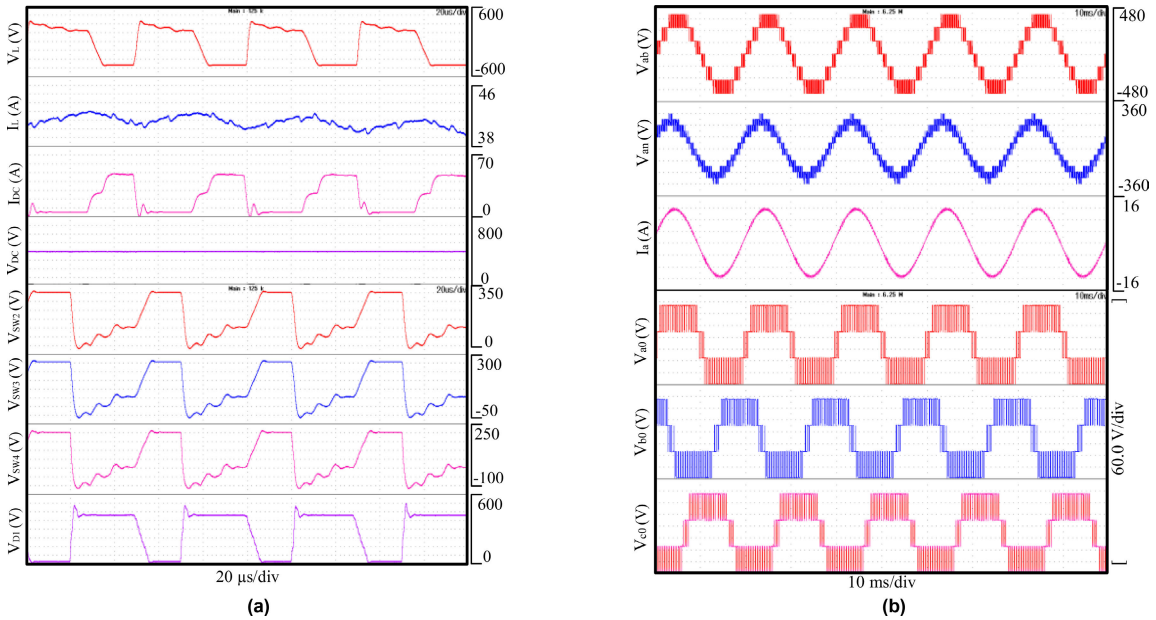

FIGURE 13. Closed loop HIL validation results showing (a) key waveforms of the MDC operation and (b) output current and voltage waveforms and the pole voltages.

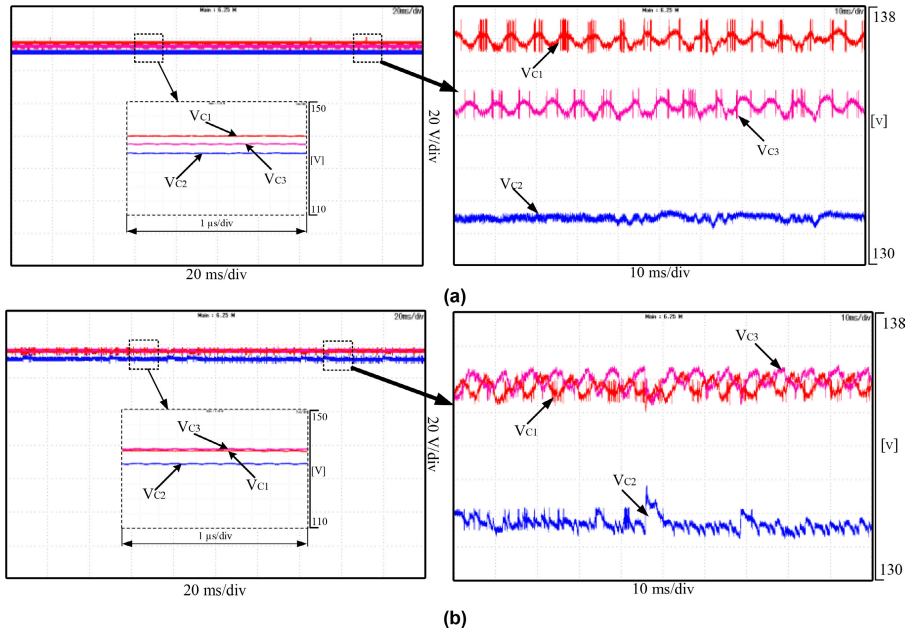

FIGURE 14. HIL execution results under closed operation of the MDC for (a) control-based dc link capacitor voltage balancing and (b) auxiliary circuit-based dc link capacitor voltage balancing.

performance characteristics. The results obtained from the closed-loop operation of the MDC section in the integrated converter system are illustrated in Figure 13. This figure showcases important measurements obtained during the operation. Additionally, a comparative analysis was conducted between the control-based and circuit-based techniques for balancing the voltage across the dc link capacitors under closed-loop conditions. The comparative results are presented in Figure 14. Once more, the circuit-based voltage balancing technique demonstrates a slightly superior performance in achieving an equal distribution of the dc link voltage among the three capacitors, without the need for the complex controller employed in the control-based technique. These findings provide further validation for the proposed integrated converter system, which effectively integrates multiple DC sources into both DC and AC grids.

Furthermore, Figure 15 presents a comparison of the auxiliary circuit-based DC link capacitor balancing and the control-based VCS method to further highlight the differences and advantages of using the circuit-based approach. The phase voltage, line current and voltage is presented in Figure 15 for both cases. The auxiliary circuit method

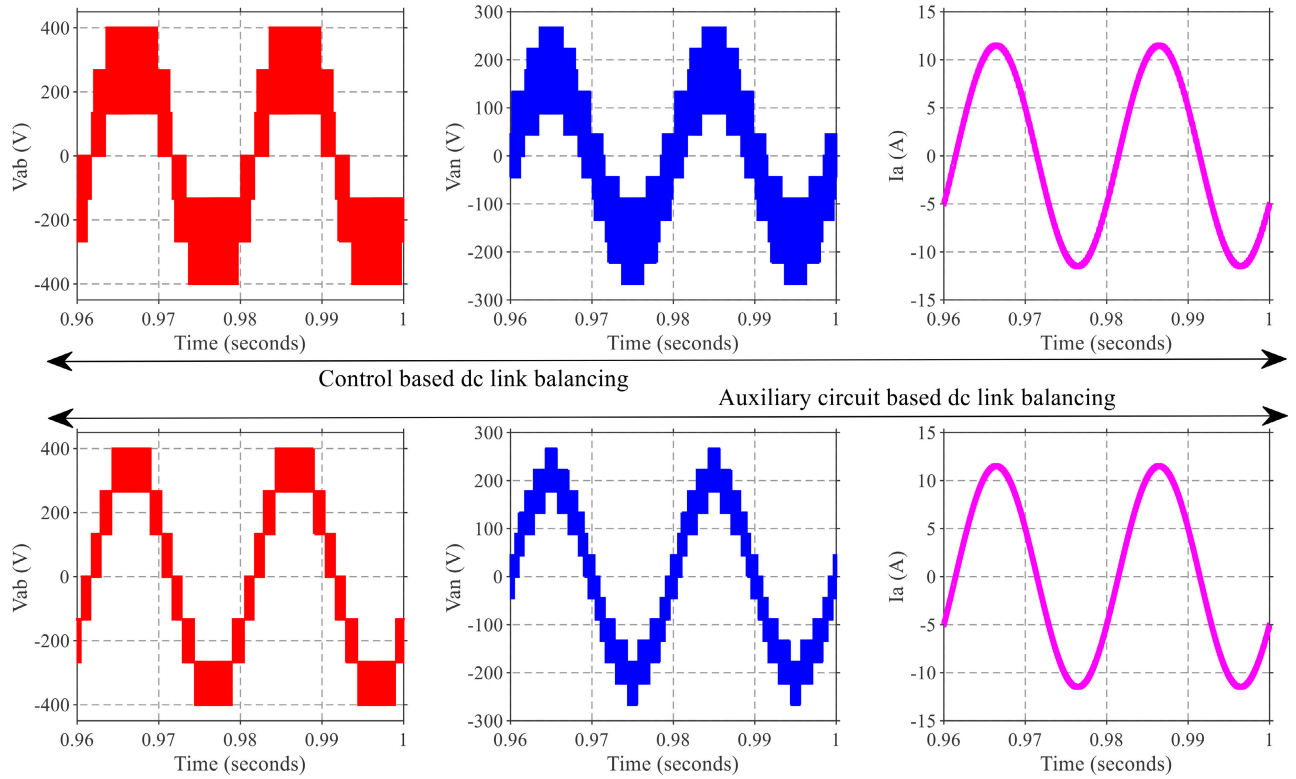

FIGURE 15. Comparison of control and auxiliary circuit-based DC link balancing showing Line and phase voltages and line currents.

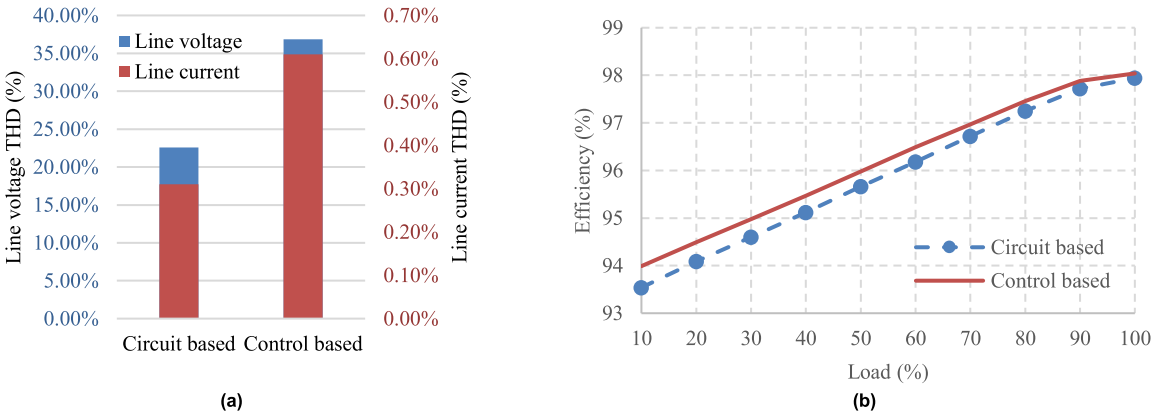

FIGURE 16. Analysis of (a) THD and (b) Efficiency of the MDC at 6 kW load.

(bottom row) produces better-quality waveforms than the control based balancing method shown in the top row of Figure 15. This is further emphasized by the comparison of the THDs presented in Figure 16 (a), comparing the line voltage and currents. The THD of the circuit based balancing method's line voltage and current is 22.56% and 0.31%, respectively, that is about 40% and 50% less than that of the VCS control-based method which is 36.85% and 0.61%, respectively. Consequently, the circuit-based method results in lower THD although at higher component count. It is worthy of note that the THD of currents are significantly low for both cases because of the inductive load. Further, to analyse the efficiency of the proposed MDC as presented in Figure 16 (b), the power losses (P_L) in MDC can be estimated using (5), consisting of the inductor and transformer winding (P_W) and core (P_C) losses [43], capacitor losses (P_{Cap}), MOSFET switching (P_{swMOS}) and conduction (P_{onMOS}) losses [44], and the losses in the diode (P_D). Where T_S is the switching period, R_{ESRL} is the inductor's equivalent series resistance (ESR), $\hat{i}_L$ is the inductor average current, Δi_L is the inductor ripple current, K, $\beta\&\alpha$ are Steinmetz parameters, R_{ESRC} is the capacitor ESR, V_{DS} is the MOSFET drain to source voltage, i_{DS} is the MOSFET drain to source current, $t_{on}\&t_{off}$ is the MOSFET ON and OFF time, R_{DSon} is the MOSFET on state resistance, D is its respective duty cycle, V_F and i_F are the diodes' forward voltage and current respectively. From

TABLE 2. Comparison of the proposed converter system with related converters.

Parameters		T_1 [30]	T_2 [27]	T_3 [28]	T_4-A [31]	T_4-B [31]	T_5 [29]	Proposed
Part Count	S	26	27	14	36	48	27	22
	D	2	0	2	0	0	0	2
	L	2	0	2	3	6	0	1
	C	4	3	3	0	0	5	3
	T	34	30	21	39	54	32	28
No. of inputs		1	3	1	6	6	1	N
IPF		NA	No	NA	No	No	NA	Yes
SPF		NA	Yes	NA	Yes	Yes	No	Yes
Isolated inputs?		No	Yes	No	Yes	Yes	No	No
No of levels		4	5	4	5	5	7	4
Boosting factor		3	2	3	$(1-D):1$	$(1-D):2$	1.5	$1/\left(1-\sum_i^N D_{ieff}\right)$
Buck-Boost?		Boost	Boost	Boost	Boost	Boost	Boost	Buck-Boost

N=No. of inputs, IPF=Independent power flow, SPF=Simultaneous PF, S=Active switch, D=Diode, L=Inductor, C=Capacitor, T=Total.

the efficiency results in Figure 16 (b), the MDC has a slightly higher efficiency if the VCS capacitor balancing scheme is adopted. This is due to the losses in the additional circuitry required in the auxiliary circuit-based capacitor balancing scheme. Overall, the efficiency of the MDC over the entire operating range is well above 90% for both VCS and the auxiliary circuit-based capacitor balancing scheme.

$$P_L \approx \left\{ \begin{array}{l} \underbrace{\frac{1}{T_S}\int_0^{T_S} R_{ESR}\left(\widehat{i_L}^2 + \frac{\Delta i_L^2}{12}\right)}_{P_W} + \underbrace{K\,\Delta i_L^{\beta} F_{SW}^{\alpha}}_{P_C} \\ + \underbrace{R_{ESRC}\left(\frac{\Delta i_L}{2\sqrt{3}}\right)^2}_{P_{Cap}} + \underbrace{\frac{1}{2} V_{DS} i_{DS} F_{SW}\left(t_{on}+t_{off}\right)}_{P_{swMOS}} \\ + \underbrace{R_{DSon} i_{DS}^2 D}_{P_{onMOS}} + \underbrace{\frac{1}{T_S}\int_0^{T_S} V_F i_F^2}_{P_D} \end{array} \right\} \tag{5}$$

IV. COMPARISON WITH RELATED TOPOLOGIES

Table 2 compares the proposed converter system with related existing converters to highlight the novelty. The selected converters are labelled topologies, $T_1 - T_5$ [27], [28], [29], [30], [31], as they are of similar structure to the converter system proposed in this paper, since the single phase topologies were converted to their three phase configurations. Firstly, by examining their component counts, only T_3 has a lower component count than the proposed converter, but T_3 has only one input port, while the proposed converter has three input ports, which can be extended for an arbitrary number of RES input ports. This is a similar case for T_1 and T_5 which have only a single input source as well, and a higher component count than the proposed converter.

In the case of T_2 and T_4 which have multiple number of RES input ports for three phases, independent power flow cannot be carried out arbitrarily from any of the input ports. Further, the voltage level of the input ports must be matched for these converters to perform optimally in simultaneous power transfer mode. Meanwhile, the proposed converter can perform arbitrary independent transfer of power from the RESs to the AC output and simultaneous power transfer under varying voltages at the RESs. In addition to this, in T_2 and T_4 with multiple inputs, these inputs need to be isolated, thus, an isolation transformer is required. While in the proposed topology, the RESs do not need to be isolated, and so the power density is higher and component count is kept lower than the converters in T_2 and T_4. Furthermore, the proposed converter system can buck and boost the input voltages while the counterparts can only boost the input. It also has the highest boosting factor of all the converters compared, a testament of the high voltage gain obtainable when the proposed converter system is applied for RES to AC grid integration.

V. CONCLUSION

This research introduced an innovative converter system that combines a new multiport DC-DC converter and a multilevel inverter topology. The new multiport DC-DC converter enables the seamless integration of various renewable energy sources, including photovoltaics, wind power, and fuel cell systems, into both DC and AC buses. Notably, the proposed configuration offers a simplified design with reduced components and complexities compared to existing approaches documented in the literature. The analysis of the proposed integrated converter system was performed considering three input sources operating in a simultaneous power flow configuration. Additionally, two different techniques for dc link capacitor voltage balancing were compared. The circuit-based balancing technique demonstrated a notable advantage, exhibiting lower total harmonic distortion compared to the control-based voltage balancing technique. The validity of the proposed integrated converter system was confirmed through numerical simulations and experimental testing on an FPGA-based high-fidelity hardware-in-the-loop implementation platform. The system's performance was evaluated in both open-loop and closed-loop operations to ensure its effectiveness and reliability.

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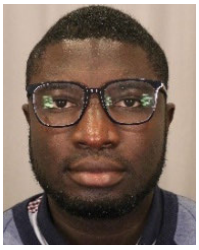

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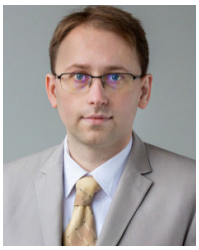

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