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RESEARCH ARTICLE

Digital Adaptive On-Time and Transient-Optimized Ripple Controlled Buck Converter

PEI-JUNG YANG, CHUN-HSUN WU, CHE-YEN YEH, AND LE-REN CHANG-CHIEN, (Senior Member, IEEE)
Department of Electrical Engineering, National Cheng Kung University, Tainan 701, Taiwan

Corresponding author: Le-Ren Chang-Chien (leren@ee.ncku.edu.tw)

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ABSTRACT Ripple-based buck converters often encounter issues of operating frequency variation, system stability, and steady-state voltage error, leading to degradation in voltage regulation performance. While analog controls are commonly employed to address these issues, they still face challenges due to process uncertainty and component parameter drifting caused by chip aging. In contrast, digital controls are more able to immune to the challenges that analog circuits faced. However, the sampling rate and analog-to-digital conversion (ADC) are the two shortfalls that degrade circuit response time compared to that of the analog circuits. The weakness is being improved by design flexibility and algorithms. This paper introduces a novel approach utilizing a digital approach to reduce the variation of operating frequency to very low range, which is called digital constant frequency (DCF) control. Additionally, the digital transient-optimized control (DTOC) is proposed to significantly shorten the transient settling time. The digital control does not need to use the ADC. Given the load current change between 100 and 500mA, the DCF control reduced the operating frequency variation from 40% to 2.8%. Furthermore, the DTOC significantly shortened the settling time for both the rising and falling responses by 60% compared to the converter without DTOC.

INDEX TERMS Ripple-based buck converter, adaptive on-time, frequency variation, load transient, digital constant frequency (DCF), digital transient-optimized control (DTOC).

I. INTRODUCTION

Within the power management unit (PMU), buck converters are widely employed to step down supply voltage for various load demands. Although buck converters exhibit higher efficiency at high loading conditions, they inherently suffer from output voltage ripple and slower transient response due to the stability issues. Therefore, the primary focuses of improvement in these converters revolve around fixed frequency operation, stability enhancement, and the reduction of steady-state errors. To enhance transient response, nonlinear controls such as ripple-based, hysteresis-based, and V^2-based have been proposed. Among the various existing control methods, the ripple-based control, commonly known as constant on-time (COT) or constant off-time (COFT) control, offers significant benefits. The controls of this type instantly respond to load or line voltage change, resulting in fast-response switching compared to that of the compensator based buck converters. However, the rippled-base converter faces issues of variable operating frequency, voltage ripple, steady-state error, and over-reacting to load transient [1].

The ripple-based buck converter is prone to switching frequency fluctuation because it is heavily influenced by factors of input voltage, output voltage, and the load current. This problem mainly gives rise to noise and electromagnetic interference [1]. The analog approach to fix this problem is to adaptively adjust on-time (AOT) [2], [3], [4], [5], [6] or utilize phase-locked loop (PLL) [7], [8], [9]. In AOT, a formula was demonstrated to show how the aforementioned factors affecting the operating frequency [1]. Therefore, the works

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proposed in [2], [3], [4], [5], [6], and [10] exert the on-time duty adjustment to reduce the switching frequency fluctuation. Approaches to implement this mechanism include pseudo-inductor current injection and a comparator delay compensation technique for the on-time generator [10], detecting the switching node voltage or introducing introduce a phase detector to achieve pseudo-constant switching frequency [11], [12]. The effectiveness of the analog approach heavily rely on the circuit parameters, which could be prone to the drift of manufacturing process or circuit aging. The other approach is to incorporate a phase-locked loop circuitry, as detailed in [7] and [8], which presented different degrees of complexity using the analog circuitry. In an effort to simplify the design, an alternative approach utilizing power MOS transistors in conjunction with RC filters has been introduced [13], with the expense of more silicon area occupied by the integration of large multistage RC filters.

The equivalent series resistance (ESR) of the output capacitor dominates steady state voltage ripple. Using a smaller ESR capacitor can effectively reduce the voltage ripple, but it adversely impacts the stability of ripple-based control [14], [15], [16], [17], [18]. Literature [15] demonstrated the occurrence of a pulse bursting phenomenon that impacts the control stability. Various methods were derived to address this issue, such as reference slope compensation, inductor current compensation, pseudo inductor current compensation, and capacitor current compensation [14], [15], [16], [17], [18]. The design trend indicates that a stable output voltage with small voltage ripple is essential to maintain the voltage quality of the ripple-based power converter.

The other inherent problem with ripple-based control is the steady-state error of the output voltage, which is influenced by the magnitude of the ripple signal. Literature [19] introduced an error amplifier to correct the steady-state error, and literature [20] proposed pseudo-wave tracking technology to correct level shifts caused by on-time control. However, both methods could prolong transient response. To improve transient response, an accelerating circuit or an embedded digital algorithm was augmented to reduce the transient recovery time [21], [22], [23], [24], [25], [26], [27], [28], [29], [30], [31], [32], [33].

In recent literatures, analog control continues to hold its dominant position as the prevailing design approach. Nevertheless, the digital implementation is being paid more attention because there has been a significant evolution in the adoption of digital implementations for PMUs in recent years. As power converter controls become more seamlessly integrated into PMUs, the demand for digital implementation has surged. Digital controls offer several significant advantages over their analog counterparts, including heightened robustness in the face of component variations, streamlined design processes, and, notably, a remarkable degree of flexibility when interfacing with digital systems [4]. Therefore, this paper takes a distinct focus on digital control as a solution to address the challenges encountered in ripple-based converters. The primary advantage of digital control lies in its integrative capability and the capacity to achieve diverse and multi-state control concurrently. Hence, in terms of cost-effectiveness, the proposed research retains substantial application value.

The key contributions of this research are summarized as follows:

1. Implementation of Full Digital Control Blocks: The research introduces a comprehensive design flow that facilitates the realization of full digital control blocks. This approach lays the groundwork for the seamless integration of PMUs.
2. Immunity to Manufacturing Uncertainty and Parameter Drift: The proposed digital circuitry exhibits robust resistance to manufacturing variations and circuit parameter drift, addressing issues that frequently affect analog counterparts.
3. Comprehensive Digital Control Solutions: The research offers fully digital control solutions that tackle multiple critical issues, including: Constant Frequency Control (DCF) to ensure consistent operating frequency under varying load conditions. Capacitance Current Sensing (CCS) Differentiator to mitigate the pulse burst phenomenon and correct voltage offset. Digital Transient Optimized Control (DTOC) to minimizing transient settling time for enhancing system performance.
4. Elimination of Analog-to-Digital Converters (A/D): Notably, the entire digital solution operates without the need for analog-to-digital converters (A/D). This represents a significant leap forward, overcoming a key limitation associated with the digital approach.

The organization of the paper is shown as follows. Section I provides comprehensive comments to the relative research. Section II discusses the cause of frequency variations and the principle behind the proposed digital constant frequency (DCF) control. Section III analyzes load transient response and introduces the proposed digital transient-optimized control (DTOC) for accelerating transient responses. Section IV introduces the sub-circuits that support the control blocks. Section V presents the validation of the circuit performance from experimental results. Section VI initiates a discussion aimed at elucidating the rationale behind selecting digital control as the central theme of this research. In Section VII, a retrospective summary of this research is made.

II. VARIABLE FREQUENCY AND PROPOSED DIGITAL CONSTANT FREQUENCY CONTROL

A. CAUSE OF THE FREQUENCY VARIATION OF THE RIPPLE-BASED BUCK CONVERTER

Ripple-based buck converter, as shown in Fig. 1, involves the feedback voltage (V_{fb}) through voltage division of the output voltage (V_o) and compares it with the reference voltage (V_{ref}) to trigger the ripple controller. The controller generates switching signals for the power stage transistors (*PMOS*, *NMOS*) to regulate the feedback voltage (V_{fb}) to match the reference voltage (V_{ref}).

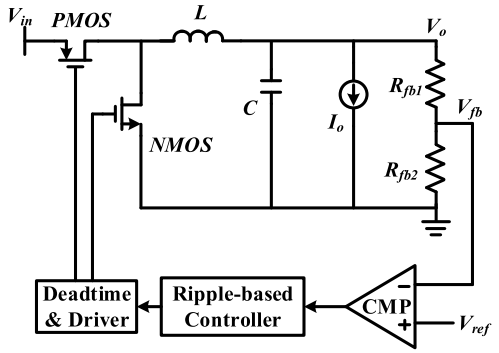

FIGURE 1. The schematic diagram of a buck converter employing ripple-based control.

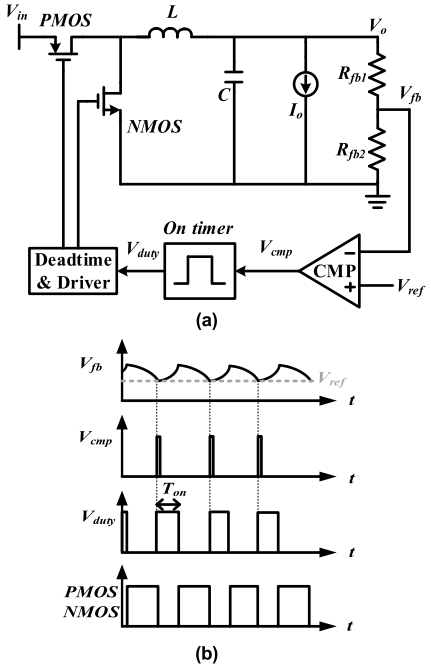

FIGURE 2. An example of the constant-on time control (a) circuit diagram (b) control waveforms.

Fig. 2 illustrates an example of the constant-on time control. When the upper arm (*PMOS*) is cut off, the inductor starts to discharge, causing the output voltage (V_o) to decrease. When the feedback voltage (V_{fb}) falls below the reference voltage (V_{ref}), the comparator output (V_{cmp}) triggers the on timer, which provides a switching signal (V_{duty}) to turn on the upper arm (*PMOS*) for a certain period of time (T_{on}). Afterward, the upper arm (*PMOS*) is turned off, which makes output voltage (V_o) decrease until the feedback voltage (V_{fb}) once again falls below the reference voltage (V_{ref}). This process is repeated by triggering the on timer, and it is known as constant-on time control.

Fig. 3 depicts a circuit of the constant on timer, which is composed of a bias voltage (V_{bias}), an operational amplifier (OP), and a resistor (R_t), forming a current source [1]. The current is amplified through the current mirrors M_1 and M_2.

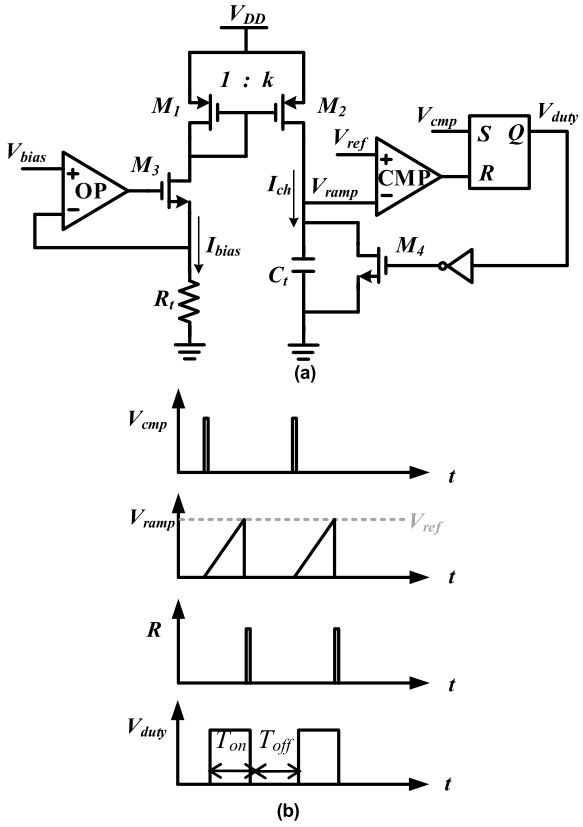

FIGURE 3. Commonly used constant on timer (a) circuit diagram (b) waveform.

When the external comparator outputs (V_{cmp}) trigger the time controller, V_{duty} switches to a high level, and at this point, the current (I_{ch}) charges the capacitor (C_t) to generate a ramp voltage (V_{ramp}). When the ramp voltage (V_{ramp}) equals the reference voltage (V_{ref}), the conduction time (T_{on}) ends, as described in equation (1). V_{duty} then switches to a low level, and the capacitor (C_t) discharges through M_4 to reset the ramp voltage (V_{ramp}) to zero. The waveform of the system is also illustrated in Fig. 3. From (1), it is evident that parameters such as the resistance (R_t), capacitance (C_t), width/length ratio (k) of the current mirror transistors (M_1M_2), bias voltage (V_{bias}), and reference voltage (V_{ref}) all could affect the on-time (T_{on}) of the circuit.

$$T_{on} = \frac{C_t R_t}{k \cdot V_{bias}} V_{ref} \tag{1}$$

Ripple-based control does not have a reference time signal like compensator-based control. Therefore, its operating frequency is more susceptible to various parameters such as input voltage, output voltage, load current, circuit parasitic parameters. The frequency variation of the output voltage can easily affect subsequent frequency-sensitive circuits, making frequency synchronization a critical issue in ripple-based control. Most constant frequency mechanisms are implemented by altering the slope of the ramp voltage (V_{ramp}) and the reference voltage (V_{ref}) [3], [4], [5], [6].

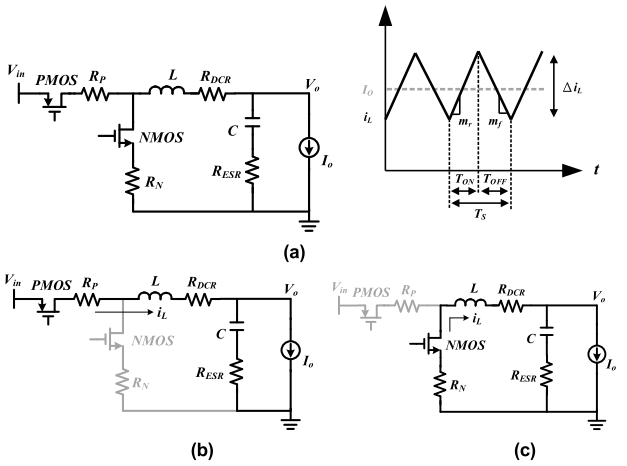

FIGURE 4. Non-ideal power stage of a buck converter (a)circuit and its waveform (b) The upper arm (PMOS) is conducting (c) The lower arm (NMOS) is conducting.

Fig. 4(a) shows the non-ideal power stage of a buck converter, taking into account parasitic parameters such as the upper-arm conduction resistance (R_P), lower-arm conduction resistance (R_N), and inductor DC resistance (R_{DCR}). When the upper arm (*PMOS*) is conducting and the lower arm (*NMOS*) is cut off, the current path is shown in Fig. 4(b), where the current flows through the upper arm (*PMOS*) and the inductor to the output terminal. Consequently, the inductor voltage drop is influenced by the upper-arm conduction resistance (R_P) and the inductor DC resistance (R_{DCR}). The inductor current at this point is given by (2). When the upper arm (*PMOS*) is cut off and the lower arm (*NMOS*) is conducting, as shown in Fig. 4(c), the current flows through the lower arm (*NMOS*) and the inductor to the output terminal. In this case, the inductor voltage drop is affected by the lower-arm conduction resistance (R_N) and the inductor DC resistance (R_{DCR}), and the inductor current is given by (3). Based on the Voltage-Second balance, the change in inductor current within one period in steady-state is zero. From (2) and (3), the relationship between the on-time (T_{on}) and the off-time (T_{off}) can be derived as shown in (4). Equation (4) shows that the off-time (T_{off}) is influenced by parasitic parameters (R_P, R_N, R_{DCR}) and load current, causing the switching period ($T_{on} + T_{off}$) to change under different light or heavy load conditions. The relationship between the on-time (T_{on}) and off-time (T_{off}) in (2) and (3) can be used to derive the duty cycle (D) as shown in (6). Different input voltages (V_{in}), output voltage (V_o) and load currents (I_o) will cause the duty cycle D to change accordingly.

$$\Delta i_{L,on} = \frac{(V_{in} - R_P \cdot I_o) - (V_o + R_{DCR} \cdot I_o)}{L} T_{on} \quad (2)$$

$$\Delta i_{L,off} = \frac{(-R_N \cdot I_o) - (V_o + R_{DCR} \cdot I_o)}{L} T_{off} \quad (3)$$

$$T_{off} = \frac{V_{in} - V_o - R_P \cdot I_o - R_{DCR} \cdot I_o}{V_o + R_N \cdot I_o + R_{DCR} \cdot I_o} T_{on} \quad (4)$$

TABLE 1. The distribution between the on-time (T_{on}) and off-time (T_{off}).

on-time (T_{on})	off-time(T_{off})		Duty ratio (D)
T_{on}=14	T_{off}=36	→	Duty = 28%
T_{on}=15	T_{off}=35	→	Duty = 30%
T_{on}=16	T_{off}=34	→	Duty = 32%
T_{on}=17	T_{off}=33	→	Duty = 34%
T_{on}=18	T_{off}=32	→	Duty = 36%
T_{on}=19	T_{off}=31	→	Duty = 38%
T_{on}=20	T_{off}=30	→	Duty = 40%
T_{on}=21	T_{off}=29	→	Duty = 42%

$$D = \frac{T_{on}}{T_{on} + T_{off}} \quad (5)$$

$$D = \frac{V_o + R_N \cdot I_o + R_{DCR} \cdot I_o}{V_{in} + R_N \cdot I_o - R_P \cdot I_o} \quad (6)$$

B. DIGITAL CONSTANT FREQUENCY (DCF) TECHNIQUE

To solve the variable frequency problem of the constant on-time control, the digital constant frequency (DCF) control is proposed. The idea of the DCF mechanism is illustrated as follows. We assume that a 50MHz digital clock (CLK) is selected for the operating frequency (F_s) of 1MHz. The counter is set to count up to 50 for representing one period. A constant frequency can be achieved by ensuring ($T_{on} + T_{off}$) always remain in 50 counts. The challenge lies in appropriately distributing the T_{on} and T_{off} within these 50 counts for meeting the constant output voltage (V_o) at variable load current (I_o).

This research adopts a concept similar to Predicting Correction Techniques (PCT) [3], where feedback of the duty cycle D is used to modify the conduction time (T_{on}). In DCF, the conduction time (T_{on}) and the cutoff time (T_{off}) are allocated based on the duty cycle and the fixed switching period ($T_{on}+T_{off}$), as illustrated in Table 1. T_{on} is adjusted according to the change of T_{off} such that sum of T_{on} and T_{off} remains 50 counts. The distribution relationship between the T_{on} and T_{off} is listed in Table 1. An example is illustrated as follows. For some instant T_{on} is set to 14 counts, while the T_{off} is set to 36 counts. When an increase in load occurs, the T_{on} remains at 14 counts but T_{off} decreases to 32 counts. The duty cycle D is then calculated as 30% at that moment. According to Table 1, the T_{on} needs to be adjusted to 15 counts for D=30%, the T_{off} then shall go to 35 counts. By maintaining a constant switching period ($T_{on} + T_{off}$), T_{on} values can be adaptively adjusted according to different duty cycles.

This work utilizes a look-up table (LUT) instead of a digital divider to calculate the duty cycle D for saving circuit design area. Initially, an initial value for the on-time (T_{on} [0]) is set. By detecting the off-time (T_{off} [n]) for each period, the next on-time (T_{on} [n+1]) to be set for the next period is determined by querying the LUT. Then, the process is repeated using the subsequent off-time (T_{off} [n+1]) as another parameter for querying the LUT to obtain a new on-time (T_{on} [n+2]). By repeating these steps, the T_{on} eventually stabilizes at some value for some specific loading condition to achieve constant

frequency operation. Note that the digital clock frequency affects the accuracy of the DCF. A higher digital clock frequency allows for a finer distribution of counts within one switching period (T_s), resulting in a more precise way to achieve the desired duty cycle D.

Considering parasitic effects, the actual duty cycle D and T_{on} are shown in (6) and (7), respectively. Assuming the digital clock frequency is X MHz, each period is 1000/X nanoseconds. Here, M represents the number of clock cycles in one period (T_s) for which the controller turns on the upper arm (*PMOS*), and N represents the possible number of clock cycles in one period (T_s) for which the upper arm (*PMOS*) turns off. Both M and N are positive integers, and T_{on} can be represented by M, as shown in (8). As it might not be possible to find an integer value for M that exactly matches the actual duty cycle D, multiple registers are used to average the result. The parameter P in (8) controls the proportional distribution to make the T_{on} closer to the required duty cycle D. The value of M, rounded to the nearest integer, can be derived from (7) and (8), which is shown in (9).

Equation (10) can be derived from (2) and (3) according to the Voltage-Second balance principle, which leads to the value of N, rounded up to the nearest integer, as shown in (11). Frequency variation (ΔF_s) can be derived from (9) and (11), shown in (12). It is observed that higher digital clock frequencies result in lower frequency variations (ΔF_s). However, higher digital clock frequencies may increase power consumption and heat dissipation, it is crucial to select an appropriate digital clock frequency based on the specified frequency variation tolerance (%) when making a choice. For instance, if the allowable operating frequency (F_s) is 1MHz $\pm$ 5%, a suitable digital clock frequency would be around 40MHz.

$$T_{\text{on}} = D \cdot 1000 = \frac{V_o + R_N \cdot I_o + R_{DCR} \cdot I_o}{V_{\text{in}} + R_N \cdot I_o - R_P \cdot I_o} \cdot 1000 \tag{7}$$

$$T_{\text{on}} = \frac{1000}{X} \cdot M \cdot P + \frac{1000}{X} \cdot (M+1) \cdot (1-P) \tag{8}$$

$$M = \left[\frac{V_o + R_N \cdot I_o + R_{DCR} \cdot I_o}{V_{\text{in}} + R_N \cdot I_o - R_P \cdot I_o} \cdot X + (P-1) \right] \tag{9}$$

$$\frac{1000}{X} \cdot (M \cdot P + (M+1) \cdot (1-P)) \cdot m_r = \frac{1000}{X} \cdot N \cdot m_f \tag{10}$$

$$N = \left[\frac{V_{\text{in}} - V_o - R_P \cdot I_o + R_{DCR} \cdot I_o}{V_{\text{in}} + R_N \cdot I_o - R_P \cdot I_o} \right] + 1 \tag{11}$$

$$\Delta F_s = \left| \frac{X}{M+N} - 1 \right| \cdot 100\% \tag{12}$$

Fig. 5 shows the block diagram of the digital constant frequency on-time control system. This system operates asynchronously to avoid metastable conditions. To prevent metastability, the input comparator output signal (V_{cmp}) passes through two stages of D flip-flops (DFF), synchronizing the triggering signal with the clock signal. The system can be divided into four main sub-blocks: The control switch signal and dead-time interval circuit (SR-latch), on-time counter

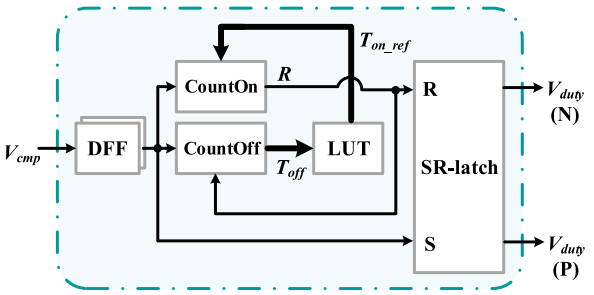

FIGURE 5. Block diagram of the digital constant frequency (DCF) on-time control system.

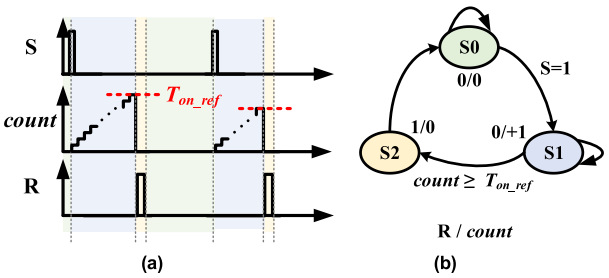

FIGURE 6. On-time counter (a) waveform diagram (b) state machine.

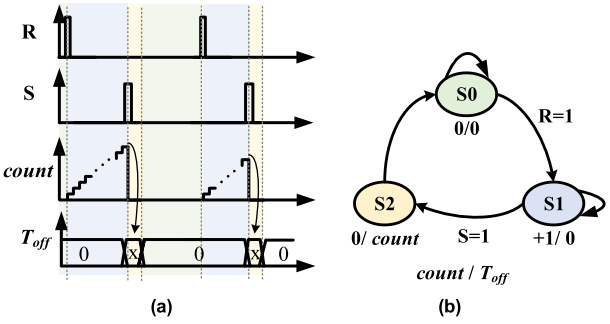

FIGURE 7. OFF-time counter (a) waveform diagram (b) state machine.

(CountOn), off-time counter (CountOff), and adaptive on-time LUT.

The waveform diagram and state machine of the on-time counter (CountOn) is shown in Fig. 6. In state 0, the counter is reset to zero. When the input signal S=1, the state changes from state 0 to state 1, and the counter starts counting until it reaches the reference on-time (T_{on_ref}) provided by the LUT. Then, the state shifts from state 1 to state 2 to generate a pulse signal R=1. Afterward, the state returns to state 0 to wait for the next trigger with input S=1. Likewise, the waveform diagram and state machine of the off-time counter (CountOff) is shown in Fig. 7. In state 0, the counter is reset to zero. When the input signal R=1, the state changes from state 0 to state 1, and the counter starts counting until the input signal S=1. Then, the state shifts from state 1 to state 2, and the value counted by the counter is the off-time (T_{off}), which is sent

TABLE 2. Example of adaptive on-time lookup table (LUT).

T_{on}[n]	T_{off}[n]	D	T_{on}[n+1]	T_{on}[n]	T_{off}[n]	D	T_{on}[n+1]
19	30	38.8	19	**20**	**29**	**40.8%**	**20**
19	31	38.0	19	**20**	**30**	**40.0%**	**20**
19	32	37.3	19	**20**	**31**	**39.2%**	**20**
19	33	36.5	18	20	32	38.5%	19
19	34	35.8	18	20	33	37.7%	19
19	35	35.2	18	**20**	**34**	**37.0%**	**19**

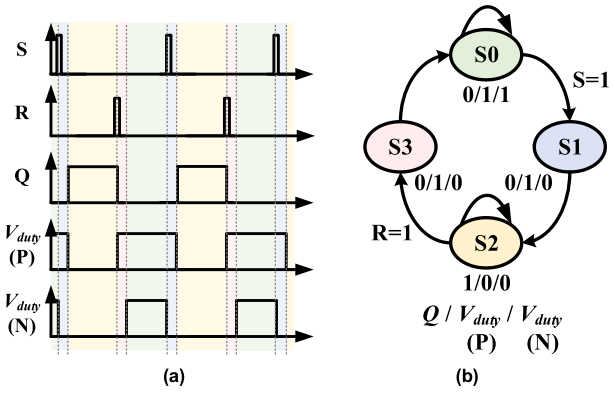

FIGURE 8. SR-latch (a) waveform diagram (b) state machine.

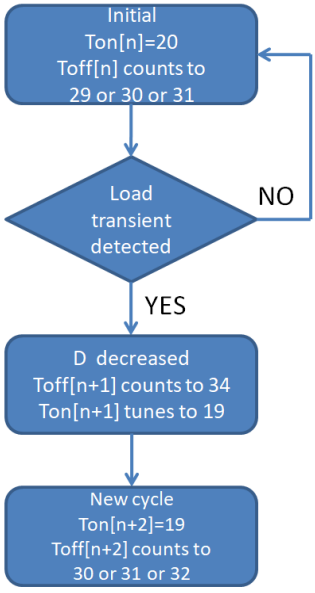

FIGURE 9. The example of the adaptive on-time lookup table (LUT).

to the adaptive on-time Lookup table (LUT). The state then returns to state 0, waiting for the next trigger with input R=1.

The waveform diagram and state machine of the control switch signal and dead-time interval circuit (SR-latch) is shown in Fig. 8. In state 0, both the control signals for the upper arm (*PMOS*) and the lower arm (*NMOS*) are at a high voltage level, making the upper arm (*PMOS*) off and the lower arm (*NMOS*) on. When the input signal S=1, the state transitions from state 0 to state 1, and the control signal for the lower arm (*NMOS*) switches to a low voltage level, causing both the upper arm (*PMOS*) and the lower arm (*NMOS*) to be off during the dead time interval. Next, the state changes from state 1 to state 2, and the control signal for the upper arm (*PMOS*) switches to a low voltage level, making the upper arm (*PMOS*) on and the lower arm (*NMOS*) off. When the input signal R=1, the state transitions from state 2 to state 3, and the control signal for the upper arm (*PMOS*) switches to a high voltage level, causing both the upper arm (*PMOS*) and the lower arm (*NMOS*) to be OFF during the dead time interval. Then, the state returns to state 0, waiting for the next trigger with input S=1.

Table 2 illustrates the adaptive on-time LUT. After reset, the initial value of the on-time (T_{on}[0]) is set. Suppose the initial value (T_{on} [0]) is 20 counts (right side). The off-time counter (CountOff) counts the off-time (T_{off}[0]) for that period and sends it to the LUT. If the off-time (T_{off} [0]) is 29, 30, or 31 counts, the next on-time remains at 20 counts. The on-time counter then gives the specified on-time, and after obtaining the off-time for the next period, it queries the table with an on-time of 20 counts to find the next on-time. Suppose a slight load variation occurs, resulting in a decrease in the duty cycle D. If the off-time counter (CountOff) counts the new off-time (T_{off} [n+1]) as 34 counts, the on-time (T_{on} [n+1]) needs to be adjusted to 19 counts. The next on-time (T_{on} [n+2]) is then queried from the table with an on-time (T_{on} [n]) of 19 counts (left side), determined by the off-time counter (CountOff) counting the off-time (T_{off} [n+2]). By repeating these steps, an adaptive T_{on} is generated for different load conditions to achieve constant frequency operation. The concept is illustrated in Fig. 9. The experimental results will be demonstrated in section V.

III. DIGITAL TRANSIENT-OPTIMIZED CONTROL

Ripple-based control naturally gives superior transient response compared to compensator-based control. However, several controls implemented in the steady state could slow down the transient response, especially the digital control is applied. To accelerate transient response in digital implementation, this paper takes the charge balance concept [21]. The digital transient-optimized control (DTOC) is designed to rapidly stabilize the output voltage (V_o) after the occurrence of transient. Fig. 10 illustrates the load transient timing diagram. In the case of a load step-up, as shown in Fig. 10(a), at time t_0, an instantaneous increase in load current (I_o)

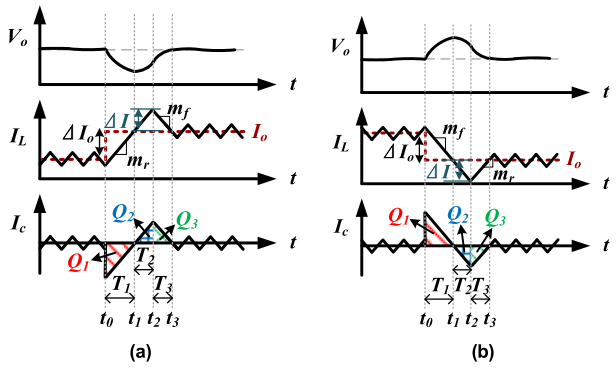

FIGURE 10. Load transient timing diagram (a) load step-up response (b) load step-down response.

occurs, causing an incremental change (ΔI_o) in the load. Because the inductor current (I_L) cannot respond quickly to the sudden current change, the output capacitor C (Q_1) release energy to the load instead, resulting in a rapid drop in the output voltage (V_o). Following that, the upper switch (PMOS) turns on to raise up the inductor current (I_L). When the inductor current catches up with the load current (I_o) at time t_1, the output voltage (V_o) reaches its minimum value. The inductor current (I_L) continues to rise until time t_2 when the upper switch (PMOS) turns off. The upper switch (PMOS) turns on again at time $t_3$to remain in steady state. Note that the injected energy (Q_2+Q_3) shall compensate for the energy released from the capacitor C (Q_1) so that the output voltage (V_o) returns to nominal value.

The proposed DTOC is to determine T_1, T_2,and T_3 for the optimal transient performance. Considering the load current flows through the upper switch on-resistance (R_P) or lower switch on-resistance (R_N) and the inductance internal resistance (R_{DCR}) that cause the voltage drops, the rising slope (m_r) and falling slope (m_f) of the inductor current are described in (13) and (14), respectively. The duty ratio D is determined by (15). The discharged energy released from the output capacitor (Q_1) is represented by (16), and the recharged energy (Q_2+Q_3) by the inductor is represented by (17). Ideally, (16) should be equal to (17) for charge balance. By substituting equations (18) and (19) into (16) and (17), respectively, T_1 and T_2 and T_3 can be derived subsequently as shown in (20) and (21), respectively. Likewise, T_1 and T_2 and T_3 can be derived subsequently as shown from (22) through (25) for the load step-down transient, as shown in Fig. 10(b). Detail mechanism behind Fig. 10(a) is described as follows. At time t_0, when the load current (I_o) suddenly increases by an amount (ΔI_o), the inductor current (I_L) cannot respond quickly to the instantaneous current change. The energy released from the internal charge (Q_1) of the output capacitor (C) supplies the load. This causes a rapid drop in output voltage (V_o), and the inductor current (I_L) rises until time t_1 when it catches up with the load current (I_o). At this moment, the output voltage (V_o) reaches its minimum value, resulting in an undershoot. The inductor current (I_L) continues to rise until time t_2, at which point the upper arm (PMOS) switches from on to off until time t_3. During this time, the inductor current (I_L) not only supplies the load current (I_o) but also replenishes the excess energy (Q2) and (Q3) to the capacitor that was released (Q1). This process restores the output voltage (V_o) back to its steady-state, ending the transient and achieving optimal transient control.

$$m_r = \frac{(V_{\text{in}} - R_P \cdot I_o) - (V_o + R_{DCR} \cdot I_o)}{L} \tag{13}$$

$$m_f = \frac{R_N \cdot I_o + (V_o + R_{DCR} \cdot I_o)}{L} \tag{14}$$

$$D = \frac{m_f}{m_r + m_r} \tag{15}$$

$$Q_1 = \frac{1}{2} \cdot \Delta I_o \cdot T_1 \tag{16}$$

$$Q_2 + Q_3 = \frac{1}{2} \cdot \Delta I \cdot (T_2 + T_3) \tag{17}$$

$$\Delta I_o = m_r \cdot T_1 \tag{18}$$

$$\Delta I = m_r \cdot T_2 = m_f \cdot T_3 \Rightarrow T_3 = \frac{m_r}{m_f} \cdot T_2 \tag{19}$$

$$T_2 = \sqrt{\frac{m_f}{m_r + m_f}} \cdot T_1 = \sqrt{D} \cdot T_1 = K_{up2} \cdot T_1 \tag{20}$$

$$T_3 = \frac{m_r}{m_f}\sqrt{\frac{m_f}{m_r + m_f}} \cdot T_1 = \left(\frac{1}{D} - 1\right)\sqrt{D} \cdot T_1 = K_{up3} \cdot T_1 \tag{21}$$

$$\Delta I_o = m_f \cdot T_1 \tag{22}$$

$$\Delta I = m_f \cdot T_2 = m_r \cdot T_3 \Rightarrow T_3 = \frac{m_f}{m_r} \cdot T_2 \tag{23}$$

$$T_2 = \sqrt{\frac{m_r}{m_r + m_f}} \cdot T_1 = \sqrt{1 - D} \cdot T_1 = K_{dw2} \cdot T_1 \tag{24}$$

$$T_3 = \frac{m_f}{m_r}\sqrt{\frac{m_r}{m_r + m_f}} \cdot T_1 = \frac{1}{\left(\frac{1}{D} - 1\right)}\sqrt{1 - D} \cdot T_1 = K_{dw3} \cdot T_1 \tag{25}$$

To initiate DTOC, a transient detection circuit is required to detect when a transient occurs and calculate the zero-crossing point at time t_1. As shown in Fig. 16, when the tr_up signal is 1, indicating a load increase, the system starts counting time T_1. Once the system obtains the information about t_1, equations (20) and (21) can be used to calculate t_2 and t_3. This information allows control of the switch-on and switch-off times based on the principle of charge balance, achieving optimal transient response as shown in Fig. 10.

Fig. 11 shows the block diagram of the digital transient-optimized control (DTOC). To avoid metastable conditions, the input signals, including the square wave capacitor current signal (V_{ccs}), load step-down transient signal (tr_{dw}), and load step-up transient signal (tr_{up}), need to pass through two D flip-flops to synchronize the trigger signals with the clock. The system can be divided into four main sub-blocks: Transient Detection Circuit (tr_dect), T_1 Interval Time Counter (CountT1), Pulse Generator, and Look-Up Table (LUT)

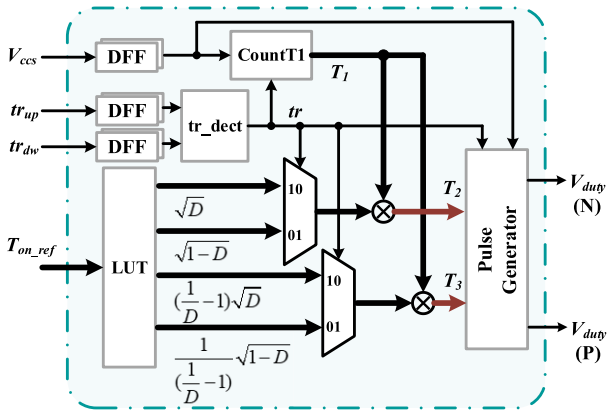

FIGURE 11. The block diagram of the digital transient-optimized control (DTOC).

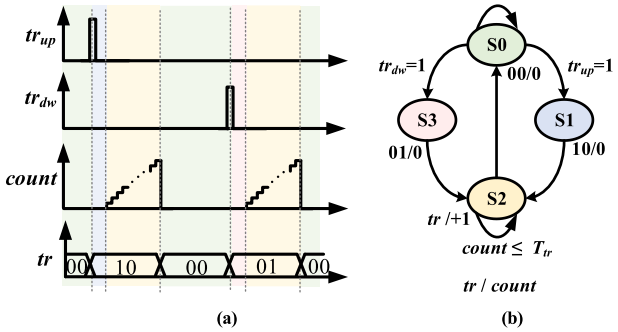

FIGURE 12. The transient detection circuit (tr_dect) (a) Waveform diagram (b) State machine.

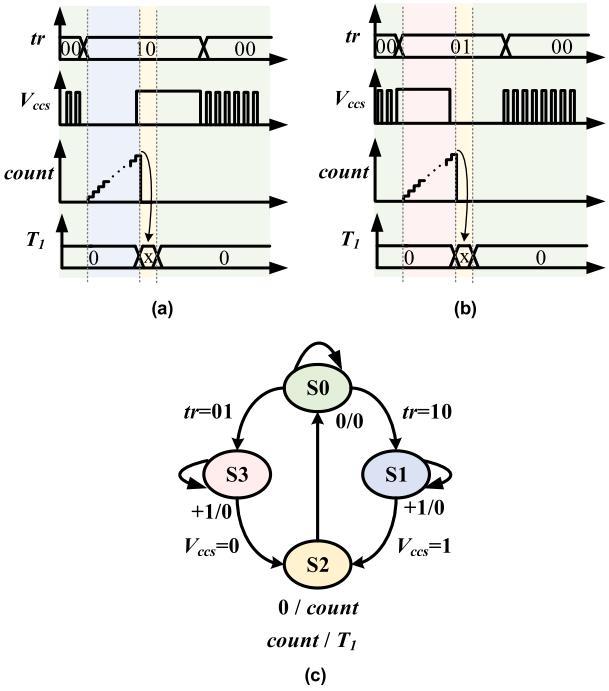

FIGURE 13. The T_1 interval time counter (CountT1) (a)load step-up waveform diagram (b)load step-down waveform diagram (c)state machine.

for the proportional parameters. Transient detection circuit (tr_dect) operates with a state machine and waveform as shown in Fig. 12. The load step-down transient signal (tr_{dw}) and load step-up transient signal (tr_{up}) serve as input signals. In state 0, the transient signal *(tr)* outputs '00,' indicating that no transient response is occurring. When the input load step-up transient signal (tr_{up}) is '1,' the state transitions from state 0 to state 1, and the transient signal (*tr*) outputs '10,' indicating entry into the load step-up response. The state remains in state 2 for a transient response time (T_{tr}) before returning to state 0, awaiting the next transient trigger. Similarly, when the input load step-down transient signal (tr_{dw}) is '1,' the state transitions from state 0 to state 3, and the transient signal (*tr*) outputs '01,' indicating entry into the load step-down response. The state remains in state 2 for a transient response time (T_{tr}) before returning to state 0, awaiting the next transient trigger. Thus, the state machine output (*tr*) reveals whether the system is in load step-up (10), load step-down (01), or steady-state (00), triggering the subsequent digital transient-optimized control.

The DTOC can be achieved by counting the T_1 interval time and multiplying the counted T_1 interval time with the output from the look-up table (LUT) of the scaling parameter to obtain T_2 and T_3 times, respectively. Therefore, a T_1 interval time counter (CountT1) is required. The waveform diagram and state machine for CountT1 is shown in Fig. 13. The input signals are the transient signal (*tr*) and the capacitor current square wave signal (V_{ccs}) from the transient detection circuit (tr_dect). After the reset, the state of the system is in state 0. When the transient signal (*tr*) transitions to "10," indicating a load step-up condition, as shown in Fig. 13(a), the state changes from state 0 to state 1. The counter starts accumulating until the capacitor current square wave signal (V_{ccs}) transitions from "0" to "1". The state then transitions from state 1 to state 2, and the output of the counter represents the T_1 interval time. The state returns to state 0, awaiting the next trigger of the transient signal (*tr*). When the transient signal (*tr*) transitions to "01," indicating a load step-down condition, as shown in Fig. 13 (b), the state changes from state 0 to state 3. The counter starts accumulating until the capacitor current square wave signal (V_{ccs}) transitions from "1" to "0". The state then makes a transition from state 3 to state 2, and the output of the counter represents the T_1 interval time. The state returns to state 0, awaiting the next trigger of the transient signal (*tr*). This control method involves adjusting the switch times T_2 and T_3 to achieve the desired transient response. The values of T_2 and T_3 are obtained by multiplying the T_1 interval time with different scaling factors according to (24) and (25). The scaling factors (K_{dw2}, K_{dw3}) are related to the duty cycle D and can be determined from the look-up table (LUT) of the adaptive conduction time in the DCF method. To simplify the circuit and reduce complexity, division and square root operations are omitted. Instead, the

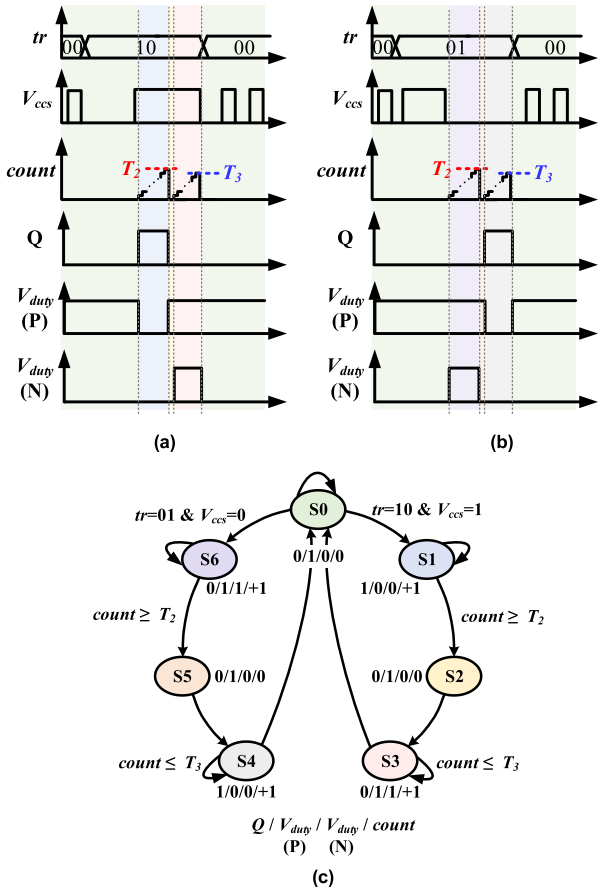

FIGURE 14. Pulse generator waveform diagram and state machine.

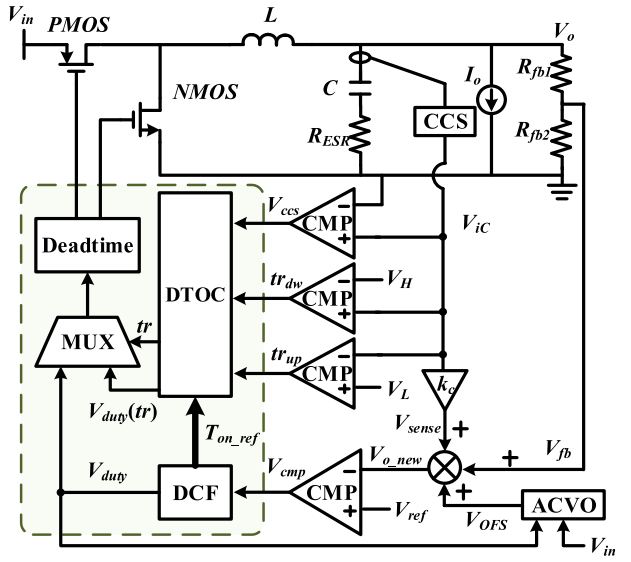

FIGURE 15. The overall control blocks of the ripple-based buck converter.

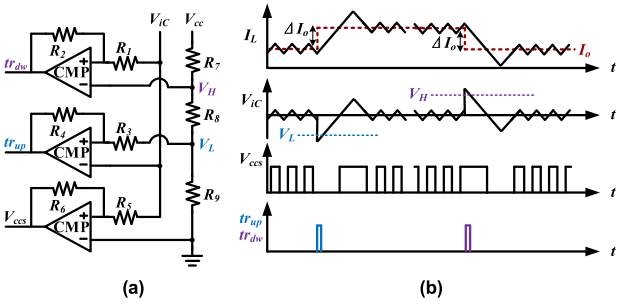

FIGURE 16. The transient detection and zero-crossing detection circuit (a)Circuit diagram (b)Waveform diagram.

scaling factors are referred to the look-up table (LUT) to determine T_2 and T_3.

The pulse generator waveform diagram and state machine in Fig. 14 shows the various states and corresponding conditions. When in steady-state, the state is 0, and both the upper arm (*PMOS*) and the lower arm (*NMOS*) switches are turned off, waiting for the transient trigger. During the load step-up response, as shown in Fig. 14(a), the state changes from 0 to 1 when the transient signal (*tr*) is "10" and the capacitor current square wave signal (V_{ccs}) changes from "0" to "1". The upper arm (*PMOS*) switch turns on, and the counter starts accumulating until T_2 time. Then, the state changes to 2, turning off both upper and lower arm switches to avoid simultaneous conduction. After that, the state changes to 3 to turn on the lower arm (*NMOS*) switch, and the counter accumulates until T_3 time. The state returns to 0 to wait for the next transient signal (*tr*) trigger. During the load step-down response, as shown in Fig. 14(b), the state changes from 0 to 6 when the transient signal (*tr*) is "01," and the capacitor current square wave signal (V_{ccs}) changes from "1" to "0". The lower arm (*NMOS*) switch turns on and the counter starts accumulating until T_2 time. Then, the state changes to 5 to turn off both upper and lower arm switches to avoid simultaneous conduction. After that, the state changes to 4 to turn on the upper arm (*PMOS*) switch, and the counter accumulates until T_3 time. The state returns to 0, waiting for the next transient signal (*tr*) trigger. The DTOC mechanism provides a simple concept for rippled-based converter to achieve transient-optimized load response. The experimental results will be demonstrated in section V.

IV. SUB-CIRCUITS APPLIED IN THE DESIGN

The proposed control system within the buck converter is shown in Fig. 15, which can be primarily divided into analog auxiliary circuits and digital control circuits. The analog circuits include the power stage of the buck converter, the Capacitor-Current-Sensor Differentiator (CCS), the Auto-Correction of Voltage Offset (ACVO) circuit, the new output voltage (V_{o_new}) generation circuit, the transient detection circuit, and the comparator. The digital circuits are mainly responsible for control (indicated in dash box), including the Digital Constant Frequency On Time Control (DCF), the Digital Transient-Optimized Control (DTOC), and the Dead-Time Control circuit.

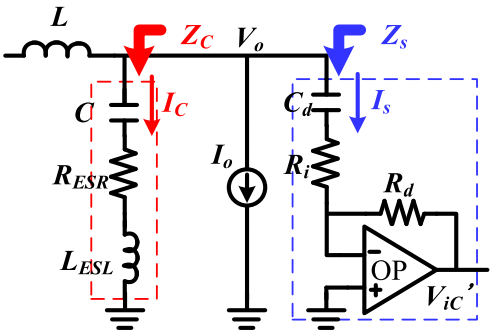

FIGURE 17. Implementation of the CCS.

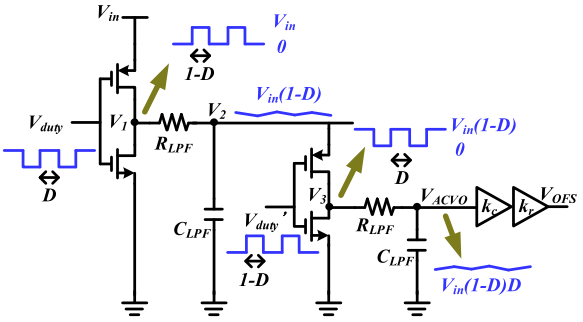

FIGURE 18. Implementation of Auto-Correction of Voltage Offset (ACVO).

TABLE 3. Buck converter specifications.

Input Voltage (V_{in})	2.7V/4.2V
Output Voltage (V_o)	1.2V
Switching Frequency (F_s)	1MHz
Output Current (Io)	100-500mA
Inductor (L)	4.7μH
DC Resistance (DCR)	30mΩ
Capacitor (C)	4.7μF
Equivalent Series Resistance (ESR)	10mΩ
Upper Arm Resistance (R_P)	0.3 Ω
Lower Arm Resistance (R_N)	0.1 Ω
Digital Clock (CLK)	50MHz

A. TRANSIENT DETECTION CIRCUIT

To incorporate DTOC, a transient detection circuit is required to detect the occurrence of transients and to calculate the zero-crossing point for T_1 time. Three sets of comparators are used to generate signals DTOC, as shown in Fig. 16. The first set of comparators processes the capacitor current signal (V_{iC}) and outputs a high voltage level when V_{iC} is greater than zero, or generates a low voltage level when V_{iC} is less than zero. It can convert the triangular waveform of the capacitor current signal (V_{iC}) into a square wave capacitor current signal (V_{ccs}), as shown in Fig. 16 (b). The voltage source (V_{cc}) is divided into lower limit voltage (V_L) and upper limit voltage (V_H) using resistors (R_7, R_8, R_9). The comparators use resistors (R_1-R_6) to create the required hysteresis interval. When the capacitor current signal (V_{iC}) is greater than the upper limit voltage (V_H), the comparator outputs the downturn transient signal (tr_{dw}). On the other hand, when the capacitor current signal (V_{iC}) is less than the lower limit voltage (V_L), the comparator outputs the uplift transient signal (tr_{up}).

B. CAPACITOR CURRENT SENSOR (CCS)

This work adopts the idea of capacitor-current sensor (CCS) [34] to avoid the pulse bursting phenomenon, as depicted in Fig. 17. A differentiator was utilized. We added a sensing path for which the input impedance is Z_s at the output in an attempt to match the Z_s and Z_c impedance, so the capacitor current signal could be replicated.

C. AUTO-CORRECTION OF VOLTAGE OFFSET (ACVO)

Because the ripple-based control does not have the error compensator to correct the steady state voltage error, an Auto-Correction of Voltage Offset (ACVO) circuit, as shown in Fig. 15, is designed to adjust the voltage offset caused by the ripple signal. Fig. 15 shows that the control signal V_{o_new}, is composed of the feedback voltage V_{fb}, ripple signal V_{sense}, and offset correction signal V_{OFS}. The offset correction signal (V_{OFS}) is determined by the duty ratio which is related to the rising slope (m_r). Their relationship are illustrated by (26) and (27), respectively. The schematics of the ACVO is shown in Fig. 18.

$$V_{OFS} = \frac{1}{2} \cdot k_c \cdot \frac{V_{in} \cdot (1-D)}{L} \cdot T_{on} = k_c \cdot k_r \cdot (V_{in} \cdot (1-D) \cdot D) \quad (26)$$

$$m_r = k_c \cdot m_r\,(V_{ic}) = k_c \cdot \frac{V_{in} \cdot (1-D)}{L} \quad (27)$$

V. REAL CIRCUIT VALIDATION

A real circuit was implemented to verify the proposed control performance. The specifications of the power stage is shown in Table 3. The FPGA ADC-SoC development board was used to implement the digital control.

Fig. 19 shows the experimental results of steady-state waveforms without/with DCF. The switching frequency for light load was 658.04kHz as shown in Fig. 19 (a). Under heavy load, the switching frequency was 1.077MHz as shown in Fig. 19 (b). The switching frequency variation between 100mA and 500mA load was 418.96kHz. When the DCF was applied, the switching frequency under light load was 1.049MHz as shown in Fig. 19 (c). Under heavy load, the switching frequency was 1.077MHz as shown in Fig. 19 (d). The switching frequency variation between 100mA and 500mA load was significantly reduced to 38kHz. It is also worth noting that both CCS and ACVO sub-circuits help reduce the voltage ripple from 16mV to 8 mV and reduce the voltage offset percentage to 0.33% (V_{OFS} / V_o).

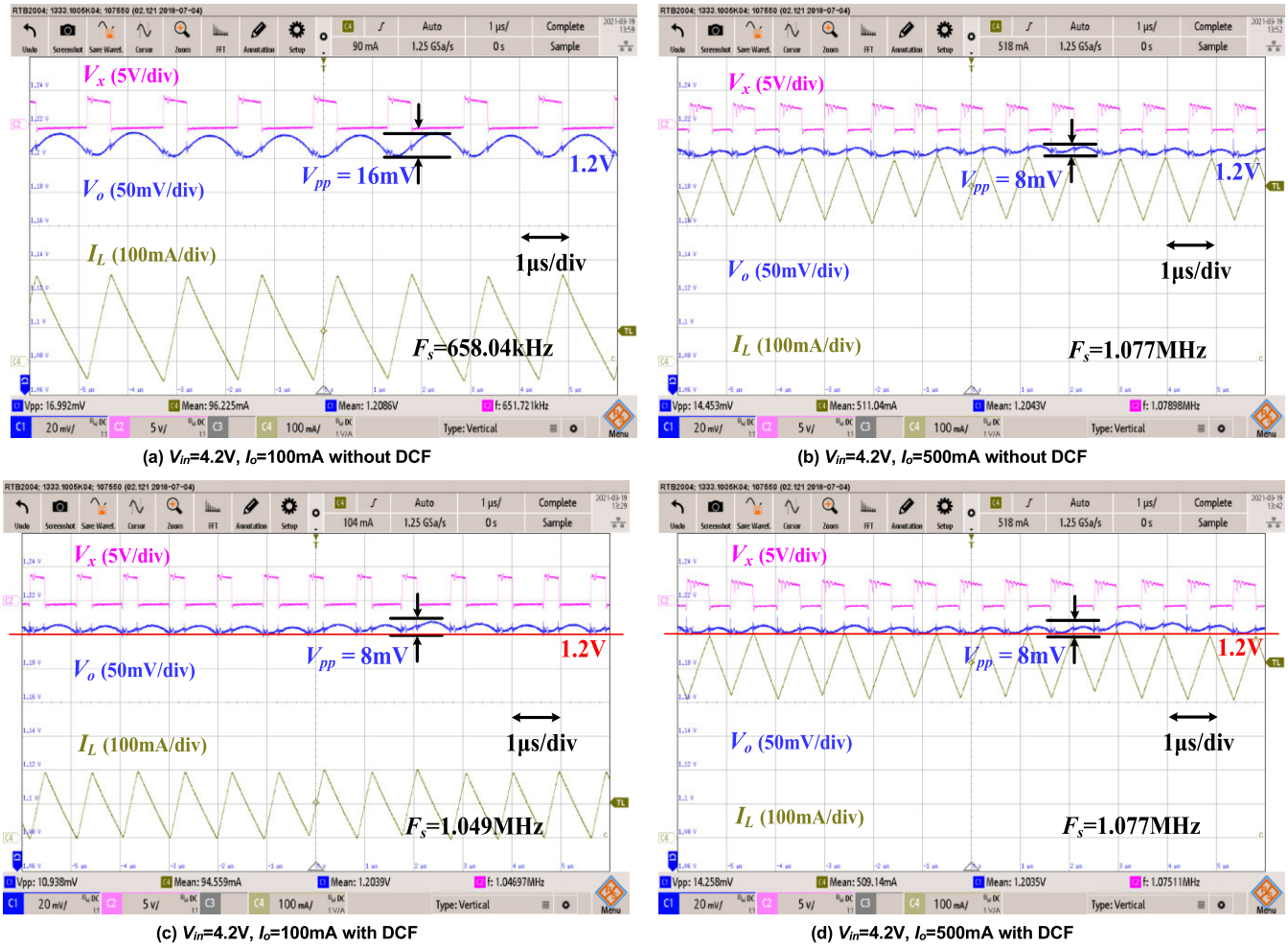

FIGURE 19. The experimental results of the buck converter without/with the DCF.

Fig. 20 (a) and (b) show the experimental results of transient response without the DTOC. When the load increased from light to heavy, the settling time was 8μs and the undershoot was 80mV. When the load decreased from heavy load to light, the settling time was 9μs and the overshoot is 75mV. Fig. 20 (c) and (d) show the experimental results as DTOC was applied under the load transients. The output voltage rapidly settled back to its steady-state as load increased. The settling time reduced from 8μs to 2.5μs and the undershoot reduced from 80mV to 50mV. When the load current decreased from heavy load to light load, the settling time reduced from 9μs to 3μs and the overshoot reduced from 75mV to 68mV. The DTOC circuit effectively shortened the settling time to approximately 60% and reduced both the undershoot and overshoot magnitudes.

A list of comparison between this work and those of prior arts is shown in Table 4. The tested system provides nearly fixed switching frequency with variation rate of 2.8%, which outperformed the case in [35] and the other COT controls because their operating frequencies are variable. Another advance of this work is to save the analog-to-digital converter (ADC) that digital circuit needs in [35]. The DC offset is small which is comparable to the other prior arts that take DC offset into consideration. Regarding transient response, it is evident that analog circuitries ([20], [28], and [30]) inherit nature of fast response compared to those of digital circuitries ([26], [35], and this work). In comparison to digital control in [26], the proposed DTOC shows less oscillation in voltage recovery, such that settling time can be minimized. In short, the overall performance indices in terms of constant frequency, output voltage offset correction, and the transient response are comparable to those of prior arts, which validate the effectiveness of the proposed methodologies.

The actual implementation of this circuit achieves an efficiency of approximately 81.6%, which is lower than the 90% efficiency achievable with analog circuits. The primary reason is that analog control circuits can achieve similar functionality using fewer transistors compared to digital circuits. Consequently, the efficiencies of analog circuits are higher than that of the digital circuits under the same functional conditions. It is noteworthy that while the experimental performance outlined in the paper may not surpass every

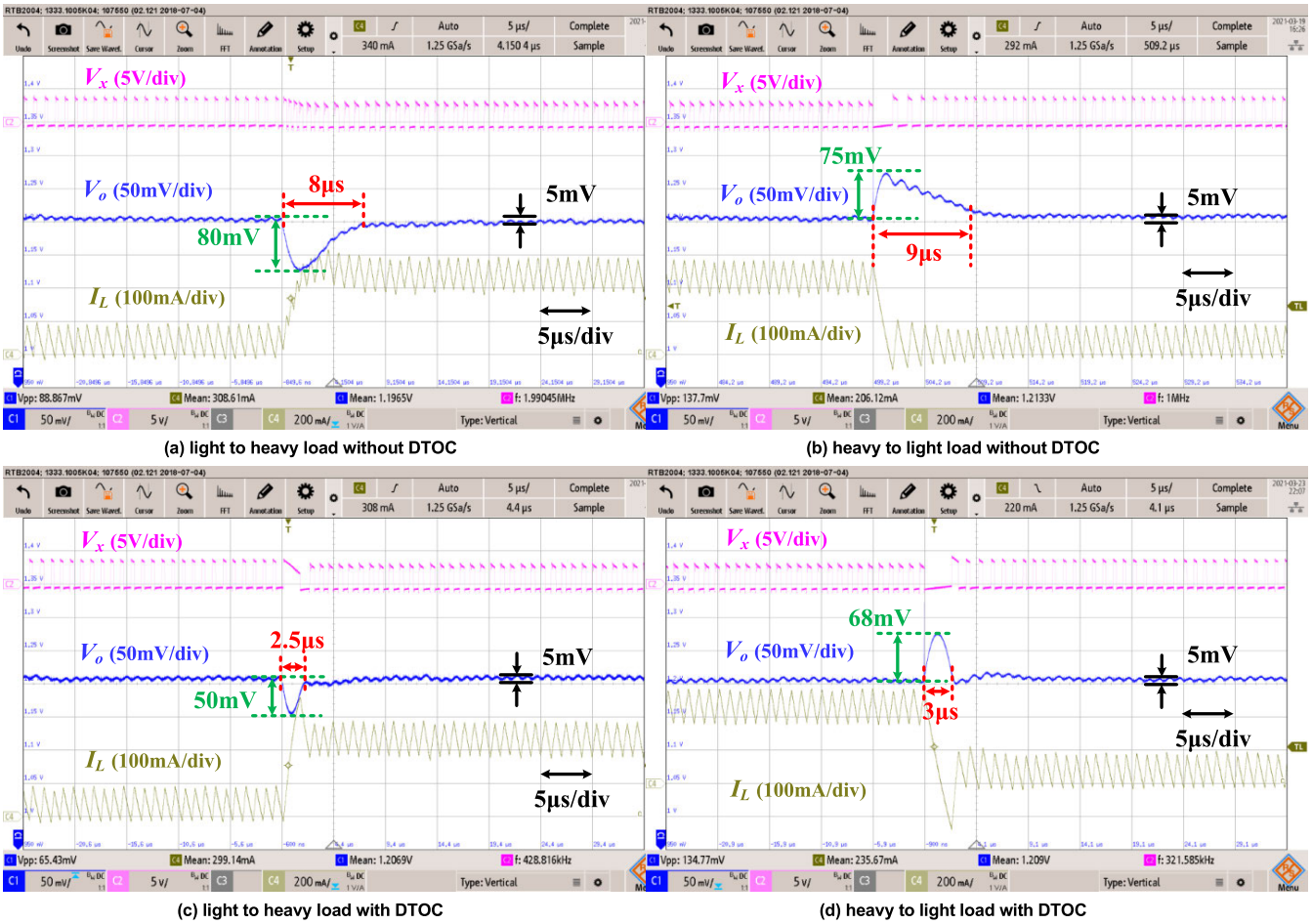

FIGURE 20. The experimental results of the buck converter without/with the DTOC.

capability of state-of-the-art analog control method, it is crucial to acknowledge the presence of inherent sampling and computational delays in digital control. Thus, achieving such improvements holds significant merit.

VI. DISCUSSION

As demonstrated in the circuit validation, there are invariably pros and cons associated with opting for a digital solution over an analog one. In the past, analog circuits frequently encountered challenges stemming from issues like process variations and chip aging, which resulted in discrepancies between designed and actual parameters. The transition to digitalization has proven highly effective in addressing these concerns. Furthermore, digital control circuits display robust noise immunity due to their reliance on straightforward binary (0 and 1) operations for internal signal transmission and logic control. This inherent simplicity makes them notably less vulnerable to errors induced by noise interference.

Another significant advantage of digital control lies in its capacity to formalize the design process. Through the composition of Hardware Description Language (HDL) code for the realization of control architectures and algorithms, the design procedures can be seamlessly amalgamated. This flexibility permits straightforward adaptations for various converter specifications, enabling swift modifications to the code to adjust design parameters. This streamlined approach simplifies the application and expedites the design process, resulting in a substantial reduction in the time required for design completion.

Given these characteristics, digital designs are highly favored in the industry and represent a significant trend in the future IC (integrated circuit) industry. Consequently, this paper serves as a pioneer for the forthcoming generation of digital power converters, as it successfully amalgamates complex control methods into a single control chip. This integrated approach lays the foundation for the development of fully digital power converters in contrast to the relatively constrained capabilities of analog control methods. While digital integration introduces heightened complexity, it concurrently empowers the simultaneous execution of diverse intricate mechanisms and computations, a progression that aligns harmoniously with the evolving trend towards integrated

TABLE 4. Circuit performance comparison between this work and prior arts.

	2022 [28]	2020 [30]	2018 [20]	2021 [26]	2014 [35]	This work
Control	Analog AOT	Analog COT	Analog COT	Digital COT	Digital AFT	Digital AOT
Extra frequency	N/A	N/A	N/A	50MHz	50MHz	50MHz
ADC	N/A	N/A	N/A	✓	✓	×
Input voltage (V)	1.6-2.2	3.3	3.3	12	2	4.2
Output voltage (V)	0.4-1.2	0.6-1.2	1.05	1	1.2	1.2
Inductor(μH) / Capacitor(μF)	0.33/10	1 / 4.7	1 / 4.7	2.2/66	4.7 / 4.7	4.7 / 4.7
Load current (mA)	50-500	0-840	300-1700	0-5000	30-400	100-500
Output voltage offset (mV)	N/A	N/A	4	20	N/A	4
V_{OFS} / V_o (%)	N/A	N/A	0.38	2	N/A	0.33
Switching frequency (MHz)	3	1.5	2.5	0.5	2	1
Δf_s / f_s (%)	N/A	N/A	N/A	N/A	6.5	2.8
Transient circuit	TAL	OTC	PWT	TAL	N/A	DTOC
Peak efficiency (%)	90.1	90.2	94	N/A	91	81.6
Trans_up Settling time (μs)	1.6	0.4	4	10	5	2.5
Trans_up Undershoot (mV)	20	10	75	100	130	50
Trans_dn Settling time (μs)	1.6	3	5	10	5	3
Trans_dn Overshoot (mV)	20	20	90	80	130	68

COT, Constant on-time
AOT, AFT: Adaptive on-time, Adaptive off-time
TAL: transient-acceleration loops
OTC: Time-optimized on-time control
PWT: Pseudowave tracking technique
DTOC: Digital transient-optimized control

Power Management Integrated Circuits (PMICs) in the future.

VII. CONCLUSION

Ripple-based buck converters often encounter issues of varying operating frequencies, system stability, and steady-state errors. Digital circuits exhibit better resilience against chip aging, maintaining their functionality as long as high and low signal levels are accurately determined. This paper has presented an innovative approach by introducing a fully digital constant frequency (DCF) control by adaptive tuning the on-time control with respect to duty cycle adjustments. Moreover, the incorporation of a digital transient-optimized control (DTOC) technique has been demonstrated to effectively reduce transient settling time. The circuit performance validation was implemented by a power stage embedded with an FPGA ADC-SoC development board. Given the load current change from 100 to 500mA, the DCF control showed a remarkable reduction (from 40% to 2.8%) in operating frequency variation. Additionally, the DTOC approach substantially expedited transient responses for both rising and falling load, achieving a 60% reduction compared to the converter without DTOC. This research paves the way for further exploration of digital control strategies to the ripple-based power converters, potentially leading to the totally digital solution to the optimal performance.

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PEI-JUNG YANG received the B.S. degree from National Sun Yat-sen University, Kaohsiung, Taiwan, in 2019, and the M.S. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 2021. Her research interests include DC–DC power converters and power electronics design.

CHUN-HSUN WU received the B.S. degree from the National Taiwan University of Science and Technology, Taipei, Taiwan, in 2003, and the Ph.D. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 2011. He has been a Postdoctorate Consultant with National Cheng Kung University, since 2021. His research interests include fast transient DC–DC converters and power management IC design.

CHE-YEN YEH received the B.S. degree from the National Taiwan University of Science and Technology, Taipei, Taiwan, in 2018, and the M.S. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 2020. His research interests include mixed-signal circuit design and power management IC design.

LE-REN CHANG-CHIEN (Senior Member, IEEE) received the B.S. degree in engineering science from National Cheng Kung University, Tainan, Taiwan, in 1993, the M.S.E.E. degree in electrical engineering from the University of Wisconsin–Madison, Madison, WI, USA, in 1998, and the Ph.D. degree in electrical engineering from Purdue University, West Lafayette, IN, USA, in 2002. He joined the Department of Electrical Engineering, National Cheng Kung University, as an Assistant Professor, in 2003, and became a Full Professor, in 2013. His research interests include power management systems, power electronics, electric machines, and renewable energy applications to power systems.