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RESEARCH ARTICLE

An Ultra-High Gain Compact Module Bidirectional DC–DC Converter for Energy Storage System

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ABSTRACT This paper presents a non-isolated bidirectional dc-to-dc converter (BDDC) topology employing a switched inductor switched capacitor (SISC) module. The bidirectional power flow capability aid to its application mainly in microgrids and electric vehicles. The switched inductor (SI) and switched capacitor (SC) cells in combination assist in the generation of high gain voltage without using a bulky transformer. The theoretical analysis of the proposed converter, its gain calculation, and small signal analysis are analyzed in detail. It benefits from having a wide voltage-gain range and less voltage stress across the power switches. Also, the proposed (SISC-BDDC) can operate both in boost and buck modes. Simulations are carried out for both the modes using MATLAB/Simulink platform. A 200 prototype is also developed to operate with $V_{in} = 12$ V and $V_{out} = 160$-200V. Using the dSPACE1104 control platform, the maximum efficiency of 95.25% of the converter is justified in steady and transient operating conditions.

INDEX TERMS Bidirectional dc-dc converter, hybrid energy sources, switched-capacitor, switched-inductor.

I. INTRODUCTION

Emissions from fossil fuel-consumed vehicles are a major source of pollution for the environment, and these emissions can be classified into air pollutants and greenhouse gas emissions [1], [2], [3]. Renewable-powered vehicles capable of operating with nearly neutral emissions are viewed as one of the solutions to effectively mitigate the energy crisis and climate change. Transportation emissions nowadays cause environmental pollution at an exponential rate [4], [5], [6]. Electric vehicles (EVs) integrating with hybrid energy sources (HES) are acting as important vehicular technology in today's world because of neutral carbon emission, mainly comprised of batteries and supercapacitors with high density to store more amount of energy in less volume. Batteries with low capacity are utilized for keeping the dc bus's high voltage constant even if the power demand has lower fluctuations. Consequently, super capacitor regulates the high-power fluctuations on accelerating or sudden braking of a vehicle by absorbing or supplying the transient power when required. So, the two sources of hybrid energy can help in improving the battery degradation caused by sudden power changes in dc buses and improve the overall system stability [7].

The hybrid energy source voltage level for EVs is relatively low. In order to accompany the gap between the high voltage dc bus and HES, a BDDC with high gain on low duty cycle is necessitated to interface the energy sources and the dc bus, in addition to the bidirectional power flow of energy sources [8]. BDDC converter is categorized into two types of converters firstly isolated DC-DC converter with transformers and secondly non-isolated DC-DC converter

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without transformers. Isolated BDDCs are commonly used in applications that require high power density, and high efficiency ($\%\eta$). The wide voltage-gain range of these converters enables them to operate bidirectionally and efficiently in both modes, making them suitable for nearly neutral carbon-emission based applications [9]. The Fly-back converter, which is a type of isolated BDDC, has a simple structure and is relatively easy to control compared to other bidirectional converters. However, it suffers from a number of drawbacks that limit its $\%\eta$ and performance. One of the main issues with the Fly-back converter is the presence of leakage inductance in the high-frequency transformer, which results in significant energy loss and reduces the efficiency ($\%\eta$) of the converter. Another issue which is observed with the Fly-back converter is that the switches used in this converter have to bear high voltage stress which makes the switches less reliable. To address these issues, alternative bidirectional converter topologies such as forward DC-DC converter, half-bridge, and full-bridge BDDC, and other DC-DC have been developed that offer improved efficiency, reduced voltage stress on power switches, and better overall performance [10]. The formation of various structures like SC, SI, Z-source, and quasi-Z-source BDDC, conventional two-level and multilevel, Sepic/Cuk/Zeta and coupled-inductor converters are examples of non-isolated BDDC or simply a unidirectional converter. In conventional two-level converters, the power switches are stressed at high voltages, the gain (V_{out}/V_{in}) range is narrow, and the power switches' extreme duty cycles limit their $\%\eta$ and response time. Therefore, they are not suitable for the HES, to integrate with electric vehicles. With a three-level DC-DC, the stress caused by the voltage on the switches is significantly reduced, however, the voltage gain is relatively low because of parasitic parameters [11], [12]. The voltage gain (V_{out}/V_{in}) of multilevel BDDC achieves high gain, but their control strategy and other hardware circuits must maintain a balance between the switch's reliability occurring at the time of implementation in real-time [13]. Authors in [14] discussed Cuk/Sepic/Zeta DC-DC converter having a wide gain (V_{out}/V in) range, their cascaded structures limit their conversion $\%\eta$. Using coupled inductors in structure, high gain (V_{out}/V_{in}) can be achieved by adjusting the coupling inductor's turn ratio, but in this type of structure the problem of imperfection due to magnetic link arises which degrades DC-DC converter $\%\eta$, so their structure becomes more complex. The coupled inductor also limits the converter's power conversion capability and more over its overall size becomes bulk because the use of a transformer in the structure and gain starts to saturate at some value of the duty cycle [15]. The family of Z-source BDDC is easy to design and control, and they are also simple to expand. These converters achieve a significant voltage gain (V_{out}/V_{in}) by transferring energy via capacitors during both charge and discharge cycles [16]. Although they sacrifice some power density due to the use of multiple inductors, switched-inductor BDDC also provides a wide range of voltage gains and low voltage stress [17]. In [17], a non-isolated single-capacitor bidirectional converter is proposed. Despite having a wide range of gain (V_{out}/V_{in}), the power switches in the converter experience high voltage stress. A DC-DC converter topology based on an SC cell is proposed in [18], despite an increase in voltage gain and having pulsating input current, the converter uses more switches and the total components count is high which makes the structure bulky in nature and the power density of the converter is low. In [19], an SC- BDDC converter is described. The $\%\eta$ is increased with this converter, but more power switches are required even though the total components count is less. In [20], a hybrid BDDC along with an SC cell which is acceptable for a DC microgrid application is proposed. Although it has a wide gain (V_{out}/V_{in}) range and reduced voltage stress on the power switches, the converter has a non-pulsating input current. Therefore, it has only a few applications. A novel BDDC coupled with an Inductor having enhanced gain (V_{out}/V_{in}) is proposed in [21], [22], [23], [24], [25], [26], and [27]. However, the coupled inductor's leakage inductance and the accompanying dv/dt issues towards the input and output grounds also need to be taken into consideration, as also voltage stress across the power switches that are adjacent to the high voltage (HV) side of the converter is large enough to reduce the overall DC-DC converter performance [28].

This paper describes a novel switched-inductor-switched-capacitor SISC-BDDC for EVs and microgrid-based applications, with HES that has the property of a wide voltage gain (V_{out}/V_{in}) range. The block diagram of SISC-BDDC is shown in Fig.1. The SISC-BDDC can achieve higher gain (V_{out}/V_{in}) with the same number of devices as compared with some recent topologies. Alternatively, way to elaborate, when the SISC-BDDC is compared against the recent topologies in the literature, the suggested SISC-BDDC design employs the least device counts to obtain the same gain (V_{out}/V_{in}) as other topologies. As a result, the SISC-BDDC utilizes switches with low volt rating and less on-state resistance, which is advantageous to the converter, and switches power loss of SISC-BDDC at actual operating conditions and at the laboratory temperature, exhibits low thermal stress on the power switches, which helps the SISC-BDDC to become more reliable is also an advantage of the SISC-BDDC.

The proposed SISC-BDDC topology has been described in Section II. Section III investigates the operational modes of SISC-BDDC. Section IV describes the converter parameter design analysis. Section V presents the comparative study of the SISC-BDDC converter. Section VI presents the linearization study of SISC-BDDC. Section VII investigates the control strategy of the proposed converter. Section VIII elaborates on the extensive simulation carried out to analyze the proposed SISC-BDDC. Section IX elaborates on the experimental findings, and finally, the paper is concluded in Section X.

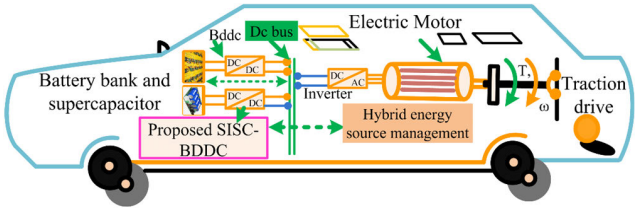


FIGURE 1. Potential application of proposed SISC-BDDC converter.

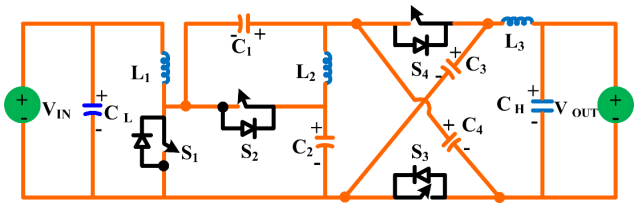


FIGURE 2. Proposed SISC-BDDC topology.

II. PROPOSED SISC-BDDC TOPOLOGY

The basic structure of the proposed SISC (switched inductor and switched capacitor) BDDC is shown in Fig. 2 Which consists of three inductors (L_1, L_2, L_3), four capacitors (C_1, C_2, C_3, C_4) and four (S_1, S_2, S_3, S_4), switches and low and high voltage side filter capacitors C_H (high) and C_L (low) make up the proposed converter. Three switches S_2, S_3, and S_4 have identical gate signals which are complementary to the gate signal of switch S_1. For the SISC -BDDC power flow between the ($V_{in} \leftrightarrow V_{out}$) sides which allows operating the proposed DC converter in boost or buck mode.

III. OPERATION AND ANALYSIS OF PROPOSED SISC- BDDC

A. OPERATIONAL PRINCIPLE OF THE SISC-BDDC

For maintaining simplicity in the analysis of SISC-BDDC, certain assumptions were considered. (1) The components are ideal, neglecting the turn-on resistance of switches (R_{DS}), and total equivalent resistance of all energy-storing components in SISC- BDDC that are inductors L_1, L_2, L_3, and capacitors C_1, C_2, C_3, C_4, C_H, C_L. (2) Linearity at the instant of increase and decrease of inductor currents and voltages of capacitors (3) capacitor voltages are constant. Fig. 3(a) and 3(b) depict typical waveforms of the SISC-BDDC in boost and buck mode for continuous conduction mode of operation (CCM).

1) SISC-BDDC BOOST MODE OPERATION

Energy is transferred from the low voltage side to the high voltage ($V_{in} \rightarrow V_{out}$) side when the SISC-BDDC operates in boost or boost mode. The relationship of switches S_1, S_2, S_3, and S_4 in terms of duty cycle is given by ($d_1 = (1 - d_2) = (1 - d_3) = (1 - d_4) = d_{boost}$.)

Mode 1 [$t_0 - t_1$]**:** During this mode of operation, S_1 is turned on, the switches S_2, S_3, and S_4 are off. V_{in} charges the inductor L_1 through S_1, and the capacitor C_1 transfers its energy to both energy storage elements C_2, and L_2 simultaneously. The capacitors C_3 and C_4 transfer their energy to load

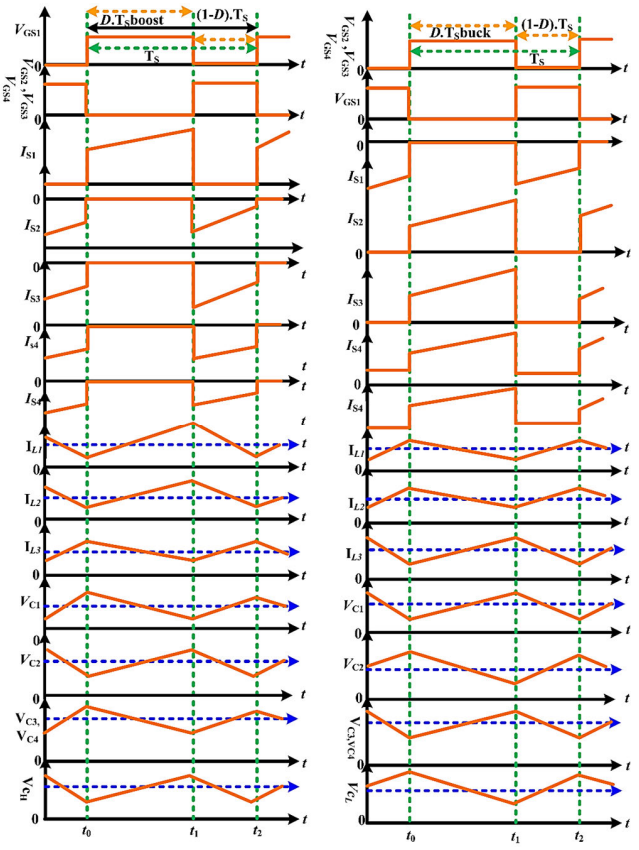


FIGURE 3. SISC-BDDC waveforms in (a) Boost (b) Buck mode of operation.

capacitor C_H. In this operating condition, the current direction paths are shown in Fig. 4(a).

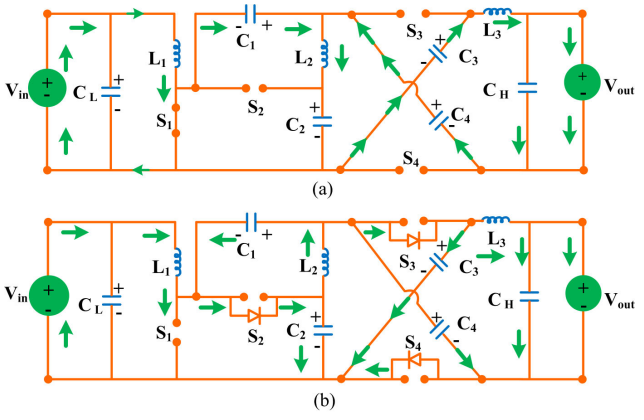


FIGURE 4. SISC-BDDC equivalent circuit during boost mode: (a) t_{on} and (b) t_{off}.

*Mode*2 [$t_1 - t_2$]**:** During this mode of operation, S_1 is turned off, and the antiparallel diodes of switches S_2, S_3, and S_4 are on. (L_1, L_2, C_2), release their energy to capacitor (C_1, C_3, C_4) also C_H is discharge through load. In this condition, the direction current paths in this operating mode are shown in Fig. 4(b).

2) SISC- BDDC BUCK MODE OPERATION

Energy is transferred from the high voltage side to the low voltage ($V_{out} \rightarrow V_{in}$) side when the SISC- BDDC operates in a buck or step-down mode. The relationship between the switches S_1, S_2, S_3, and S_4 in terms of duty cycle is given by ($d_3 = d_2 = d_4 = (1 - d_1) = d_{buck}$).

Mode 1 [t_0− t_1]**:** During this mode of operation, S_1 is turned off, S_2, S_3, and S_4 are on. V_{in} and C_H transfer their energy to (C_3, C_4, L_3) and (L_1, L_2, C_2) release their energy through load. In this condition, the direction current paths in this operating mode are shown in Fig. 5(a).

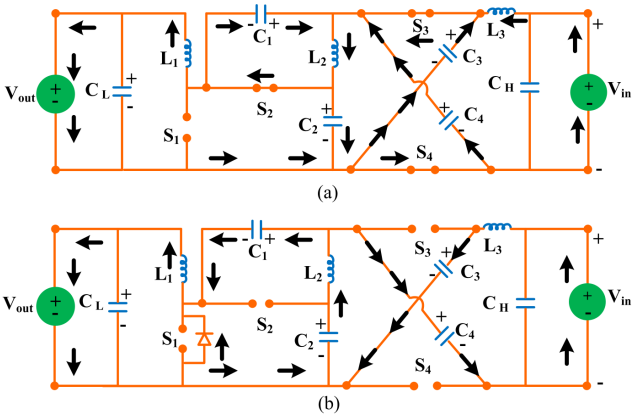


FIGURE 5. SISC-BDDC equivalent circuit during buck mode: (a) t_{on} and (b) t_{off}.

Mode 2 [t_1− t_2]**:** During this mode of operation, the antiparallel diode of switch S_1 is turned on, and the switches S_2, S_3, and S_4 are off. the inductor L_3, C_3, C_4 and C_1 transfer their energy to L_1, L_2, C_2 through load. In this operating condition, the current direction paths are shown in Fig. 5(b).

For deriving the gain (V_{OUT}/V_{IN}) of the SISC-BDDC, the following equation (1), (2), (3), and (4), are equated for both modes of the operations, applying the volt-second balance principle on L_1, L_2, and L_3, which states that the total area of voltage (V_L) across the inductor in a complete switching period must be zero. The voltage gain for the proposed SISB-BDDC in boost and buck operating modes is given in (5).

$$\begin{cases} V_{L1} = VI_N - V_{C2} \\ V_{L2} = V_{C1} = V_{C4} - V_{C2} \\ V_{L3} = -V_{OUT} + V_{C3} \\ V_{C3} = V_{C4} \end{cases} \tag{1}$$

$$\begin{cases} V_{L1} = DV_{IN} + (1 - D) \cdot (V_{IN} - V_{C2}) = 0 \\ DV_{IN} + V_{IN} - V_{C2} - DV_{IN} + DV_{C2} = 0 \\ V_{C2}\,(1 - D) = V_{IN} \\ V_{C2} = \dfrac{V_{IN}}{1 - D} \end{cases} \tag{2}$$

$$\begin{cases} V_{L1} = V_{IN} \\ V_{L2} = V_{C1} - V_{C2} \\ V_{L3} = -V_{OUT} + V_{C4} - V_{L2} - V_{C2} + V_{C3} \end{cases} \tag{3}$$

$$\begin{cases} V_{L2} = D\,(V_{C1} - V_{C2}) + (1 - D)\,(V_{C4} - V_{C2}) = 0 \\ (1 - D)\,V_{C4} = V_{C2} - DV_{C1} = \dfrac{V_{IN}}{1 - D} - \dfrac{V_{IN}.D^2}{1 - D} \\ V_{C4} = \dfrac{V_{IN}\,(1 + D)}{(1 - D)} = V_{C3} \\ V_{L3} = (-V_{OUT} + V_{C4} - V_{C2} + V_{C3}) \\ D + (1 - D)\,(V_{C3} - V_2) = 0 \\ V_{OUT}\,(1 - D) + D = DV_{C4} - DV_{C1} + DV_{C3} \\ + (1 - D)\,V_{C3} \\ V_{OUT} = (1 + D)V_{C4} - DV_{C1} \end{cases} \tag{4}$$

$$\begin{cases} V_{OUT} = \dfrac{V_{IN}\,(1 + D)^2}{1 - D} - \dfrac{D^2.V_{IN}}{1 - D} = \dfrac{1 + 2D}{(1 - D)} V_{IN} \\ \Rightarrow \dfrac{D}{3 - 2D} V_{IN} \end{cases} \tag{5}$$

B. FUNCTIONING OF SISC-BDDC

Fig. 6 shows the proposed SISC-BDDC bidirectional power flow control technique. SISC-BDDC integrates with the high-voltage HV DC bus to low voltage supercapacitor. The control signal (I_{cn}) generated from the proper energy management power flow technique is ignored in the control strategy and may be used to switch between the two operational modes of the converter in the HES.

Taking into consideration, the boosting condition the converter remains in boost condition only when I_{cn} is greater than zero. The close loop controller generates the initial voltage which is indicated as the reference voltage ($V_{ref-Boost}$) and a reference current ($I_{ref-Boost}$) in SISC-BDDC. Here the close-loop control variables are ($V_{ref-Boost}$) and ($I_{ref-Boost}$) coming from the HV dc voltage bus and inductor current. As a result, in boost mode, the pulse width modulation (PWM) generator generates the proper gate pulses for the switches S_1-S_4.

In step-down conditions, if the SISC-BDDC control signal I_{cn} is less than zero, the SISC-BDDC transitioned to function in buck mode. Here close-loop control variables are ($V_{ref-Buck}$) and ($I_{ref-Buck}$), coming from supercapacitor and inductor current. This close loop controller is used to generate four gate pulses for the switches S_1-S_4 through a pulse-width modulation PWM generator. Overall, this control system regulates the output voltage and current of the converter in the buck mode by adjusting the duty cycle of the PWM pulse signals given to the SISC-BDDC switches S_1-S_4.

IV. PARAMETERS DESIGN AND ANALYSIS

A. VOLTAGE STRESS ON SWITCHES

The voltage stress on switches S_1–S_4 of the proposed SISC-BDDC converter is calculated by applying Kirchhoff's voltage (KVL) principal and considering the switches as open, which is shown in Fig. 4(a) and 4(b), where d_{boost} = 1-d_{buck}. And the voltage stress on switches S_1–S_4 are equal in magnitude as obtained in (6) and the magnitude is the same

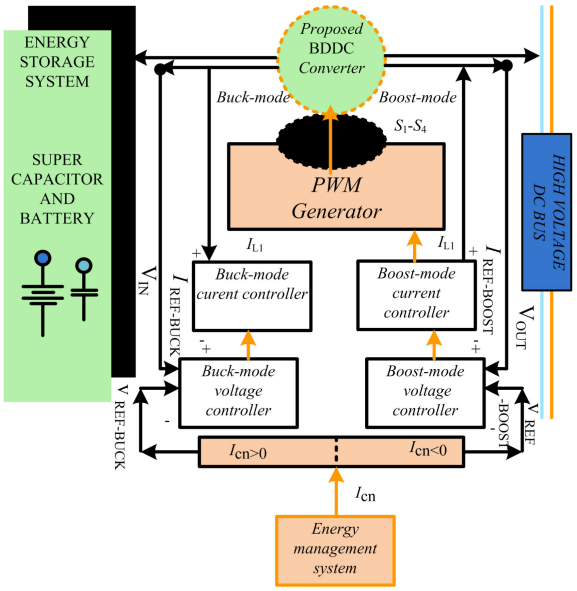


FIGURE 6. Bidirectional power flow control strategy.

in both modes of operation.

$$\begin{cases} S_1 = \dfrac{Vin}{(1-D)} S_2 = \dfrac{Vin}{(1-D)}, \\ S_3 = \dfrac{Vin\,(1+D)}{(1-D)}, \quad S_4 = \dfrac{DV_{IN}}{1-D} \end{cases} \tag{6}$$

B. CURRENT STRESS ON SWITCHES/DIODE

The current stress on switches S_1–S_4 and the antiparallel diode of the proposed SISC-BDDC converter in buck and boost mode is calculated by applying Kirchhoff's current law (KCL) which is shown in Fig. 5(a) and 5(b) and the equation (7) represents the magnitude of current stress in boost mode and equation (8) shows the magnitude current stress in buck condition.

C. INDUCTORS SELECTION

For proper design of the inductor to operate the SISC-BDDC in CCM the value of the inductor is taken greater than the critical value. The L_1, L_2, and L_3 are chosen by assuming the current ripple of less than 10% in the CCM operation, which is depicted in equation (9).

$$\begin{cases} i_{S1} = \dfrac{3}{(1-D)} i_{high}\,, i_{D2} = \dfrac{1}{(1-D)} i_{high} \\ i_{D3} = \dfrac{1}{(1-D)} i_{high}, i_{D4} = \dfrac{1}{(1-D)} i_{high} \end{cases} \tag{7}$$

$$\begin{cases} i_{S2} = \dfrac{1}{(3-2D)} i_{low}\,, i_{S4} = \dfrac{1}{(3-2D)} i_{low} \\ i_{D1} = \dfrac{3}{(3-2D)} i_{low}, i_{S3} = \dfrac{1}{(3-2D)} i_{low} \end{cases} \tag{8}$$

$$\begin{cases} L_{1critical} = \dfrac{D.(1-D)^2 R_{O^{high}}}{(1+2D)^2 2.f} \\ L_{2critical} = \dfrac{D.(1-D).R_{O^{high}}}{(1+2D)2.f} \; L_{3critical} = \dfrac{D^2 R_{O^{high}}}{(1+2D).2.f} \end{cases} \tag{9}$$

D. CAPACITORS SELECTION

For proper design of capacitor for the proposed SISC-BDDC to operate in CCM the value of the inductor is taken to greater than the critical value. The C_1, C_2 C_3, C_4, and C_H are chosen by assuming the current ripple of less than 10% in the CCM operation, which is given in equation (10).

$$\begin{cases} C_{1critical} = \dfrac{(1+2D)}{R_{O^{high}} f} \; C_{2critical} = \dfrac{D.(1+2D)}{R_{O^{high}} D.2.f} \\ C_{4critical} = C_{3critical} = \dfrac{D.(1+D)}{R_{O^{high}}.2.f(1+D)} \\ C_{4critical} = C_{3critical} = \dfrac{D.(1+D)}{R_{O^{high}}.2.f(1+D)} \\ C_{Hcritical} = \dfrac{D}{R_{O^{high}} 8.f^2.L_{3cr}} \; C_{Lcritical} = \dfrac{D}{8.f^2.L_{1cr}} \end{cases} \tag{10}$$

V. COMPARISON ANALYSIS OF SISC-BDDC IN REFERENCE TO OTHER TOPOLOGIES

The SISC-BDDC is compared to the conventional two-level BDDC, the buck-boost BDDC, the conventional three-level BDDC, the quadratic BDDC, the conventional Z-source converter, the conventional quasi-Z-source BDDC, and the conventional BDDC with the presumption of the equal duty cycle (D) and without taking the conduction loss, switching frequency loss and power density in various topologies into comparison, the voltage stress, current stress taken into consideration, shown in Table 1. Table 2 depicts the comparison of proposed SISC-BDDC with the recent literature based on components count, power density, switching frequency, efficiency, common ground, and bidirectional power flow. High switching frequency leads to a decrease in passive volume and the passive integration technique can help to achieve high power density. Based on the SISC-BDDC switching frequency (f_s), mass and volume specification shown in Table 3, the power density of the proposed topology is medium. The proposed topology and topologies reported in [22], [23], and [25] have no common ground which leads to a decrease in converter efficiency because of Electromagnetic interference. The proposed converter has the capability of bidirectional power flow which is not present in other topologies. Its continuous input current aid the benefits of the proposed SISC-BDDC converter, since it has less input current ripple as compared to other topologies [23], [25], [26] in literature.

Fig. 7(a), (b) shows the switch voltage stress versus duty cycle duty cycle (D) varying between (0.2, 0.8) and input voltage of proposed SISC-BDDC and other conventional converters in the two operating modes, the switch voltage stress of any converter is depending on the duty cycle and input voltage as observed from the derived equation of voltage stress. Therefore, from the comparison it is observed that the SISC-BDDC has low voltage stress as compared to other conventional topologies which aids in reducing the conduction losses of converter and also helps improving its efficiency. The proposed SISC-BDDC requires four switches which

TABLE 1. Comparative analysis of SISC-BDDC with respect to different topologies.

Mode	[T]	(Vout/Vin)	[Voltage Stress]	[Switch Current Stress]			
				(S_1)	(S_2)	(S_3)	(S_4)
Boost mode	[P]	$\frac{1+2D}{(1-D)}V_{in}$,	$\frac{V_{in}}{(1-D)},\frac{V_{in}}{(1-D)},\frac{V_{in}(1+D)}{(1-D)},\frac{DV_{in}}{1-D}$	$\frac{2}{1-D_{bst}}I_{out}$	$\frac{1}{1-D_{bst}}I_{out}$	$-\frac{1}{1-D_{bst}}I_{out}$	$\frac{1}{1-D_{bst}}I_{out}$
	[21]	$\frac{1}{(1-d_{bst})}$	$V_{high}/(1-d_{bst})$	$\frac{I_{high}}{(1-d_{bst})}$	$I_{high}/(d_{bst})$	$\frac{I_{high}}{(1+d_{bst})}$	$I_{high}/(1-d_{bst})$
	[22]	$d_{bst}/(1-d_{bst})$	V_{high}/d_{bst}	$\frac{I_{high}d_{bst}}{(1-d_{bst})}$	$\frac{I_{high}d_{bst}}{(2-d_{bst})}$	$\frac{I_{high}}{(1+d_{bst})}$	$\frac{I_{high}}{(1-d_{bst})}$
	[23]	$(2-d_{bst})/(1-d)^2$	$V_{high}/2$	$\frac{2d_{bst}I_o}{(1-d_{bst})^2}$	$\frac{2d_{bst}}{(1-d_{bst})^2}$	$\frac{(2-d_{bst})I_o}{(1-d_{bst})^2}$	$\frac{2d_{bst}I_o}{(1-d_{bst})^2}$
	[24]	$(1/(1-d_{bst})^2$	$(1-d_{bst})V_{high}$	$\frac{I_{high}}{(1-d_{bst})^2}$	$\frac{I_{high}}{(1-d_{bst})}$	$\frac{I_{high}}{(1+d_{bst})}$	$I_{high}/(1-d_{bst})$
	[25]	$(1/(1-2d_{bst}))$	V_{high}	$\frac{2I_{high}d_{bst}}{(1+d_{bst})}$	$-\frac{1}{1-d_{bst}}I_{out}$	$\frac{1}{1-d_{bst}}I_{out}$	$I_{high}/(1-d_{bst})$
	[26]	$(1-d_{bst})/(1-2d_{bst})$	$V_{high}/(2+d_{bst})$	$\frac{I_{high}(1-2d_{bst})}{(1-d_{bst})}$	$\frac{1}{1-d_{bst}}I_{out}$	$I_{high}/(1-2d_{bst})$	$\frac{2}{1-d_{bst}}I_{out}$
	[27]	$(1/(1-d_{bst}))$	$V_{high}/(1-d_{bst})$	$2I_{high}d_{bst}/(1-d_{bst})$	$2I_{high}d_{bst}/(2-d_{bst})$	$I_{high}/(1-d_{bst})$	$I_{high}/(1-2d_{bst})$
	[28]	$\frac{(1+d_{bst})}{(1-d_{bst})}$	$V_{high}/(1+d_{bst})$	$\frac{2I_{high}d_{bst}}{(1-2d_{bst})}$	$\frac{I_{high}}{(1-2d_{bst})}$	$\frac{2I_{high}d_{bst}}{(1-2d_{bst})}$	$\frac{I_{high}}{(1-2d_{bst})}$
Buck mode	[P]	$\frac{(3-2D)}{D}V_{IN}$	$\frac{V_{in}}{(1-D)},\frac{V_{in}D}{(1-D)},\frac{V_{in}}{(1-D)},\frac{DV_{in}}{1-D}$	$-\frac{2}{2-D_{Buk}}I_{in}$	$\frac{1}{1-D_{buk}}I_{out}$	$\frac{1}{1-D_{buk}}I_{out}$	$\frac{1}{1-D_{buk}}I_{out}$
	[21]	$d_{Buk}/(2-d_{Buk})$	V_{high}	$I_{low}/2$	$\frac{(2d_{Buk}-1)}{(d_{Buk}-1)}$	$\frac{1}{1-d_{buk}}I_{out}$	$-\frac{1}{1-d_{bst}}I_{out}$
	[22]	$d_{Buk}/(1-d_{Buk})$	$V_{high}/(1-d_{Buk})$	$\frac{(d_{Buk}+1)i_{low}}{d_{Buk}}$	$-\frac{1}{2-D_{Buk}}I_{in}$	I_{low}	$\frac{(d_{Buk}-1)I_{low}}{d_{Buk}}$
	[23]	$d_{Buk}/(2-d_{Buk})$	$(V_{high}/2)$	I_{low}	$-\frac{1}{2-d_{Buk}}I_{in}$	$-\frac{1}{1-d_{Buk}}I_{in}$	$\frac{(2d_{Buk}-1)I_{low}}{d_{Buk}}$
	[24]	d^2_{Buk}	$d_{Buk}V_{high}$	$I_{low}/(1-d_{Buk})$	$I_{low}/(1-d_{Buk})$	I_{low}	$I_{low}d_{Buk}$
	[25]	$2d_{Buk}-1$	$V_{high}/(1-d_{Buk})$	$2I_{low}$	I_{low}	$I_{low}/(2-d_{Buk})$	$(2d_{Buk}-1)I_{low}/d_{Buk}$
	[26]	$(2d_{Buk}-1/d_{Buk})$	$(1+d_{Buk})V_{high}$	(i_{low})	$i_{low}/(2-d_{Buk})$	$i_{low}/(1-d_{Buk})$	$i_{low}/(2-d_{Buk})$
	[27]	$2d_{Buk}-1$	$V_{high}/2$	$2i_{low}$	$i_{low}(2-d_{Buk})/d_{Buk}$	I_{low}/d_{Buk}	$(2d_{Buk}-1)i_{low}/d_{Buk}$
	[28]	$d_{Buk}/(1-d_{Buk})$	$(2-d_{Buk})/V_{high}$	$i_{low}/(2-d_{Buk})$	$i_{low}/(1-d_{Buk})$	$i_{low}/(2-d_{Buk})$	$I_{low}/(2-d_{Buk})$
d_{bst}=duty cycle in boost mode, d_{buk}=duty cycle in buck mode							

makes its initial cost a little high, however, it experiences less current stress on the switches which is relatively low in magnitude as compared to the conventional two-level DC-DC converter and buck-boost converter [21]. However, it also has extended gain (V_{out}/V_{in}) while operating in boost and buck mode which significantly reduces voltage stress across the switches. The SISC-BDDC uses less number of power switches even, it has to switch voltage under dynamic conditions and current stresses are marginally lower than those of the conventional three-level BDDC [22], additionally, the V_{OUT}/V_{IN} range is enhanced further. The SISC-BDDC overall components cost more than the quadratic converter [23], notwithstanding it uses less number of switches in its complete design. Further, the SISC-BDDC has reduced voltage

TABLE 2. SISC-BDDC comparison with other similar non-isolated topologies [21], [22], [23], [24], [25], [26], [27], [28].

Topology	Number of components	Efficiency	Power Density	Input Current	Common ground	Bidirectional Power flow	*Switching frequency (fs)*
[21]	14	94%	Medium	Continuous	Yes	No	20KHz
[22]	16	93.4%	Medium	Continuous	No	No	20KHz
[23]	22	94%	High	Pulsating	No	No	50KHz
[24]	21	95%	Low	Continuous	No	No	10KHz
[25]	11	95%	High	Pulsating	No	No	50KHz
[26]	12	95%	Low	Pulsating	Yes	No	10KHz
[27]	13	94.9%	Medium	Continuous	Yes	No	20KHz
[28]	15	95%	High	Continuous	No	No	20KHz
[Proposed]	12	95.25%	Medium	Continuous	No	Yes	20KHz

TABLE 3. Proposed SISC-BDDC converter specification.

Parameters	*Specified values*
L_1	1.2mH
L_2	5 *m*H
L_3	6 *m*H
f_s	20 kHz
V_{in}	12-30 V
V_{out}	160-200 V
MOSFETs: S_1- S_4	IXTH 88N30P
C_1, C_2	470 µF
C_4, C_L, C_H	520 µF

and current stress on the switches as compared to the quadratic converter. Despite having a higher gain (V_{out}/V_{in}), the earlier converter is less efficient than SISC-BDDC the because of its cascaded structure. The SISC-BDDC requires the same number of components as the conventional Z source and quasi-Z source BDDC [23] and [24]. The proposed SISC-BDDC has more reliable switches, which can significantly decrease the voltage and current stresses on the switches, but at the expense of a slight reduction in gain (V_{out}/V_{in}). When compared to Z-source BDDC [25], the proposed one requires an additional switch but at the same time eliminates one inductor. Furthermore, the current and voltage stress on the switches of the SISC-BDDC converter is significantly reduced, and it retains the benefit of reliability of switching devices at different operating temperatures. When compared to the BDDC with an SC-cell in [26], the SISC-BDDC has a simple structure, despite having the same number of components, the proposed converter offers reduced voltage and current stresses, along with nearly equal gain at the same D in literature [27], [28]. As shown in Fig. 8, the SISC-BDDC is compared with some recent topologies [17], [18], [20] based on the number of devices count and gain (V_{out}/V_{in}) of components, which clearly shows that the V_{out}/V_{in} of the SISC-BDDC is high.

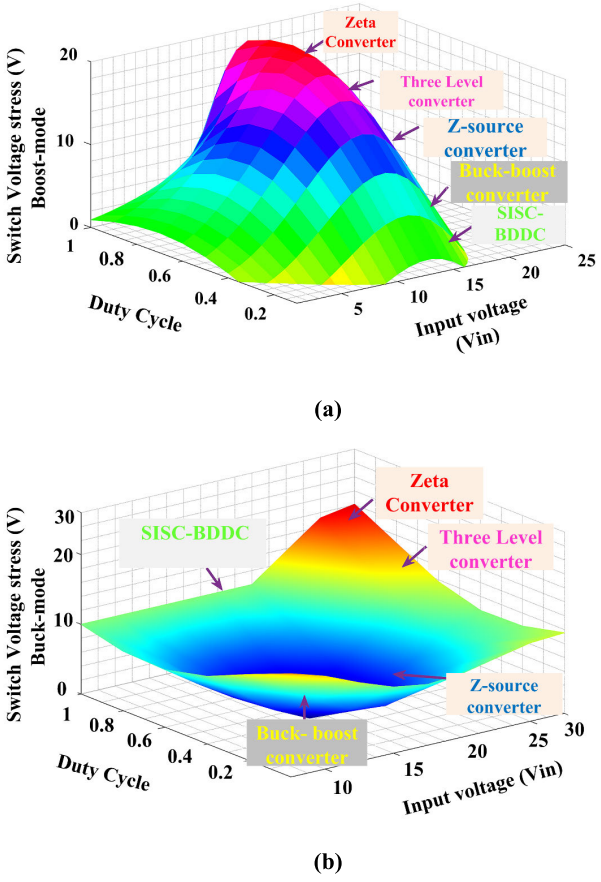


FIGURE 7. Switch voltage stress of SISC-BDDC and other conventional converter versus input voltage and duty cycle (a) boost (b) buck mode of operation.

Equation (11), as shown at the bottom of page 9. Equations (12)–(16), as shown at the bottom of page 10.

VI. SMALL SIGNAL ANALYSIS OF SISC-BDDC

The state-space averaging technique is used to describe the input and output relation of the proposed SISC-BDDC

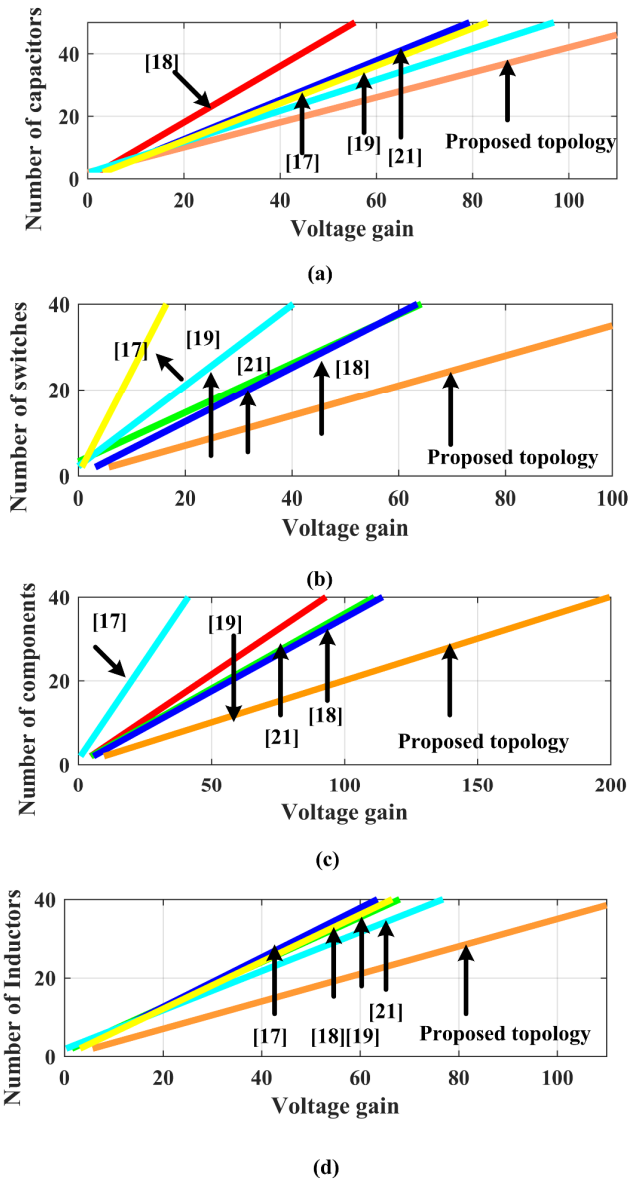


FIGURE 8. Total number of (a) capacitors (b)switches (c) components (d) Inductors in [17], [18], and [20] topologies and SISC-BDDC versus gain M.

converter having different modes of operations, for deriving the state-space analysis of the SISC-BDDC, the ripples content constraints ΔI_L in inductor currents and capacitor voltages ΔV_c are excluded from the analysis.

$$\dot{x} = A_1 x + B_1 u; \quad Y = C_1 x \tag{17}$$

$$\dot{x} = A_2 x + B_2 u; \quad Y = C_2 x \tag{18}$$

where x $=[i_{L1},\ i_{L2},\ i_{L3}, v_{C1},\ v_{C2}, v_{C3}, v_{C4},\ v_{CH}\ ]^T$ in boost mode and x $=[i_{L1},\ i_{L2},\ i_{L3}, v_{C1},\ v_{C2}, v_{C3}, v_{C4},\ v_{CL}\ ]^T$ in buck mode.During buck mode, $V_{out}(t)$ is the source variable and $V_{in}(t)$ is the load variable, and in boost condition $V_{out}(t)$ load variable $V_{in}(t)$ source variable where $i_{L1}(t), i_{L2}(t), i_{L3}(t)$, $V_{C1}(t)$, $V_{C2}(t)$, $V_{C3}(t)$, $V_{C4}(t)$ and $V_{CL}(t)$, $V_{CH}(t)$ are the state variables, r is series resistance of C_H to decrease additional coupling occurring between capacitors C_1, C_2, C_3, C_4 and to eliminate extra state space variables. So, putting the values of various parameters from Table 3 in state space equations (11), (12) the proposed SISC-BDDC converter small-signal transfer functions in boost and buck mode are obtained and the equations are represented in (13) and (14) respectively.

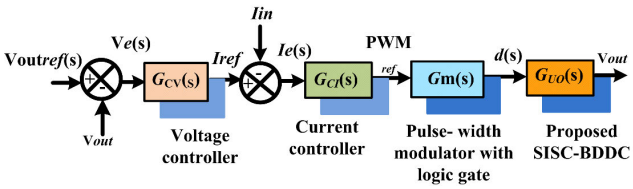


FIGURE 9. Proposed SISC-BDDC control scheme.

VII. CONTROL TECHNIQUE OF PROPOSED SISC-BDDC

The proposed SISC-BDDC converter uses an outer voltage control loop and an inner current control loop, as shown in Fig. 9. Gcv(s) is the proportional-integral (PI) voltage controller transfer function, G_{CI}(s) is the transfer function of the PI current controller. Gm(s) is the transfer function of pulse-width modulator with logic gate. G_{UO}(s) is the voltage transfer function of the proposed SISC converter. For achieving better stability of SISC-BDDC, the tuning of K_p and K_i is done for both voltage and current loop controllers. The frequency plot transfer function with PI voltage controller in boost and buck mode are shown in Fig. 10 and given in equation (12), (16). The basic state-space equations, governing the system modeling in boost and buck modes of operations, for the proposed SISC-BDDC are represented in equations (17), (18). From the two bode plots, in both the mode of operation it is observed that the phase margin and gain margin both are > zero which validates the stability of SISC-BDDC.

VIII. SIMULATION RESULTS

The MATLAB/Simulink platform is utilized for acquiring results of SISC-BDDC for the both operating modes (boost and buck) which is depicted in Fig. 11 and Fig. 12, and it also correlates with the experimental results. The parameters under which the results are obtained for the figures 11 and 12 are given as below. (a) I_{L1}, I_{L2}, I_{L3}, V_C under constant input V_{in} = 20 V, and constant load R =300Ω and (b) V_{in}, V_o, I_o under dynamic input 12-30 V and load constant R = 300 Ω (c) V_{in}, V_o, I_o under constant input V_{in} =12V and load varying 300Ω-500 Ω.

IX. EXPERIMENTAL ANALYSIS OF SISC-BDDC

The effectiveness of the 200W SISC-BDDC is validated through a prototype as shown in Fig. 13. The various parameter values used in the experimental prototype are listed

in Table 3. The experimental prototype was developed using a dSPACE 1104 controller with power PC and C/C+ compiler ver.38.61, with 33MHz/32-bit 5 V PCI slots. A TLP250 optocoupler-based gate driver circuit is used for amplification of the pulses to drive the switches. A lead acid battery with a capacity of 20 Ah is used in the prototype, the voltage and current ratings are 12 V, 6 A, respectively with a dimension of 185∗165∗75mm. A combination of CAP-X supercapacitors GY12R718960V107R with a capacity 100μF. For observation and storage of hardware results, a 4-channel digital storage oscilloscope with a manufacturing number DSOX1204A, with bandwidth 250Mhz, sampling rate 2Ga/s, and mouser number 372-DSOX1204A-70-WW is utilized.

$$
\left\{
\begin{bmatrix}
\frac{d\hat{i}_{L_1}(t)}{dt} \\ \frac{d\hat{i}_{L_2}(t)}{dt} \\ \frac{d\hat{i}_{L_3}(t)}{dt} \\ \frac{d\hat{v}_{C_1}(t)}{dt} \\ \frac{d\hat{v}_{C_2}(t)}{dt} \\ \frac{d\hat{v}_{C_3}(t)}{dt} \\ \frac{d\hat{v}_{C_4}(t)}{dt} \\ \frac{d\hat{v}_{C_H}(t)}{dt}
\end{bmatrix}
=
\begin{bmatrix}
0 & 0 & -\frac{1}{L_1} & 0 & 0 & 0 & 0 & 0 \\
0 & -\frac{r}{L_2} & \frac{1}{L_2} & -\frac{1}{L_2} & \frac{1}{L_2} & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & \frac{1}{L_3} & 0 & 0 \\
0 & -\frac{1}{C} & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & \frac{1}{C} & -\frac{1}{(C\times r)} & -\frac{1}{(C\times r)} & \frac{1}{(C\times r)} & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & \frac{1}{C\times r} & \frac{1}{(C\times r)} & \frac{-1}{(C\times r)} & (\frac{1}{(C\times r+C\times R)}+\frac{1}{(C\times r)}) \\
0 & 0 & 0 & 0 & \frac{1}{(C\times r+C\times R)} & \frac{1}{Cr} & \frac{1}{(C\times r)} & 0 \\
0 & 0 & \frac{-1}{(C\times r)} & 0 & \frac{-1}{(C\times r)} & \frac{1}{(C\times r)} & \frac{-1}{(C\times r)} & 0
\end{bmatrix}
\begin{bmatrix}
\hat{i}_{L_1}(t) \\ \hat{i}_{L_2}(t) \\ \hat{i}_{L_3}(t) \\ \hat{v}_{C_1}(t) \\ \hat{v}_{C_2}(t) \\ \hat{v}_{C_3}(t) \\ \hat{v}_{C_4}(t) \\ \hat{v}_{C_H}(t)
\end{bmatrix}
+
\begin{bmatrix}
\frac{1}{L_1} \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0
\end{bmatrix}
\hat{V}_L(t) +
\right.
$$

$$
\left.
\begin{bmatrix}
0 & 0 & \frac{1}{L_1} & 0 & 0 & 0 & 0 & 0 \\
0 & -\frac{r}{L_2} & 0 & -\frac{1}{L_2} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & -\frac{1}{L_3} & 0 & 0 & 0 & 0 \\
-\frac{1}{C} & 0 & 0 & 0 & 0 & 0 & \frac{1}{C} & 0 \\
0 & -\frac{1}{C} & -\frac{1}{C} & (\frac{1}{C\times r}+\frac{1}{C\times R}) & 0 & (\frac{1}{C\times r}+\frac{1}{C\times r}) & -\frac{1}{(C\times r)} & 0 \\
0 & 0 & 0 & 0 & (\frac{1}{C\times r}+\frac{1}{C\times R}) & (\frac{1}{C\times r}+\frac{1}{C\times r}) & 0 & -\frac{1}{(C\times r)} \\
0 & 0 & 0 & \frac{-1}{(C\times r)} & \frac{-1}{(C\times r)} & 0 & \frac{-1}{(C\times r+C\times R)} & \frac{1}{(C\times r)} \\
0 & 0 & \frac{-1}{(C\times r)} & 0 & 0 & \frac{-1}{(C\times r)} & \frac{-1}{(C\times r+C\times R)} & \frac{1}{(C\times r)}
\end{bmatrix}
\begin{bmatrix}
i_{L_1} \\ i_{L_2} \\ i_{L_3} \\ vc_1 \\ vc_2 \\ vc_3 \\ vc_4 \\ v_{C_H}
\end{bmatrix}
\times \hat{d}_H
\right\}
\tag{11}
$$

A. EXPERIMENTAL RESULTS OF SISC-BDDC IN BOOST CONDITION

Fig. 14 (a) to (e) depicts the operation of SISC-BDDC in boost mode. It is observed that the voltage stress of 100 V is appeared across the switches S_1, S_2, S_3, and S_4 as shown in Fig. 14(a) and (b). This voltage stress of 100V is slightly higher than half of the higher side voltage V_{out}. The current ripple in the inductors L_1, L_2, and L_3 are 25%, 20% and 15%, respectively as shown in Fig. 14(c). The ripple content meets the inductors' design constraints because of low average value of inductor current. The dynamic behavior of the output voltage is illustrated in Fig. 14(d). In boost mode when V_{in} is varying from 30 V to 12 V due of sudden discharge of energy, then fall of terminal voltage is observed which shows that the SISC-BDDC has a high ($V_{\text{out}}/V_{\text{in}}$) range. It can be observed that the SISC-BDDC operates in boost mode with a closed-loop controller, and the output voltage is maintained at nearly 160V when the output power P_{o} is changed

$$\left\{\begin{bmatrix} \frac{d\hat{i}_{L_1}(t)}{dt} \\ \frac{d\hat{i}_{L_2}(t)}{dt} \\ \frac{d\hat{i}_{L_3}(t)}{dt} \\ \frac{d\hat{v}_{C_1}(t)}{dt} \\ \frac{d\hat{v}_{C_2}(t)}{dt} \\ \frac{d\hat{v}_{C_3}(t)}{dt} \\ \frac{d\hat{v}_{C_4}(t)}{dt} \\ \frac{d\hat{v}_{C_L}(t)}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -\frac{1}{L_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{r}{L_2} & \frac{1}{L_2} & -\frac{1}{L_2} & \frac{1}{L_2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{L_3} & 0 & 0 \\ \frac{-1}{C} & \frac{-1}{C} & \frac{-1}{(C\times r)} & 0 & \frac{-1}{(C\times r)} & \frac{1}{(C\times r)} & 0 & 0 \\ 0 & \frac{1}{C} & -\frac{1}{(C\times r)} & 0 & -\frac{1}{(C\times r)} & 0 & 0 & 0 \\ 0 & \frac{1}{C} & \frac{1}{(C\times r)} & \frac{1}{(C\times r)} & \frac{-1}{(C\times r)} & \frac{1}{(C\times r)} & 0 & 0 \\ 0 & \frac{1}{C} & -\frac{1}{(C\times r)} & 0 & -\frac{1}{(C\times r)} & 0 & \frac{1}{C} & 0 \\ 0 & \frac{1}{C} & 0 & \frac{1}{(C\times r)} & \frac{-1}{(C\times r)} & -\frac{1}{(C\times r)} & 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{i}_{L_1}(t) \\ \hat{i}_{L_2}(t) \\ \hat{i}_{L_3}(t) \\ \hat{v}_{C_1}(t) \\ \hat{v}_{C_2}(t) \\ \hat{v}_{C_3}(t) \\ \hat{v}_{C_4}(t) \\ \hat{v}_{C_L}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \frac{1}{L_3} \\ 0 \\ \frac{1}{C\times r} \\ 0 \\ \frac{1}{C\times r} \\ 0 \end{bmatrix} \hat{V}_H + \begin{bmatrix} 0 & 0 & \frac{1}{L_1} & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{r}{L_2} & 0 & -\frac{1}{L_2} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L_3} & 0 & 0 & -\frac{1}{L_3} & 0 \\ -\frac{1}{C} & 0 & 0 & 0 & 0 & \frac{1}{C} & 0 & 0 \\ 0 & -\frac{1}{C} & -\frac{1}{C} & (\frac{1}{C\times r}+\frac{1}{C\times R}) & 0 & 0 & (\frac{1}{C\times r}+\frac{1}{C\times r}) & 0 \\ 0 & 0 & 0 & 0 & (\frac{1}{C\times r}+\frac{1}{C\times R}) & (\frac{1}{C\times r}+\frac{1}{C\times r}) & 0 & -\frac{1}{(C\times r)} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & (\frac{1}{C\times r}+\frac{1}{C\times r}) & (\frac{1}{C\times r}+\frac{1}{C\times R}) & (\frac{1}{C\times r}+\frac{1}{C\times r}) & (\frac{1}{C\times r}+\frac{1}{C\times r}) & -\frac{1}{(C\times r)} \end{bmatrix} \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ i_{L_3} \\ vc_1 \\ vc_2 \\ vc_3 \\ vc_4 \\ vc_L \end{bmatrix} \times \hat{d}_L \right\} \tag{12}$$

$$\begin{cases} G_{oV_H boost}(s) = \dfrac{\hat{V}_H}{\hat{d}_H} = \dfrac{-2.7\times10^4\times s^7 - 2.73\times10^8\times s^6 - 4\times10^{12}\times s^5 + 1.5\times10^{14}\times s^4 - 43.74\times10^{18}\times s^3 + 1.31\times10^{21}s^2 - 4.51\times10^{18}\times s + 2.4\times10^{24}}{s^8 + 2.73\times10^4\times s^7 + 5.40\times10^6\times s^6 + 1.5\times10^{10}\times s^5 - 7.74\times10^{12}\times s^4 + 9.53\times10^{21}s^3 - 4.51\times10^{18}\times s^2 + 4.9\times10^{24}\times s + 5.92\times10^{20}} & (13) \\ G_{oV_L buck}(s) = \dfrac{\hat{V}_L}{\hat{d}_L} = \dfrac{1.1\times10^8\times s^6 - 2.73\times10^8\times s^5 - 4\times10^{12}\times s^4 + 1.5\times10^{14}\times s^3 - 43.74\times10^{18}\times s^2 + 1.31\times10^{21}s^1 - 2.4\times10^{18}}{s^8 + 7.11\times10^4\times s^7 + 9.92\times10^6\times s^6 + 5.03\times10^{10}\times s^5 - .4.38\times10^{12}\times s^4 + 1.12\times10^{21}s^3 - 4.51\times10^{18}\times s^2 + 4.9\times10^{24}\times s + 7.60\times10^{20}} & (14) \end{cases}$$

$$\begin{cases} G_{oboost}(s) = G_C(s)\,Gm(s)\,G_{V_H oboost}(s)\,H(s) \\ G_{oV_{OUT}boost}(s) = \dfrac{\hat{V}_{OUT}}{\hat{d}_H} = \dfrac{-2.7\times10^4\times s^7 - 2.73\times10^8\times s^6 - 4\times10^{12}\times s^5 + 1.5\times10^{14}\times s^4 - 43.74\times10^{18}\times s^3 + 1.31\times10^{21}s^2 - 4.51\times10^{18}\times s + 2.4\times10^{24}}{s^8 + 2.73\times10^4\times s^7 + 4.30\times10^6\times s^6 + 1.5\times10^{10}\times s^5 - 7.74\times10^{12}\times s^4 + 9.53\times10^{21}s^3 - 4.51\times10^{18}\times s^2 + 4.9\times10^{24}\times s + 5.92\times10^{20}} \end{cases} \tag{15}$$

$$\begin{cases} G_{obuck}(s) = G_C(s)\,Gm(s)\,G_{V_L buck}(s)\,H(s) \\ G_{oV_L buck}(s) = \dfrac{\hat{V}_L}{\hat{d}_L} = \dfrac{1.1\times10^8\times s^6 - 2.73\times10^8\times s^5 - 4\times10^{12}\times s^4 + 1.5\times10^{14}\times s^3 - 43.74\times10^{18}\times s^2 + 1.31\times10^{21}s^1 - 2.4\times10^{18}}{s^8 + 7.11\times10^4\times s^7 + 5.65\times10^6\times s^6 + 1.2\times10^{10}\times s^5 - .4.38\times10^{12}\times s^4 + 1.12\times10^{21}s^3 - 4.51\times10^{18}\times s^2 + 4.9\times10^{24}\times s + 7.60\times10^{20}} \end{cases} \tag{16}$$

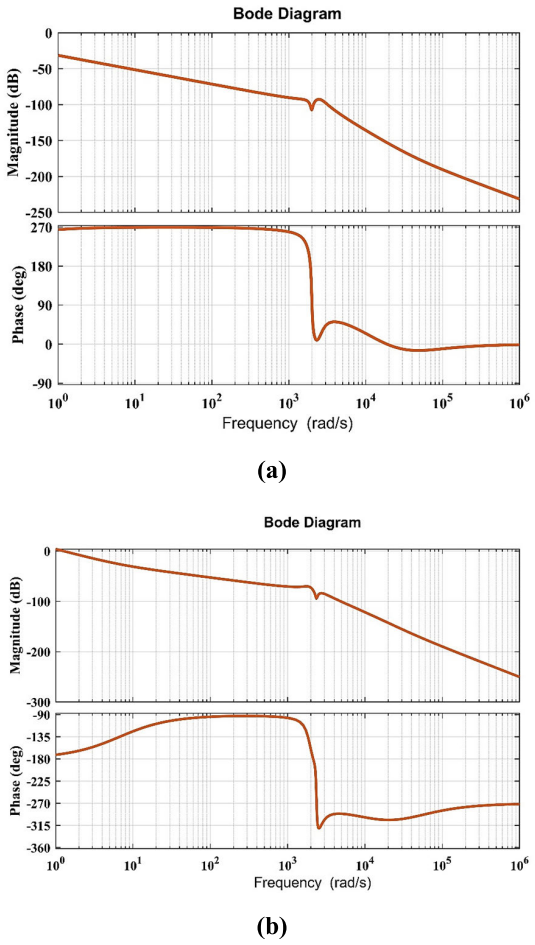


FIGURE 10. Frequency responses of the SISC-BDDC (a) Boost mode (b) Buck mode.

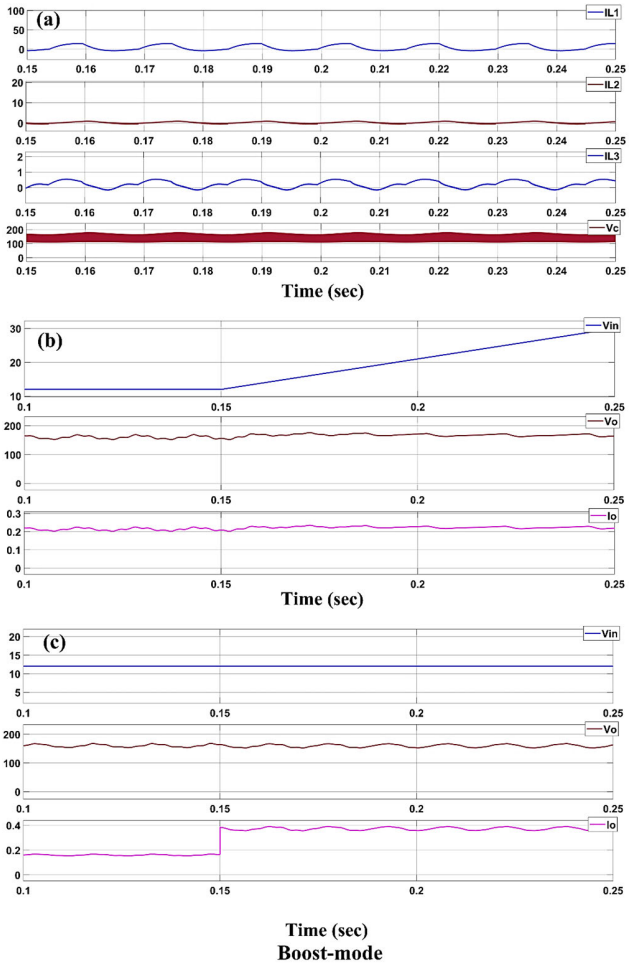


FIGURE 11. Boost-mode simulation results under (a) (I_{L1}, I_{L2}, I_{L3}, V_C) constant input (V_{in}), and constant load and (b) (V_{in}, V_o, I_o) under dynamic input and load (c) (V_{in}, V_o, I_o) under constant input (V_{in}) and load varying.

from 150 to 300W, which is depicted in Fig. 14(e) with small transient voltage fluctuations are ignored in this operating condition.

B. EXPERIMENTAL RESULTS OF SISC-BDDC IN BUCK CONDITION

Fig. 14 (f) to (k) depicts the operation of SISC-BDDC in buck mode. For the four switches S_1, S_2, S_3, and S_4, the voltage stress of 100V is shown in Fig. 14(f) and (g). This voltage stress is slightly more than half the value of the higher side voltage V_{high}, and this matches the theoretical calculation at rated condition. The current ripple of L_1, L_2, and L_3 are 25.67%,16%,15% as shown in Fig. 14 (h), and their ripple content meet the inductors' design constraints because of low average value of inductor current. Fig. 14 (i) shows the output voltage behavior of SISC-BDDC under dynamic condition when it is tested to change from 160V to 100V while the input voltage V_{in} is maintained at 12V. This experimental finding is used to simulate how the energy rises continuously at the source side in charging conditions, and the terminal voltage starts to rise. When the V_{in} of SISC-BDDC remains at 12V, the V_{out} rises from 100V to 160V in 10 seconds, allowing the SISC-BDDC to operate in the buck mode, which indicates a high gain ($V_{\text{out}}/V_{\text{in}}$) of SISC-BDDC in buck mode. When the power available at the load (P_{o}) is slightly step-changing between 160W and 250W, the corresponding output voltage and load current are shown in Fig. 14 (j). It is observed that when the SISC-BDDC operates in buck mode with a closed-loop controller, the input voltage V_{in} can be maintained approximately at 30V, and the voltage fluctuations are slightly small so that it can be omitted.

C. BIDIRECTIONAL EXPERIMENTAL RESULTS OF SISC-BDDC AND THERMAL LOSS DESCRIPTION OF SWITCHES

The hybrid energy sources on integrated with SISC-BDDC which incorporates the two sources battery and supercapacitor into a vehicle. The supercapacitor provides the required dc bus power when the vehicle is accelerating through the proposed SISC-BDDC because of its quick dynamic response characteristics. During the braking process, the regenerative energy absorbs in control way through the battery and supercapacitor through BDDC converters. In uniform

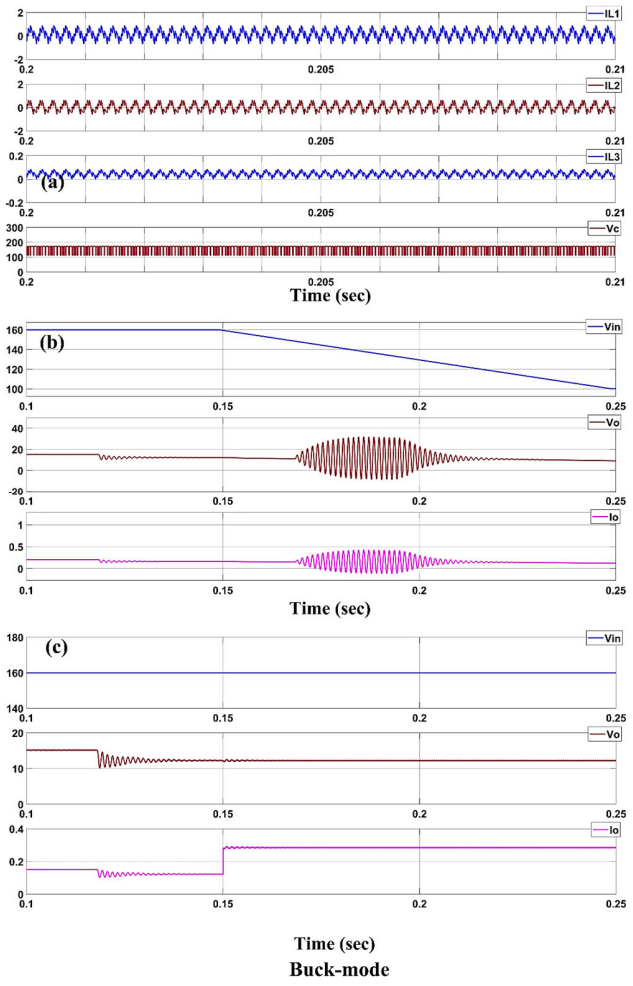


FIGURE 12. Buck-mode simulation results under (a) (I_{L1}, I_{L2}, I_{L3}, V_C) constant input (V_{in}), and constant load and (b) (V_{in}, V_o, I_o) under dynamic input and load (c) (V_{in}, V_o, I_o) under constant input (V_{in}) and load varying.

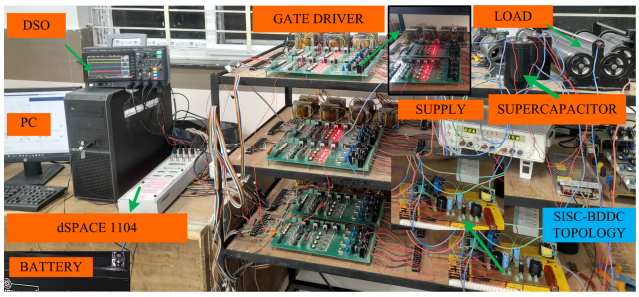


FIGURE 13. Experimental prototype of the proposed topology.

running condition, the battery provides the constant energy for DC bus with the help of BDDC and charges the supercapacitor through proposed SISC-BDDC if required. Fig. 14 (k) illustrates bidirectional results of SISC-BDDC, super capacitor current I_{sc} and the battery currents I_{bat}. It can be observed that when HVDC bus demand of power is rapidly adjusted from 300W to 550W, the I_{cn} generated is greater than zero by the hybrid energy sources. Accordingly, the designed SISC-BDDC responds quickly to operate in boost mode. The super capacitor current I_{sc} increases suddenly from zero to 5 A in about 20 microseconds, in this stage super capacitor supplies the required instantaneous current I_{sc} for the HV dc bus, while the battery output current I_{bat} increases relatively slowly which is shown in the experimental result. The battery powers the dc bus with static power when I_{sc} decreases from 5 A to 0 A and I_{bat} gradually increases from 8.8 to 13 A. Similarly, the control signal I_{cn} is smaller than 0 when the dc bus power demand is abruptly dropped from 650 to 350W, SISC-BDDC reacts quickly and works in buck mode at the same time.

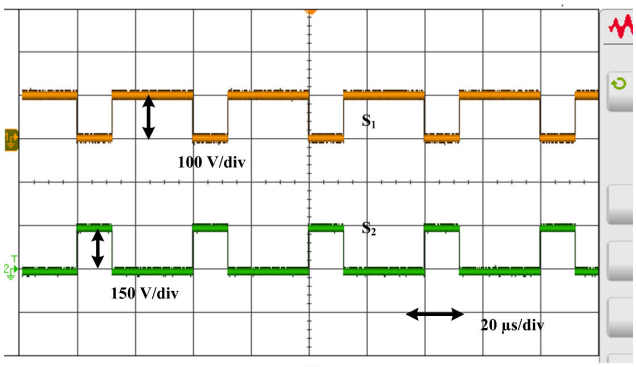
The supercapacitor absorbs the (HV) dc bus sudden decrement in power and the current I_{sc} rises from 0 to -4 A over the period of about 20 ms. The current I_{bat} steadily decreases from 13 to 8.8A and when the current I_{sc} drops to 0 from −5 A, and accordingly, the battery gradually absorbs the instant power from the HV DC bus.

The average switching loss and average conduction loss of MOSFET switches are calculated for the proposed converter to examine the reliability of switches.

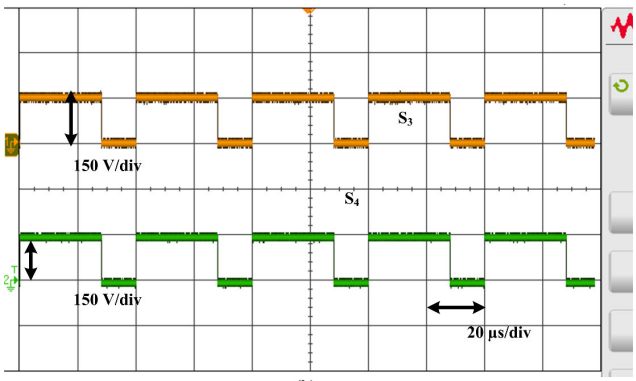
The device manufacturer's data in the data sheet is imported to the PLECS software using the import wizard of the thermal file's description tool. Fig. 14 (l) depicts the turn on switching Energy Loss as a function of the device's ambient temperature in a 3D look-up table, whereas Fig. 14 (m) depicts the turn-off switching Energy Loss.

D. PROPOSED SISC- BDDC EFFICIENCY AND POWER LOSS ANALYSIS

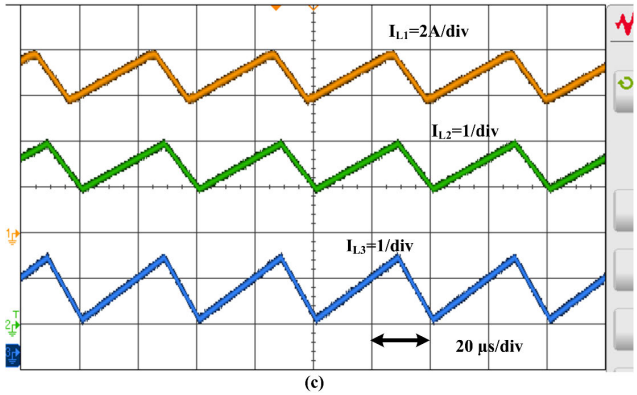
Fig. 15 shows the experimental efficiency of the proposed SISC-BDDC with output power. The efficiency is calculated using a power analyzer (Fluke 125B). Fig. 15 shows that the SISC-BDDC achieves a maximum efficiency of 95.25% and a minimum $\%\eta$ of 92.25% in the boost mode, while it achieves a maximum efficiency of 95.24% and a minimum $\%\eta$ of 87.31% in the buck mode of operation. The $\%\eta$ of SISC-BDDC is steadily increases with increasing input voltage for the same output power, as shown in the graph. The maximum theoretical efficiencies of proposed SISC-BDDC are compared to those achieved by other converters in the literature [17], [18] which shows that the proposed SISC-BDDC having leading efficiency as compared to others in the comparison which is shown in Fig. 16. This is due to the reduced losses resulting from the low input current. Fig. 17 depicts the theoretical efficiency curve and experimental curve of the proposed converter. A minor difference in the experimental curve is observed due to the presence of parasitic in passive components of the proposed designed converter. The sum of total losses of SISC-BDDC in buck mode is 10.25 W, as confirmed by Fig. 18(a), while the sum of power loss in buck mode is 11.06 W, as confirmed by the breakdown loss distribution curve in Fig. 18(b).



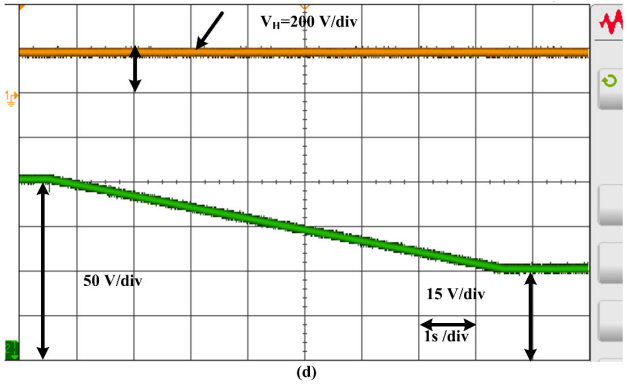
(a)



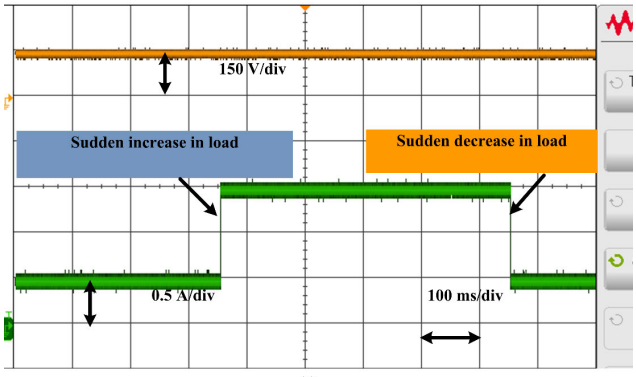
(b)



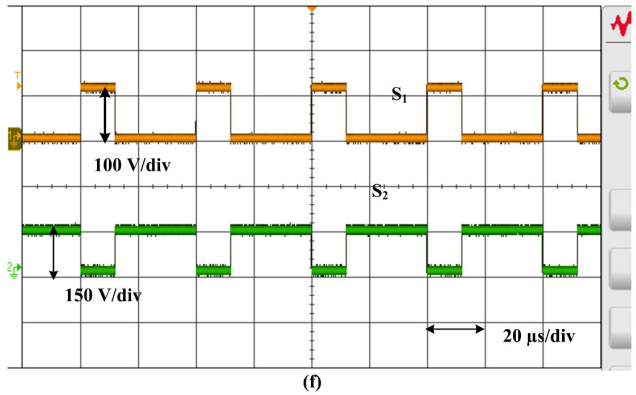
(c)



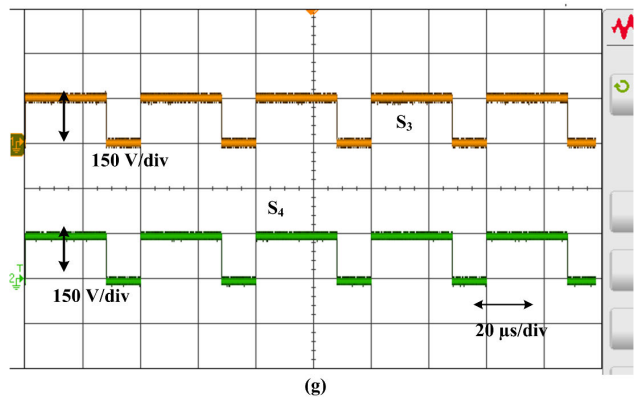
(d)



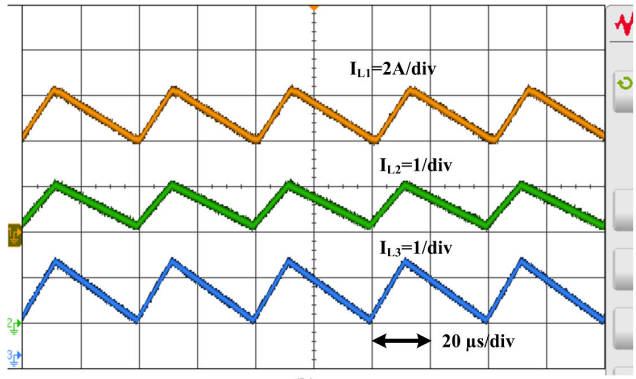
(e)



(f)



(g)



(h)

FIGURE 14. Hardware results of boost mode from (a)-(e) and buck mode from (f)-(k). Thermal loss of the MOSFET (l) turn-on power loss (m) turn-off power loss.

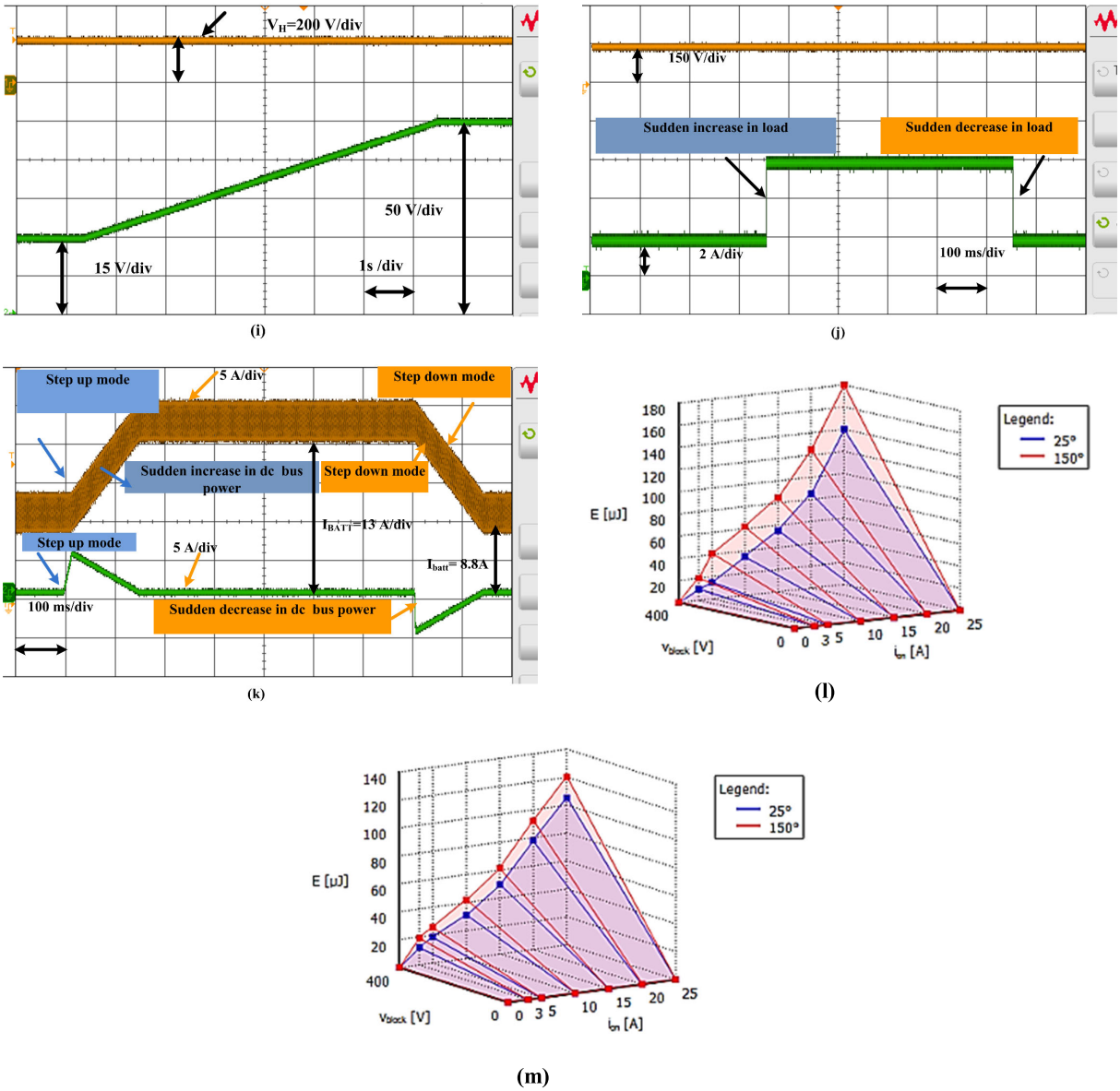


FIGURE 14. *(Continued.)* **Hardware results of boost mode from (a)-(e) and buck mode from (f)-(k). Thermal loss of the MOSFET (l) turn-on power loss (m) turn-off power loss.**

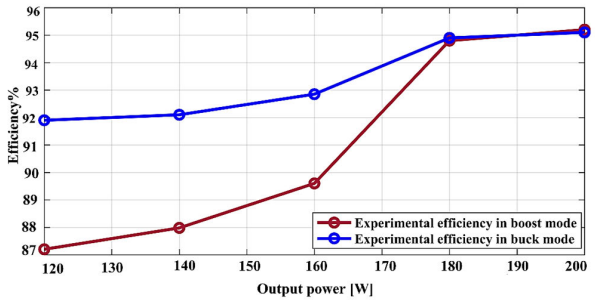


FIGURE 15. **SISC-BDDC efficiency curve in boost and buck mode.**

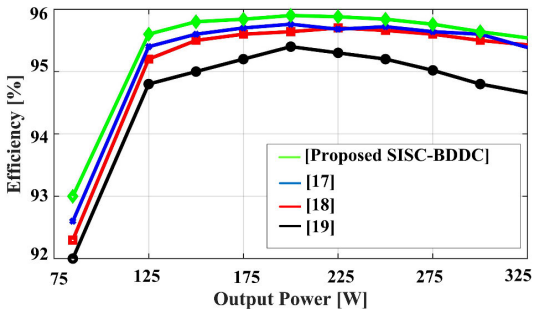


FIGURE 16. **Theoretical efficiency comparison of SISC-BDDC and topologies in [17] and [18].**

The efficiency can be clearly validated by the two pie-chart curves in Fig. 18. It is concluded that most of the loss that occurs in the converter is because of the switches in SISC-BDDC.

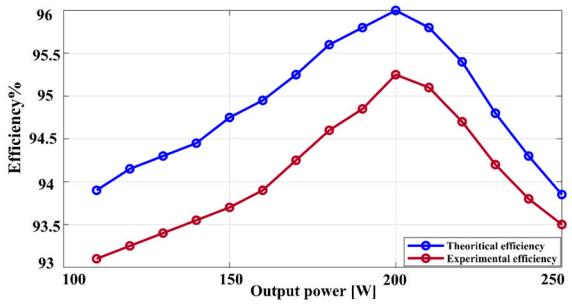
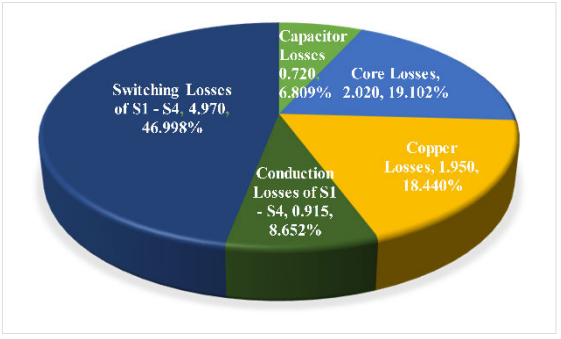
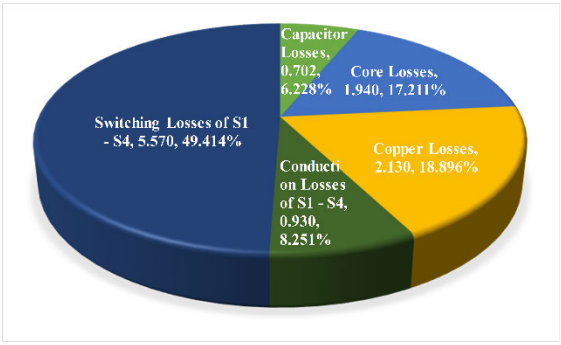


FIGURE 17. Theoretical and experimental efficiency curve versus output power of SISC-BDDC.



(a)



(b)

FIGURE 18. Loss distribution curve of SISC-BDDC in (a) boost (b) buck-mode.

X. CONCLUSION

A novel non-isolated SISC-BDDC has been proposed in this work. The SISC-BDDC has a broad voltage-gain range in boost and buck modes, simple in design, compact owing to only four active power switches. Theoretical aspects of the proposed converter, including its operating mode analysis and small signal models, have been derived thoroughly. The controller design technique, small signal modelling for validating the converters stability has been discussed. Following that, both the simulation and experimental findings have been presented under various operating condition to verify the theoretical analysis. The maximum efficiency of 95.25% is achieved for the SISC-BDDC at 200W output power. Loss calculations are performed in on and off condition at changing temperature to examine the reliability of the switches. Lower voltage stress and current stress across the switches has been verified from comparison with other similar topologies. Good dynamic performance of the SISC-BDDC justifies that it can be a suitable alternative in microgrids, electric vehicles and renewable energy applications.

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