IEEE Access
Multidisciplinary ⋮ Rapid Review ⋮ Open Access Journal

Received 1 October 2023, accepted 16 November 2023, date of publication 20 November 2023,
date of current version 29 November 2023.

Digital Object Identifier 10.1109/ACCESS.2023.3335044

RESEARCH ARTICLE

A ±0.48°C (3σ) Inaccuracy BJT-Based Temperature Sensor With 241 μs Conversion Time for Display Driver IC in 40 nm CMOS

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This work was supported in part by the Ministry of Science and ICT (MSIT), South Korea, under the Information Technology Research Center (ITRC) Support Program, supervised by the Institute for Information and Communications Technology Planning and Evaluation (IITP), under Grant IITP-2021-0-02052; and in part by the National Research Foundation of Korea (NRF), funded by the Korean Government (MSIT) under Grant 2023R1A2C1006578 and Grant 2020M3H2A1076786.

ABSTRACT This paper describes a fast BJT-based temperature sensor with ±0.48°C inaccuracy embedded in a display driver integrated circuit (DDIC) for detecting the temperature of a display module. It utilizes the base-emitter voltage difference between two BJT elements in a bandgap reference (BGR) circuit to create a voltage proportional to the absolute temperature, which is then converted to a digital value through an analog-to-digital converter (ADC). The voltage varies proportionally with the temperature change obtained from the temperature sensor and is directly digitized without removing the offset errors from the analog circuit stage. The error is mitigated through a proposed digital correction method. The proposed on-chip temperature sensing circuit for sophisticated DDIC applications shows an inaccuracy of ±0.48°C and a resolution of 0.25°C by applying a digital compensation method including thermal resistance calibration considering an operation mode of a display. The conversion time of the temperature to digital converter is only 241 μs. The prototype dissipates only 129.17 μW and achieves high energy-efficiency of 31.1 nJ/conversion.

INDEX TERMS Temperature sensor, display driver integrated circuit (DDIC), analog-to-digital converter (ADC), digital compensation, high energy-efficiency.

I. INTRODUCTION

Temperature sensors are widely used in our daily lives. In healthcare applications, temperature sensors are utilized to quickly check body temperature by measuring the temperature inside the ear or the temperature on the wrist [1], [2]. Temperature sensors for automotive are used to check the temperature of an engine and detect overheating conditions to prevent abnormal failures [3]. In the field of electronics, temperature sensors are used to measure the temperature of chips to determine their lifetime or change their behavior to ensure stable operation [4], [5].

In this paper, a temperature sensor is embedded in a display driver integrated circuit (DDIC) to detect the temperature of a chip and display module to prevent image quality degradation and extend the life of the panel. To achieve the temperature information between frames, a fast read-out characteristic is required in display applications. The performance degradation of a display module is predictable based on the performance index of the display module according to the temperature change. Using temperature information, the brightness of the screen can be adjusted accordingly, or the driving voltage of the display can be changed to prepare for a decrease in lifespan and performance degradation of the display panel [6].

To design a highly energy-efficient on-chip temperature sensor, it is important not only to develop advanced process [7], [8], but understand which elements in the CMOS process have values that change with temperature. In the case of MOSFETs, both the mobility and threshold voltage change

The associate editor coordinating the review of this manuscript and approving it for publication was Kuan Chee.

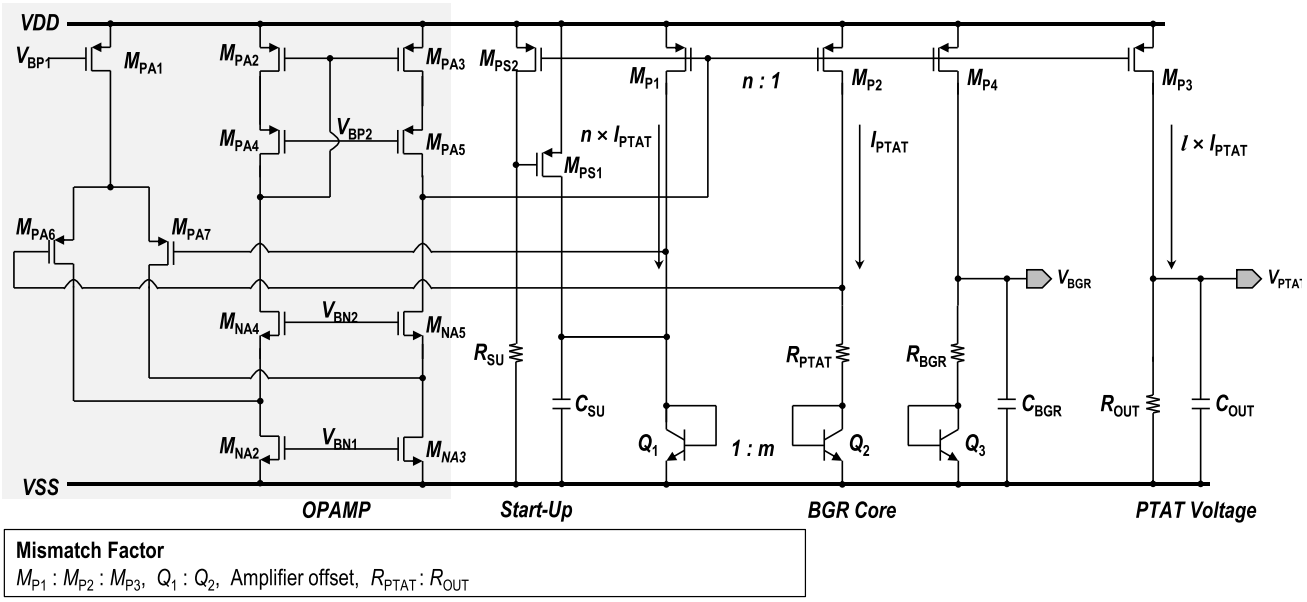

FIGURE 1. Temperature sensing circuit (V_{PTAT} generator) based on the BGR circuit.

with temperature. The drain current of a MOSFET varies with the square of the temperature, making temperature circuit design difficult due to the characteristics of MOSFETs. In the case of BJTs, however, the difference between two base-emitter voltages, ΔV_{BE}, changes linearly with temperature. In addition, BJT-based bandgap reference (BGR) circuits are widely used in CMOS processes to generate a stable reference voltage, and a general DDIC also uses them to generate a reference voltage.

To generate an absolute reference voltage that is independent of changes in temperature, V_{BE}, which has complementary to absolute temperature (CTAT) characteristic, and ΔV_{BE}, which has proportional to absolute temperature (PTAT) characteristic, of a BJT are used in the BGR. In this paper, ΔV_{BE}, which has a linear characteristic with respect to temperature, is read out by an analog-to-digital converter (ADC) to measure the ambient temperature.

For a fast data conversion and read-out flexibility, a digital filter with median and average functions is implemented to have minimum power consumption and area occupation in analog domain. To achieve a reliable temperature sensor, a digital calibration is used to suppress the offset error from the temperature sensor. Furthermore, calibration methodology that compensates for the thermal resistance effect is also utilized.

This article is organized as follows. In Section II, the characteristics of a bandgap-based temperature sensor and a following 10-bit ADC are described, including the operation sequence of the DDIC. Section III describes the temperature compensation method of the temperature sensor and the thermal resistance calibration. Section IV presents the experimental results of 40 chips. This article ends with conclusions in Section V.

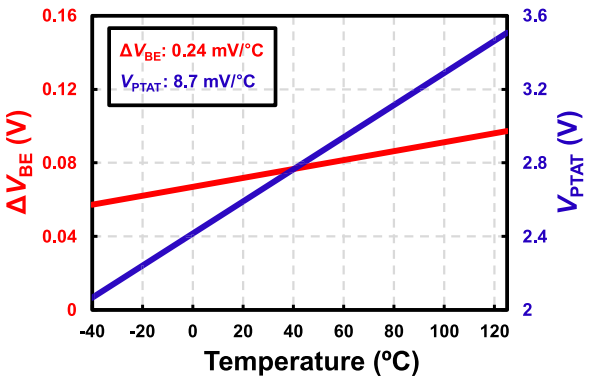

FIGURE 2. ΔV_{BE} and V_{PTAT} versus temperature.

II. TEMPERATURE SENSOR

Fig. 1 shows a block diagram of a temperature sensor including a BGR. A BJT-based bandgap circuit produces a zero temperature coefficient (TC) output with a combination of a base-emitter voltage (V_{BE}) of and a difference of base-emitter voltage (ΔV_{BE}). In the proposed circuit, to fully utilize the dynamic range (DR) of the ADC, the signal gain of the temperature sensor is decided by the proper ratio of the BJT (Q_1: Q_2), current mirror (M_{P1}: M_{P2}: M_{P3}), and resistors (R_{PTAT}: R_{OUT}).

Fig. 2 shows a post-layout simulation result of proportional voltage versus absolute temperature. The PTAT current I_{PTAT} for the core circuit can be expressed as:

$$I_{PTAT} = V_T \cdot ln(m \cdot n)/R_{PTAT} \quad (1)$$

where m and n are the ratio of M_{P1} to M_{P2} and Q_1 to Q_2, respectively. As expected in (1), the PTAT current increases

TABLE 1. Monte-carlo post-layout simulation results.

	30 °C	90 °C	Conversion Gain
Min.	2.32 V	2.8 V	8.01 mV/°C
Mean	2.67 V	3.19 V	8.72 mV/°C
Max	3.04 V	3.61 V	9.46 mV/°C
1-σ	0.11 V	0.12 V	–
Calculated Value	2.61 V	3.12 V	8.7 mV/°C

due to an increase in thermal voltage as the temperature increases. The PTAT current is mirrored to M_{P3} to generate a voltage of V_{PTAT}. This is the output of the temperature sensor, which can be achieved as follows:

$$V_{PTAT} = l \cdot R_{OUT} \cdot V_T \cdot ln(m \cdot n)/R_{PTAT} \quad (2)$$

where l, m, n, and R_{OUT}/R_{PTAT} are 2, 8, 2, and 18, respectively. The resulting output voltage V_{PTAT} is $100V_T$ with these design coefficients. The conversion gain of the temperature sensor is then 8.7 mV/°C. To ensure stable operation, commercial DDIC products typically require a temperature range of −20°C to 85°C. This temperature sensing circuit with PTAT characteristic results in an output voltage range of 913 mV. The output voltage of the temperature sensor is digitized by the following SAR ADC to calibrate and utilize in digital domain.

A. THE OFFSET OF THE TEMPERATURE SENSING CIRCUIT

For operations that use an operational amplifier to generate V_T, an unintended amplifier offset is added to the result. The output of the temperature sensor with the amplifier offset can be derived as:

$$V_{PTAT} = (l \cdot R_{OUT} \cdot V_T \cdot ln(m \cdot n) + l \cdot R_{OUT} \cdot V_{OS})/R_{PTAT} \quad (3)$$

where V_{OS} is the offset of the amplifier. The offset of the circuit increases with the ratio of R_{OUT} and R_{PTAT}.

Table 1 shows the results of a global Monte-Carlo post-layout simulation of the on-chip temperature sensor at 30°C and 90°C. At both temperatures, the standard deviation is more than 0.1 V, and this results in an equivalent 3-σ temperature error of ±40°C, which must be suppressed with trimming and calibration.

B. 10-BIT ANALOG-TO-DIGITAL CONVERTER

Fig. 3 shows a simplified block diagram of the proposed ADC, which is implemented to digitize the temperature information. The 10-bit ADC consists of a resistor-based digital-to-analog converter (DAC) and a successive approximation register (SAR) structure. V_{REFH} and V_{REFL} should be chosen based on the output range of the temperature sensor. The designed conversion gain of the temperature sensor is 8.7 mV/°C, and the brightness of organic light emmiting diodes (OLEDs) in a panel changes with temperature by approximately 1.1 cd/m^2/°C [6], [9]. The resolution of

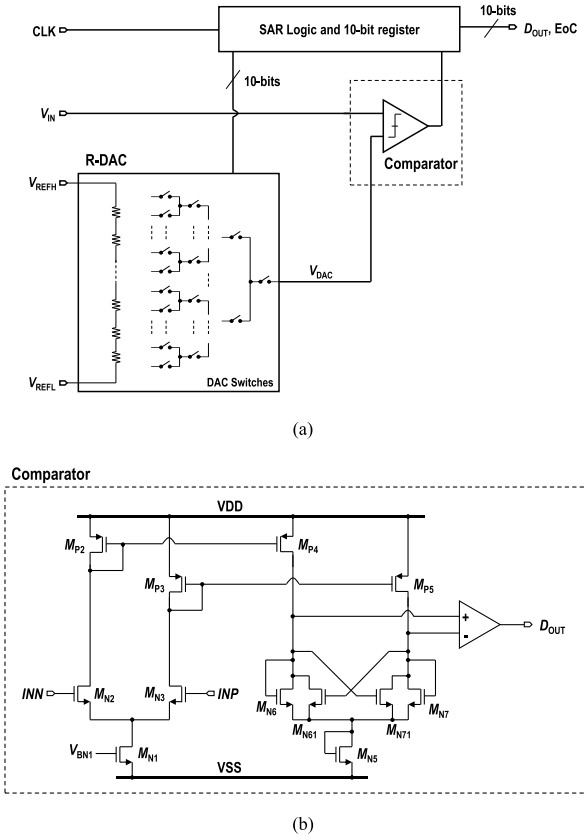

FIGURE 3. Simplified block diagram of (a) the resistor ADC based SAR ADC and (b) the comparator.

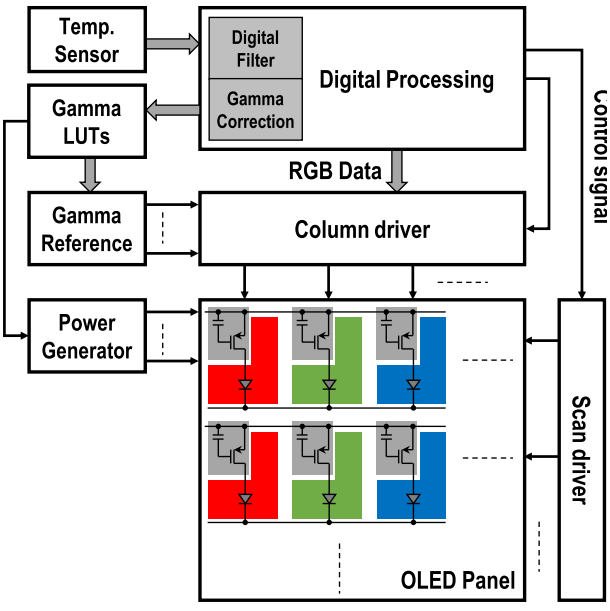

FIGURE 4. Overall architecture of the OLED DDIC.

the ADC is set to 2.175 mV/LSB, which is equivalent to 0.25°C/LSB to compensate for the OLED brightness degradation by detecting a temperature change. Considering the required temperature range, the reference voltages of V_{REFH} and V_{REFL} are chosen as 3.6 V and 2 V, respectively.

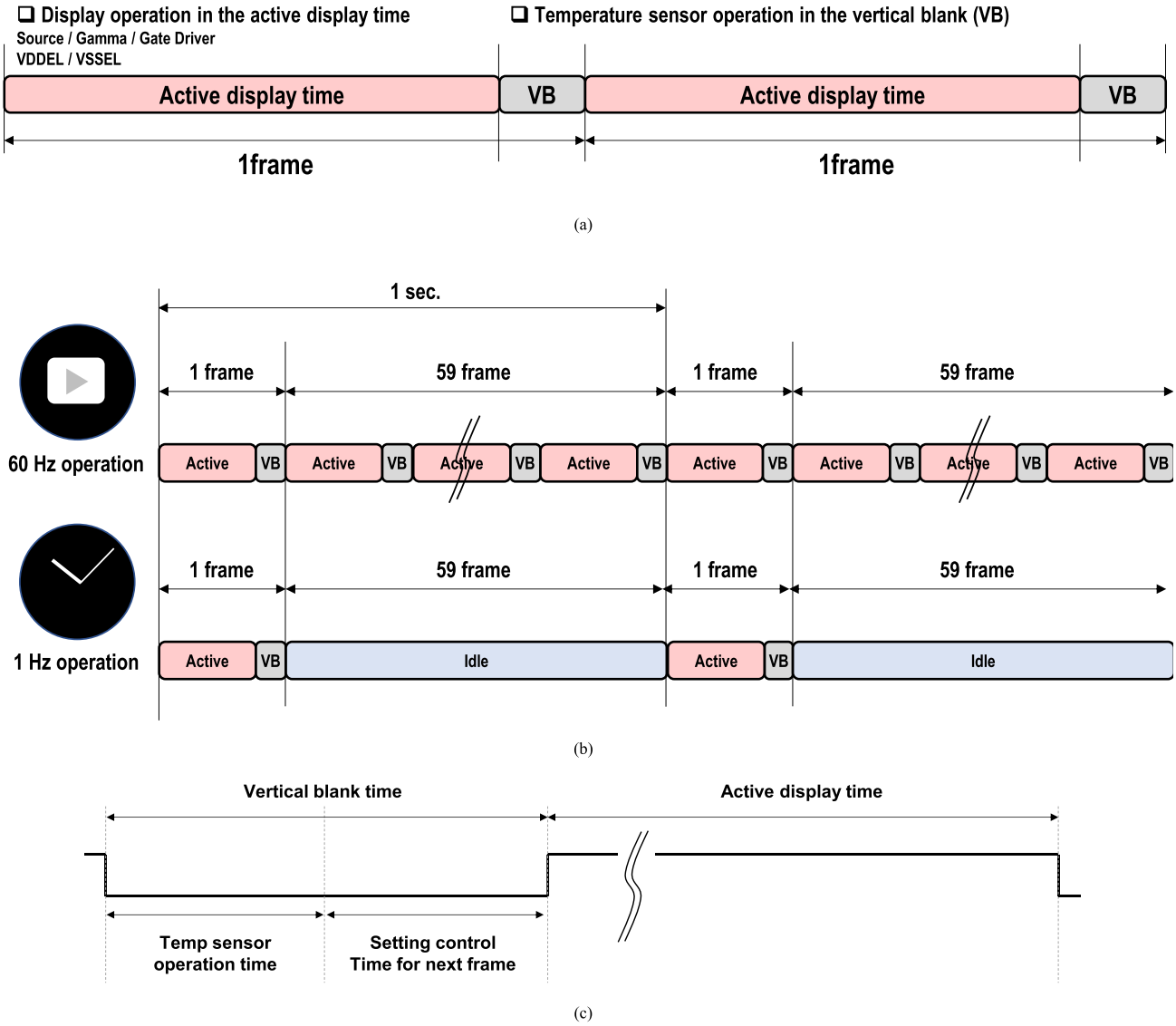

FIGURE 5. (a) The timing diagram of the display operation with temperature measurement, (b) the timing comparison between 60 Hz and 1 Hz display operation, and (c) the simplified timing diagram of the vertical blank (VB) time.

For generating the stable reference voltages and temperature data, a stabilization time of 20 μs is required, and an additional 20 μs is required for data digitization of the SAR ADC. A minimum conversion time of 40 μs is thus required for the temperature data. The SAR ADC operates with a 600 kHz clock and the operation of the data converter is completed in 12 clock cycles considering the SAR ADC operation stabilization and end of completion (EoC) time.

The performance of the 10-bit 50 kS/s ADC is affected by the AC gain of the sample and hold amplifier (SHA), the differential non-linearity (DNL) characteristics of the resistor-based DAC, and the AC gain of the comparator. An effective number of bits (ENOB) of 9.9-bits is achieved with the proposed SAR ADC in a post-layout simulation. To improve the signal-to-noise ratio (SNR) of the temperature sensing system, a 3-tap window shift rank and moving average filters are also implemented in the digital filter. The comparator and SAR logic opearte at 3.6 V and 1.1 V, respectively.

C. TEMPERATURE SENSOR IN DISPLAY DRIVER IC

Figure 4 shows the overall architecture of the OLED DDIC. The column driver drives the panel by selecting a voltage from the gamma reference to represent the gradation of a pixel according to the incoming RGB data. The scan driver selects each OLED line to update the gray scale voltage to the pixels on each line. In addition, the power generator supplies the voltage required for the emission of the OLED. The OLED system is operated by the timing control of the digital processing [10]. OLEDs experience changes in luminance and color depending on temperature and usage time [11], [12]. To suppress this, information about gamma is set in the loop-up

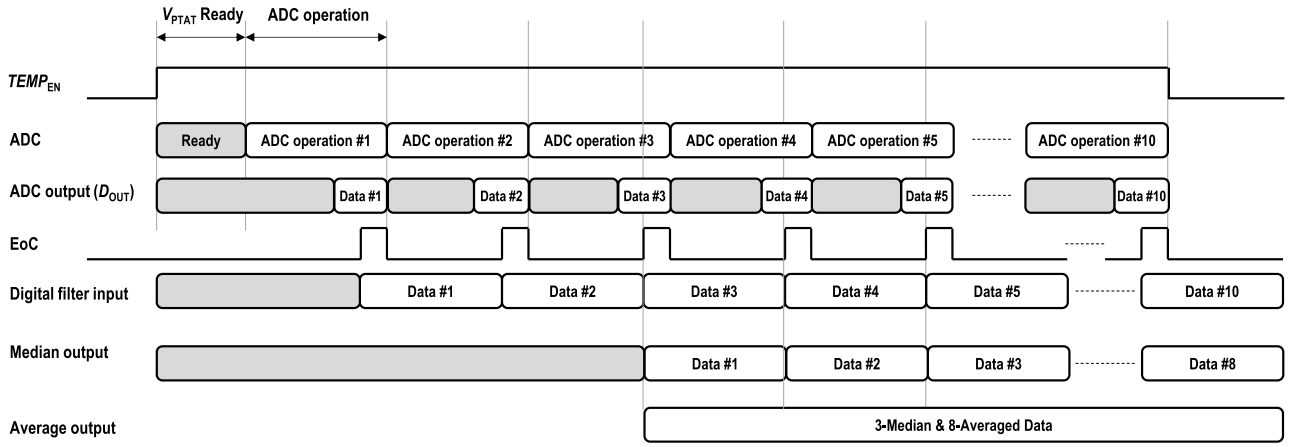

FIGURE 6. The timing diagram of the ADC and the digital filter in a temperature measurement operation.

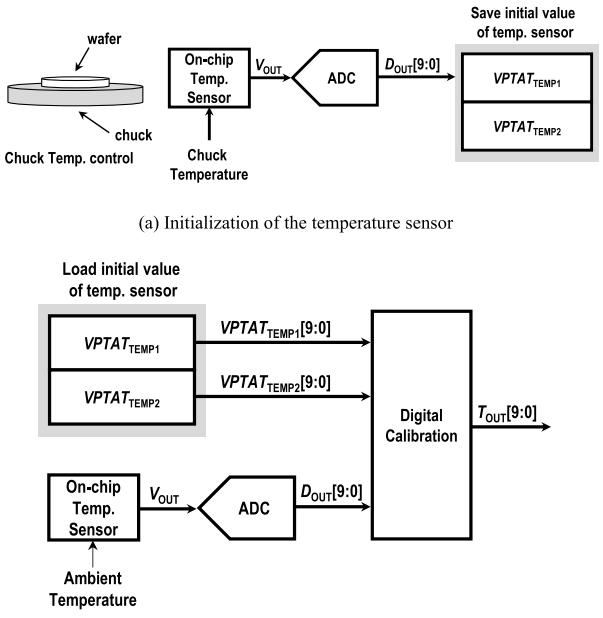

FIGURE 7. Digital calibration sequence.

tables (LUTs) based on statistical data obtained through evaluation of the panel in advance. By combining the digitized temperature data and the usage time information, the input for the gamma reference can be set to compensate for changes in luminance and color caused by the usage environment.

Since the introduction of low-temperature polycrystalline oxide (LTPO) panels for mobile product displays, the main technique for reducing power consumption has been to vary the display frame rate from 1 Hz to 120 Hz [13], [14]. 1 Hz operation is mainly used for always-on-display (AOD) mode, and the panel updates the display information only once a second. For this reason, the proposed temperature sensor is also designed to support the minimum update time to 1 s.

The DDIC is divided into an active display section to drive the display and a vertical blank (VB) section to change the settings of the DDIC. The temperature sensor of the DDIC is operated in the VB section when the display is stopped to minimize errors in temperature measurement due to noise generated during display operation. In the VB section, input data and settings for changing the brightness of the screen are changed, and sensors related to the display are operated. In the 1 Hz interval, the display frame is updated only once per second and remains idle for the rest of the interval. The temperature sensor also operates once in the VB interval after the active display interval.

Fig. 5 shows the sections of the display where the temperature sensor is active. In basic 60 Hz operation, there is a VB interval every frame, which allows the temperature sensor to be active in every interval. To optimize the power consumption of the system, however, the temperature sensor is only active once per second. In 1 Hz operation, the display is only updated once per second, so when the display is updated once per second, the temperature sensor is also active during every VB interval. A display system for a smart watch has a resolution of approximately 396 × 396 and a VB section time of approximately 400 μs. The V-BLANL time is composed of temperature sensor operation time and settling time of control signal for a next frame (Fig. 4(c)). In this prototype, the settling time for a next frame is 159 μs, which is for setting a gamma voltage of a display panel based on the measured temperature and ambient brightness. Because the information about the ambient brightness is irregular and unexpected, so it is stored and utilized with the temperature data in the VB time between frames. The remaining 241 μs of the VB time is for sensing and calibrating temperature data. The temperature sensing should be completed in the interval between frames to avoid affecting normal operation [15]. Because a long VB time reduces the brightness of the panel, a fast temperature read-out characteristic is one of the most important requirements in the display systems.

Fig. 6 shows a timing diagram of the ADC and digital filter during temperature sensor operation before the start of each frame. $TEMP_{EN}$ is a signal that determines the operation

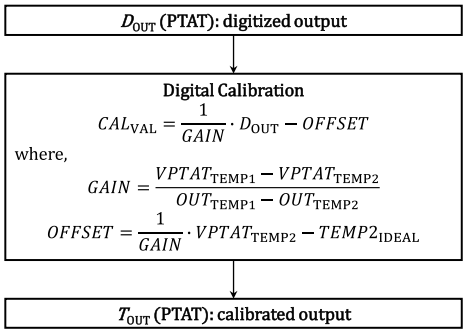

FIGURE 8. Digital calibration sequence.

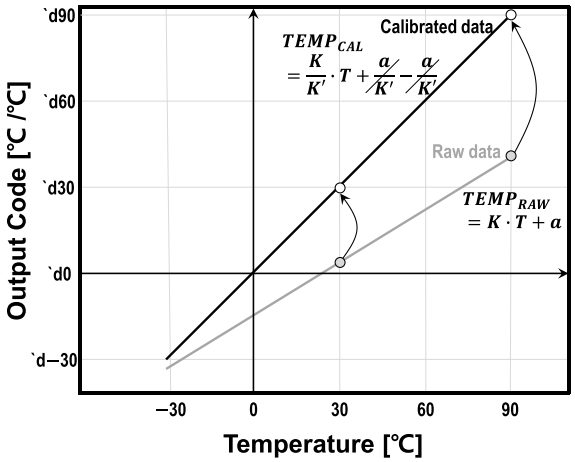

FIGURE 9. The graph of raw data and calibrated data.

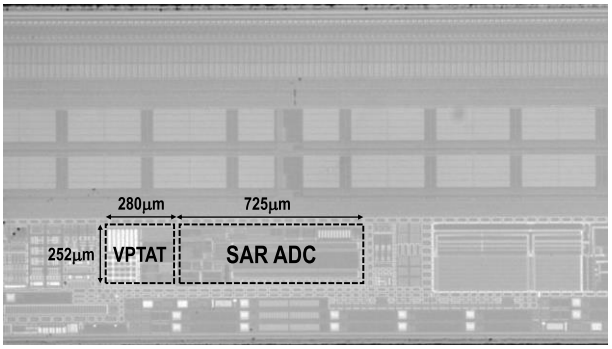

FIGURE 10. Chip micrograph.

of the temperature sensing circuit and comparator. When $TEMP_{EN}$ is turned on, the temperature sensor and the following SAR A DC start operating for temperature to digital conversion. The data is taken from the digital block according to the EoC of the ADC. The digitized temperature data is processed by a median filter and an average filter to suppress analog noise and then saved as final data. These median and average filters draw 13.55 μA from 1.1 V.

The start-up time for stable output settling of the temperature sensor is set to 20 μs based on the worst-case simulation results. The SAR ADC operates with 10 operating clock

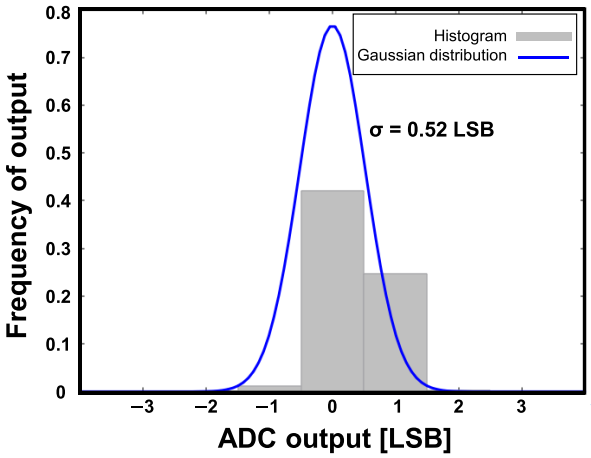

FIGURE 11. Measured noise histogram of the ADC with 2^{11} digitized data.

cycles to process 10-bit data and additional 2 operating clock cycles for margin. Temperature to digital conversion including 3-tap median and 8 average filters takes 220 μs, and an additional 21 μs is required for the digital processing, which results in a total temperature measurement time of 241 μs.

III. CALIBRATION METHODOLOGY

A. DIGITAL CALIBRATION METHODOLOGY

As described above, the on-chip temperature sensor has a large offset deviation, so it is suppressed in a digital domain. For temperature calibration, the gain and offset of the digitized output curve should be determined by measuring two different external temperatures.

Fig. 7 shows a simplified block diagram of the initialization and operation of the temperature sensor. In the proposed auto-test environment (ATE), a wafer is placed on a chuck, and the chuck temperature is set to control the temperature of the wafer. The chuck temperature is set, and the on-chip temperature circuit is triggered to store the digitized output. In this work, a wafer test is performed twice for different temperature settings, and a test chip is operated to store each output of measured digitized and external temperature data in the on-chip one-time programmable (OTP) memory. Based on these stored values, the digital calibration is performed.

Fig. 8 shows the digital calibration sequence for the measured temperature output. To obtain the gain, the difference between each measured digital value ($VPTAT_{TEMP1} - VPTAT_{TEMP2}$) and each external temperature value ($OUT_{TEMP1} - OUT_{TEMP2}$) is divided. To obtain the offset, the digital value ($VPTAT_{TEMP2}$) should be divided by the gain and subtracted the ideal digitized output. The obtained gain and offset are used to digitally calibrate the value of the measured raw data. Fig. 9 shows the relationship between raw data and calibrated data. The output of the calibrated data intersects the origin after calibration based on the raw data acquired.

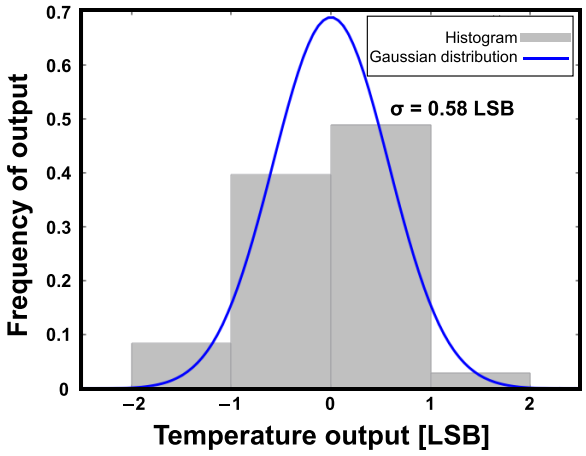

FIGURE 12. Measured noise histogram of the digitized temperature output with 2^{11} digitized data.

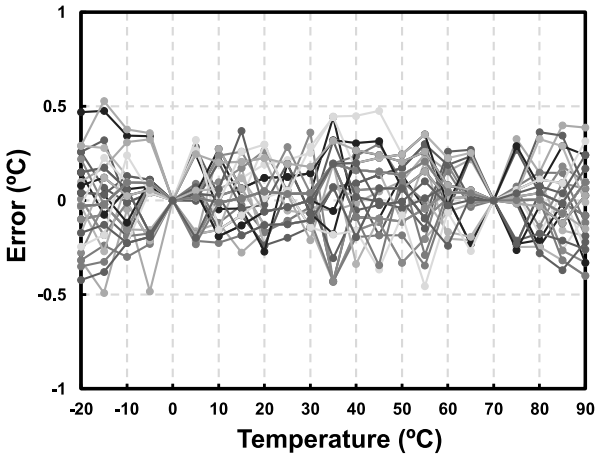

FIGURE 13. Measured temperature error of 40 sample chips.

B. CALIBRAITON METHODOLOGY ACCORDING TO THERMAL RESISTANCE

The on-chip temperature sensor needs to be calibrated by measuring the ambient temperature for high accuracy. The on-chip temperature sensor measures an internal junction temperature, which is not the same as the ambient temperature. The temperature of the chip is affected by the power consumption of the circuits, and the relationship between the junction temperature and the ambient temperature is as follows [16]:

$$T_J = T_A + R_{TH} \cdot P \tag{4}$$

where T_J is the junction temperature, T_A is the ambient temperature, R_{TH} is the thermal resistance between the junction and ambient atmosphere, and P is the power dissipation.

In this paper, a digital calibration methodology that compensates for the thermal resistance effect is proposed. The prototype chip shows a chip temperature increase of approximately 0.15°C for every 1 mW increase. To suppress this temperature characteristic with power consumption dependency, a case-specific calibration method with on-chip memory is used for the thermal resistance calibration. There are four modes in 60 Hz display applications. The first is a sleep mode that does not use display. In this case, the host system does not transmit video data to the DDIC, but only sends commands for setting the chip or reads information about the status of the chip. There are no writes and reads to the frame buffer, and the analog circuits for driving the panel are not working. The second is low power mode with low frequency operation and is mainly used to implement AOD function. Video data is transmitted from the host system at 1 Hz and written to the frame buffer. Then, the information in the frame buffer is read at 1 Hz to drive the panel. The third is the still image mode. Video data is transmitted from the host at 1 Hz, and the data is written to the frame buffer. The information in the frame buffer is read at 60 Hz to drive the panel. The fourth is video mode. It drives the panel by writing video data to the frame buffer every frame at high speed and reading it every frame. For the prototype, the thermal resistance calibration is utilized considering three different display cases except the sleep mode. The power consumption of the digital circuits is predicted by operation mode because it is most affected by the frequency of use of the frame buffer. Because the power consumption of the analog circuits is affected by a previous horizontal line of a display, the power consumption information should be updated line-by-line for an accurate thermal resistance calibration. The data read from the frame buffer is transferred to the DAC and drives the panel through the source amplifier. At this time, based on the difference between the data of the previous line input to the DAC and the current drive line, the power consumption of the analog circuits can be estimated. The proposed temperature sensing system uses the power consumption data on a case-by-case basis to compensate for thermal resistance effects.

IV. EXPERIMENTAL RESULTS

The proposed on-chip temperature sensing system is implemented in a 40 nm CMOS process technology. It consists of a PTAT voltage generation circuit, a 10-bit SAR ADC, and a digital filter for post-processing. Fig. 10 shows a chip micrograph of the temperature sensor, which has an area of 0.25 mm^2. The digital filter is embedded in the digital processing block of the system, and includes a mean filter, median filter, gain compensation, offset compensation, and a compensation circuit for the thermal resistance effect.

Fig. 11 shows the measured output noise histogram of the SAR ADC. It is obtained by taking 2^{11} consecutive measurements and has a noise characteristic of 0.52 LSB, which corresponds to a noise-free resolution (NFR) of 8.22-bits. The NFR is determined from a 6.6-σ noise distribution for the industry-standard reliability of 99.9%. The measured noise histogram of the digitized temperature output is shown in Fig. 12. A standard deviation of 0.58 LSB is achieved, which is equivalent to 0.145°C. Considering the

TABLE 2. Performance summary and comparison with other reported BJT temperature sensors.

	This work	[17]	[18]	[19]	[20]
Tech. (nm)	40	180	28	180	160
Area (mm^2)	0.25*	0.42**	0.01	0.35**	0.15**
Voltage (V)	3.6	1.5-2	1.8	1.6-2.2	1.8
Resolution (°C)	0.25	0.012	0.15	0.0017	0.023
3σ inaccuracy (°C)	0.48	0.45	1.85	0.25	0.25
Conversion time (ms)	0.241	8.3	8.2	218	20
Power (μW)	129.17	5.7	18.75	9	9.75
Energy/ Conversion (nJ/Conv.)	31.1	47.3	153.8	1962	195

* The area for the on-chip digital filter (8070 gate count) is not included.
** The digital filter is implemented off-chip.

noise increase from 0.52 LSB to 0.58 LSB, the noise contribution of the temperature sensor core circuit can be derived as 0.26 LSB, which is equivalent to 0.065°C.

A DDIC requires a high drive voltage for a display panel [6]. A minimum range of the drive voltage from 0.3 V to 3.3 V is required to display gradients on the display panel, which requires a supply voltage of at least 3.6 V for the drive circuit. The temperature sensor for PTAT voltage generation draws only 4 μA at 3.6 V, and the SAR ADC draws 21 μA and 11.6 μA at 3.6 V and 1.1 V, respectively. The on-chip reconfigurable digital filter including median and average filters consumes 13.55 μA, and the digital calibration block consumes 10.46 μA. This synthesized digital part consists of 8070 gate count. The power consumption of the BGR is excluded in the total power consumption of the proposed temperature to digital converter because the internal BGR is always required for DDIC system operation.

Fig. 13 shows the measured temperature error of 40 sample chips on a single wafer. It shows a maximum temperature error of 0.5°C with an inaccuracy of ±0.48°C (3-σ) after two-point calibration with the on-chip digital calibration and thermal resistance compensation. To verify the error characteristics of the temperature sensor, 40 samples from a single typical wafer were measured in an automated test environment (ATE).

Table 2 summarizes the performance of the temperature sensing system and compares it with other works. In this paper, the ADC is designed to operate with a short conversion time. To share the ADC with other DDIC circuits, the supply voltage of the temperature to digital converter is the same as that of the internal gamma reference circuit for display panel operation. Because all the operation based on the temperature must be completed in the short VB for DDIC applications, the fast temperature sensor is proposed with a small conversion time of 241 μs. This temperature sensor also achieves high energy-efficiency of 31.1 nJ/conversion. Regarding the area occupation, the reference circuit and the ADC are also utilized with another DDIC function, so a simple current mirrored transistor, resistor, and stabilization capacitor are added. This results in an actual total area of 0.01 mm^2.

V. CONCLUSION

This paper presents a fast temperature sensor for DDIC applications with a conversion time of 241 μs. The offset and error of the temperature to digital conversion circuit is corrected by digital calibration without any reference circuit or noise shaping architecture, which degrades the power-area efficiency of the temperature measurement system. An energy-efficiency of 31.1 nJ/conversion and a temperature inaccuracy of ±0.48°C are achieved with the digital calibration including the considerations of the thermal resistance effect. Furthermore, the power consumption and area occupation are optimized by sharing the reference circuit in the DDIC with the gamma reference circuit and the built-in low-dropout regulator (LDO). The proposed temperature sensor in this paper could also be used as a defect detector for detecting cracks in a display panel and diagnosing power abnormalities in DDIC applications.

ACKNOWLEDGMENT

The authors thank the IC Design Education Center (IDEC) Program of Korea, and for its hardware and software assistance for the design and simulation.

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